HD66726

(Graphics LCD Controller/Driver
with Key Scan Function)

HITACHI

ADE-207-310(Z)
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Description

The HD66726, dot-matrix graphics LCD controller and driver LSI incorporating a key scan function up to a 4-by-8 key matrix, displays characters such as alphanumerics, katakana, hiragana and symbols as well as graphics such as kanji and pictograms. It can be configured to drive a dot-matrix liquid crystal display and control key scan functions under the control of the microprocessor connected via the clock-synchronized serial or 4/8-bit bus. A single HD66726 is capable of displaying up to five 16-character lines, 96-by-40 dot graphics and 192 segments. Of the 192 segments displayed, 64 segments can be grayscaled. The HD66726 has a smooth vertical scroll display and double-width display so that the user can easily see a variety of information within a small LCM.

The HD66726 has various functions to reduce the power consumption of an LCD system such as low-voltage operation of 2.2 V or less, a booster to generate maximum quadruple LCD drive voltage from the supplied voltage, and voltage-followers to decrease the direct current flow in the LCD drive bleeder-resistors. Combining these hardware functions with software functions such as standby and sleep modes allows fine power control. The HD66726 is suitable for any portable battery-driven product requiring long-term driving capabilities and small physical dimensions such as cellular phones, pagers, portable audio devices, or electronic wallets.45

Features

- Control and drive of a character and graphics LCD with built-in key scan functions
- Five 16-character lines, 96-by-40 dot graphics, and 192 segments
- 64 grayscale segments
- Control up to a 4×8 (32 key) matrix key scan.
- 3 general ports built-in
- Low-power operation support:
  - Vcc = 2.2 to 5.5 V (low voltage)
  - V_{LCD} = 4.0 to 13.0 V (liquid crystal drive voltage)
  - Single, double, triple, or quadruple booster for liquid crystal drive voltage
  - Contrast adjuster and voltage followers to decrease direct current flow in the LCD drive bleeder-resistors

  - — Power-save functions such as the standby mode and sleep mode supported
  - — Wake-up feature using key scan interrupt
  - — Programmable drive duty ratios and bias values displayed on LCD
- Clock-synchronized serial interface
- 4-/8-bit bus interface capability (except when key scan circuit is used)
- 80 × 8-bit display data RAM (80 characters max)
- 20,736-bit (6 × 8 dots : 432 characters) character generator ROM
- 480 × 8-bit (96 × 40 dots) character generator RAM
- 96 × 8-bit (192 segment icons and marks max) segment RAM
- 96-segment × 42-common liquid crystal display driver
- Programmable display sizes and duty ratios
- Vertical smooth scroll
- Vertical double-height display by each display line
- Black-white reversed display
- Selectable CGROM memory bank by each display line (max. 432 fonts)
- Wide range of instruction functions:
  - — Clear display, display on/off control, icon and mark control, character blink, black-white reversed blinking cursor, return home, cursor on/off, black-white reversed raster-row
- No wait time for instruction execution and RAM access
- Internal oscillation with external and hardware reset
- Shift change of segment and common driver
- Slim chip with bumps for chip-on-glass (COG) mounting, and tape carrier package (TCP)

Table 1 Progammable Display Sizes and Duty Ratios

		Character Display	Graphic Display				
Duty Ratio	**Optimum Drive Bias**	**6-dot Font Width**	**Bit Map**	**16 x 16-dot Font Width**	**Segment Display**	**Scanned Keys**	**General Ports**
1/2	1/2	Unavailable	Unavailable	Unavailable	192	32 (4 x 8)	3
1/10	1/4	1 line x 16 characters	96 x 8 dots	Unavailable	(Grayscale segments: 64)		
1/18	1/5	2 lines x 16 characters	96 x 16 dots	1 line x 6 characters			
1/26	1/6	3 lines x 16 characters	96 x 24 dots	1.5 lines x 6 characters			
1/34	1/6	4 lines x 16 characters	96 x 32 dots	2 lines x 6 characters			
1/42	1/7	5 lines x 16 characters	96 x 40 dots	2.5 lines x 6 characters			

<Target values>

Total Current Consumption Characteristics (Vcc = 3 V, fosc = 50 kHz, TYP Conditions, LCD Drive Power Current Included)

				Total Power Consumption				
				Normal Display Operation				
Character Display Size	Duty Ratio	Optimum Drive Bias	Frame Frequency	Internal Logic	LCD Power	Total*	Sleep Mode	Standby Mode
Segment only	1/2	1/2	74 Hz	(20 µA)	(10 µA)	Single (30 µA)	(15 µA)	0.1 µA
1 line x 12 characters	1/10	1/4	74 Hz	(25 µA)	(15 µA)	Double (55 µA)	(15 µA)	
2 lines x 12 characters	1/18	1/5	73 Hz	(25 µA)	(15 µA)	Double (55 µA)	(15 µA)	
3 lines x 12 characters	1/26	1/6	74 Hz	(25 µA)	(15 µA)	Double (45 µA)	(15 µA)	
4 lines x 12 characters	1/34	1/6	74 Hz	(25 µA)	(15 µA)	Triple (70 µA)	(15 µA)	
5 lines x 12 characters	1/42	1/7	74 Hz	(25 µA)	(15 µA)	Triple (70 µA)	(15 µA)	

Note : When duty ratio = 1/2 and a booster is not used:
the total power consumption = Internal logic current + LCD power current

When duty ratio = 1/10 and a double, triple, or quadruple booster is used:
the total power consumption = Internal logic current + LCD power current x 2 (double booster),
the total power consumption = Internal logic current + LCD power current x 3 (triple booster), and
the total power consumption = Internal logic current + LCD power current x 4 (quadruple booster)

Type Name

Types	External Dimensions	Operation Voltages	Internal Fonts
HD66726A03TB0L	TCP	2.2 V to 5.5 V	Katakana, alphanumerics, symbols and European fonts
HD66726A03BP	Au-bumped chip		

LCD-II Family Comparison

Items	HD66712U	HD66720	HD66705U
Character display sizes	12 characters x 4 lines	8 characters x 2 lines	12 characters x 2 lines
Graphic display sizes	—	—	—
Multiplexing icons	60	42	40
Annunciator	—	—	Static: 10
Key scan control	—	5 x 6	—
LED control ports	—	2	—
General output port	—	—	—
Operating power voltages	2.7 V to 5.5 V	2.7 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 11 V	3 V to 9 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Possible	Possible	Impossible
Liquid crystal drive duty ratios	1/17, 33	1/9, 17	1/10, 18
Liquid crystal drive biases	1/4 to 1/6, 7	1/4 to 1/5	1/4
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Double or triple
Bleeder-resistor for liquid crystal drive	External	External	Incorporated (external)
Liquid crystal drive operational amplifier	—	—	Incorporated
Liquid crystal contrast adjuster	—	—	Incorporated
Horizontal smooth scroll	Dot unit	Dot unit	—
Vertical smooth scroll	—	—	Line unit
Double-height display	—	—	Yes
DDRAM	80 x 8	40 x 8	60 x 8
CGROM	9,600	9,600	9,600
CGRAM	64 x 8	64 x 8	32 x 5
SEGRAM	16 x 8	16 x 8	8 x 5
No. of CGROM fonts	240	240	240
No. of CGRAM fonts	8	8	4
Font sizes	5 x 8	5 x 8	5 x 8
Bit map area	—	—	—
R-C oscillation resistor/oscillation frequency	External resistor (270 kHz)	External resistor (150 kHz)	External resistor (40, 80 kHz)
Reset function	Incorporated, external	Incorporated, external	External
Low power control	LP display mode	LP display mode Simple standby	Partial display off Display off Oscillation off Liquid crystal power off
SEG/COM direction switching	—	—	SEG only
QFP package	(S mask)	QFP-1420	—
TQFP package	—	TQFP-1414	—
TCP package	TCP-128	—	TCP-153
Bare chip	Yes	Yes	Yes
Bumped chip	Yes	—	Yes
No. of pins	128	100	153
Chip sizes	4.95 x 5.27	5.60 x 6.00	9.69 x 2.73
Pad intervals	128 μm	160 μm	120 μm

LCD-II Family Comparison (cont)

Items	HD66717	HD66727	HD66724
Character display sizes	12 characters x 4 lines	12 characters x 4 lines	12 characters x 3 lines
Graphic display sizes	—	—	72 x 26 dots
Multiplexing icons	40	40	144
Annunciator	Static: 10	Static: 12	1/2 duty: 144
Key scan control	—	4 x 8	8 x 4
LED control ports	—	3	—
General output ports	—	3	3
Operating power voltages	2.4 V to 5.5 V	2.4 V to 5.5 V	1.8 V to 5.5 V
Liquid crystal drive voltages	3 V to 13 V	3 V to 13 V	3 V to 6.5 V
Serial bus	I2C, Clock-synchronized serial	I2C, Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	—	4 bits, 8 bits
Expansion driver control	Impossible	Impossible	Impossible
Liquid crystal drive duty ratios	1/10, 18, 26, 34	1/10, 18, 26, 34	1/2, 10, 18, 26
Liquid crystal drive biases	1/4, 1/6	1/4, 1/6	1/4 to 1/6.5
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Double or triple	Double or triple	Single, double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	Incorporated (external)
Liquid crystal drive operational amplifier	Incorporated	Incorporated	Incorporated
Liquid crystal contrast adjuster	Incorporated	Incorporated	Incorporated
Horizontal smooth scroll	—	—	3-dot unit
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	Yes
DDRAM	60 x 8	60 x 8	80 x 8
CGROM	9,600	11,520	20,736
CGRAM	32 x 5	32 x 6	384 x 8
SEGRAM	8 x 5	8 x 6	72 x 8
No. of CGROM fonts	240	240	240 + 192
No. of CGRAM fonts	4	4	64
Font sizes	5 x 8	5 x 8, 6 x 8	6 x 8
Bit map area	—	—	72 x 26
R-C oscillation resistor/ oscillation frequency	External resistor (40-160 kHz)	External resistor (40-160 kHz)	External resistor, incorporated (32 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt
SEG/COM direction switching	SEG only	SEG, COM	SEG, COM
QFP package	—	—	—
TQFP package	—	—	—
TCP package	TCP-153	TCP-158	TCP-146
Bare chip	Yes	Yes	—
Bumped chip	Yes	Yes	Yes
No. of pins	153	158	146
Chip sizes	10.88 x 2.89	11.39 x 2.89	10.34 x 2.51
Pad intervals	120 μm	120 μm	80 μm

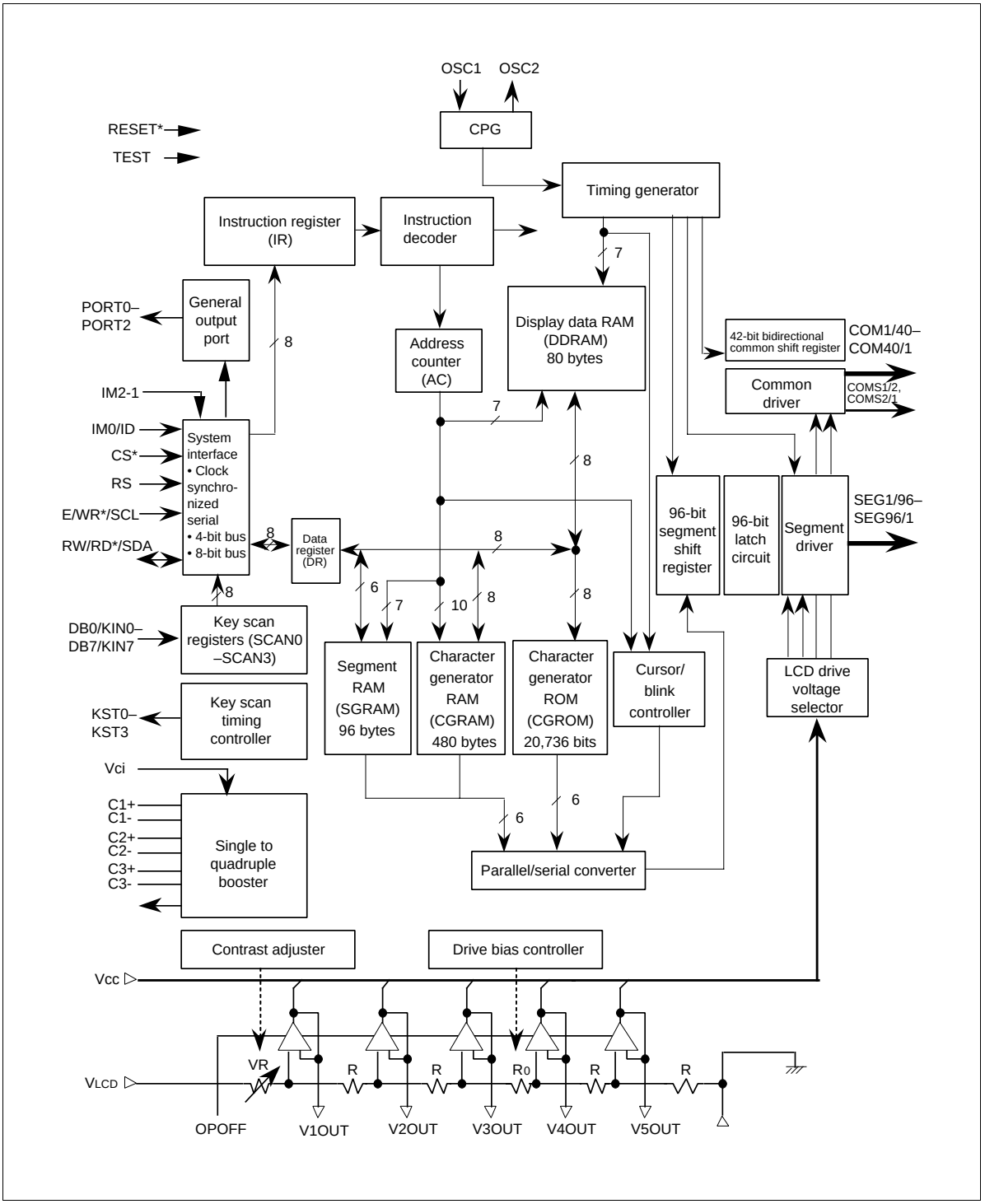
LCD-II Family Comparison (cont)

Items	HD66725	HD66726	HD66730
Character display sizes	16 characters x 3 lines	16 characters x 5 lines	6 (12) characters x 2 lines
Graphic display sizes	96 x 26 dots	96 x 42 dots	—
Multiplexing icons	192	192	71
Annunciator	1/2 duty: 192	1/2 duty: 192	—
Key scan control	8 x 4	8 x 4	—
LED control ports	—	—	—
General output ports	3	3	—
Operating power voltages	1.8 V to 5.5 V	2.2 V to 5.5 V	2.4 V to 5.5 V
Liquid crystal drive voltages	3.0 V to 6.5 V	4 V to 13 V	3 V to 15 V
Serial bus	Clock-synchronized serial	Clock-synchronized serial	Clock-synchronized serial
Parallel bus	4 bits, 8 bits	4 bits, 8 bits	8 bits
Expansion driver control	Impossible	Impossible	Possible
Liquid crystal drive duty ratios	1/2, 10, 18, 26	1/2, 10, 18, 26, 34, 42	1/14, 27, 40, 53
Liquid crystal drive biases	1/4 to 1/6.5	1/2 to 1/8	1/4 to 1/8.3
Liquid crystal drive waveforms	B	B	B
Liquid crystal voltage booster	Single, double, or triple	Single, double, triple, or quadruple	Double or triple
Bleeder-resistor for liquid crystal drive	Incorporated (external)	Incorporated (external)	External
Liquid crystal drive operational amplifier	Incorporated	Incorporated	—
Liquid crystal contrast adjuster	Incorporated	Incorporated	—
Horizontal smooth scroll	3-dot unit	3-dot unit	Display unit
Vertical smooth scroll	Line unit	Line unit	Line unit
Double-height display	Yes	Yes	—
DDRAM	80 x 8	80 x 8	80 x 8
CGROM	20,736	20,736	506,880 + 9,216
CGRAM	384 x 8	480 x 8	32 x 6
SEGRAM	96 x 8	96 x 8	8 x 6
No. of CGROM fonts	240 + 192	240 + 192	3,840
No. of CGRAM fonts	64	64	8
Font sizes	6 x 8	6 x 8	11 x 12
Bit map areas	96 x 26	96 x 42	—
R-C oscillation resistor/ oscillation frequency	External resistor, incorporated (32 kHz)	External resistor (50 kHz)	External resistor (70–450 kHz)
Reset function	External	External	External
Low power control	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Partial display off Display off Oscillation off Liquid crystal power off Key wake-up interrupt	Booster off Internal division function
SEG/COM direction switching	SEG, COM	SEG, COM	—
QFP package	—	—	QFP-1420
TQFP package	—	—	—
TCP package	TCP-170	TCP-188	—
Bare chip	—	—	Yes
Bumped chip	Yes	Yes	—
No. of pins	170	188	128
Chip sizes	10.97 x 2.51	13.13 x 2.51	7.48 x 6.46
Pad intervals	80 µm	80 µm	180 µm

LCD-II Family Comparison (cont)

Items	HD66731
Character display sizes	10 (20) characters x 4 lines
Graphic display sizes	—
Multiplexing icons	120
Annunciator	—
Key scan control	—
LED control ports	—
General output ports	—
Operating power voltages	2.4 V to 5.5 V
Liquid crystal drive voltages	3 V to 15 V
Serial bus	Clock-synchronized serial
Parallel bus	8 bits
Expansion driver control	Possible
Liquid crystal drive duty ratios	1/14, 27, 40, 53
Liquid crystal drive biases	1/4 to 1/8.3
Liquid crystal drive waveforms	B
Liquid crystal voltage booster	Double or triple
Bleeder-resistor for liquid crystal drive	External
Liquid crystal drive operational amplifier	—
Liquid crystal contrast adjuster	—
Horizontal smooth scroll	Display unit
Vertical smooth scroll	Line unit
Double-height display	—
DDRAM	80 x 8
CGROM	506,880 + 9,216
CGRAM	32 x 6
SEGRAM	8 x 6
No. of CGROM fonts	3,840
No. of CGRAM fonts	8
Font sizes	11 x 12
Bit map areas	—
R-C oscillation resistor/ oscillation frequency	External resistor (70–450 kHz)
Reset function	External
Low power control	Booster off Internal division function
SEG/COM direction switching	—
QFP package	—
TQFP package	—
TCP package	TCP-170, 206
Bare chip	—
Bumped chip	Yes
No. of pins	206
Chip sizes	7.48 x 6.46
Pad intervals	80 µm

HD66726 Block Diagram

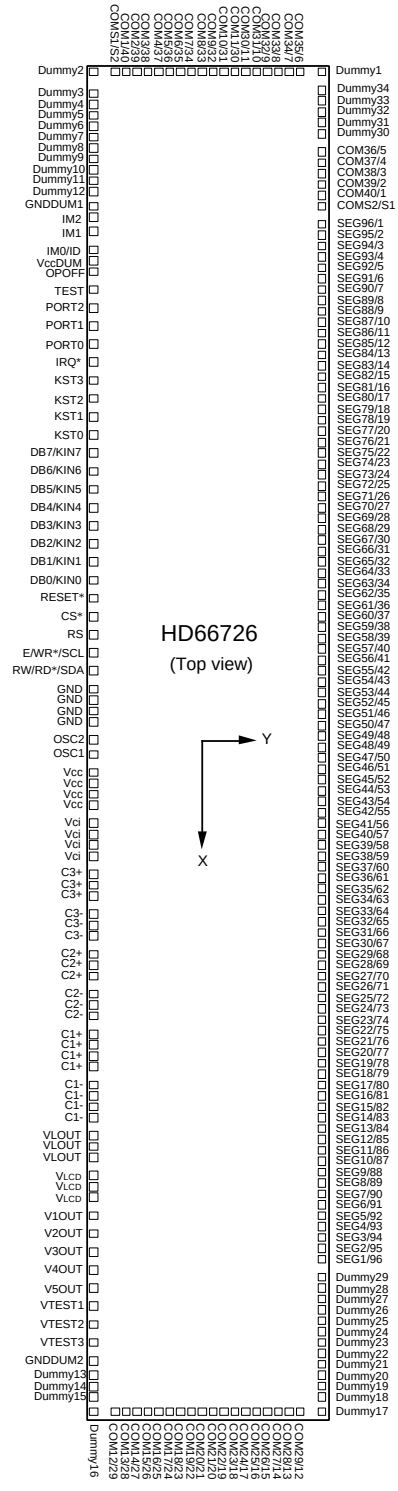


HD66726 Pad Coordinates

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
–	Dummy1	–6339	1080	21	DB2/KIN2	–1589	–1089	71	V3OUT	4951	–1002	104	SEG9/88	3933	1029	154	SEG59/38	–1071	1029
198	COM35/6	–6339	851	22	DB1/KIN1	–1405	–1089	72	V4OUT	5081	–1002	105	SEG10/87	3833	1029	155	SEG60/37	–1171	1029
199	COM34/7	–6339	751	23	DB0/KIN0	–1221	–1089	73	V5OUT	5211	–1002	106	SEG11/86	3733	1029	156	SEG61/36	–1271	1029
200	COM33/8	–6339	651	24	RESET*	–1037	–1089	74	VTEST1	5341	–1002	107	SEG12/85	3633	1029	157	SEG62/35	–1371	1029
201	COM32/9	–6339	550	25	CS*	–853	–1089	75	VTEST2	5471	–1002	108	SEG13/84	3533	1029	158	SEG63/34	–1471	1029
202	COM31/10	–6339	450	26	RS	–669	–1089	76	VTEST3	5601	–1002	109	SEG14/83	3433	1029	159	SEG64/33	–1571	1029
203	COM30/11	–6339	350	27	E/WR*/SCL	–506	–1089	77	GNDDUM2	5732	–1040	110	SEG15/82	3333	1029	160	SEG65/32	–1671	1029
204	COM11/30	–6339	250	28	RW/RD*/SDA	–376	–1089	–	Dummy13	5875	–1089	111	SEG16/81	3232	1029	161	SEG66/31	–1772	1029
205	COM10/31	–6339	150	29	GND	–193	–1089	–	Dummy14	5975	–1089	112	SEG17/80	3132	1029	162	SEG67/30	–1872	1029
206	COM9/32	–6339	50	30	GND	–63	–1089	–	Dummy15	6075	–1089	113	SEG18/79	3032	1029	163	SEG68/29	–1972	1029
207	COM8/33	–6339	–50	31	GND	67	–1089	–	Dummy16	6339	–1089	114	SEG19/78	2932	1029	164	SEG69/28	–2072	1029
208	COM7/34	–6339	–150	32	GND	197	–1089	78	COM12/29	6339	–851	115	SEG20/77	2832	1029	165	SEG70/27	–2172	1029
209	COM6/35	–6339	–250	33	OSC2	379	–1089	79	COM13/28	6339	–751	116	SEG21/76	2732	1029	166	SEG71/26	–2272	1029
210	COM5/36	–6339	–350	34	OSC1	563	–1089	80	COM14/27	6339	–651	117	SEG22/75	2632	1029	167	SEG72/25	–2372	1029
211	COM4/37	–6339	–450	35	V_{CC}	743	–1029	81	COM15/26	6339	–550	118	SEG23/74	2532	1029	168	SEG73/24	–2472	1029
212	COM3/38	–6339	–550	36	V_{CC}	874	–1029	82	COM16/25	6339	–450	119	SEG24/73	2432	1029	169	SEG74/23	–2572	1029
213	COM2/39	–6339	–651	37	V_{CC}	1004	–1029	83	COM17/24	6339	–350	120	SEG25/72	2332	1029	170	SEG75/22	–2672	1029
214	COM1/40	–6339	–751	38	V_{CC}	1134	–1029	84	COM18/23	6339	–250	121	SEG26/71	2232	1029	171	SEG76/21	–2772	1029
215	COMS1/S2	–6339	–851	39	Vci	1368	–1029	85	COM19/22	6339	–150	122	SEG27/70	2132	1029	172	SEG77/20	–2872	1029
–	Dummy2	–6339	–1089	40	Vci	1468	–1029	86	COM20/21	6339	–50	123	SEG28/69	2031	1029	173	SEG78/19	–2973	1029
–	Dummy3	–6075	–1089	41	Vci	1568	–1029	87	COM21/20	6339	50	124	SEG29/68	1931	1029	174	SEG79/18	–3073	1029
–	Dummy4	–5975	–1089	42	Vci	1668	–1029	88	COM22/19	6339	150	125	SEG30/67	1831	1029	175	SEG80/17	–3173	1029
–	Dummy5	–5875	–1089	43	C3+	1798	–1029	89	COM23/18	6339	250	126	SEG31/66	1731	1029	176	SEG81/16	–3273	1029
–	Dummy6	–5775	–1089	44	C3+	1898	–1029	90	COM24/17	6339	350	127	SEG32/65	1631	1029	177	SEG82/15	–3373	1029
–	Dummy7	–5675	–1089	45	C3+	1998	–1029	91	COM25/16	6339	450	128	SEG33/64	1531	1029	178	SEG83/14	–3473	1029
–	Dummy8	–5575	–1089	46	C3–	2128	–1029	92	COM26/15	6339	550	129	SEG34/63	1431	1029	179	SEG84/13	–3573	1029
–	Dummy9	–5475	–1089	47	C3–	2228	–1029	93	COM27/14	6339	651	130	SEG35/62	1331	1029	180	SEG85/12	–3673	1029
–	Dummy10	–5374	–1089	48	C3–	2328	–1029	94	COM28/13	6339	751	131	SEG36/61	1231	1029	181	SEG86/11	–3773	1029
–	Dummy11	–5274	–1089	49	C2+	2459	–1029	95	COM29/12	6339	851	132	SEG37/60	1131	1029	182	SEG87/10	–3873	1029
–	Dummy12	–5174	–1089	50	C2+	2559	–1029	–	Dummy17	6339	1080	133	SEG38/59	1031	1029	183	SEG88/9	–3973	1029
1	GNDDUM1	–5000	–1089	51	C2+	2659	–1029	–	Dummy18	6075	1080	134	SEG39/58	931	1029	184	SEG89/8	–4073	1029
2	IM2	–4900	–1089	52	C2–	2789	–1029	–	Dummy19	5975	1080	135	SEG40/57	831	1029	185	SEG90/7	–4173	1029
3	IM1	–4716	–1089	53	C2–	2889	–1029	–	Dummy20	5875	1080	136	SEG41/56	730	1029	186	SEG91/6	–4274	1029
4	IM0/ID	–4540	–1089	54	C2–	2989	–1029	–	Dummy21	5775	1080	137	SEG42/55	630	1029	187	SEG92/5	–4374	1029
5	V_{CC}DUM	–4440	–1089	55	C1+	3119	–1029	–	Dummy22	5675	1080	138	SEG43/54	530	1029	188	SEG93/4	–4474	1029
6	OPOFF	–4340	–1089	56	C1+	3219	–1029	–	Dummy23	5575	1080	139	SEG44/53	430	1029	189	SEG94/3	–4574	1029
7	TEST	–4164	–1089	57	C1+	3319	–1029	–	Dummy24	5475	1080	140	SEG45/52	330	1029	190	SEG95/2	–4674	1029
8	PORT2	–3980	–1089	58	C1+	3419	–1029	–	Dummy25	5374	1080	141	SEG46/51	230	1029	191	SEG96/1	–4774	1029
9	PORT1	–3796	–1089	59	C1–	3550	–1029	–	Dummy26	5274	1080	142	SEG47/50	130	1029	192	COMS2/S2	–4974	1029
10	PORT0	–3612	–1089	60	C1–	3650	–1029	–	Dummy27	5174	1080	143	SEG48/49	30	1029	193	COM40/1	–5074	1029
11	IRQ*	–3428	–1089	61	C1–	3750	–1029	–	Dummy28	5074	1080	144	SEG49/48	–70	1029	194	COM39/2	–5174	1029
12	KST3	–3244	–1089	62	C1–	3850	–1029	–	Dummy29	4974	1080	145	SEG50/47	–170	1029	195	COM38/3	–5274	1029
13	KST2	–3060	–1089	63	VLOUT	3980	–1029	96	SEG1/96	4734	1029	146	SEG51/46	–270	1029	196	COM37/4	–7374	1029
14	KST1	–2876	–1089	64	VLOUT	4080	–1029	97	SEG2/95	4634	1029	147	SEG52/45	–370	1029	197	COM36/5	–5475	1029
15	ST0	–2692	–1089	65	VLOUT	4180	–1029	98	SEG3/94	4533	1029	148	SEG53/44	–471	1029	–	Dummy30	–5675	1080
16	DB7/KIN7	–2508	–1089	66	VLCD	4310	–1029	99	SEG4/93	4433	1029	149	SEG54/43	–571	1029	–	Dummy31	–5775	1080
17	DB6/KIN6	–2325	–1089	67	VLCD	4410	–1029	100	SEG5/92	4333	1029	150	SEG55/42	–671	1029	–	Dummy32	–5875	1080
18	DB5/KIN5	–2141	–1089	68	VLCD	4510	–1029	101	SEG6/91	4233	1029	151	SEG56/41	–771	1029	–	Dummy33	–5975	1080
19	DB4/KIN4	–1957	–1089	69	V1OUT	4690	–1002	102	SEG7/90	4133	1029	152	SEG57/40	–871	1029	–	Dummy34	–6075	1080
20	DB3/KIN3	–1773	–1089	70	V2OUT	4821	–1002	103	SEG8/89	4033	1029	153	SEG58/39	–971	1029				

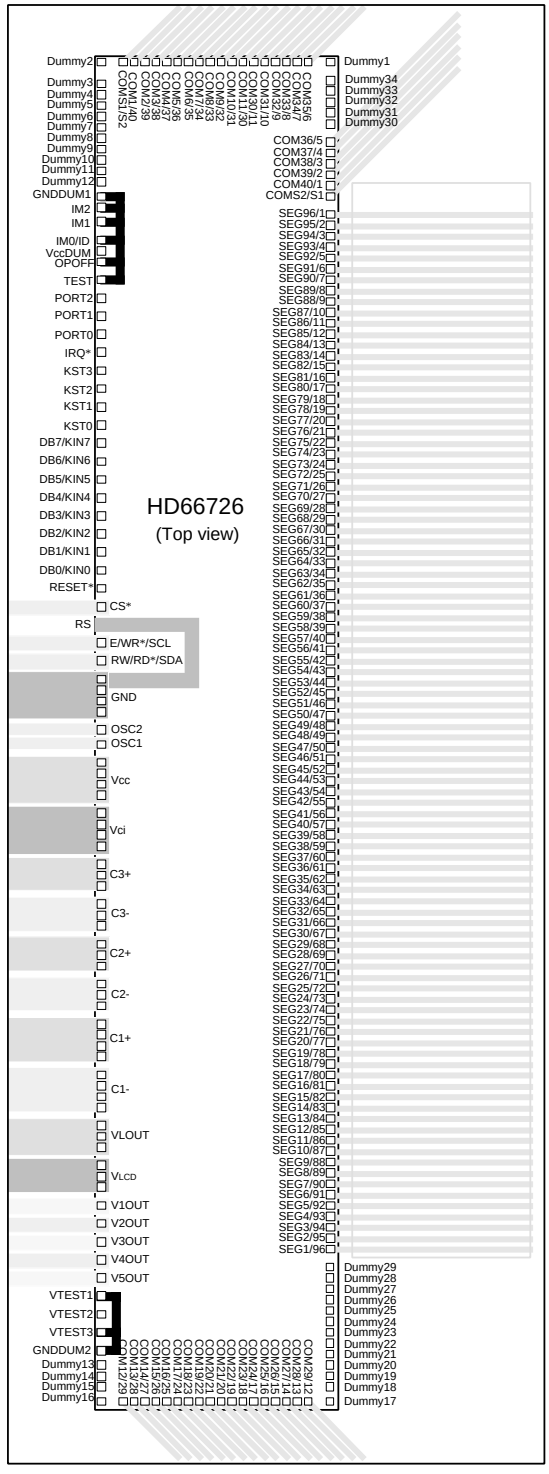
HD66726 Pad Arrangement

- Chip size : 13.13 × 2.51 mm†
- Pad coordinate : Pad center
- Coordinate origin : Chip center
- Pad pitch : 100 µm (min.)
- Au bump size : 70 × 70 µm†
- Au bump height : 20 µm (typ.)
- Al pad size : 80 × 80 µm†

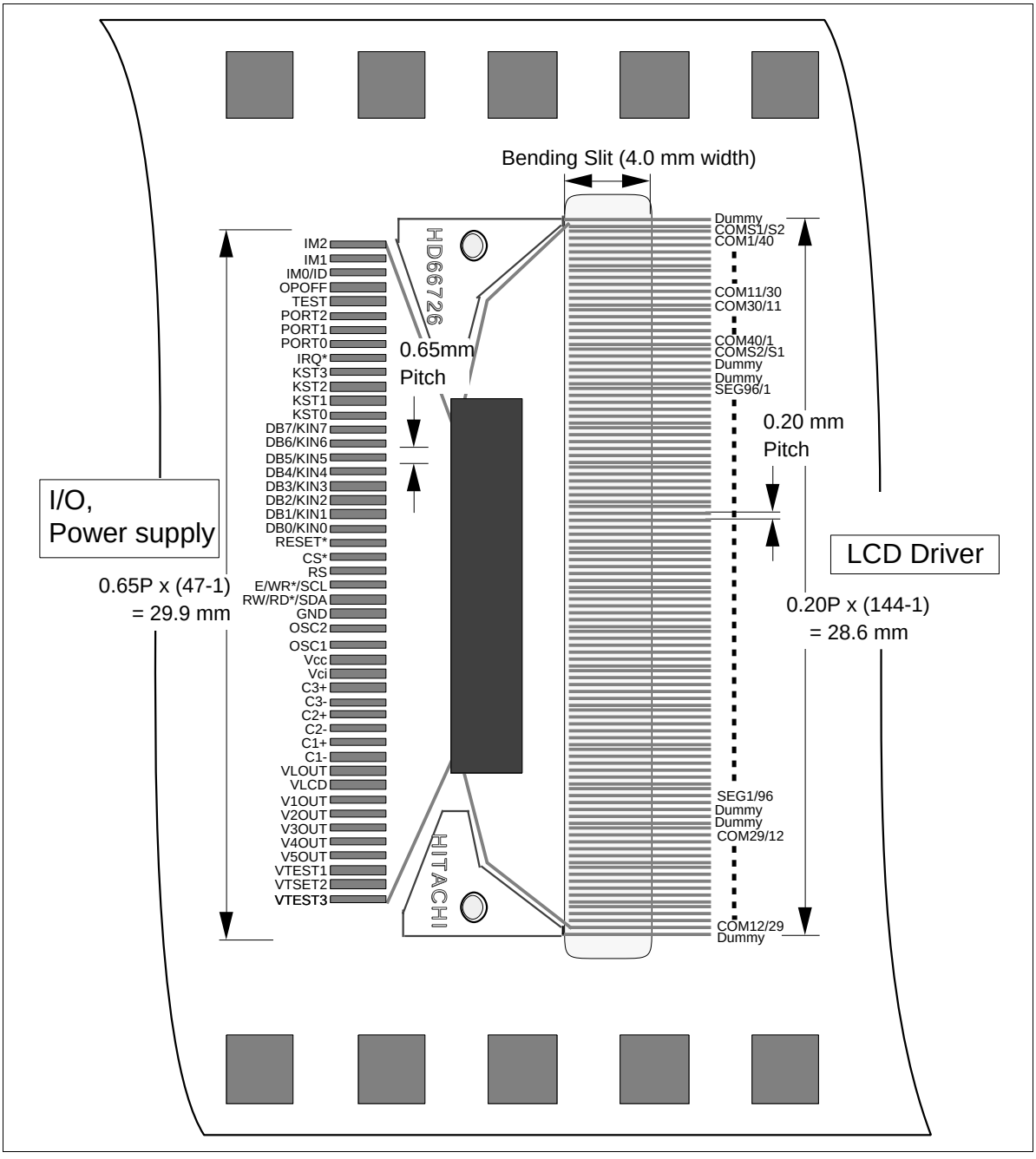


Chip-on-Glass (COG) Routing Example

- Clock-synchronized serial bus
- Unused key scan
- Unused port output
- Quadruple booster
- Internal operational amplifier



TCP Dimensions (HD66726TB0)



Pin Functions

Table 2 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2, IM1	2	I	V_{CC} or GND	Selects the MPU interface mode: IM2 "GND" IM1 "GND" MPU interface: Clock-synchronized serial interface IM2 "GND" IM1 "Vcc" MPU interface: 68-system parallel bus interface IM2 "Vcc" IM1 "GND" MPU interface: Setting inhibited IM2 "Vcc" IM1 "Vcc" MPU interface: 80-system parallel bus interface
IM0/ID	1	I	V_{CC} or GND	Inputs the ID of the device ID code for a serial bus interface. Selects the transfer bus length for a parallel bus interface. GND: 8-bit bus, Vcc: 4-bit bus
CS*	1	I	MPU	Selects the HD66726: Low: HD66726 is selected and can be accessed High: HD66726 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register for a parallel bus interface. Low: Instruction High: RAM access Selects the key scan interrupt method in the standby period for a serial interface. Monitors a total of eight keys connected to KST0 at the GND level and monitors all keys at the Vcc level to generate an interrupt. Must be fixed at the GND or Vcc level.
E/WR*/SCL	1	I	MPU	Inputs the serial transfer clock for a serial interface. Fetches data at the rising edge of a clock. For a 68-system parallel bus interface, serves as an enable signal to activate data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and writes data at the low level.
RW/RD*/ SDA	1	I or I/O	MPU	Serves as the bidirectional serial transfer data for a serial interface. Sends/Receives data. For a 68-system parallel bus interface, serves as a signal to select data read/write operation. For an 80-system parallel bus interface, serves as a write strobe signal and reads data at the low level.
IRQ*	1	O	MPU	Generates the key scan interrupt signal.
KST0– KST3	4	O	Key matrix	Generates strobe signals for latching scanned data from the key matrix at specific time intervals. Available for a serial interface only.
DB0/KIN0– DB7/KIN7	8	I or I/O	Key matrix or MPU	Samples key state from key matrix synchronously with strobe signals for a serial interface. Serves as a bidirectional data bus for a parallel bus interface. For a 4-bit bus, data transfer uses KIN7/DB7-KIN4/DB4; leave KIN3/DB3-KIN0/DB0 disconnected.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
PORT0–PORT2	3	O	General output	General output ports. These ports cannot drive current such as for LEDs or backlighting control. Boost the current using an external transistor.
COMS1/2, COMS2/1	2	O	LCD	Common output signals for segment-icon display.
COM1/40–COM40/1	40	O	LCD	Common output signals for character/graphics display: COM1 to COM8 for the first line, COM9 to COM16 for the second line, COM17 to COM24 for the third line, COM25 to COM32 for the fourth line, and COM33 to COM40 for the fifth line. All the unused pins output unselected waveforms. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The CMS bit can change the shift direction of the common signal. For example, if CMS = 0, COM1/40 is COM1. If CMS = 1, COM1/40 is COM40.
SEG1/96–SEG96/1	96	O	LCD	Segment output signals for segment-icon display and character/graphics display. In the sleep mode (SLP = 1) or standby mode (STB = 1), all pins output GND level. The SGS bit can change the shift direction of the segment signal. For example, if SGS = 0, SEG1/96 is SEG1. If SGS = 1, SEG1/96 is SEG96.
V1OUT–V5OUT	10	I or O	Open or external bleeder-resistor	Used for output from the internal operational amplifiers when they are used (OPOFF = GND); attach a capacitor to stabilize the output. When the amplifiers are not used (OPOFF = V_{CC}), V1 to V5 voltages can be supplied to these pins externally.
V_{LCD}	3	—	Power supply	Power supply for LCD drive. V_{LCD} – GND = 13 V max.
V_{CC}, GND	7	—	Power supply	V_{CC}: +2.2 V to +5.5 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor or clock	For R-C oscillation using an external resistor, connect an external resistor. For R-C oscillation using an internal resistor, connect R1 to R3 to OSC2 and leave OSC1 disconnected. For external clock supply, input clock pulses to OSC1.
Rdummy	3	—	Open	Dummy pad. Must be left disconnected.
Vci	3	I	Power supply	Inputs a reference voltage and supplies power to the booster; generates the liquid crystal display drive voltage from the operating voltage. Vci = 0 V to 4.0 V ≤ V_{CC} Must be left disconnected when the booster is not used.

Table 2 Pin Functional Description (cont)

Signals	Number of Pins	I/O	Connected to	Functions
VLOUT	3	O	V_{LCD} pin/booster capacitance	Potential difference between Vci and GND is single- to quadruple-boosted and then output. Magnitude of boost is selected by instruction.
C1+, C1–	8	—	Booster capacitance	External capacitance should be connected here when using the double, triple, or quadruple booster.
C2+, C2–	8	—	Booster capacitance	External capacitance should be connected here when using the triple or quadruple booster.
C3+, C3–	8	—	Booster capacitance	External capacitance should be connected here when using the quadruple booster.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must reset after power on.
OPOFF	1	I	V_{CC} or GND	Turns the internal operational amplifier off when OPOFF = V_{CC}, and turns it on when OPOFF = GND. If the amplifier is turned off (OPOFF = V_{CC}), V1 to V5 must be supplied to the V1OUT to V5OUT pins.
VccDUM	1	O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM	1	O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
VTEST1	1	I	V_{CC} or GND	Controls LCD driving power of the interval operational amplifier. When VTEST1 = GND, normal power driving mode is selected. And VTEST1 = V_{CC}, high power driving mode is selected.
VTEST2	1	—	Open	Test pin. Must be left disconnected.
VTEST3	1	—	V_{CC} or GND	Adjust the driving ability of the internal LCD operational amplifier. Normal or high power drive mode in the GND side, low-power drive mode in the V_{CC} side.

Block Function Description

System Interface

The HD66726 has five types of system interfaces, and a clock-synchronized serial, a 68-system 4-bit/8-bit bus, and a 80-system 4-bit/8-bit bus. The interface mode is selected by the IM2-0 pins. The key scan of the HD66726 is not available for the 4-bit/8-bit bus interface. Instead, use the clock-synchronized serial interface.

The HD66726 has two 8-bit registers: an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as clear display, display control, and address information for the display data RAM (DDRAM), character generator RAM (CGRAM), and segment RAM (SEGRAM).

The DR temporarily stores data to be written into the DDRAM, CGRAM, or SEGRAM. Data written into the DR from the MPU is automatically written into the DDRAM, CGRAM, or SEGRAM by internal operation. When address information is written into the IR, data is read and then stored in the DR from DDRAM, CGRAM, or SEGRAM by internal operation. Data is read through the DR when reading from the RAM, and the first read data is invalid and the second and the following data are normal. After reading, data in DDRAM, CGRAM, or SEGRAM at the next address is sent to the DR for the next reading from the MPU.

Execution time for instruction excluding clear display is 0 clock cycle and instructions can be written in succession.

Table 3 Register Selection by RS and R/W Bits

R/W Bits	RS Bits	Operations
0	0	IR write as an internal operation
1	0	Read key scan data (SCAN0-3)
0	1	DR write as an internal operation (DR to DDRAM, CGRAM, or SEGRAM)
1	1	DR read as an internal operation (DDRAM, CGRAM, or SEGRAM to DR)

Key Scan Registers (SCAN0 to SCAN3)

The key matrix scanner senses and holds the key states at each rising edge of the key strobe signals that are output by the HD66726. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key status on eight inputs from KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into register SCAN0. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into registers SCAN1 to SCAN3, respectively.

General Output Ports (PORT0 to PORT 2)

The HD66726 has three general output ports. These ports control drive current such as that for LEDs or backlighting by using the current boosted by an external transistor.

Address Counter (AC)

The address counter (AC) assigns addresses to DDRAM, CGRAM, or SEGRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC. Selection of DDRAM, CGRAM, and SEGRAM is also determined concurrently by the RAM select bit (RM1/0).

After writing into (reading from) DDRAM, CGRAM, or SEGRAM, the AC is automatically incremented by 1 (or decremented by 1). The cursor display position is determined by the address counter value.

Display Data RAM (DDRAM)

Display data RAM (DDRAM) stores display data represented in 8-bit character codes in the character display mode. Its capacity is 80 × 8 bits, or 80 characters, which is equivalent to an area of 16 characters × 5 lines. Any number of display lines (LCD drive duty ratio) from 1 to 4 can be selected by software. Here, assignment of DDRAM addresses is the same for all display modes (table 5). The line to be displayed at the top of the display (display-start line) can also be selected by register settings. The graphics display mode does not use data in the DDRAM.

Character Generator ROM (CGROM)

Character generator ROM (CGROM) generates 6 × 8-dot character patterns from 8-bit character codes. It is equipped with a memory bank to generate 240 character patterns or 192 character patterns, switch able according to applications. For details, see the CGROM Bank Switching Function section. Table 6 illustrates the relation between character codes and character patterns for the Hitachi standard CGROM. User-defined character patterns are also available using a mask-programmed ROM (see the Modifying Character Patterns section).

Character Generator RAM (CGRAM)

Character generator RAM (CGRAM) allows the user to redefine the character patterns in the character display mode. Up to 64 character patterns of 6 x 8-dot characters can be simultaneously displayed. DRAM-specified character code can be selected to display one of these user font patterns.

The CGRAM serves as a RAM to store 96 x 40-dot bit pattern data in the graphics display mode. Here, display patterns are directly written into CGRAM. Character codes set in the DDRAM are not used. For details, see the Graphics Display section.

Segment RAM (SEGRAM)

Segment RAM (SEGRAM) is used to enable control of segments such as icons and marks through the user program. Segments and characters are driven by a multiplexing drive method.

SEGRAM has a capacity of 96×2 bits, to control the display of a maximum of 192 icons and marks. While COMS1 and COMS2 outputs are being selected, SEGRAM is read and segments (icons and marks) are displayed by a multiplexing drive method (96 segments each during COMS1 and COMS2 selection).

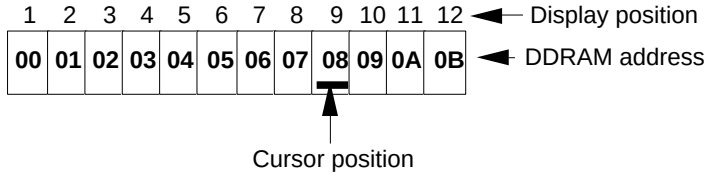
Bits in SEGRAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DDRAM and CGRAM.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DDRAM, CGROM, CGRAM, and SEGRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. This prevents flickering in areas other than the display area when writing data to DDRAM, for example.

Cursor/Blink Controller

The cursor/blink (or black-white reversed) control is used to create a cursor or a flashing area on the display in a position corresponding to the location stored in the address counter (AC).



Note: The cursor/blink or black-white reversed control is also active when the address counter indicates the CGRAM or SEGRAM. However, it has no effect on the display.

Figure 1 Cursor Position and DDRAM Address

Oscillation Circuit (OSC)

The HD66726 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 42 common signal drivers (COM1 to COM40, COMS1, and COMS2) and 96 segment signal drivers (SEG1 to SEG96). When the number of lines are selected by a program, the required common signal drivers automatically output drive waveforms, while the other common signal drivers continue to output unselected waveforms.

Character pattern data is sent serially through a 96-bit shift register and latched when all needed data has arrived. The latched data then enables the segment signal drivers to generate drive waveform outputs.

The shift direction of 96-bit data can be changed by the SGS bit. The shift direction for the common driver can also be changed by the CMS bit by selecting an appropriate direction for the device mounting configuration.

When multiplexing drive is not used, or during the standby or sleep mode, all the above common and segment signal drivers output the GND level, halting the display.

Booster (DC-DC Converter)

The booster doubles, triples, or quadruples a voltage input to the Vci pin. With this, both the internal logic units and LCD drivers can be controlled with a single power supply. Boost output level from single to quadruple boost can be selected by software. For details, see the Power Supply for Liquid Crystal Display Drive section.

V-Pin Voltage Follower

A voltage follower for each voltage level (V1 to V5) reduces current consumption by the LCD drive power supply circuit. No external resistors are required because of the internal bleeder-resistor, which generates different levels of LCD drive voltage. This internal bleeder-resistor can be software-specified from 1/2 bias to 1/8 bias, according to the liquid crystal display drive duty value. The voltage followers can be turned off while multiplexing drive is not being used. For details, see the Power Supply for Liquid Crystal Display Drive section.

Contrast Adjuster

The contrast adjuster can be used to adjust LCD contrast in 32 steps by varying the LCD drive voltage by software. This can be used to select an appropriate LCD brightness or to compensate for temperature.

DDRAM Address Map

Table 4 DDRAM Addresses and Display Positions

Display Line	1st Char.	2nd Char.	3rd Char.	4th Char.	5th Char.	6th Char.	7th Char.	8th Char.	9th Char.	10th Char.	11th Char.	12th Char.	13th Char.	14th Char.	15th Char.	16th Char.
1st	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
2nd	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
3rd	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F
4th	30	31	32	33	34	35	36	37	38	39	3A	3B	3C	3D	3E	3F
5th	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

Note: When SGS = 0, SEG 1/96 to SEG 6/91 appear at the first character at the extreme left of the screen.
When SGS = 1, SEG 96/1 to SEG 91/6 appear at the first character at the extreme left of the screen.

Table 5 Display-line Modes, Display-start Line, and DDRAM Addresses

			Display-start Lines				
Display-line Mode	**Duty Ratio**	**Common Pins**	**1st Line (SN = 000)**	**2nd Line (SN = 001)**	**3rd Line (SN = 010)**	**4th Line (SN = 011)**	**5th Line (SN = 100)**
1-line (NL = 001)	1/10	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
2-line (NL = 010)	1/18	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
2-line (NL = 010)	1/18	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
3-line (NL = 011)	1/26	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
3-line (NL = 011)	1/26	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
3-line (NL = 011)	1/26	COM17–COM24	20H–2FH	30H–3FH	40H–4FH	00H–0FH	10H–1FH
4-line (NL = 100)	1/34	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
4-line (NL = 100)	1/34	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
4-line (NL = 100)	1/34	COM17–COM24	20H–2FH	30H–3FH	40H–4FH	00H–0FH	10H–1FH
4-line (NL = 100)	1/34	COM25–COM32	30H–3FH	40H–4FH	00H–0FH	10H–1FH	20H–2FH
5-line (NL = 101)	1/42	COM1–COM8	00H–0FH	10H–1FH	20H–2FH	30H–3FH	40H–4FH
5-line (NL = 101)	1/42	COM9–COM16	10H–1FH	20H–2FH	30H–3FH	40H–4FH	00H–0FH
5-line (NL = 101)	1/42	COM17–COM24	20H–2FH	30H–3FH	40H–4FH	00H–0FH	10H–1FH
5-line (NL = 101)	1/42	COM25–COM32	30H–3FH	40H–4FH	00H–0FH	10H–1FH	20H–2FH
5-line (NL = 101)	1/42	COM33–COM40	40H–4FH	00H–0FH	10H–1FH	20H–2FH	30H–3FH

Table 6 CGROM Memory Bank 0 (ROM Bit = 0)

Upper bits / Lower bits	x 0	x 1	x 2	x 3	x 4	x 5	x 6	x 7	x 8	x 9	x A	x B	x C	x D	x E	x F
0 y	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (9)	CGRAM (10)	CGRAM (11)	CGRAM (12)	CGRAM (13)	CGRAM (14)	CGRAM (15)	CGRAM (16)
1 y																
2 y																
3 y																
4 y																
5 y																
6 y																
7 y																
8 y																
9 y																
A y																
B y																
C y																
D y																
E y																
F y																

Table 7 CGROM Memory Bank 1 (ROM Bit = 1)

Upper bits \ Lower bits	x 0	x 1	x 2	x 3	x 4	x 5	x 6	x 7	x 8	x 9	x A	x B	x C	x D	x E	x F
0 y	CGRAM (1)	CGRAM (2)	CGRAM (3)	CGRAM (4)	CGRAM (5)	CGRAM (6)	CGRAM (7)	CGRAM (8)	CGRAM (9)	CGRAM (10)	CGRAM (11)	CGRAM (12)	CGRAM (13)	CGRAM (14)	CGRAM (15)	CGRAM (16)
1 y	CGRAM (17)	CGRAM (18)	CGRAM (19)	CGRAM (20)	CGRAM (21)	CGRAM (22)	CGRAM (23)	CGRAM (24)	CGRAM (25)	CGRAM (26)	CGRAM (27)	CGRAM (28)	CGRAM (29)	CGRAM (30)	CGRAM (31)	CGRAM (32)
2 y																
3 y																
4 y																
5 y																
6 y																
7 y																
8 y	CGRAM (33)	CGRAM (34)	CGRAM (35)	CGRAM (36)	CGRAM (37)	CGRAM (38)	CGRAM (39)	CGRAM (40)	CGRAM (41)	CGRAM (42)	CGRAM (43)	CGRAM (44)	CGRAM (45)	CGRAM (46)	CGRAM (47)	CGRAM (48)
9 y	CGRAM (49)	CGRAM (50)	CGRAM (51)	CGRAM (52)	CGRAM (53)	CGRAM (54)	CGRAM (55)	CGRAM (56)	CGRAM (57)	CGRAM (58)	CGRAM (59)	CGRAM (60)	CGRAM (61)	CGRAM (62)	CGRAM (63)	CGRAM (64)
A y																
B y																
C y																
D y																
E y																
F y																

CGRAM Address Map

Table 8 Relationship between Character Code in Character Display Mode (GR = 0) and CGRAM (1) (RM1/0 = 10) Address

Font Bank	Memory Bank: ROM = 0, 1															
Character Code	"00"H	"01"H	"02"H	"03"H	"04"H	"05"H	"06"H	"07"H	"08"H	"09"H	"0A"H	"0B"H	"0C"H	"0D"H	"0E"H	"0F"H
CGRAM Address (HEX)	000 to 005	006 to 00B	00C to 011	012 to 017	018 to 01D	01E to 023	024 to 029	02A to 02F	030 to 035	036 to 03B	03C to 041	042 to 047	048 to 04D	04E to 053	054 to 059	05A to 05F
Font Bank	Memory Bank: ROM = 1															
Character Code	"10"H	"11"H	"12"H	"13"H	"14"H	"15"H	"16"H	"17"H	"18"H	"19"H	"1A"H	"1B"H	"1C"H	"1D"H	"1E"H	"1F"H
CGRAM Address (HEX)	100 to 105	106 to 10B	10C to 111	112 to 117	118 to 11D	11E to 123	124 to 129	12A to 12F	130 to 135	136 to 13B	13C to 141	142 to 147	148 to 14D	14E to 153	154 to 159	15A to 15F
Font Bank	Memory Bank: ROM = 1															
Character Code	"80"H	"81"H	"82"H	"83"H	"84"H	"85"H	"86"H	"87"H	"88"H	"89"H	"8A"H	"8B"H	"8C"H	"8D"H	"8E"H	"8F"H
CGRAM Address (HEX)	200 to 205	206 to 20B	20C to 211	212 to 217	218 to 21D	21E to 223	224 to 229	22A to 22F	230 to 235	236 to 23B	23C to 241	242 to 247	248 to 24D	24E to 253	254 to 259	25A to 25F
Font Bank	Memory Bank: ROM = 1															
Character Code	"90"H	"91"H	"92"H	"93"H	"94"H	"95"H	"96"H	"97"H	"98"H	"99"H	"9A"H	"9B"H	"9C"H	"9D"H	"9E"H	"9F"H
CGRAM Address (HEX)	300 to 305	306 to 30B	30C to 311	312 to 317	318 to 31D	31E to 323	324 to 329	32A to 32F	330 to 335	336 to 33B	33C to 341	342 to 347	348 to 34D	34E to 353	354 to 359	35A to 35F

Notes: 1. In the character display mode (GR = 0), RM1/0 = 10 is set and CGRAM (1) is used.

2. In the character display mode (GR = 0), the CGRAM font pattern is displayed using character codes set to the DDRAM as per the above table. In the graphics display mode (GR = 1), the CGRAM data is displayed irrespective of the DDRAM set data (character code).

3. When the memory bank switching bit generates ROM = 0, CGRAM fonts for 16 character codes "00"H to "0F"H can be displayed. When ROM = 1, CGRAM fonts for 64 character codes "00"H to "1F"H and "80"H to "9F"H can be displayed.

Table 9 Relationship between CGRAM Address and Character Pattern (CGRAM Data)

Character Code	"00"H						"01"H								"8F"H					
CGRAM Address	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	-------	35A	35B	35C	35D	35E	35F
DB0	0	0	1	1	1	0	0	1	1	1	1	0	0	-------	0	1	1	1	1	1
DB1	0	1	0	0	0	1	0	1	0	0	0	1	0	-------	0	1	0	0	0	0
DB2	0	1	0	0	0	1	0	1	0	0	0	1	0	-------	0	1	0	0	0	0
DB3	0	1	0	0	0	1	0	1	1	1	1	0	0	-------	0	1	1	1	1	0
DB4	0	1	1	1	1	1	0	1	0	0	0	1	0	-------	0	1	0	0	0	0
DB5	0	1	0	0	0	1	0	1	0	0	0	1	0	-------	0	1	0	0	0	0
DB6	0	1	0	0	0	1	0	1	1	1	1	0	0	-------	0	1	0	0	0	0
DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	-------	0	0	0	0	0	0

Notes: 1. The least significant bit (LSB) of the write data is displayed on the first line. The most significant bit (MSB) is displayed on the 8th raster-row.
2. The 8th raster-row is the cursor position and its display is formed by a logical OR with the cursor.
3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 10 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1) (CGRAM (1): RM1/0 = "10")

Segment Driver		SEG1/96	SEG2/95	SEG3/94	SEG4/93	SEG5/92	SEG6/91	SEG7/90	SEG8/89	SEG9/88	SEG10/87	SEG11/86	SEG12/85	SEG13/84	SEG14/83	SEG15/82	SEG16/81	SEG17/80	--	SEG92/5	SEG93/4	SEG94/3	SEG95/2	SEG96/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	...	05B	05C	05D	05E	05F	(HEX)
	SGS="1"	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	...	004	003	002	001	000	
	DB0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM1
	DB1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	...	0	1	1	0	0	COM2
	DB2	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	...	0	0	1	0	0	COM3
	DB3	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	0	1	0	0	COM4
	DB4	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM5
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	1	0	0	COM6
	DB6	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	...	0	1	1	1	0	COM7
	DB7	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	...	0	0	0	0	0	COM8
Address	SGS="0"	100	101	102	103	104	105	106	107	108	109	10A	10B	10C	10D	10E	10F	110	...	15B	15C	15D	15E	15F	(HEX)
	SGS="1"	15F	15E	15D	15C	15B	15A	159	158	157	156	155	154	153	152	151	150	14F	...	104	103	102	101	100	
	DB0	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	..	0	1	1	1	0	COM9
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	..	1	0	0	0	1	COM10
	DB2	0	0	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	..	0	0	0	0	1	COM11
	DB3	0	0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	..	0	0	0	1	0	COM12
	DB4	0	0	0	0	1		0	0	1	0	0	0	1	0	0	0	0	..	0	0	1	0	0	COM13
	DB5	0	0	0	1	0	0	0	0	1	0	0	0	0	1	0	0	0	..	0	1	0	0	0	COM14
	DB6	0	1	1	0	0	0	0	0	1	0	0	0	0	0	1	1	0	..	1	1	1	1	1	COM15
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	..	0	0	0	0	0	COM16
Address	SGS="0"	200	201	202	203	204	205	206	207	208	209	20A	20B	20C	20D	20E	20F	210	..	25B	25C	25D	25E	25F	(HEX)
	SGS="1"	25F	25E	25D	25C	25B	25A	259	258	257	256	255	254	253	252	251	250	24F	..	204	203	202	201	200	
	DB0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	..	1	1	1	1	1	COM17
	DB1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	..	0	0	0	1	0	COM18
	DB2	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	1	0	0	COM19
	DB3	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	0	1	0	COM20
	DB4	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	0	0	1	COM21
	DB5	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	1	0	0	0	1	COM22
	DB6	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	1	1	1	0	COM23
	DB7	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	..	0	0	0	0	0	COM24
Address	SGS="0"	300	301	302	303	304	305	306	307	308	309	30A	30B	30C	30D	30E	30F	310	..	35B	35C	35D	35E	35F	(HEX)
	SGS="1"	35F	35E	35D	35C	35B	35A	359	358	357	356	355	354	353	352	351	350	34F	..	304	303	302	301	300	
	DB0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	0	1	0	COM25
	DB1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	1	1	0	COM26
	DB2	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	1	0	1	0	COM27
	DB3	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	1	0	0	1	0	COM28
	DB4	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	1	1	1	1	1	COM29
	DB5	0	0	0	1	1	1	1	1	1	1	1	1	1	1	0	0	0	..	0	0	0	1	1	COM30
	DB6	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	..	0	0	0	1	0	COM31
	DB7	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	..	0	0	0	0	0	COM32

Notes: 1. When the RM1/0 bit is set to "10", CGRAM (1) can be selected.

2. In the graphics display mode (GR = 1), the CGRAM data is displayed irrespective of the DDRAM set data.

3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

Table 11 Relationship between Display Position and CGRAM Address in Graphics Display Mode (GR = 1) (CGRAM (2): RM1/0 = "01")

Segment Driver		SEG1/96	SEG2/95	SEG3/94	SEG4/93	SEG5/92	SEG6/91	SEG7/90	SEG8/89	SEG9/88	SEG10/87	SEG11/86	SEG12/85	SEG13/84	SEG14/83	SEG15/82	SEG16/81	SEG17/80	--	SEG92/5	SEG93/4	SEG94/3	SEG95/2	SEG96/1	Segment / Common
Address	SGS="0"	000	001	002	003	004	005	006	007	008	009	00A	00B	00C	00D	00E	00F	010	...	05B	05C	05D	05E	05F	(HEX)
	SGS="1"	05F	05E	05D	05C	05B	05A	059	058	057	056	055	054	053	052	051	050	04F	...	004	003	002	001	000	
	DB0	0	1	1	0	0	0	1	1	0	0	0	1	1	1	1	1		...	1	1	1	1	1	COM33
	DB1	1	1	1	1	0	1	1	1	1	0	1	0	0	0	0	0	1	...	1	0	0	0	0	COM34
	DB2	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	0	0	...	1	1	1	1	0	COM35
	DB3	1	1	1	1	1	1	1	1	1	0	0	1	1	1	1	1	0	...	0	0	0	0	1	COM36
	DB4	1	1	1	1	1	1	1	1	1	0	1	1	1	0	1	1	1	...	0	0	0	0	1	COM37
	DB5	0	1	1	1	1	1	1	1	0	0	1	1	0	0	0	1	1	...	1	0	0	0	1	COM38
	DB6	0	0	1	1	1	1	1	0	0	0	1	1	1	0	1	1	1	...	0	1	1	1	0	COM39
	DB7	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	0	...	0	0	0	0	0	COM40

Notes: 1. When the RM1/0 bit is set to "01", CGRAM (2) can be selected.

2. In the graphics display mode (GR = 1), CGRAM data is displayed irrespective of the DDRAM set data.

3. A set bit in CGRAM data 1 corresponds to display selection (lit) and 0 to non-selection (unlit).

SEGRAM Address Map

Table 12 Relationship between SEGRAM Address and Screen Display Position

Segment Driver		SEG1/96	SEG2/95	SEG3/94	SEG4/93	SEG5/92	SEG6/91	SEG7/90	SEG8/89	SEG9/88	SEG10/87	SEG11/86	SEG12/85	SEG13/84	SEG14/83	SEG15/82	SEG16/81	SEG17/80	...	SEG92/5	SEG93/4	SEG94/3	SEG95/2	SEG96/1	Segment / Common
Address	SGS="0"	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	...	5B	5C	5D	5E	5F	(HEX)
	SGS="1"	5F	5E	5D	5C	5B	5A	59	58	57	56	55	54	53	52	51	50	4F	...	04	03	02	01	00	
	DB0	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COMS1
	DB1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	
	DB2	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	
	DB3	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	
	DB4	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	COMS2
	DB5	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	
	DB6	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	
	DB7	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	...	0/1	0/1	0/1	0/1	0/1	

Table 13 Relationship between Segment Driver Output Pin and Segment Display Function

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/96, SEG4/93, SEG7/90, SEG10/87, SEG13/84, SEG16/81, SEG19/78, SEG22/75, SEG25/72, SEG28/69, SEG31/66, SEG34/63, SEG37/60, SEG40/57, SEG43/54, SEG46/51, SEG49/48, SEG52/45, SEG55/42, SEG58/39, SEG61/36, SEG64/33, SEG67/30, SEG70/27, SEG73/24, SEG76/21, SEG79/18, SEG82/15, SEG85/12, SEG88/9, SEG91/6, SEG94/3	SEG96/1, SEG93/4, SEG90/7, SEG87/10, SEG84/13, SEG81/16, SEG78/19, SEG75/22, SEG72/25, SEG69/28, SEG66/31, SEG63/34, SEG60/37, SEG57/40, SEG54/43, SEG51/46, SEG48/49, SEG45/52, SEG42/55, SEG39/58, SEG36/61, SEG33/64, SEG30/67, SEG27/70, SEG24/73, SEG21/76, SEG18/79, SEG15/82, SEG12/85, SEG9/88, SEG6/91, SEG3/94	Grayscale segment display allowed (Reflective color segment supported)
Output pins other than above	Output pins other than above	Segment blinking allowed

Note: For details, see the Reflective Color Mark/Blink Mark Display section.

Table 14 Relationship between SEGRAM Data and Grayscale Control Segment Display

SEGRAM Data Setting				Effective Applied Voltage for COMS1 Segment	SEGRAM Data Setting				Effective Applied Voltage for COMS2 Segment
DB3	DB2	DB1	DB0		DB7	DB6	DB5	DB4	
0	0	0	0	0 (Always unlit)	0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)	0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)	0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)	0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)	0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)	0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)	0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)	0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display)*	1	0	0	0	(Blink display)*
1	0	0	1	0.53 (Grayscale display)	1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)	1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)	1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)	1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)	1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)	1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)	1	1	1	1	0.72 (Grayscale display)

Note: Blinking is provided by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.

Table 15 Relationship between SEGRAM Data and Blinking Control Segment Display (Blinking Control Segment Driver)

SEGRAM Data Setting				LCD Display Control for COMS1 Segment	SEGRAM Data Setting				LCD Display Control for COMS2 Segment
DB3	DB2	DB1	DB0		DB7	DB6	DB5	DB4	
0	*[1]	*[1]	0	0 (Always unlit)	0	*[1]	*[1]	0	0 (Always unlit)
0	*[1]	*[1]	1	1 (Always lit)	0	*[1]	*[1]	1	1 (Always lit)
1	*[1]	*[1]	0	Blinking display	1	*[1]	*[1]	0	Blinking display
1	*[1]	*[1]	1	Double-speed blinking display	1	*[1]	*[1]	1	Double-speed blinking display

Notes: 1. 0 or 1.
2. Blinking is provided by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.
3. Double-speed blinking is provided by repeatedly turning on the segment for 16 frames and turning it off for the next 16 frames.

Modifying Character Patterns

Character Pattern Development Procedure

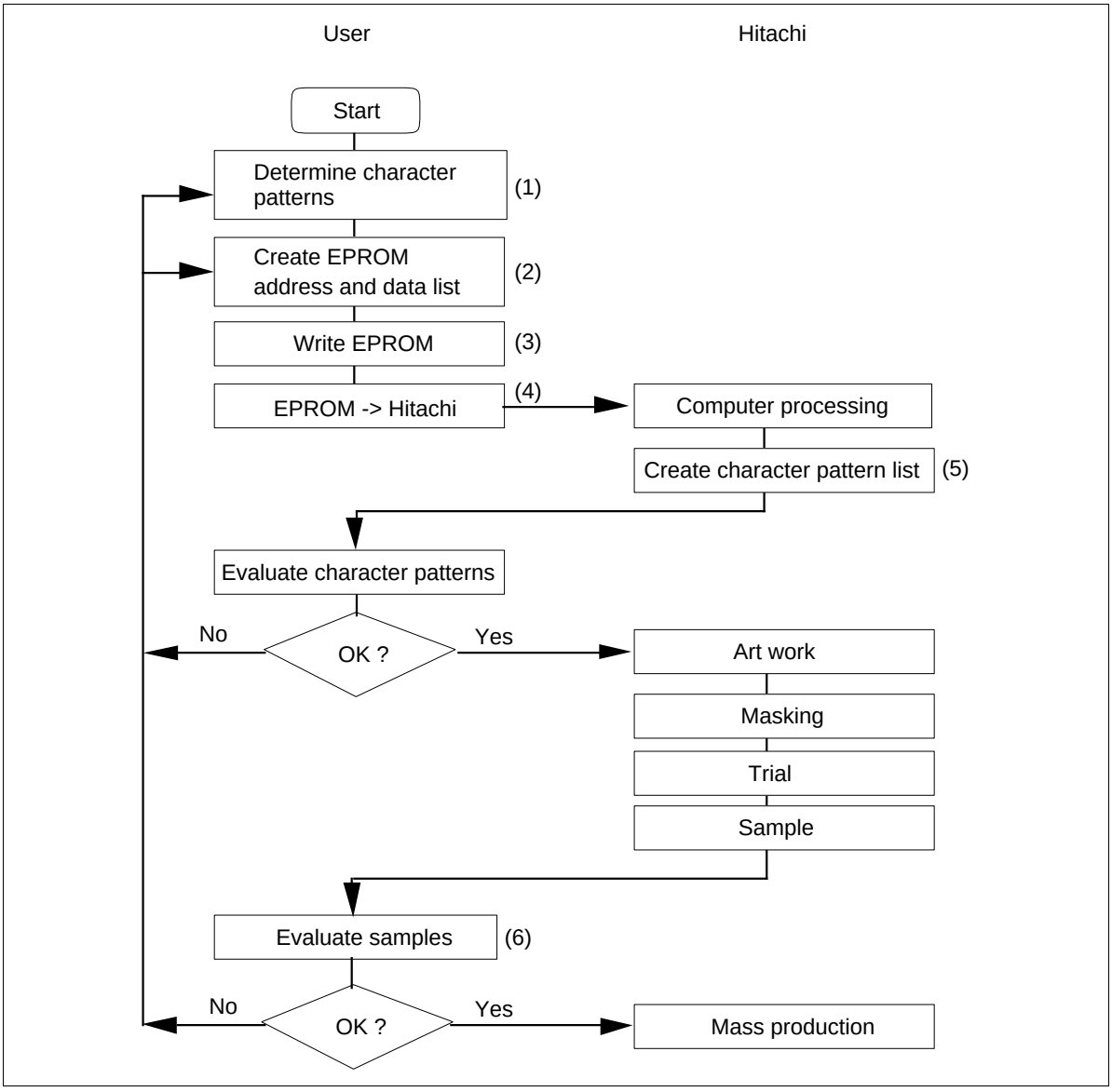


Figure 2 Character Pattern Development Procedure

The following operations correspond to the numbers listed in figure 2:

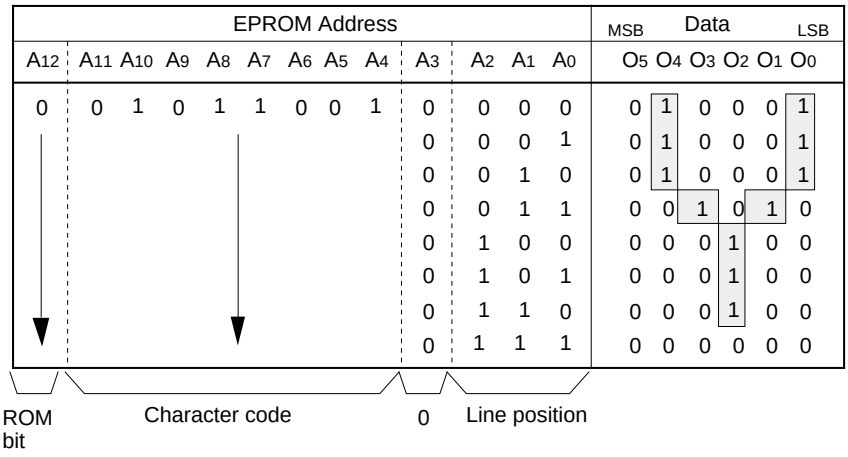
1. Determine the correspondence between character codes and character patterns.
2. Create a list indicating the correspondence between EPROM addresses and data.
3. Program the character patterns into an EPROM.
4. Send the EPROM to Hitachi.
5. Computer processing of the EPROM is performed at Hitachi to create a character pattern list, which is sent to the user.
6. If there are no problems within the character pattern list, a trial LSI is created at Hitachi and samples are sent to the user for evaluation. When the user confirms that the character patterns are correctly written, Hitachi will start LSI mass production.

Programming Character Patterns

This section explains the correspondence between addresses and data used for program character patterns in EPROM.

Programming to EPROM: The HD66726 character generator ROM can generate 432 6 × 8-dot character patterns. Table 16 shows the correspondence between the EPROM address, data, and the character pattern.

Table 16 Examples of Correspondence between EPROM Address, Data, and Character Pattern (6 × 8 Dots)



Notes:
1. EPROM address: Bit A12 corresponds to the CGROM memory bank switch bit ("ROM").
2. EPROM address: Bits A11 to A4 correspond to a character code.
3. EPROM address: Bits A2 to A0 specify the line position of the character pattern.
   EPROM address: Bit A3 must be set to 0.
4. EPROM data: Bits O5 to O0 correspond to character pattern data.
5. Areas which are lit (indicated by shading) are stored as 1, and unlit areas as 0.
6. The eighth raster-row is also stored in the CGROM, and must also be programmed. If the eighth raster-row is used for a cursor, this data must all be set to zero.
7. EPROM data: Bits O7 to O6 are invalid. 0 must be written in all bits.

Handling Unused Character Patterns:

1. EPROM data outside the character pattern area: This is ignored by character generator ROM for display operation so any data is acceptable.
2. EPROM data in CGRAM area: Always fill with zeros.
3. Treatment of unused user patterns in the HD66726 EPROM: Depending on to the user application, these are handled in either of two ways:
   a. When unused character patterns are not programmed: If an unused character code is written into DDRAM, all its dots are lit, because the EPROM is filled with 1s after it is erased.
   b. When unused character patterns are programmed as 0s: Nothing is displayed even if unused character codes are written into DDRAM. (This is equivalent to a space.)

Instructions

Outline

Only the instruction register (IR) and the data register (DR) of the HD66726 can be controlled by the MPU. Before starting internal operation of the HD66726, control information is temporarily stored in these registers to allow interfacing with various peripheral control devices or MPUs which operate at different speeds. The internal operation of the HD66726 is determined by signals sent from the MPU. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signal (DB0 to DB7), make up the HD66726 instructions. There are five categories of instructions that:

- Control the display
- Control power management
- Set internal RAM addresses
- Transfer data with the internal RAM
- Control key scan (when serial interface mode)

Normally, instructions that perform data transfer with the internal RAM are used the most. However, auto-incrementation by 1 (or auto-decrementation by 1) of internal HD66726 RAM addresses after each data write can lighten the MPU program load.

Because instructions other than clear display instruction are executed in 0 cycle, instructions can be written in succession.

While the clear display instruction is being executed for internal operation, or during reset, no instruction other than the key scan read instruction can be executed.

Instruction Descriptions

Key Scan Data Read

In the serial interface mode, the key scan data read instruction reads scan data in scan registers SCAN0 to SCAN3. Following transfer of the start byte, scan data read operation starts from scan register SCAN0 and proceeds in the order of SCAN1, SCAN2, and SCAN3. When data read from SCAN 0 to SCAN3 is complete, the operation starts from SCAN0 again. For details, see the Key Scan Control section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	**SD7**	**SD6**	**SD5**	**SD4**	**SD3**	**SD2**	**SD1**	**SD0**

Figure 3 Key Scan Data Read Instruction

Clear Display

The clear display instruction writes space code 20H (character pattern for character code 20H must be a blank pattern) into all DDRAM addresses. It then sets DDRAM address 0 into the address counter (AC). It also sets I/D to 1 (increment mode) in the entry mode set instruction. Since the execution time of this instruction is 85 clock cycles, do not transfer the next instruction during this time.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Figure 4 Clear Display Instruction

Return Home

The return home instruction sets DDRAM address 0 into the address counter. The DDRAM contents do not change. The cursor or blinking goes to the top left of the display.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Figure 5 Return Home Instruction

Start Oscillation

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**

Figure 6 Start Oscillation Instruction

Driver Output Control

CMS: Selects the output shift direction of a common driver. When CMS = "0", COM1/40 shifts to COM1, and COM40/1 to COM40. When CMS = "1", COM1/40 shifts to COM40, and COM40/1 to COM1. Output position of a common driver shifts depending on the CEN bit setting. For details, see the Display On/Off Control section.

SGS: Selects the output shift direction of a segment driver. When SGS = "0", SEG1/96 shifts to SEG1, and SEG96/1 to SEG96. When SGS = "1", SEG1/96 shifts SEG96, and SEG96/1 to SEG1.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**0**	**1**	**CMS**	**SGS**

Figure 7 Driver Output Control Instruction

Power Control

AMP: When AMP = 1, each voltage follower for V1 to V5 pins and the booster are turned on. When AMP = 0, current consumption can be reduced while the display is not being used.

SLP: When SLP = 1, the HD66726 enters the sleep mode, where the internal operations are halted except for the key scan function and the R-C oscillator, thus reducing current consumption. For details, see the Sleep Mode section. Only the following instructions can be executed during the sleep mode.

a. Key scan data read
b. Key scan control (IRE, KF1/0 bit)
c. Power control (AMP, SLP, and STB bits)
d. Port control (PT2-0 bits)

During the sleep mode, the other RAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66726 enters the standby mode, where display operation and key scan completely stops, halting all the internal operations including the internal R-C oscillator. Further, no

external clock pulses are supplied. This setting can be used as the system wake-up, because an interrupt is generated when a specific key is pressed. For details, see the Standby Mode section.

Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = 0)
b. Voltage follower circuit on/off (AMP = 1/0)
c. Start oscillation
d. Key scan interrupt generation enabled/disabled (IRE = 1/0)
e. Port control (PT2-0 bits)

During the standby mode, the other RAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**0**	**0**	**1**	**AMP**	**SLP**	**STB**

Figure 8 Power Control Instruction

Contrast Control 1/2

SW: Switches the bit configuration for the contrast control instruction. SW = 0 corresponds to CT4 to CT0. SW = 1 corresponds to BT1/0 and BS2 to BS0.

CT4–CT0: When SW = 0, they control the LCD drive voltage (potential difference between V1 and GND) to adjust contrast. A 32-step adjustment is possible. For details, see the Contrast Adjuster section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
0	0	**0**	**0**	**0**	**1**	**0**	**SW**	**CT4**	**CT3**	(SW = 0)
								BT1	**BT0**	(SW = 1)
0	0	**0**	**0**	**0**	**1**	**1**	**CT2**	**CT1**	**CT0**	(SW = 0)
							BS2	**BS1**	**BS0**	(SW = 1)

Figure 9 Contrast Control 1/2 Instruction

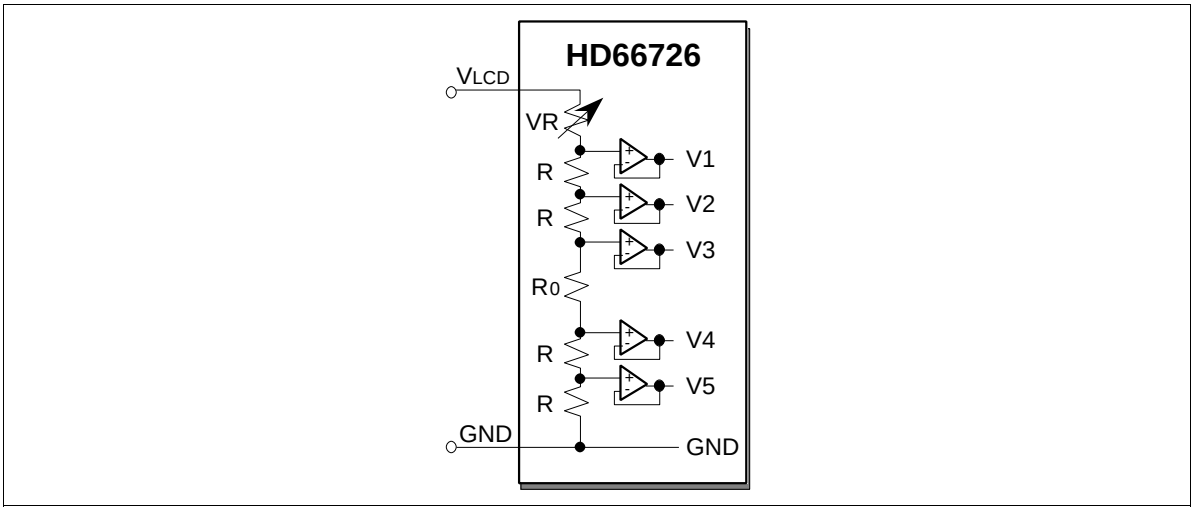


Figure 10 Contrast Adjuster

Table 17 CT Bits and Variable Resistor Value of Contrast Adjuster

CT Set Value					Variable	CT Set Value					Variable
CT4	CT3	CT2	CT1	CT0	Resistor (VR)	CT4	CT3	CT2	CT1	CT0	Resistor (VR)
0	0	0	0	0	3.2 x R	1	0	0	0	0	1.6 x R
0	0	0	0	1	3.1 x R	1	0	0	0	1	1.5 x R
0	0	0	1	0	3.0 x R	1	0	0	1	0	1.4 x R
0	0	0	1	1	2.9 x R	1	0	0	1	1	1.3 x R
0	0	1	0	0	2.8 x R	1	0	1	0	0	1.2 x R
0	0	1	0	1	2.7 x R	1	0	1	0	1	1.1 x R
0	0	1	1	0	2.6 x R	1	0	1	1	0	1.0 x R
0	0	1	1	1	2.5 x R	1	0	1	1	1	0.9 x R
0	1	0	0	0	2.4 x R	1	1	0	0	0	0.8 x R
0	1	0	0	1	2.3 x R	1	1	0	0	1	0.7 x R
0	1	0	1	0	2.2 x R	1	1	0	1	0	0.6 x R
0	1	0	1	1	2.1 x R	1	1	0	1	1	0.5 x R
0	1	1	0	0	2.0 x R	1	1	1	0	0	0.4 x R
0	1	1	0	1	1.9 x R	1	1	1	0	1	0.3 x R
0	1	1	1	0	1.8 x R	1	1	1	1	0	0.2 x R
0	1	1	1	1	1.7 x R	1	1	1	1	1	0.1 x R

BT1-0: When SW = 1, they switch the output of V5OUT between single, double, triple, and quadruple boost. The liquid crystal display drive voltage level can be selected according to its drive duty ratio and bias. A lower amplification of the booster consumes less current.

BS2-0: When SW = 1, they set the crystal display drive bias value within the range of 1/2 to 1/8 bias. The liquid crystal display drive bias value can be selected according to its drive duty ratio and voltage. For details, see the Liquid Crystal Display Drive Bias Selector Circuit section.

Table 18 BT Bits and Output Level

BT1	BT0	V5OUT Output Level
0	0	Single boost (no boost)
0	1	Double boost
1	0	Triple boost
1	1	Quadruple boost

Table 19 BS Bits and LCD Drive Bias Value

BS2	BS1	BS0	Liquid Crystal Display Drive Bias Value
0	0	0	1/8 bias drive
0	0	1	1/7 bias drive
0	1	0	1/6 bias drive
0	1	1	1/5.5 bias drive
1	0	0	1/5 bias drive
1	0	1	1/4.5 bias drive
1	1	0	1/4 bias drive
1	1	1	1/2 bias drive

Entry Mode

REV: Displays all character and graphics display sections except for the segment display section with black-white reversal. For details, see the Reversed Display Function section.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DDRAM address by 1 when a character code is written into or read from DDRAM. The cursor or blinking moves to the right when incremented by 1 and to the left when decremented by 1. The same applies to the writing and reading of CGRAM and SEGRAM.

GR: Activates the character mode when GR = 0. Displays the font pattern on the CGROM or CGRAM according to the character code written in the DDRAM. Activates the graphics mode when GR = 1. Displays a given pattern according to the bit map data written in the CGRAM. In this case, data in the DDRAM is not used for display. Segment pattern display set to the SEGRAM is enabled both in the character mode and graphics mode. For details, see the Graphics Display Function section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**0**	**0**	**REV**	**I/D**	**GR**

Figure 11 Entry Mode Set Instruction

Cursor Control

B/W: When B/W = 1 and LC = 1, the character at the cursor position is cyclically (every 32 frames) blink-displayed with black-white reversal.

When B/W = 1 and LC = 1, all characters including the cursor on the display line appear with black-white reversal. The characters do not blink. For details, see the Line-cursor Display section.

C: The cursor is displayed on the 8th raster-row when C = 1. The 6-dot cursor is ORed with the character pattern and displayed on the 8th raster-row.

B: The character indicated by the cursor blinks when B = 1. The blinking is displayed as switching between all black dots and displayed characters every 32 frames. The cursor and blinking can be set to display simultaneously. When LC =1, setting B = 1 alternately displays all white dots and character pattern in a line unit.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**0**	**1**	**B/W**	**C**	**B**

Figure 12 Cursor Control Instruction

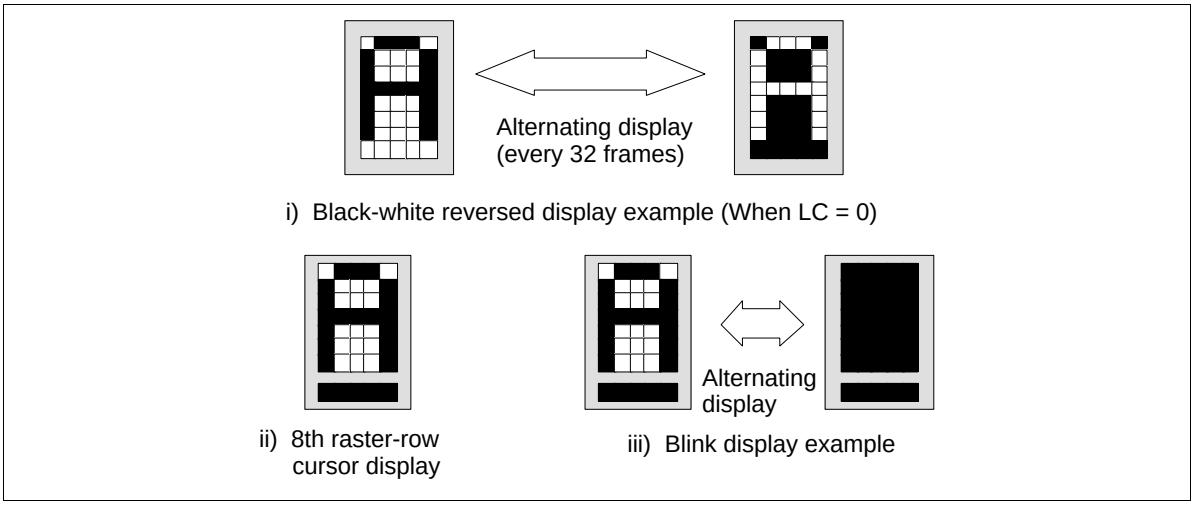


Figure 13 Cursor Control Examples

Display On/Off Control

D: Display is on when D = 1 and off when D = 0. When off, the display data remains in the DDRAM, and can be displayed instantly by setting D = 1. When D is 0, the display is off with the SEG1 to SEG96 outputs, COM1 to COM40 outputs, and COMS1/2 output set to the GND level and off. Because of this, the HD66726 can control charging current for the LCD with AC driving.

CEN: Switches the COM1 output start position. When CEN = 1, it outputs COM1 from the center of the screen (the second line). For details, see the Partial-display-on Function section.

LC: When LC = 1, a cursor attribute is assigned to the line that contains the address counter (AC) value. Cursor mode can be selected with the B/W, C, and B bits. For details, see the Line-cursor Display section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**1**	**0**	**D**	**CEN**	**LC**

Figure 14 Display On/Off Control Instruction

Table 20 Common Driver Pin Function

	Common Driver Pin Function			
	CEN = 0 (Normal Output)		CEN = 1 (Center Output)	
Common Driver Pin	CMS = 0 (Normal Display)	CMS = 1 (Reversed Display)	CMS = 0 (Normal Display)	CMS = 1 (Reversed Display)
COM1/40	**COM1**	COM40	COM33	COM32
COM2/39	COM2	COM39	COM34	COM31
COM3/38	COM3	COM38	COM35	COM30
COM4/37	COM4	COM37	COM36	COM29
COM5/36	COM5	COM36	COM37	COM28
COM6/35	COM6	COM35	COM38	COM27
COM7/34	COM7	COM34	COM39	COM26
COM8/33	COM8	COM33	COM40	COM25
COM9/32	COM9	COM32	**COM1**	COM24
COM10/31	COM10	COM31	COM2	COM23
COM11/30	COM11	COM30	COM3	COM22
COM12/29	COM12	COM29	COM4	COM21
COM13/28	COM13	COM28	COM5	COM20
COM14/27	COM14	COM27	COM6	COM19
COM15/26	COM15	COM26	COM7	COM18
COM16/25	COM16	COM25	COM8	COM17
COM17/24	COM17	COM24	COM9	COM16
COM18/23	COM18	COM23	COM10	COM15
• • •	• • •	• • •	• • •	• • •
COM24/17	COM24	COM17	COM16	COM9
COM25/16	COM25	COM16	COM17	COM8
COM26/15	COM26	COM15	COM18	COM7
• • •	• • •	• • •	• • •	• • •
COM32/9	COM32	COM9	COM24	**COM1**
COM33/8	COM33	COM8	COM25	COM40
COM34/7	COM34	COM7	COM26	COM39
• • •	• • •	• • •	• • •	• • •
COM40/1	COM40	**COM1**	COM32	COM33
COMS1/2	COMS1	COMS2	COMS1	COMS2
COMS2/1	COMS2	COMS1	COMS2	COMS1

Display Line Control

NL2-0: Specify the display lines. Display lines change the liquid crystal display drive duty ratio. DDRAM address mapping does not depend on the number of display lines.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**0**	**1**	**1**	**1**	**NL2**	**NL1**	**NL0**

Figure 15 Display Line Control Instruction

Table 21 NL Bits and Display Lines

NL2	NL1	NL0	Display Lines	Liquid Crystal Display Drive Duty Ratio	Common Driver Used
0	0	0	Segment display	1/2 Duty	COMS1, COMS2
0	0	1	One character line + segment display	1/10 Duty	COM1–8, COMS1, COMS2
0	1	0	Two character lines + segment display	1/18 Duty	COM1–16, COMS1, COMS2
0	1	1	Three character lines + segment display	1/26 Duty	COM1–24, COMS1, COMS2
1	0	0	Four character lines + segment display	1/34 Duty	COM1–32, COMS1, COMS2
1	0	1	Five character lines + segment display	1/42 Duty	COM1–40, COMS1, COMS2

Double-height Display Control

DL3-1: Specify the double-height display for a given line. When DL1 = 1, the first line is displayed at double height. When DL2 = 1, the second line is displayed at double height. When DL3 = 1, the third line is displayed at double height. Double-height display of multiple lines is possible. When the fourth line is displayed at double height, set CEN to 1, shift the display position towards the center by one line, and set DL3 to 1. For details, see the Double-height Display section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**0**	**0**	**DL3**	**DL2**	**DL1**

Figure 16 Double-height Display Control Instruction

Vertical Scroll Control 1/2

SN2-0: Specify the display start line output from COM1. Because the DDRAM is assigned a 5-line display area, the data is displayed sequentially from the first line to the fifth line then repeated from the first line again.

SL2–0: Select the top raster-row to be displayed (display-start raster-row) in the display-start line specified by SN2 to SN0. Any raster-row from the first to eighth can be selected (table 23). This function is used to achieve vertical smooth scrolling together with SN2 to SN0. For details, see the Vertical Smooth Scroll section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**0**	**1**	**SN2**	**SN1**	**SN0**
0	0	**0**	**1**	**0**	**1**	**0**	**SL2**	**SL1**	**SL0**

Figure 17 Vertical Scroll Control 1/2 Instruction

Table 22 SN Bits and Display-start Lines

SN2	SN1	SN0	Display-start Line
0	0	0	1st line
0	0	1	2nd line
1	1	0	3rd line
1	1	1	4th line
1	0	0	5th line
1	0	1	Setting inhibited
1	1	0	Setting inhibited
1	1	1	Setting inhibited

Table 23 SL Bits and Display-start Raster-row

SL2	SL1	SL0	Display-start Raster-row
0	0	0	1st raster-row
0	0	1	2nd raster-row
0	1	0	3rd raster-row
0	1	1	4th raster-row
1	0	0	5th raster-row
1	0	1	6th raster-row
1	1	0	7th raster-row
1	1	1	8th raster-row

CGROM Bank Control 1/2

RL5–1: Switch the CGROM memory bank for a given line. Bank 0 and bank 1 of the CGROM incorporate 240 and 192 fonts, respectively, and can display 432 fonts in total. Bits RL1–RL5 select CGROM bank 0/1 for each display line unit. When RL1 = 0, the first line selects bank 0. When RL1 = 1, the first line selects bank 1. Bits RL2, RL3, RL4, and RL5 select the memory banks in the second to fifth lines. For details, see the CGROM Bank Switching Function section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**0**	**1**	**1**	**(0)**	**RL5**	**RL4**
0	0	**0**	**1**	**1**	**0**	**0**	**RL3**	**RL2**	**RL1**

Figure 18 CGROM Bank Control 1/2 Instruction

Key Scan Control

IRE: When IRE = 1, it permits interrupts when a key is pressed. This causes interrupts to occur in the standby period when the oscillator clock is halted, as well as key scan interrupts during normal operation, allowing system wake-up.

KF1-0: Set the key scan cycle. The following table shows the key scan pulse width and key scan cycle used when the oscillation frequency (fosc) is 50 kHz, which depend on the oscillation frequency. For details, see the Key Scan Control section.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**1**	**0**	**1**	**IRE**	**KF1**	**KF0**

Figure 19 Key Scan Control Instruction

Table 24 KF Bits and Key Scan Cycle

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.16 ms	0.64 ms (32 clock cycles)
0	1	0.32 ms	1.28 ms (64 clock cycles)
1	0	0.64 ms	2.56 ms (128 clock cycles)
1	1	1.28 ms	5.12 ms (256 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 50 kHz. The value depends on the oscillation frequency.

Port Control

PT2-0: Control the output level of a port output pin (PORT2-PORT0). When PT0 = 0, the PORT0 pin outputs the GND level, and when PT0 = 1, it outputs the VCC level. Similarly, PT1 and PT2 bits control PORT1 and PORT2 output levels respectively.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**0**	**1**	**1**	**1**	**0**	**PT2**	**PT1**	**PT0**

Figure 20 Port Control Instruction

RAM Address Set

RM1-0: Select DDRAM, CGRAM, and SEGRAM. The selected RAM is accessed with this setting.

AD9-0: Initially set RAM addresses to the address counter (AC). Once the RAM data is accessed, the AC is automatically updated according to the I/D bit. This allows consecutive accesses without resetting addresses. RAM address setting is not allowed in the sleep mode or standby mode.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	**1**	**0**	**RM1**	**RM0**	**AD9**	**AD8**	**AD7**	**AD6**
0	0	**1**	**1**	**AD5**	**AD4**	**AD3**	**AD2**	**AD1**	**AD0**

Figure 21 RAM Address Set Instruction

Table 25 RM Bits and RAM Selection

RM1	RM0	RAM Selection
0	0	DDRAM
0	1	CGRAM (2)
1	0	CGRAM (1)
1	1	SEGRAM

Table 26 AD Bits and DDRAM Setting

RM1/0	AD9–AD0	DDRAM Setting
00	"000"H–"00F"H	Character code on the 1st line
00	"010"H–"01F"H	Character code on the 2nd line
00	"020"H–"02F"H	Character code on the 3rd line
00	"030"H–"03F"H	Character code on the 4th line
00	"040"H–"04F"H	Character code on the 5th line

Table 27 AD Bits and CGRAM (1) Setting (GR = 0)

RM1/0	AD9–AD0	CGRAM (1) Setting in the Character Mode (GR = 0)
10	"000"H–"05F"H	Font pattern of CGRAM characters (1) to (16)
10	"100"H–"15F"H	Font pattern of CGRAM characters (17) to (32)
10	"200"H–"25F"H	Font pattern of CGRAM characters (33) to (48)
10	"300"H–"35F"H	Font pattern of CGRAM characters (49) to (64)

Table 28 AD Bits and CGRAM (1) and (2) Settings (GR = 1)

RM1/0	AD9–AD0	CGRAM (1) (2) Setting in the Graphics Mode (GR = 1)
10	"000"H–"05F"H	Bit map data for COM1 to COM8
10	"100"H–"15F"H	Bit map data for COM9 to COM16
10	"200"H–"25F"H	Bit map data for COM17 to COM24
10	"300"H–"35F"H	Bit map data for COM25 to COM32
01	"000"H–"05F"H	Bit map data for COM33 to COM40

Table 29 AD Bits and SEGRAM Setting

RM1/0	AD9–AD0	SEGRAM Setting
11	"000"H–"05F"H	SEGRAM display data

Write Data to RAM

WD7-0 : Write 8-bit data to the DDRAM and CGRAM, and lower 2-bit data to the SEGRAM. The DDRAM/CGRAM/SEGRAM is selected by the previous specification of the RM 1/0 bit. After a write, the address is automatically incremented or decremented by 1 according to the I/D bit setting in the entry mode set instruction. During the sleep and standby modes, the DDRAM, CGRAM, or SEGRAM cannot be accessed.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	**WD7**	**WD6**	**WD5**	**WD4**	**WD3**	**WD2**	**WD1**	**WD0**

Figure 22 Write Data to RAM Instruction

Read Data from RAM

RD7-0 : Read 8-bit data from the DDRAM, CGRAM or SEGRAM. The unused six upper bits of the SEGRAM data are read as 000000. The DDRAM/CGRAM/SEGRAM is selected by the previous specification of the RM 1/0 bit. In the parallel bus interface mode, the first-byte data read will be invalid immediately after the RAM address set, and the consecutive second-byte data will be read normally. In the serial interface mode, two bytes will be invalid immediately after the start byte, and the consecutive third-byte data will be read normally. For details, see the Serial Data Transfer section.

After a RAM read, the address is automatically incremented or decremented by 1 according to the entry mode set instruction.

R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	**RD7**	**RD6**	**RD5**	**RD4**	**RD3**	**RD2**	**RD1**	**RD0**

Figure 23 Read Data from RAM Instruction

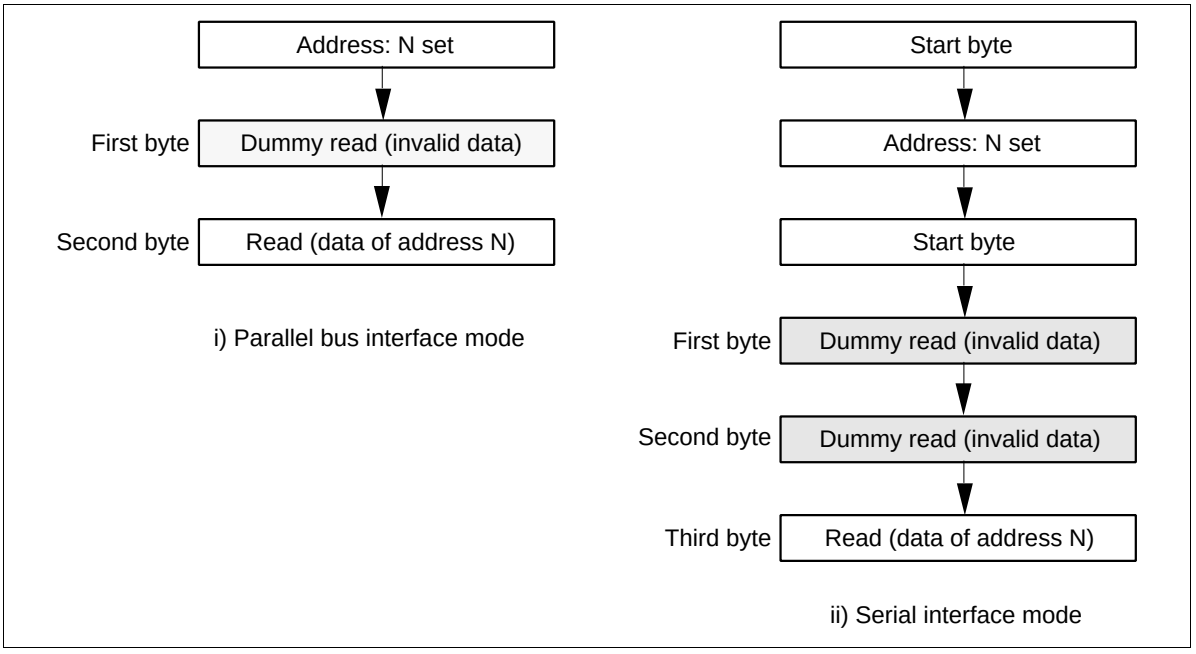


Figure 24 RAM Read Sequence

Table 30 Instruction List

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle*
Key scan data read	1	0				KSD					Reads key scan data (KSD).	0
No operation	0	0	0	0	0	0	0	0	0	0	No operation (NOP).	0
Clear display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets address 0 into the address counter (AC).	85
Return home	0	0	0	0	0	0	0	0	1	0	Sets DDRAM address 0 into the address counter.	0
Start oscillation	0	0	0	0	0	0	0	0	1	1	Starts the oscillation standby mode.	—
Driver output control	0	0	0	0	0	0	0	1	CMS	SGS	Selects the common driver shift direction (CMS) and segment driver shift direction (SGS).	0
Power control	0	0	0	0	0	0	1	AMP	SLP	STB	Turns on LCD power supply (AMP), and sets the sleep mode (SLP) and standby mode (STB).	0
Contrast control 1	0	0	0	0	0	1	0	SW	CT4	CT3	Sets the register selection (SW), upper contrast adjustment bits (CT4-3) or boost level (BT1/0).	0
									BT1	BT0		
Contrast control 2	0	0	0	0	0	1	1	CT2	CT1	CT0	Sets the lower contrast adjustment bits (CT2-0) or LCD bias value (BS2-0).	0
								BS2	BS1	BS0		
Entry mode set	0	0	0	0	1	0	0	REV	I/D	GR	Sets the black-white reversal (REV), address update direction after RAM access (I/D), and graphics mode (GR).	0
Cursor control	0	0	0	0	1	0	1	B/W	C	B	Sets black-white reversed cursor (B/W), 8th raster-row cursor (C), and blink cursor (B).	0
Display on/off control	0	0	0	0	1	1	0	D	CEN	LC	Sets display on (D), centers the screen (CEN), and displays the line cursor (LC).	0
Display line control	0	0	0	0	1	1	1	NL2	NL1	NL0	Sets the number of display lines (NL2-0).	0
Double-height display control	0	0	0	1	0	0	0	DL3	DL2	DL1	Specifies double-height display lines (DL3-1).	0
Vertical scroll control 1	0	0	0	1	0	0	1	SN2	SN1	SN0	Sets the display-start line (SN2-0).	0

Table 30 Instruction List (cont)

Register Name	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Cycle*
Vertical scroll control 2	0	0	0	1	0	1	0	SL2	SL1	SL0	Sets the display-start raster-row (SL2-0).	0
CGROM bank control 1	0	0	0	1	0	1	1	<0>	RL5	RL4	Selects the CGROM memory bank in the fourth to fifth lines.	0
CGROM bank control 2	0	0	0	1	1	0	0	RL3	RL2	RL1	Selects the CGROM memory bank in the first to third lines.	0
Key scan control	0	0	0	1	1	0	1	IRE	KF1	KF0	Sets the key scan interrupt (IRE) and key scan cycle (KF1/0).	0
Port control	0	0	0	1	1	1	0	PT2	PT1	PT0	Sets the general port output (PT2-0).	0
RAM address set (upper bits)	0	0	1	0	RM1	RM0		AD9-6 (upper bits)			Sets the RAM selection (RM1/0) and initial upper RAM address to the address counter (AC).	0
RAM address set (lower bits)	0	0	1	1				AD5-0 (lower bits)			Sets the initial lower RAM address to the address counter (AC).	0
Write data to RAM	0	1					Write data				Writes data to DDRAM, CGRAM, or SEGRAM.	0
Read data from RAM	1	1					Read data				Reads data from DDRAM, CGRAM, or SEGRAM.	0

Note: Represented by the number of operating clock pulses; the execution time depends on the supplied clock frequency or the internal oscillation frequency.

Bit definition:

CMC = 0: COM1/40 => COM1

SGS = 0: SEG1/96 => SEG1

AMP = 1: Operational amplifier and booster circuit on

SLP = 1: Sleep mode

STB = 1: Standby mode

SW = 0: CT4-0 access

SW = 1: BT1/0 and BS2-0 access

CT4-0: Contrast adjustment

BT1/0: Boost level selection (00: Single, 01: Double, 10: Triple, 11: Quadruple)

BS2-0: LCD drive bias selection

REV = 0: Normal display

REV = 1: Black-white reversed display of the character and graphics display, but excluding the segment display

ID = 1: Address increment

ID = 0: Address decrement

GR = 1: Graphics display mode

GR = 0: Character display mode

B/W = 1: Black-white reversed cursor on

C = 1: 8th raster-row cursor on

B = 1: Blink cursor on

D = 1: Display on

CEN = 1: Centering display by one line

LC = 1: Cursor display for the all display lines including AC

NL2-0: Display line setting (000: 1/2 duty ratio, 001: 1/10 duty ratio, 010: 1/18 duty ratio, 011: 1/26 duty ratio, 100: 1/34 duty ratio, 101: 1/42 duty ratio)

DL3-1: Double-height line specifications (DL1: 1st line, Dl2: 2nd line, Dl3: 3rd line)

SN2-0: Display-start line (000: 1st line, 001: 2nd line, 010: 3rd line, 011: 4th line, 100: 5th line)

SL2-0: Display-start raster-row specifications (000: 1st raster-row...111: 8th raster-row)

SE1-5: CGROM memory bank switching selection (0: bank 0, 1: bank 1)

(RL1: 1st line, RL2: 2nd line, RL3: 3rd line, RL4: 4th line, RL5: 5th line)

IRE = 1: Key scan interrupt generation enabled

KF1/0: Key scan cycle set

PT2-0: Port output control (PT2 = 1: PORT2 = Vcc, PT1 = 1: PORT1 = Vcc, PT0 = 1: PORT0 = Vcc)

RM1/0: RAM selection (00/01: DDRAM, 01: CGRAM (2), 10: CGRAM (1), 11: SEGRAM)

ADD9-0: DDRAM/CGRAM/SEGRAM address set (DDRAM: 000H-04FH, CGRAM: 000H-35FH, SEGRAM: 000H-05FH)

Reset Function

The HD66726 is internally initialized by RESET input. During initialization, the system executes a clear display instruction after reset is canceled. The system executes the other instructions during the reset period. Because the busy flag (BF) indicates a busy state (BF = 1) during the reset period and the clear display instruction is executed following reset cancellation, no instruction or RAM data access from the MPU is accepted. The reset input must be held for at least 1 ms. Any initializing instruction must wait for 1000 clock cycles after the reset is canceled so that execution of the clear display instruction can be completed.

Instruction Set Initialization:

1. Clear display executed (Writes 20H to DDRAM)
2. Return home executed (Sets the address counter (AC) to 00H to select DDRAM)
3. Start oscillation executed
4. Driver output control (SGS = 0, CMS = 0)
5. Power control (AMP = 0: LCD power off, SLP = 0: Sleep mode off, STB = 0: Standby mode off)
6. Single boost (BT1/0 = 00), 1/8 bias drive (BS2/1/0 = 000), Weak contrast (CT4-0 = 00000)
7. Entry mode set (REV = 0: Normal display, I/D = 1: Increment by 1, GR = 0: Character display mode)
8. Cursor display off (B/W = 0, C = 0, B = 0)
9. Display on/off control (D = 0: Display off, CEN = 0: Normal position, LC = 0: Line-cursor off)
10. Display line control (NL2/1/0 = 100: 1/34 duty ratio)
11. Double-height display off (DL3/2/1 = 000)
12. Vertical scroll control (SN2/1/0 = 000: First line displayed at the top, SL2/1/0: First raster-row displayed at the top of the first line)
13. CGROM memory bank 0 selection (RL5/4/3/2/1 = 00000)
14. Key scan control (IRE = 0: Key scan interrupt (IRQ) generation disabled, KF1/0 = 00: Key scan set to 32 cycles)
15. Port control (PT2/1/0 = 000: PORT2/1/0 output = GND level)

RAM Data Initialization:

1. DDRAM

   All addresses are initialized to 20H by the clear display instruction after the reset is canceled.
2. CGRAM/SEGRAM

   This is not automatically initialized by reset input but must be initialized by software while display is off (D = 0).

Output Pin Initialization:

1. LCD driver output pins (SEG/COM): Outputs GND level
2. Booster output pins (VLOUT): Outputs GND level
3. Oscillator output pin (OSC2): Outputs oscillation signal
4. Key strobe pins (KST0 to KST3): Output strobe signals at specified time intervals
5. Key scan interrupt pin (IRQ*): Outputs V_{CC} level

6. General output ports (PORT0–PORT2): Output GND level

Serial Data Transfer

Setting the IM1 and IM2 pins (interface mode pins) to the GND level allows standard clock-synchronized serial data transfer, using the chip select line (CS*), serial data line (SDA), and serial transfer clock line (SCL). For a serial interface, the IM0/ID pin function uses an ID pin.

The HD66726 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66726 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66726. The HD66726, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66726 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, an instruction can be issued or key scan data can be read, and when RS = 1, data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit) as shown in table 32.

After receiving the start byte, the HD66726 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. To transfer data consecutively, note that only the display-clear instruction requires a longer execution time than the others (see table 30, Instruction List).

Two bytes of RAM read data after the start byte are invalid. The HD66726 starts to read correct RAM data from the third byte.

Table 31 Start Byte Format

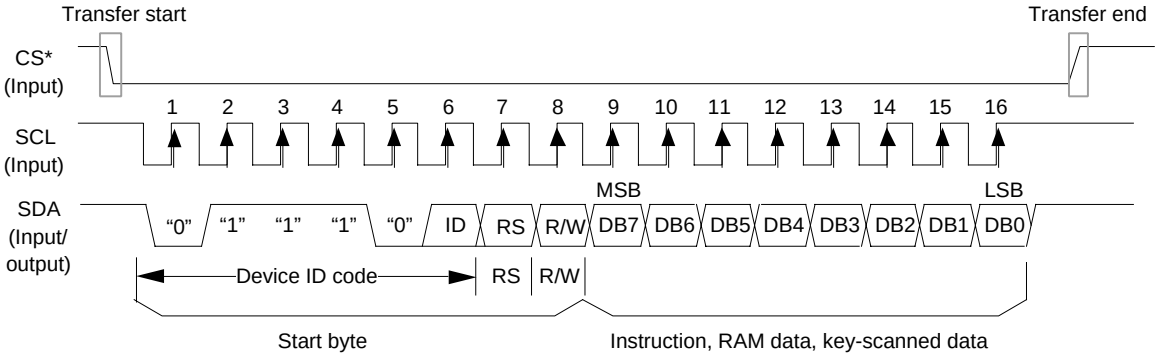
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

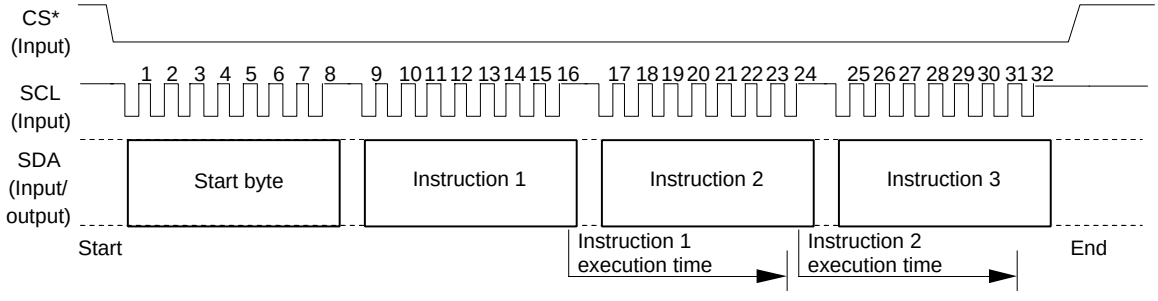
Table 32 RS and R/W Bit Function

RS	R/W	Function
0	0	Writes instruction
0	1	Reads key scan data
1	0	Writes RAM data
1	1	Reads RAM data

a) Basic Data-transfer Timing through Clock-synchronized Serial Bus Interface

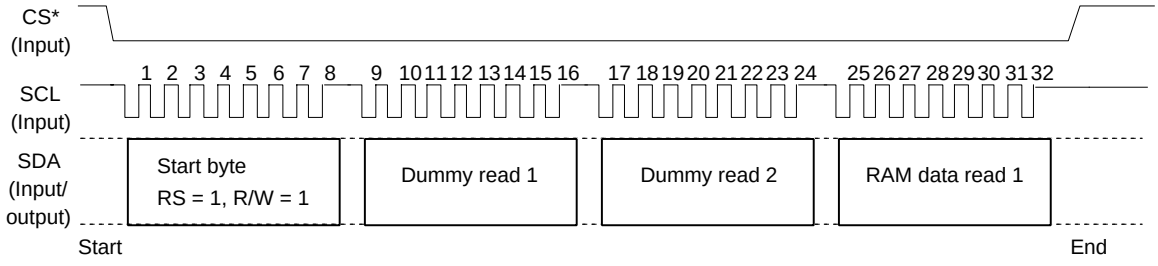


b) Consecutive Data-transfer Timing through Clock-synchronized Serial Bus Interface



Note: When instruciton 1 is a clear display instruction, adjust the transfer rate so that the 8th bit of instruction 2 is transferred after execution of the clear display instruction.

c) RAM Data Read-transfer Timing



Note: Two bytes of the RAM read data after the start byte are invalid. The HD66726 starts to read the correct RAM data from the third byte.

Figure 25 Clock-synchronized Serial Interface Timing Sequence

Key Scan Control

The key matrix scanner senses and holds the key states at each rising edge of key strobe signals (KST) that are output by the HD66726. The key strobe signals are output as time-multiplexed signals from KST0 to KST3. After passing through the key matrix, these strobe signals are used to sample the key state of eight inputs KIN0 to KIN7, enabling up to 32 keys to be scanned.

The states of inputs KIN0 to KIN7 are sampled by key strobe signal KST0 and latched into the SCAN0 register. Similarly, the data sampled by strobe signals KST1 to KST3 is latched into the SCAN1 to SCAN3 registers, respectively. Key pressing is stored as 1 in these registers.

The generation cycle and pulse width of the key strobe signals depend on the operating frequency (oscillation frequency) of the HD66726 and the key scan cycle determined by the KF0 and KF1 bits. For example, when the operating frequency is 50 kHz and KF0 and KF1 are both 10, the generation cycle is 2.56 ms and the pulse width is 0.64 ms. When the operating frequency (oscillation frequency) is changed, the above generation cycle and the pulse width are changed in inverse proportion.

In order to compensate for the mechanical features of the keys, such as chattering and noise and for the key-strobe generation cycle and the pulse width of the HD66726, software should read the scanned data two to three times in succession to obtain valid data. Multiple keypress combinations should also be processed in the software.

Up to three keys can be pressed simultaneously. Note, however, that if the third key is pressed on the intersection between the rows and columns of the first two keys pressed, incorrect data will be sampled. For three-key input, the third key must be on a separate column or row.

The input pins KIN0 to KIN7 are pulled up to V_{CC} with internal MOS transistors (see the Electrical Characteristics section). External resistors may also be required to further pull the voltages up when the internal pull-ups are insufficient for the desired noise margins or for a large key matrix.

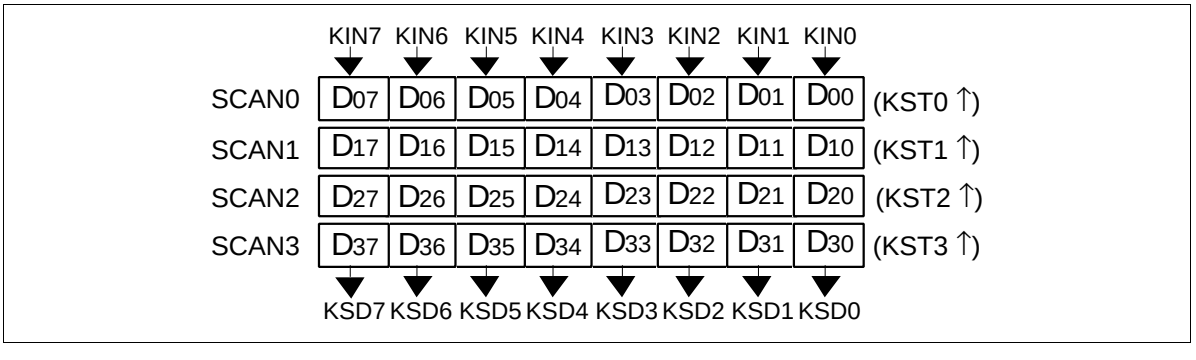


Figure 26 Key Scan Register Configuration

Table 33 Key Scan Cycles for Each Operating Frequency

KF1	KF0	Key Scan Pulse Width	Key Scan Cycle
0	0	0.16 ms	0.64 ms (32 clock cycles)
0	1	0.32 ms	1.28 ms (64 clock cycles)
1	0	0.64 ms	2.56 ms (128 clock cycles)
1	1	1.28 ms	5.12 ms (256 clock cycles)

Note: The data is a value obtained when the oscillation frequency (fosc) is 50 kHz. The value depends on the oscillation frequency.

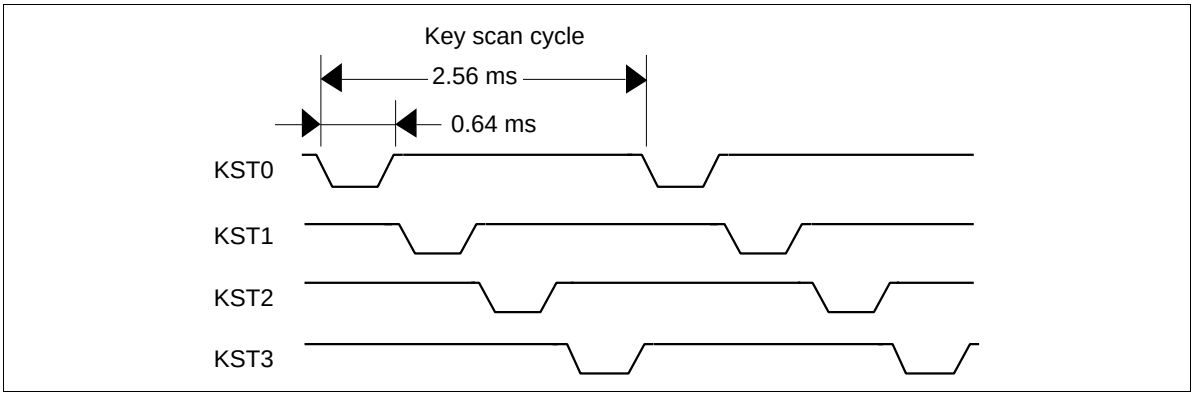


Figure 27 Key Strobe Output Timing (KF1/0 = 10, fcp/fosc = 50 kHz)

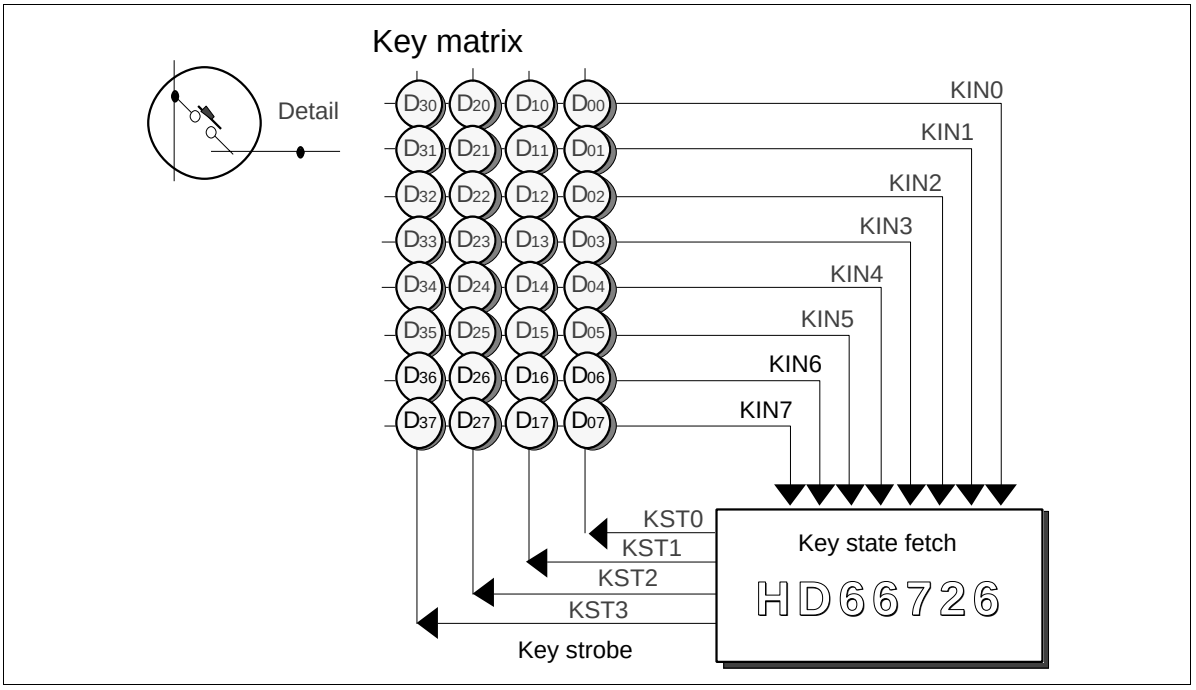
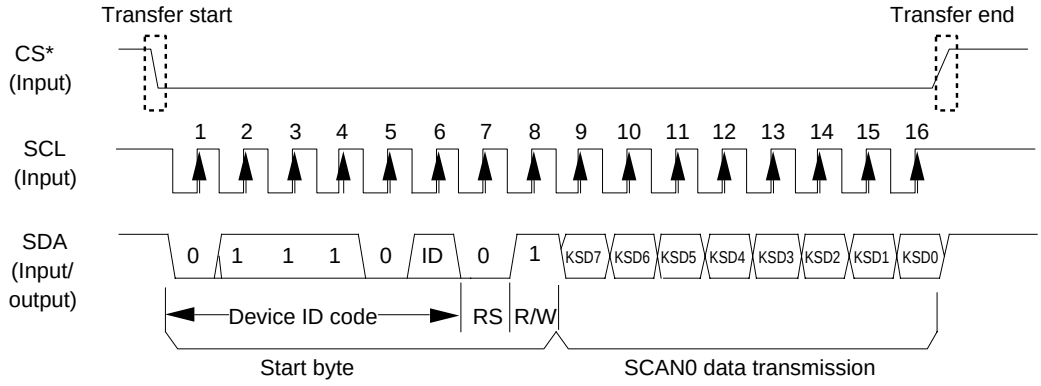


Figure 28 Key Scan Configuration

The key-scanned data can be read by an MPU via a serial interface. First, a start byte should be transferred. After the HD66726 has received the start byte, the MPU reads scan data KSD7 to KSD0 from the SCAN0 register starting from the MSB. Similarly, the MPU reads data from SCAN1, SCAN2 and SCAN3 in that order. After reading SCAN3, the MPU starts at SCAN0 again.

The HD66726 may be read out while it is latching scan data and is thus unstable. Consequently, it should also be reconfirmed with software if required.

a) Scan Data Read Timing through Clock-synchronized Serial Bus Interface



b) Consecutive Scan Data Read Timing

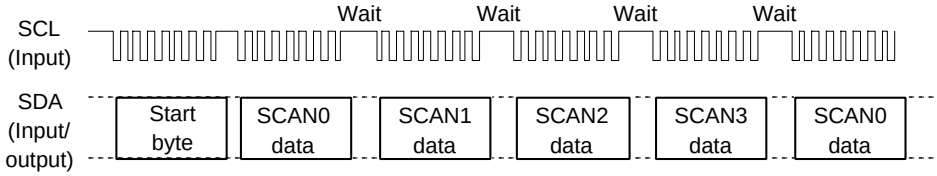


Figure 29 Scan Data Serial Transfer Timing

Key Scan Interrupt (Wake-up Function)

If the interrupt enable bit (IRE) is set to 1, the HD66726 sends an interrupt signal to the MPU on detecting that a key has been pressed in the key scan circuit by setting the IRQ* output pin to a low level. An interrupt signal can be generated by pressing any key in a 32-key matrix. The interrupt level continues to be output during the key scan cycle while the key is being pressed.

Normal key scanning is performed and interrupts can occur in the HD66726 sleep mode (SLP = 1). Accordingly, power consumption can be minimized in the sleep mode, by triggering the MPU to read key states via the interrupt which is generated only when the HD66726 detects a key input. For details, see the Sleep Mode section.

On the other hand, normal key scanning and the internal operating clock stop in the standby mode (STB = 1). During this period, the KST0 output is kept low, so the HD66726 can always monitor eight key inputs (KIN0-KIN7) connected to KST0 when RS = GND. Therefore, if any of the eight keys is pressed, an interrupt occurs. When RS = Vcc, all outputs KST0 to KST3 are kept low, so the HD66726 can always monitor 32 key inputs. If any of 32 keys is pressed, an interrupt occurs. Accordingly, power consumption can further be minimized in the standby mode, where the whole system is inactive, by triggering the MPU via the interrupt which is generated only when the HD66726 detects a key input from the above keys. For details, see the Standby Mode section.

The IRQ* output pin is pulled up to the V_{CC} with an internal MOS resistor of approximately 50 kΩ. Additional external resistors may be required to obtain stronger pull-ups. Interrupts may occur if noise occurs in KIN0-KIN7 input during key scanning. Interrupts must be inhibited if not needed by setting the interrupt enable bit (IRE) to 0.

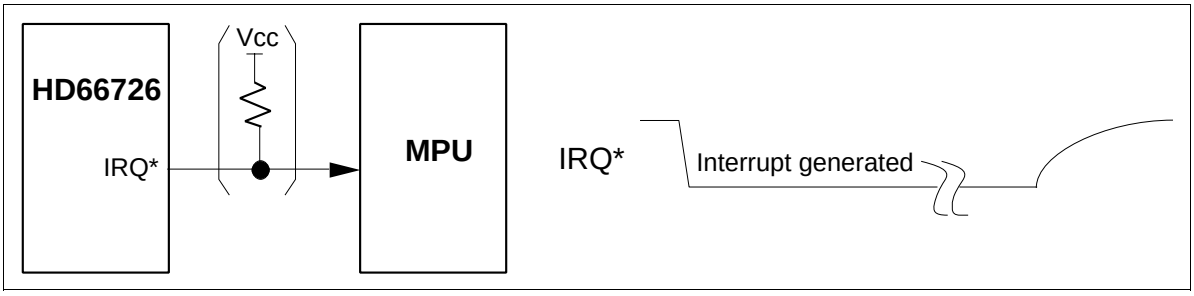


Figure 30 Interrupt Generator

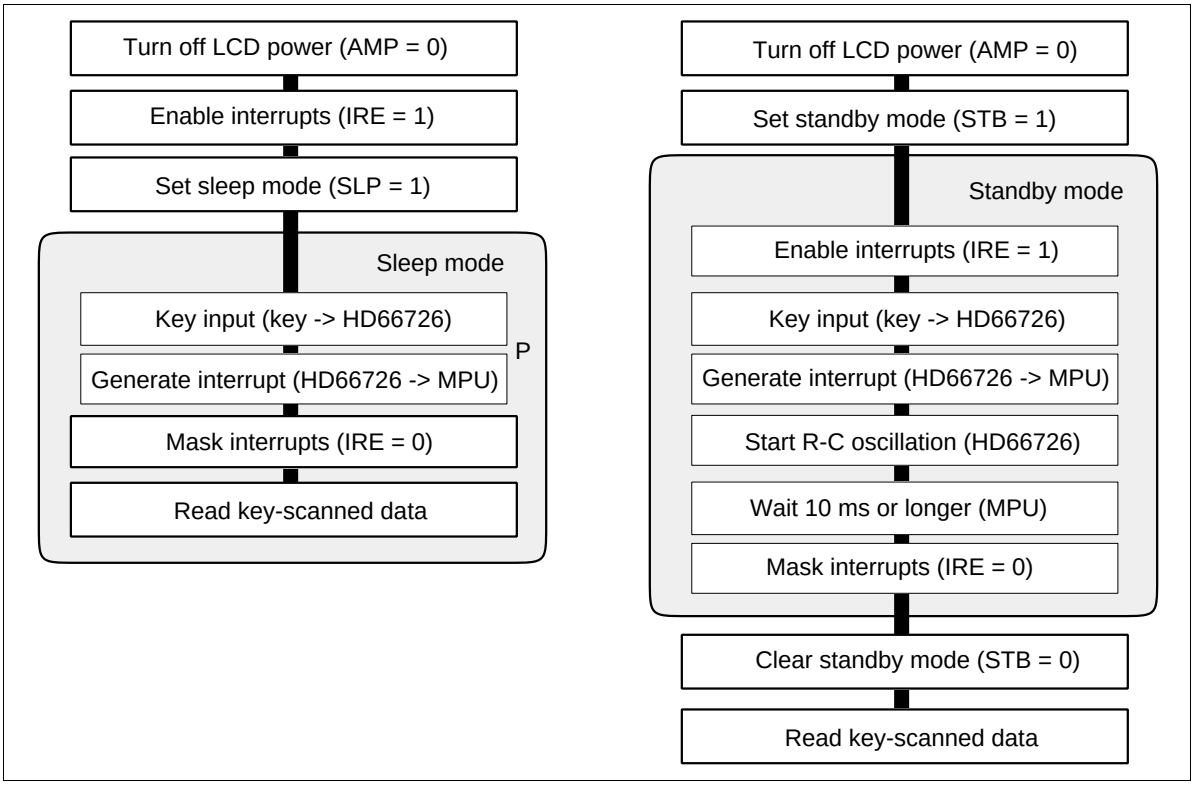


Figure 31 Key Scan Interrupt Processing Flow in Sleep and Standby Modes

Parallel Data Transfer

8-bit Interface

Setting the IM2/1/0 (interface mode) to the GND/V_{CC}/GND level allows 8-bit parallel data transfer. A direct interface using the 8-bit E-clock-synchronized bus or an interface via the I/O bus can be established. When the number of buses or the mounting area is limited, use a 4-bit bus interface or serial data transfer.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

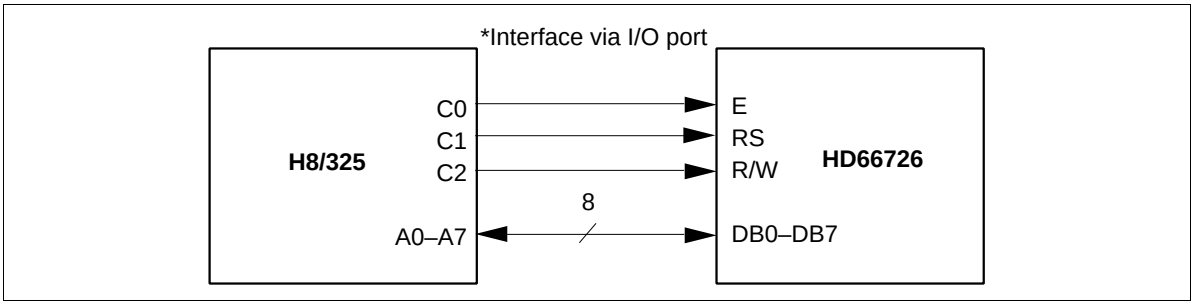


Figure 32 Interface to 8-bit Microcomputer

4-bit Interface

Setting the IM2/1/0 (interface mode) to the GND/V_{CC}/V_{CC} level allows 4-bit parallel data transfer using pins DB7/KIN7-DB4/KIN4. 8-bit instructions and RAM data are divided into four upper/lower bits and transfer starts from the upper four bits.

Using a parallel bus interface disables the key scan function. To prevent this, use a clock-synchronized serial interface.

Note: Transfer synchronization function for a 4-bit bus interface
The HD66726 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 4-bit data transfer in the 4-bit bus interface. Noise causing transfer mismatch between the four upper and lower bits can be corrected by a reset triggered by consecutively writing a 0000 instruction four times. The next transfer starts from the upper four bits. Executing synchronization function periodically can recover any runaway in the display system.

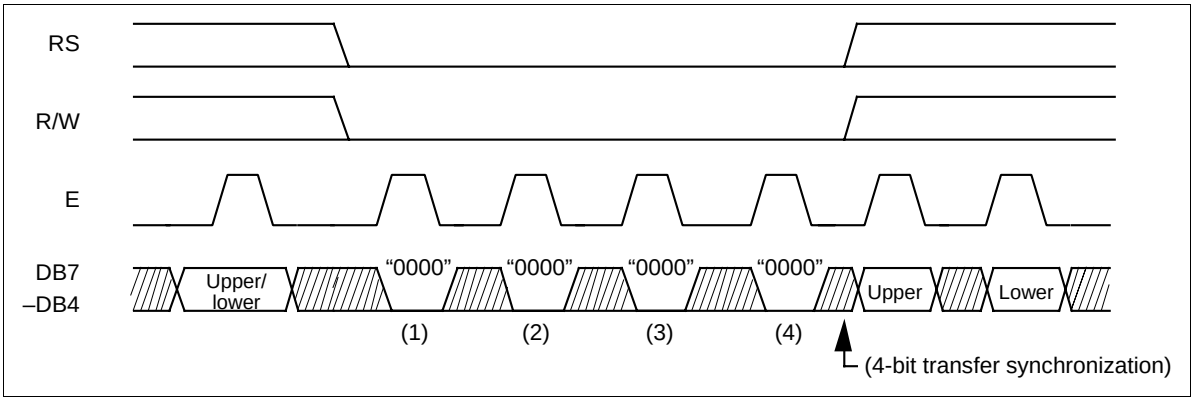


Figure 33 4-bit Transfer Synchronization

Oscillation Circuit

The HD66726 can either be supplied with operating pulses externally (external clock mode), oscillate using an internal R-C oscillator with an external oscillator-resistor (external resistor oscillation mode).

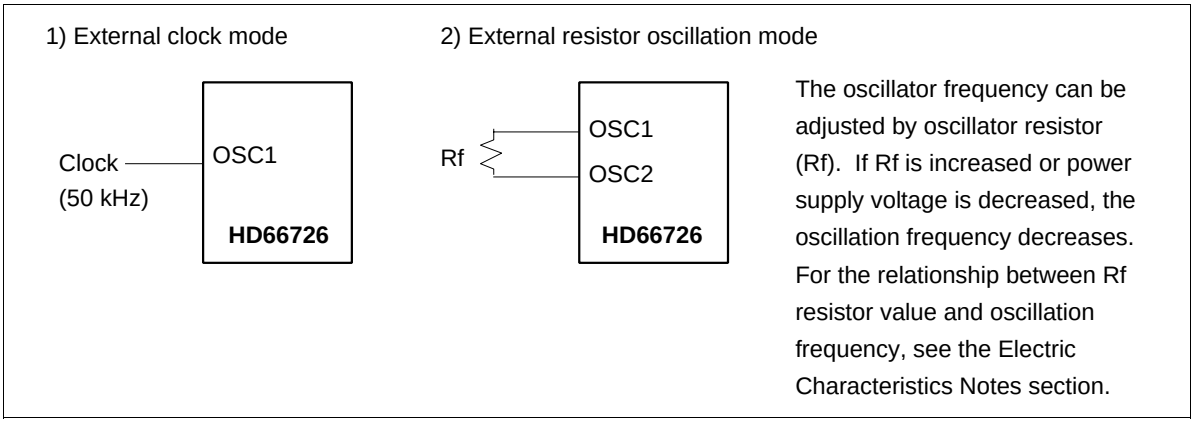


Figure 34 Oscillation Circuits

Table 34 Relationship between Drive Duty Ratio and Frame Frequency (fosc = 50 kHz)

	Display mode					
	Segment Display	**1-line Display**	**2-line Display**	**3-line Display**	**4-line Display**	**5-line Display**
	Set value for NL2–0					
LCD Drive	**000**	**001**	**010**	**011**	**100**	**101**
Multiplexing duty ratio	1/2	1/10	1/18	1/26	1/34	1/42
Optimum drive bias (recommend-ed value)	1/2	1/4	1/5	1/6	1/6	1/7
Frame frequency	74 Hz	74 Hz	73 Hz	74 Hz	74 Hz	74 Hz

Note: If the frame frequency is low and the display flickers, increase the oscillation frequency (fosc).

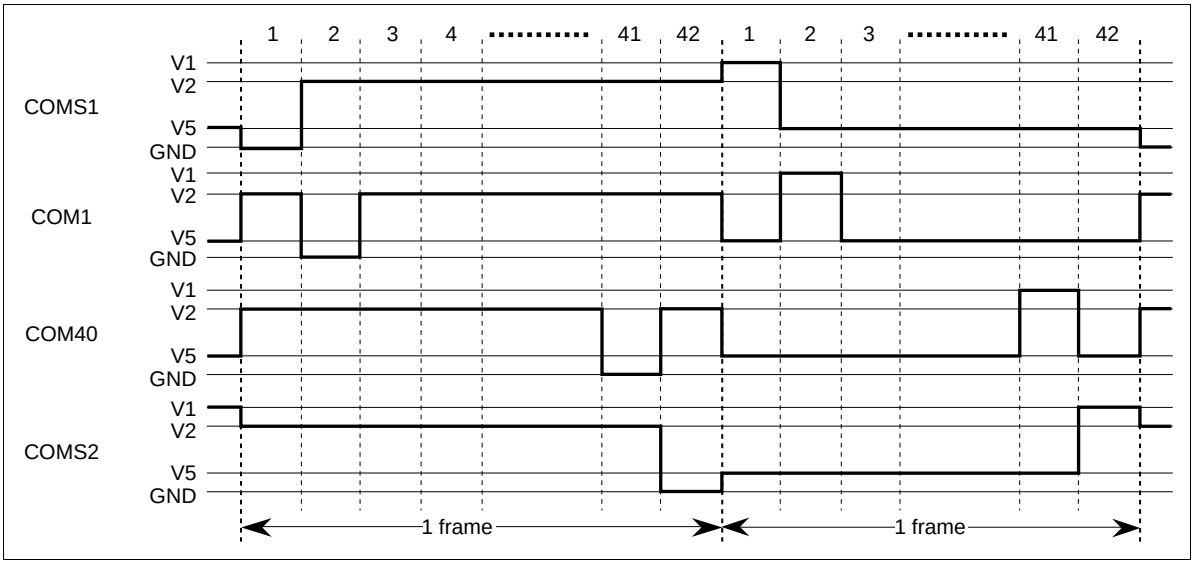


Figure 35 LCD Drive Output Waveform (5-line Display with 1/42 Multiplexing Duty Ratio)

Liquid Crystal Display Voltage Generator

When External Power Supply and Internal Operational Amplifiers are Used

To supply LCD drive voltage directly from the external power supply without using the internal booster, circuits should be connected as shown in figure 36. Here, contrast can be adjusted by software through the CT bits of the contrast adjustment register.

The HD66726 incorporates a voltage-follower operational amplifier for each V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different levels of liquid-crystal drive voltages. Thus, potential differences between V_{LCD} and V1 and between V5 and GND must be 0.1 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.

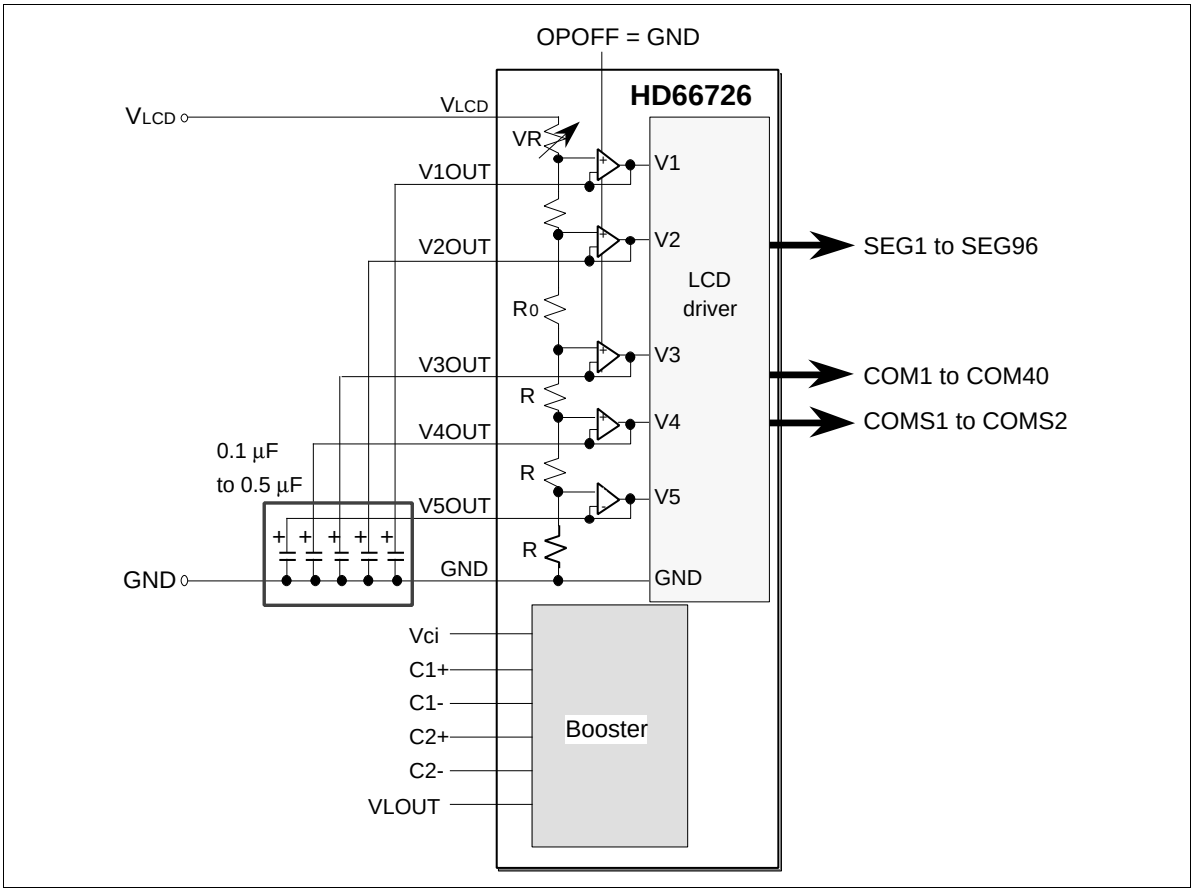


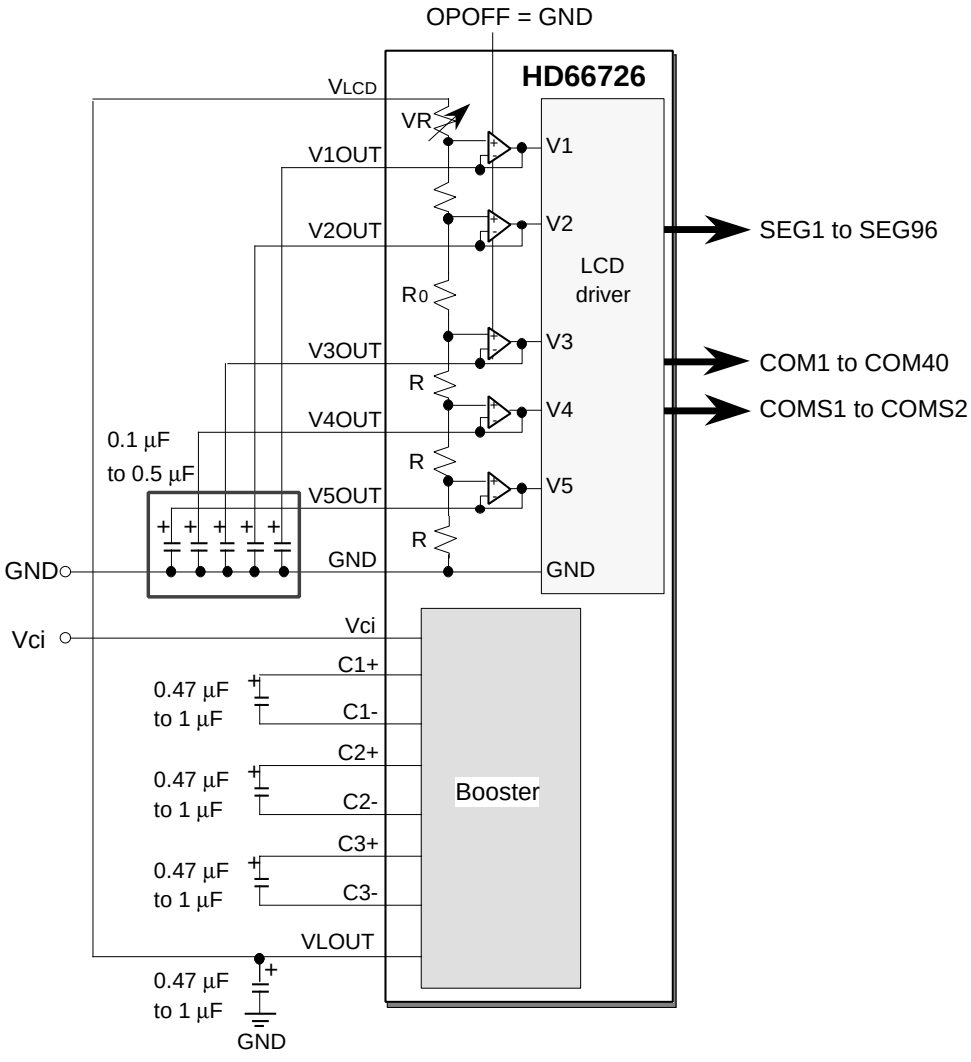
Figure 36 External Power Supply Circuit for LCD Drive Voltage Generation

When an Internal Booster and Internal Operational Amplifiers are Used

To supply LCD drive voltage using the internal booster, circuits should be connected as shown in figure 37. Here, contrast can be adjusted through the CT bits of the contrast control instruction. Temperature can be compensated either through the CT bits or by controlling the reference voltage for the booster (Vci pin) using a thermistor.

Note that Vci is both a reference voltage and power supply for the booster. The reference voltage must therefore be adjusted using an emitter-follower or a similar element so that sufficient current can be supplied. In this case, Vci must be equal to or smaller than the V_{CC} level.

The HD66726 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder-resistors, which generate different liquid-crystal drive voltages. Thus, the potential differences between V_{LCD} and V1 and between V5 and GND must be 0.1 V or higher. Note that the OPOFF pin must be grounded when using the operational amplifiers. Place a capacitor of about 0.1 µF to 0.5 µF between each internal operational amplifier V1OUT to V5OUT output and GND and stabilize the output level of the operational amplifier.



Notes:
1. The reference voltage input (Vci) must be adjusted so that the output voltage after boosting will not exceed the absolute maximum rating for the liquid-crystal power supply voltage (13 V). Particularly, Vci must be 3.3 V or less for quadruple boosting.
2. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
3. Vci must be smaller than Vcc.
4. Polarized capacitors must be connected correctly.
5. Circuits for temperature compensation should be based on the sample circuit in figure 38.

Figure 37 Internal Booster for LCD Drive Voltage Generation

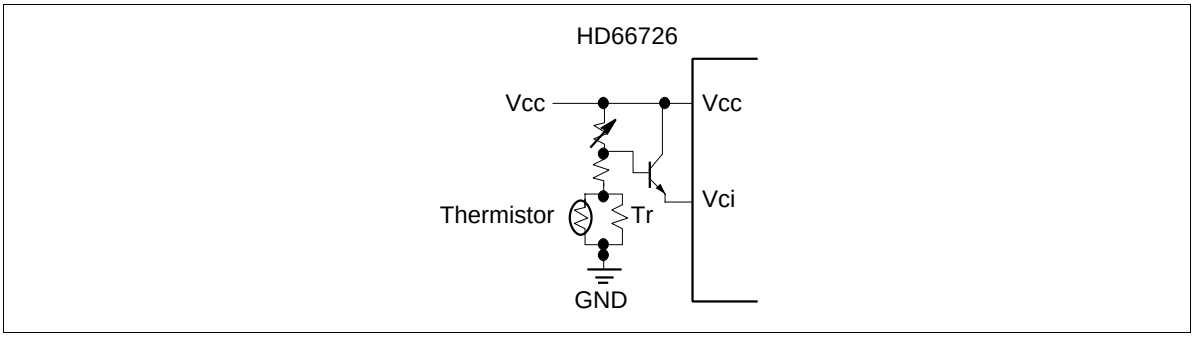


Figure 38 Temperature Compensation Circuit

Instruction bits (BT1/0 bits) can optionally select the boosting multiplying factor of the internal booster. According to the display status, power consumption can be reduced by changing the LCD drive duty and the LCD drive bias, and by controlling the boosting multiplying factor for the minimum requirements. For details, see the Partial-display-on Function section.

Due to the maximum boosting multiplying factor, the following external capacitor needs to be connected. For example, when the maximum boosting is tripled, the capacitors between C3+ and C3– for quadruple boosting are not needed, so these pins must be open.

Table 35 VLOUT Output Status

BT1	BT0	VLOUT Output Status
0	0	Single output (The potential difference between Vci and GND is output to the VLOUT.)
0	1	Double boosting output
1	0	Triple boosting output
1	1	Quadruple boosting output

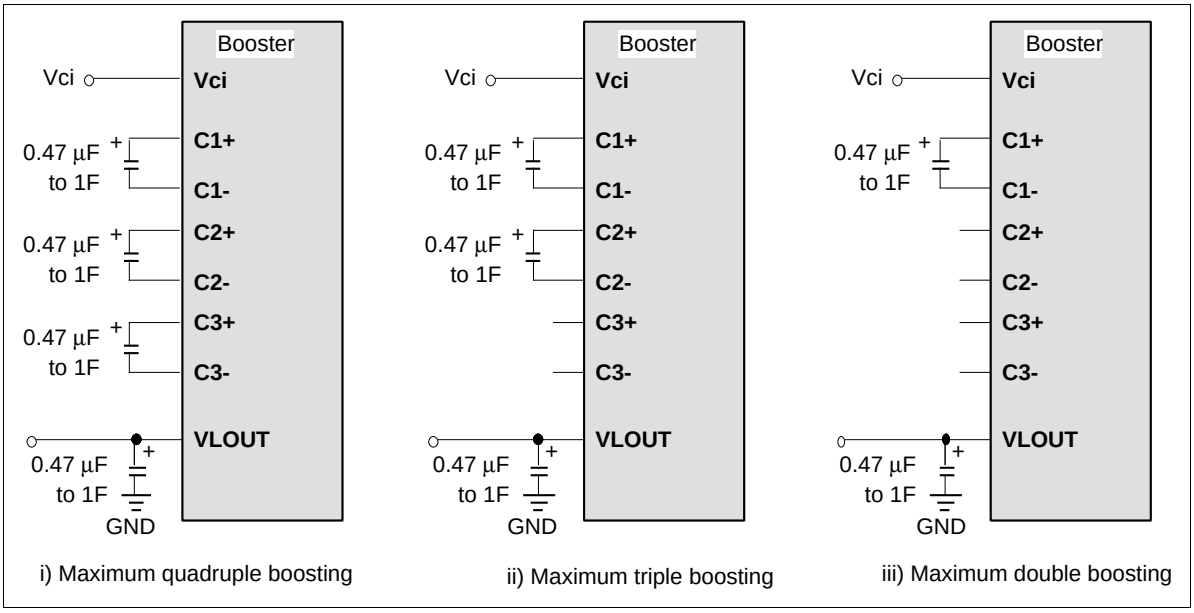
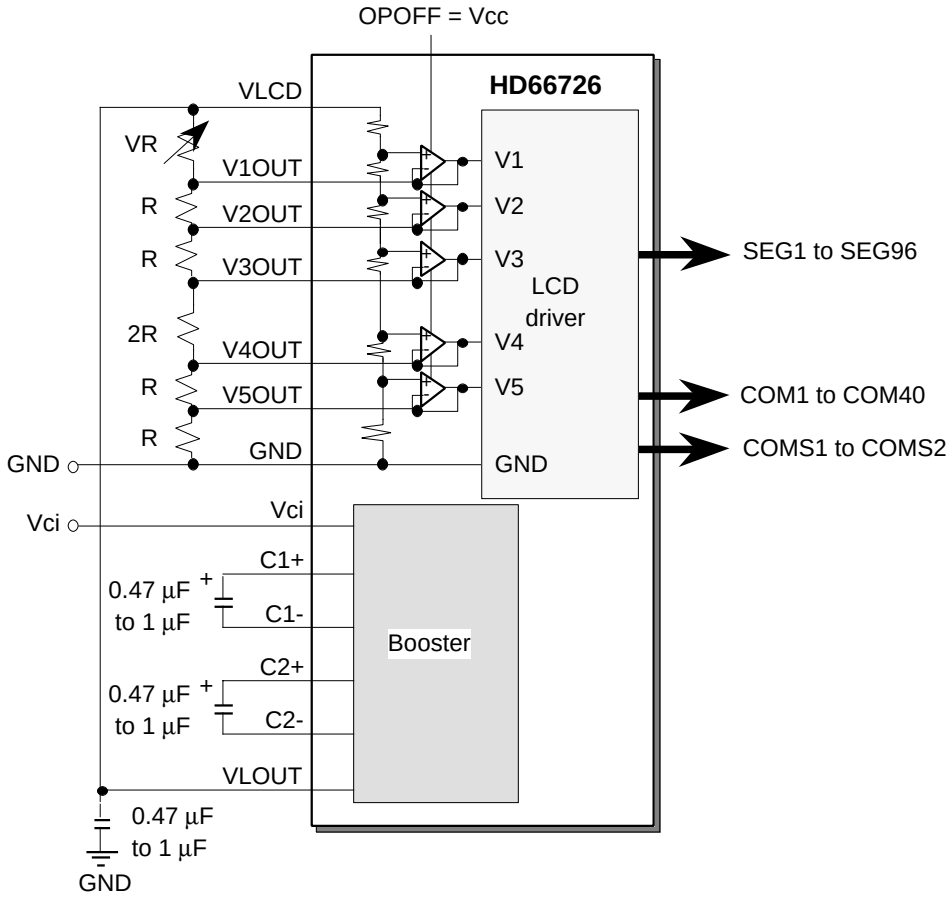


Figure 39 Booster Output Multiplying Factor Switching

When an Internal Booster and External Bleeder Resistors are Used

When internal operational amplifiers cannot fully drive the LCD panel used, V1 to V5 voltages can be supplied through external bleeder resistors (figure 40). Here, the OPOFF pin must be set to the V_{CC} level to turn off the internal operational amplifiers. Since the internal contrast adjuster is disabled, contrast must be adjusted externally. Connection of external bleeder-resistors can specify a given bias value from 1/2 to 1/7. Figure 40 shows connection for 1/6-bias drive voltage generation. Internal boosters can be used as they are.



Notes:
1. Resistance of each external bleeder resistor should be 4.7 kΩ to 25 kΩ.
2. When 0.1 µF to 0.5 µF capacitors are added in parallel with each external bleeder resistor, resistance can be increased to 47 kΩ to 75 kΩ, and the through current in the bleeder resistors can be considerably reduced (see figure 41).
3. The bias current value for driving LCDs can be varied by adjusting the resistance (2R) between the V3OUT and V4OUT pins.
4. The internal contrast adjuster is disabled; contrast must be adjusted either by controlling the external variable resistor between VLCD and V1 for the booster.
5. Vci is both a reference voltage and power supply for the booster; connect it to Vcc directly or combine it with a transistor so that sufficient current can be obtained.
6. Vci must be smaller than Vcc.

Figure 40 Circuit Using External Bleeder Resistors

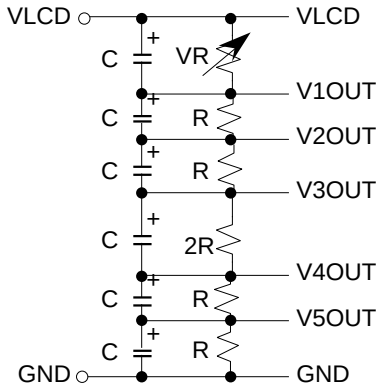


Figure 41 Low-current Consumption Bleeder Resistor

Contrast Adjuster

Software can adjust contrast for an LCD by varying the liquid-crystal drive voltage (potential difference between V_{LCD} and V1) through the CT bits of the contrast adjustment register (electron volume function). The value of a variable resistor (VR) can be adjusted within a range from 0.1 x R through 3.2 x R, where R is a reference resistance obtained by dividing the total resistance between V_{LCD} and V1.

The HD66726 incorporates a voltage-follower operational amplifier for each of V1 to V5 to reduce current flowing through the internal bleeder resistors, which generate different liquid-crystal drive voltages. Thus, CT4-0 bits must be adjusted so that the potential differences between V_{LCD} and V1 and between V5 and GND are 0.1 V or higher when liquid-crystal drives.

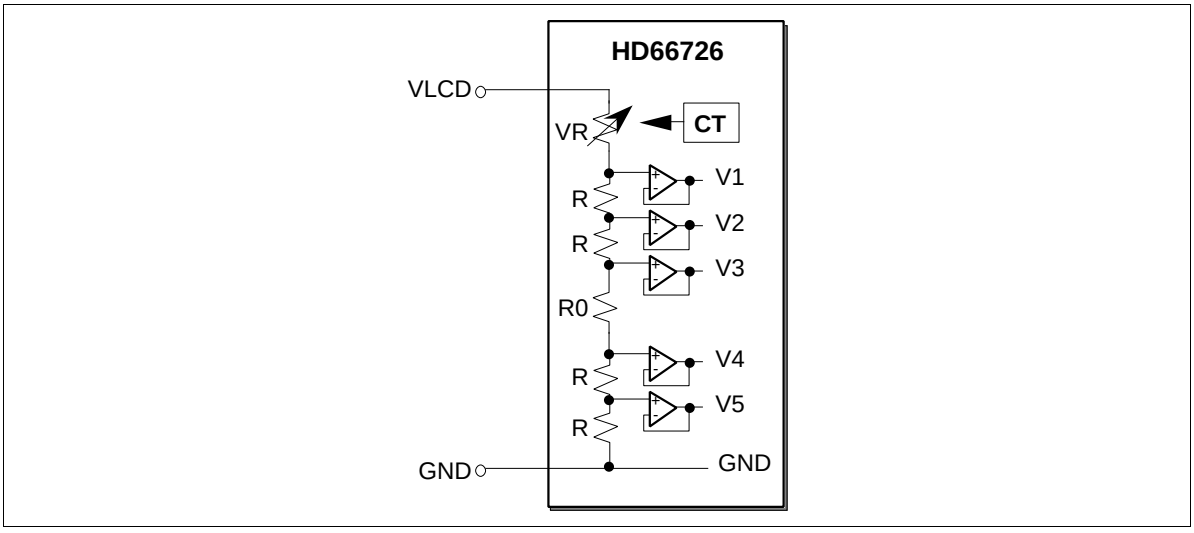


Figure 42 Contrast Adjuster

Table 36 Contrast Adjustment Bits (CT) and Variable Resistor Values

CT Set Value					Variable Resistor Value (VR)	Potential Difference between V1 and GND	Display Color
CT4	CT3	CT2	CT1	CT0			
0	0	0	0	0	3.2 x R	(Small)	(Light)
0	0	0	0	1	3.1 x R		
0	0	0	1	0	3.0 x R		
0	0	0	1	1	2.9 x R		
0	0	1	0	0	2.8 x R		
0	0	1	0	1	2.7 x R		
0	0	1	1	0	2.6 x R		
0	0	1	1	1	2.5 x R		
0	1	0	0	0	2.4 x R		
0	1	0	0	1	2.3 x R		
0	1	0	1	0	2.2 x R		
0	1	0	1	1	2.1 x R		
0	1	1	0	0	2.0 x R		
0	1	1	0	1	1.9 x R		
0	1	1	1	0	1.8 x R		
0	1	1	1	1	1.7 x R		
1	0	0	0	0	1.6 x R		
1	0	0	0	1	1.5 x R		
1	0	0	1	0	1.4 x R		
1	0	0	1	1	1.3 x R		
1	0	1	0	0	1.2 x R		
1	0	1	0	1	1.1 x R		
1	0	1	1	0	1.0 x R		
1	0	1	1	1	0.9 x R		
1	1	0	0	0	0.8 x R		
1	1	0	0	1	0.7 x R		
1	1	0	1	0	0.6 x R		
1	1	0	1	1	0.5 x R		
1	1	1	0	0	0.4 x R		
1	1	1	0	1	0.3 x R		
1	1	1	1	0	0.2 x R		
1	1	1	1	1	0.1 x R	(Large)	(Deep)

Table 37 Contrast Adjustment per Bias Drive Voltage

Bias	LCD drive voltage: V_{DR}	Contrast adjustment range
1/7 bias drive	$\frac{7 \times R}{7 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.686 \times (V_{LCD}-GND) \le V_{DR} \le 0.986 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{7 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{7 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/6 bias drive	$\frac{6 \times R}{6 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.652 \times (V_{LCD}-GND) \le V_{DR} \le 0.984 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{6 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{6 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/5.5 bias drive	$\frac{5.5 \times R}{5.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.632 \times (V_{LCD}-GND) \le V_{DR} \le 0.982 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{5.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/5 bias drive	$\frac{5 \times R}{5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.610 \times (V_{LCD}-GND) \le V_{DR} \le 0.980 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/4.5 bias drive	$\frac{4.5 \times R}{4.5 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \le V_{DR} \le 0.978 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{4.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4.5 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/4 bias drive	$\frac{4 \times R}{4 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.556 \times (V_{LCD}-GND) \le V_{DR} \le 0.976 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{4 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{4 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]
1/2 bias drive	$\frac{2 \times R}{2 \times R + VR} \times (V_{LCD} - GND)$	- LCD drive voltage adjustment range : $0.385 \times (V_{LCD}-GND) \le V_{DR} \le 0.952 \times (V_{LCD}-GND)$ - Limit of potential difference between V5 and GND : $\frac{R}{2 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V] - Limit if potential difference between VLCD and V1 : $\frac{VR}{2 \times R + VR} \times (V_{LCD}-GND) \ge 0.1$ [V]

Liquid Crystal Display Drive Bias Selector

An optimum liquid crystal display bias value can be selected using BS2-0 bits, according to the liquid crystal drive duty ratio setting (NL2-0 bits). Liquid crystal display drive duty ratio and bias value can be displayed while switching software applications to match the LCD panel display status. The optimum bias value calculated using the following expression is an ideal value where the optimum contrast is obtained. Driving by using a lower value than the optimum bias value provides lower contrast and lower liquid crystal display voltage (potential difference between V1 and GND). When the liquid crystal display voltage is insufficient even if a triple booster is used or output voltage is lowered because the battery life has been reached, the display can be made easier to see by lowering the liquid crystal bias.

The liquid crystal display can be adjusted by using the contrast adjustment register (CT4-0 bits) and selecting the booster output level (BT1/0 bits).

$$\text{Optimum bias value for 1/N duty ratio drive voltage} = \frac{1}{\sqrt{N} + 1}$$

Table 38 Optimum Drive Bias Values

LCD drive duty ratio (NL2-0 set value)	1/42 duty ratio (NL2-0 = 101)	1/34 duty ratio (NL2-0 = 100)	1/26 duty ratio (NL2-0 = 011)	1/18 duty ratio (NL2-0 = 010)	1/10 duty ratio (NL2-0 = 001)	1/2 duty ratio (NL2-0 = 000)
Optimum drive bias value (BS2-0 set value)	1/7 bias (BS2-0 = 001)	1/6 bias (BS2-0 = 010)	1/6 bias (BS2-0 = 010)	1/5 bias (BS2-0 = 100)	1/4 bias (BS2-0 = 110)	1/2 bias (BS2-0 = 111)

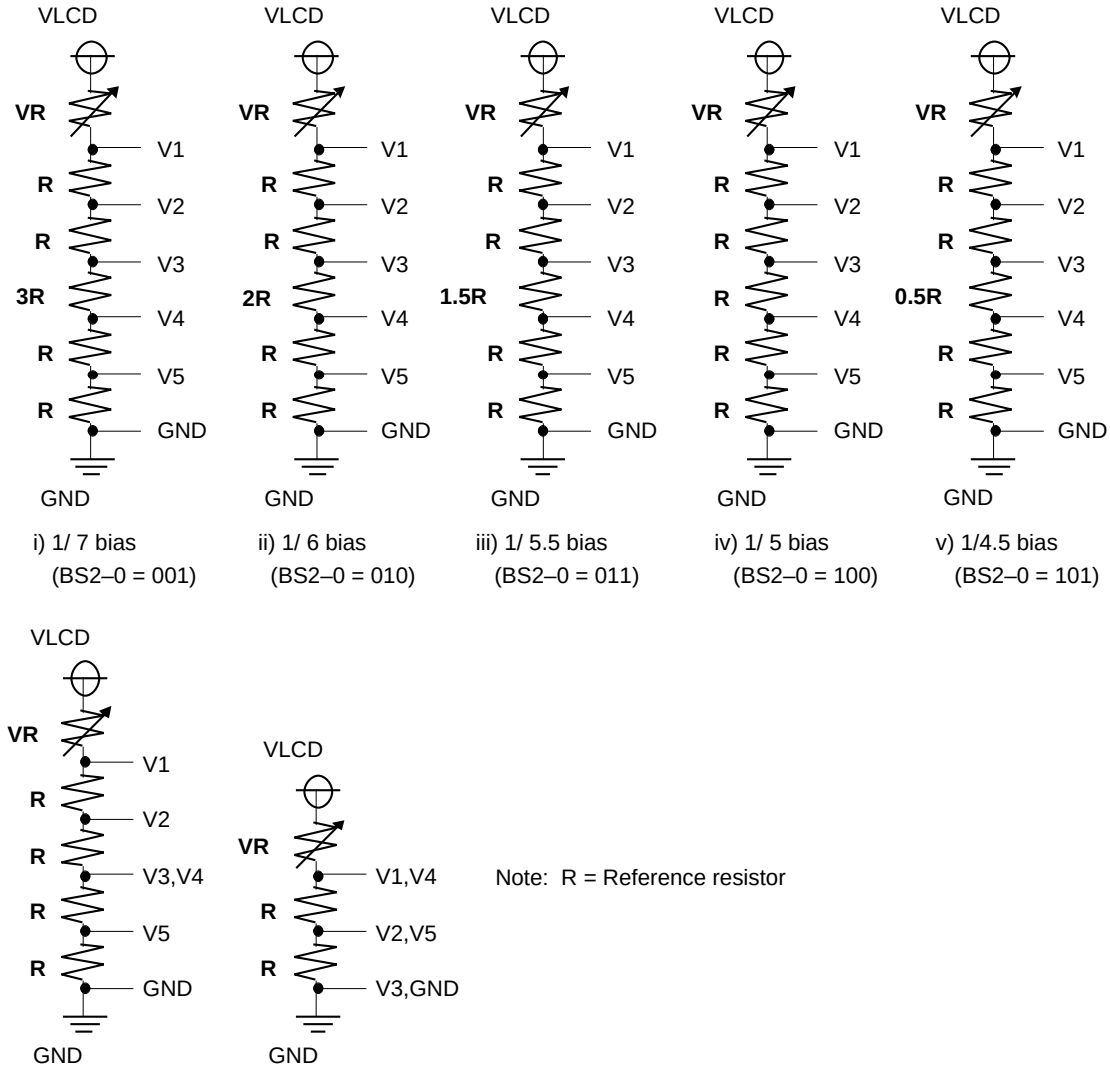


Figure 43 Liquid Crystal Display Drive Bias Circuit

LCD Panel Interface

The HD66726 has a function for changing the common driver/segment driver output shift direction using the CMS bit and SGS bit to meet the chip mounting positions of the HD66726. This is to facilitate the interface wiring to the LCD panel with COG or TCP installed.

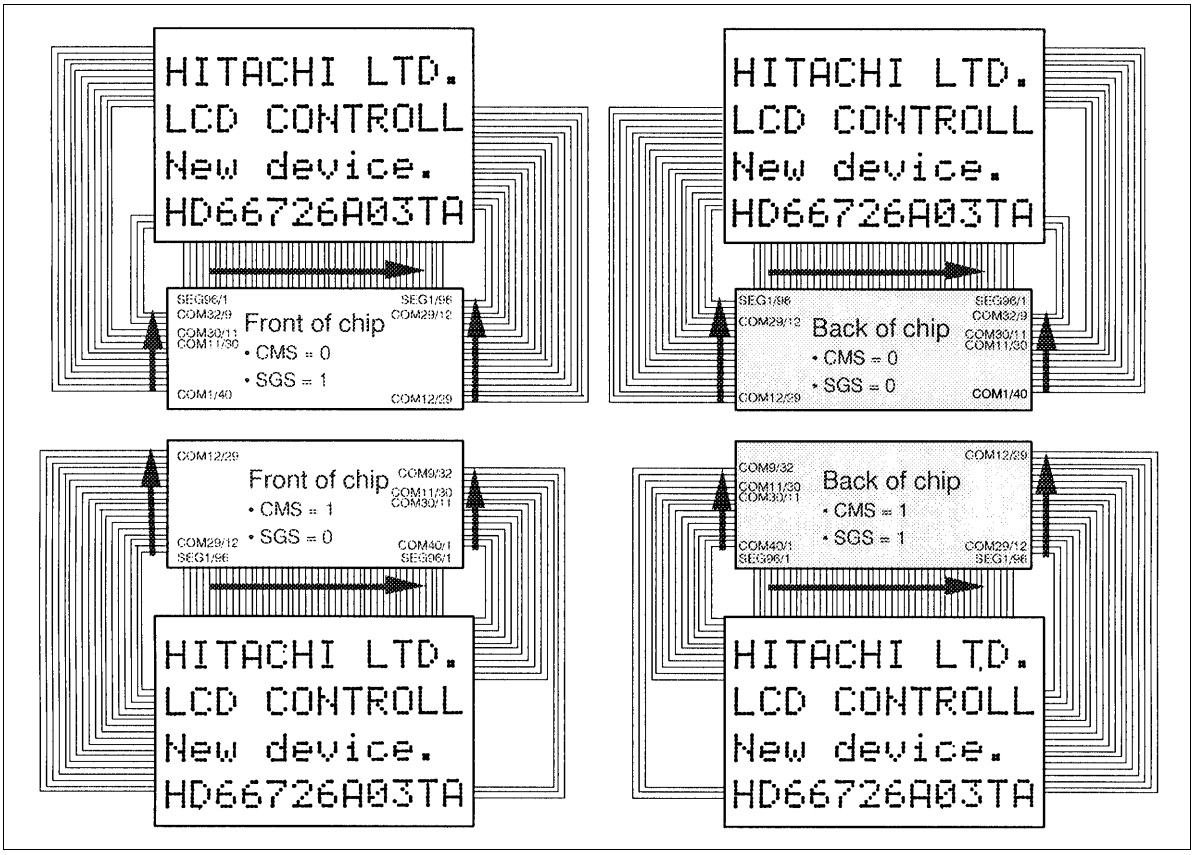


Figure 44 4-line Display Pattern Wiring

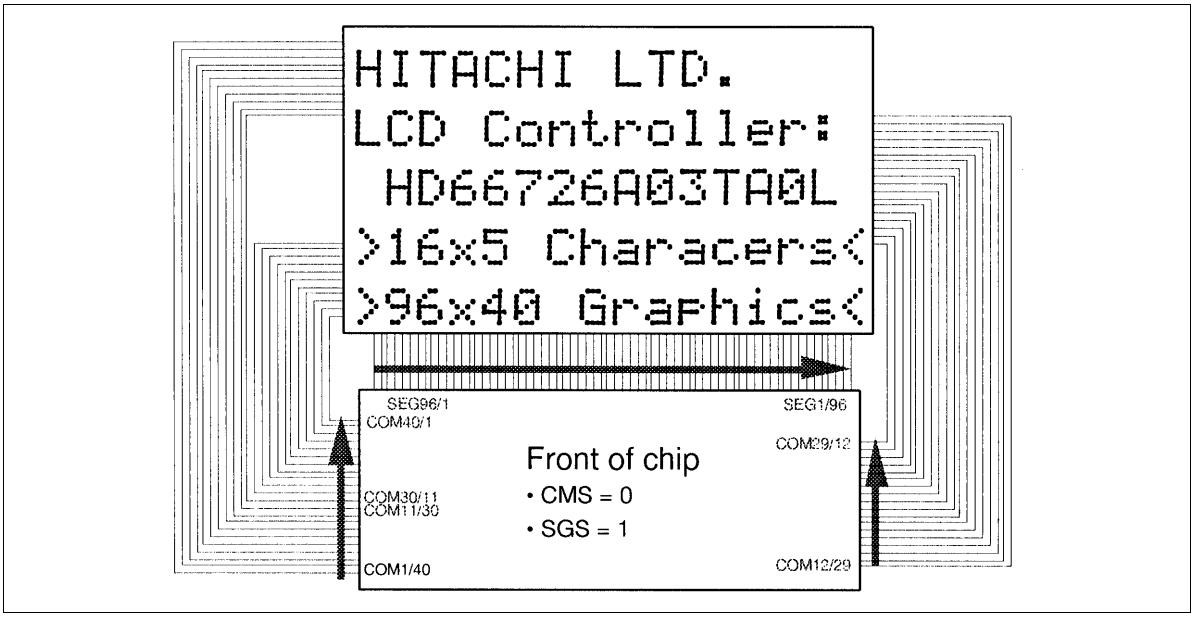


Figure 45 5-line Display Pattern Wiring

CGROM Bank Switching Function

The HD66726 incorporates two pages of CGROM. Switching the memory bank in a display line unit using the CGROM bank switching bits (RL1 to RL5) can display a total of 432 font patterns. Since each display line switches memory bank 0/1, the number of fonts which can be displayed in the same display line is 240 CGROMs + 16 CGRAMs when memory bank 0 is selected, and 192 CGROMs + 64 CGRAMs when memory bank 1 is selected. Font displays for CGRAMs (1) to (16) are used in common with memory bank 0 and memory bank 1.

With the number of fonts is extended, multinational fonts, special symbols, and icons can be displayed. In addition, the character display mode can simply implement multiple displays: graphic pictograms or graphic mark displays that use a one-line display, and menu bar displays by using the black-white reversed fonts that are supported by the graphics display.

Table 39 RL Bit Setting

Bit Set Value	Set RLn = 0	Set RLn = 1
RL1 bit	The first line is displayed by memory bank 0.	The first line is displayed by memory bank 1.
RL2 bit	The second line is displayed by memory bank 0.	The second line is displayed by memory bank 1.
RL3 bit	The third line is displayed by memory bank 0.	The third line is displayed by memory bank 1.
RL4 bit	The fourth line is displayed by memory bank 0.	The fourth line is displayed by memory bank 1.
RL5 bit	The fifth line is displayed by memory bank 0.	The fifth line is displayed by memory bank 1.

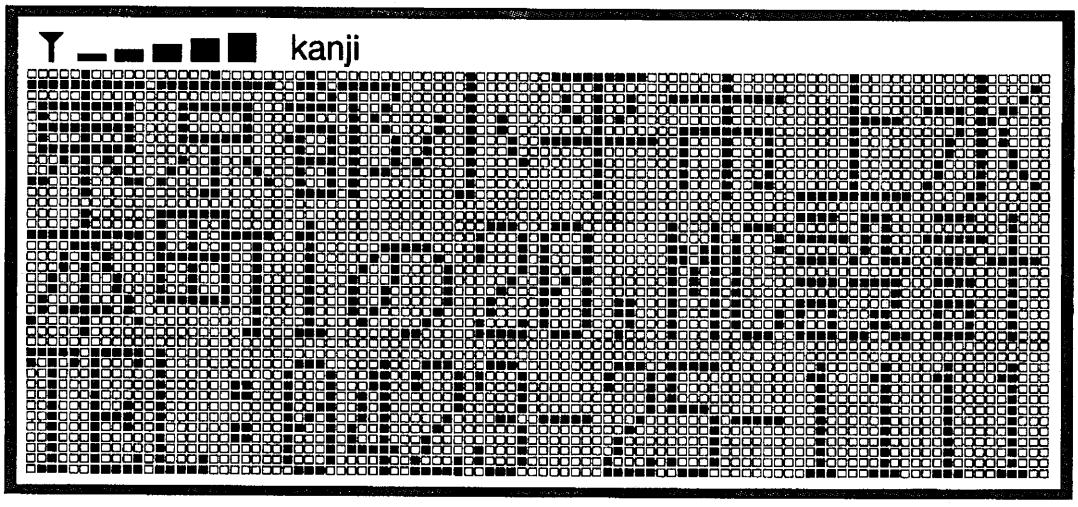
Table 40 Relationship between Character Code and Memory Bank

Character Code	Memory Bank 0 (RL1–5 = 0)	Memory Bank 1 (RL1–5 = 1)
"00"H to "0F"H	***CGRAM (1) to (16)***	***CGRAM (1) to (16)***
"10"H to "1F"H	CGROM (1) to (16)	***CGRAM (17) to (32)***
"20"H to "2F"H	CGROM (17) to (32)	CGROM (241) to (256)
"30"H to "3F"H	CGROM (33) to (48)	CGROM (257) to (272)
"40"H to "4F"H	CGROM (49) to (64)	CGROM (273) to (288)
"50"H to "5F"H	CGROM (65) to (80)	CGROM (289) to (304)
"60"H to "6F"H	CGROM (81) to (96)	CGROM (305) to (320)
"70"H to "7F"H	CGROM (97) to (112)	CGROM (321) to (336)
"80"H to "8F"H	CGROM (113) to (128)	***CGRAM (33) to (48)***
"90"H to "9F"H	CGROM (129) to (144)	***CGRAM (49) to (64)***
"A0"H to "AF"H	CGROM (145) to (160)	CGROM (337) to (352)
"B0"H to "BF"H	CGROM (161) to (176)	CGROM (353) to (368)
"C0"H to "CF"H	CGROM (177) to (192)	CGROM (369) to (384)
"D0"H to "DF"H	CGROM (193) to (208)	CGROM (385) to (400)
"E0"H to "EF"H	CGROM (209) to (224)	CGROM (401) to (416)
"F0"H to "FF"H	CGROM (225) to (240)	CGROM (417) to (432)

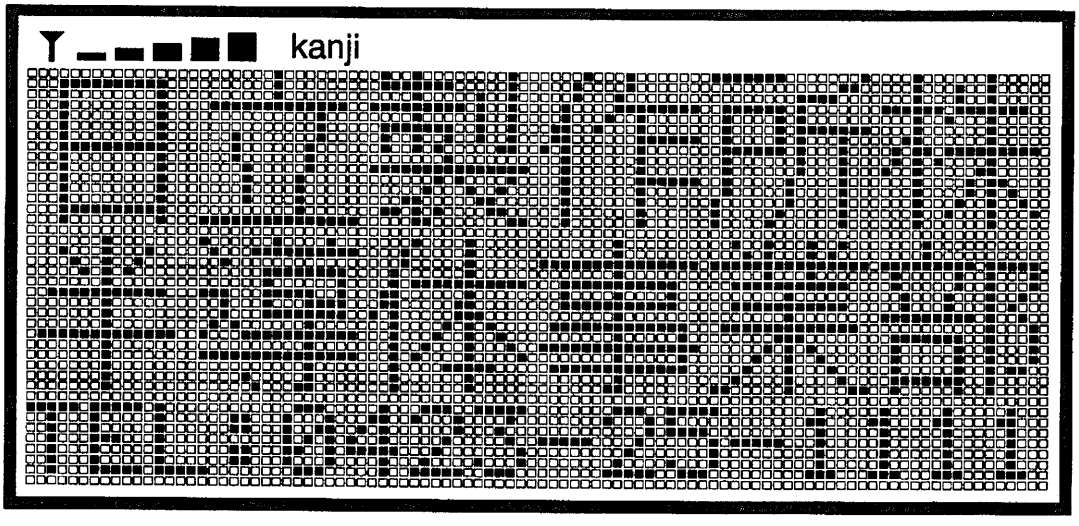
Graphics Display Function

The HD66726 has a character display mode (GR = 0) where CGRAM or CGROM is used to display font patterns, and a graphics display mode (GR = 1) where the bit pattern data is set to CGRAM to display given patterns. In the character display mode, an LCD panel display can easily be provided by sending byte-per-character character codes to DDRAM, but any pattern not set to CGROM or CGRAM cannot be displayed. In the graphics display mode, all bit pattern data to be displayed must be sent although any pattern can be displayed. The HD66726 supports both of these modes which can easily be switched using the GR bit.

In the graphics display mode, kanji characters, special symbols, and graphic icons can be displayed. Up to 96 x 40-dot display is allowed using CGRAM and SEGRAM. Thus, for a 11 x 12-dot kanji font, up to a 3-line x 8-character kanji display, and for a 15 x 15-dot kanji font, up to a 2.5-line x 6-character kanji display and a 192-segment display are allowed.



i) Example of 11 x 12-dot kanji font (3-line x 8-character display)



ii) Example of 15 x 15-dot kanji font (2.5-line x 6-character display)

Figure 46 Kanji Display in Graphics Display Mode

Vertical Smooth Scroll

The HD66726 can scroll vertically in units of raster-rows. This is achieved by writing display data into a one-line area that is not being used for display. In other words, one line can be used to achieve continuous smooth vertical scroll even in a 4-line or less display. Here, after the fifth line is displayed, the first line is displayed again. In the fifth line display mode, all one-line display data must be rewritten immediately after scrolling because there is no non-displayed area. The segment (mark) display is system-fixed and the scroll function cannot be used.

Specifically, this function is controlled by incrementing or decrementing the value in the display-start line bits (SL2 to SL0) and display-start raster-row bits (SN2 to SN0) by 1. For example, to smoothly scroll up, first set line bits SN2 to SN0 to 000, and increment SL2 to SL0 by 1 from 000 to 111 to scroll seven raster-rows. Then increment line bits SN2 to SN0 to 001, and again increment SL2 to SL0 by 1 from 000 to 111.

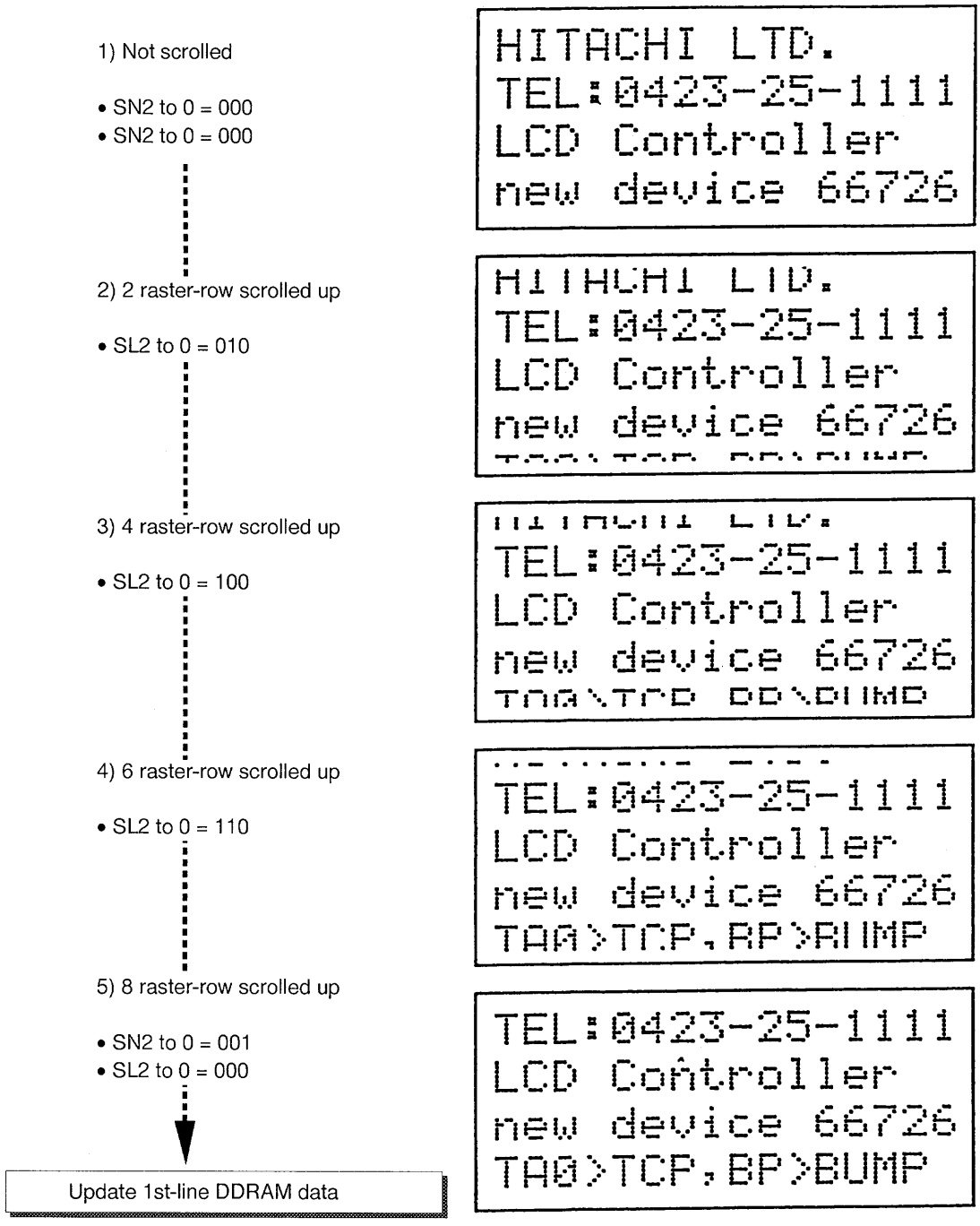
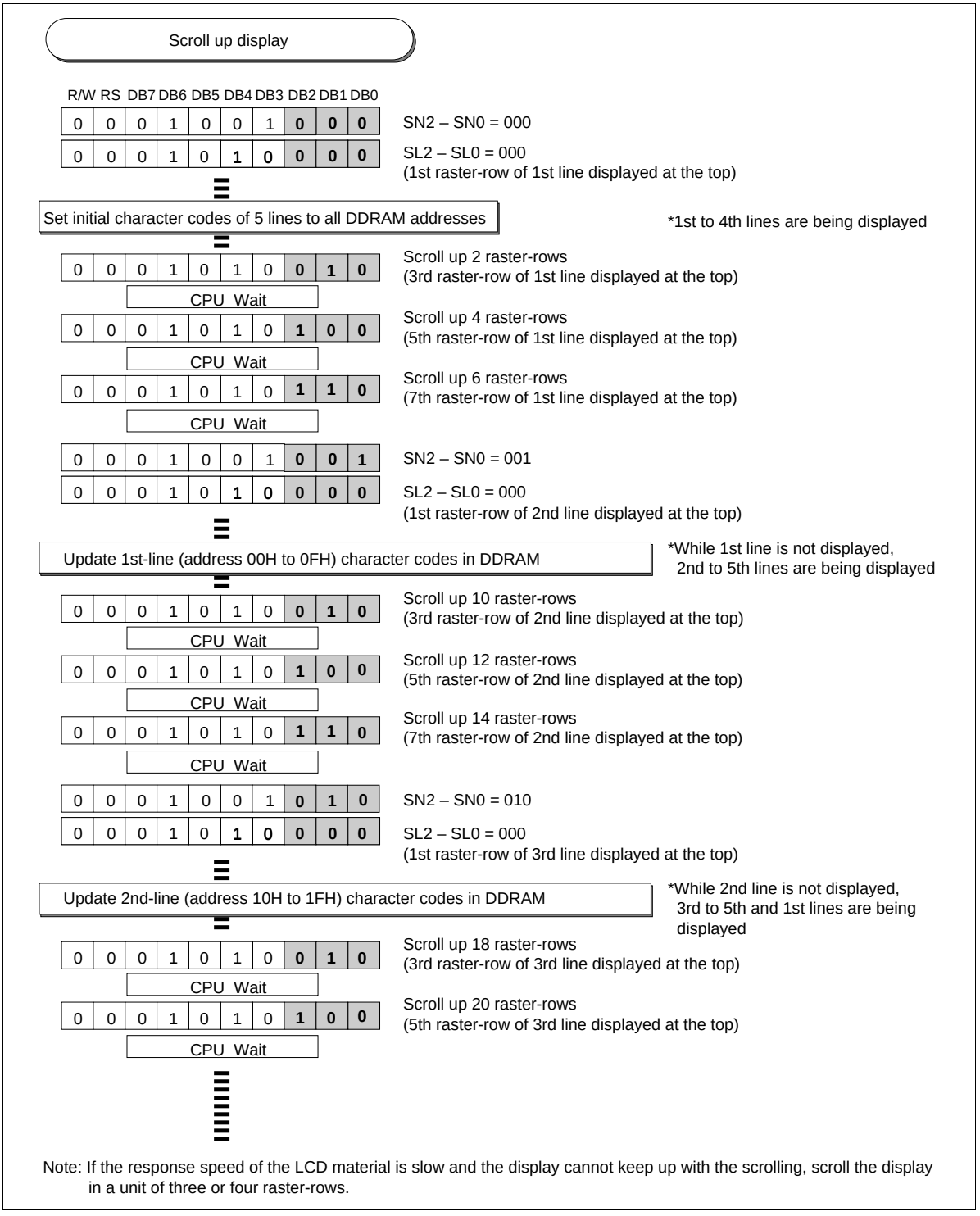


Figure 47 Vertical Smooth Scroll (4-line Display)

Setting Instructions (Character Display Mode: GR = 0, 4-line Display: NL2-0 = 100)



Note: If the response speed of the LCD material is slow and the display cannot keep up with the scrolling, scroll the display in a unit of three or four raster-rows.

Figure 48 Setting Instructions for Vertical Smooth Scroll (Character Display Mode)

Setting Instructions (Graphics Display Mode: GR = 1, 5-line Display: NL2-0 = 101)

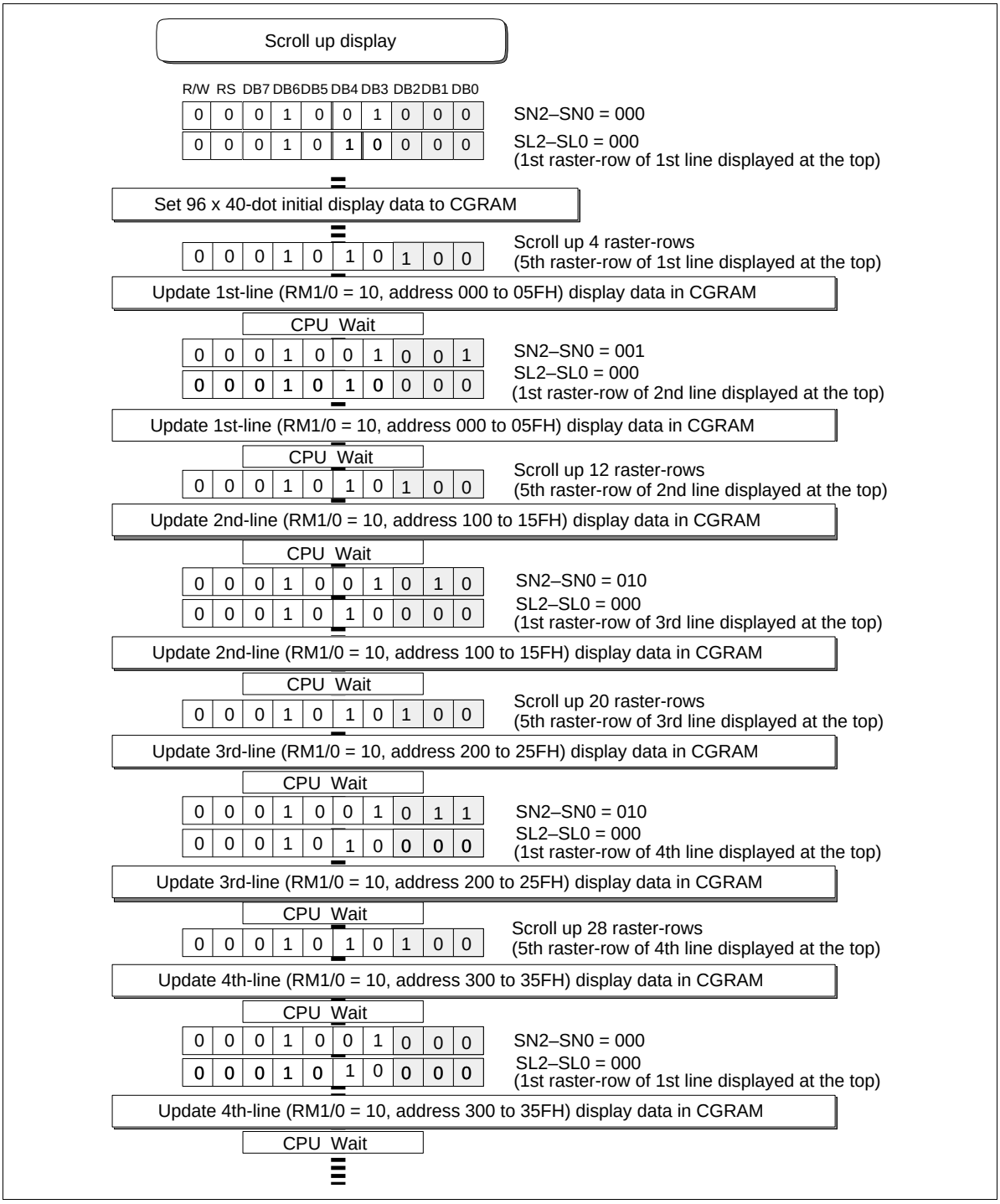


Figure 49 Setting Instructions for Vertical Smooth Scroll (Graphics Display Mode)

Double-height Display

The HD66726 can double the height of any desired line from the first to third lines. A line can be selected by the DL3 to DL1 bits as listed in table 41. All the standard font characters stored in the CGROM and CGRAM can be doubled in height, allowing easy recognition. Note that there should be no space between the lines for double-height display (figure 50).

In the 5-line display mode (NL2 to NL0 = 1001), when the double-height display is applied using the fourth and fifth lines, the CEN bit should be set to 1 and DL3 to 1 after the display position is moved by one line.

Table 41 Double-height Display Specifications

Bit Setting			2-line Display	3-line Display	4-line Display	5-line Display
DL3	DL2	DL1	(NL2-0 = 010)	(NL2-0 = 011)	(NL2-0 = 100)	(NL2-0 = 101)
0	0	0	1st to 2nd lines: normal	1st to 3rd lines: normal	1st to 4th lines: normal	1st to 5th lines: normal
0	0	1	1st line: double-height	1st line: double-height, 2nd line: normal	1st line: double-height, 2nd to 3rd lines: normal	1st line: double-height, 2nd to 4th lines: normal
0	1	0	Disabled	2nd line: double-height, 1st line: normal	2nd line: double-height, 1st and 3rd lines: normal	2nd line: double-height, 1st and 3rd to 4th lines: normal
0	1	1	1st line: double-height	Disabled	1st to 2nd lines: normal	1st to 2nd lines: double-height, 3rd line: normal
1	0	0	1st to 2nd lines: normal	Disabled	3rd line: double-height, 1st to 2nd lines: normal	3rd line: double-height, 1st to 2nd and 4th lines: normal
1	0	1	1st line: double-height	1st line: double-height, 2nd line: normal	Disabled	1st & 3rd lines: double-height, 2nd line: normal
1	1	0	Disabled	2nd line: double-height, 1st line: normal	Disabled	2nd and 3rd lines: double-height, 1st line: normal
1	1	1	1st line: double-height	Disabled	1st to 2nd lines: normal	Disabled

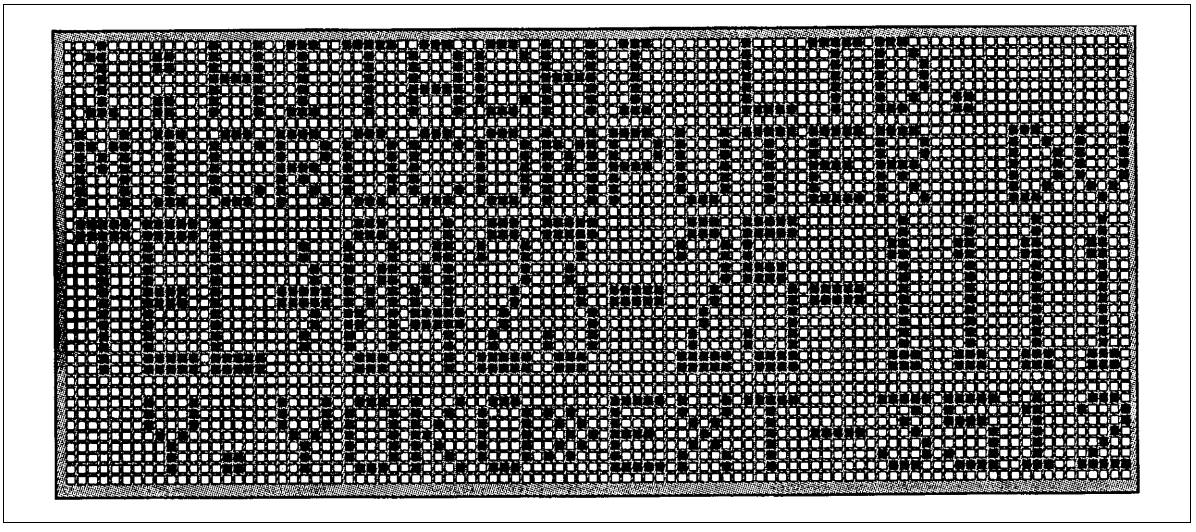


Figure 50 Double-height Display (3rd Line)

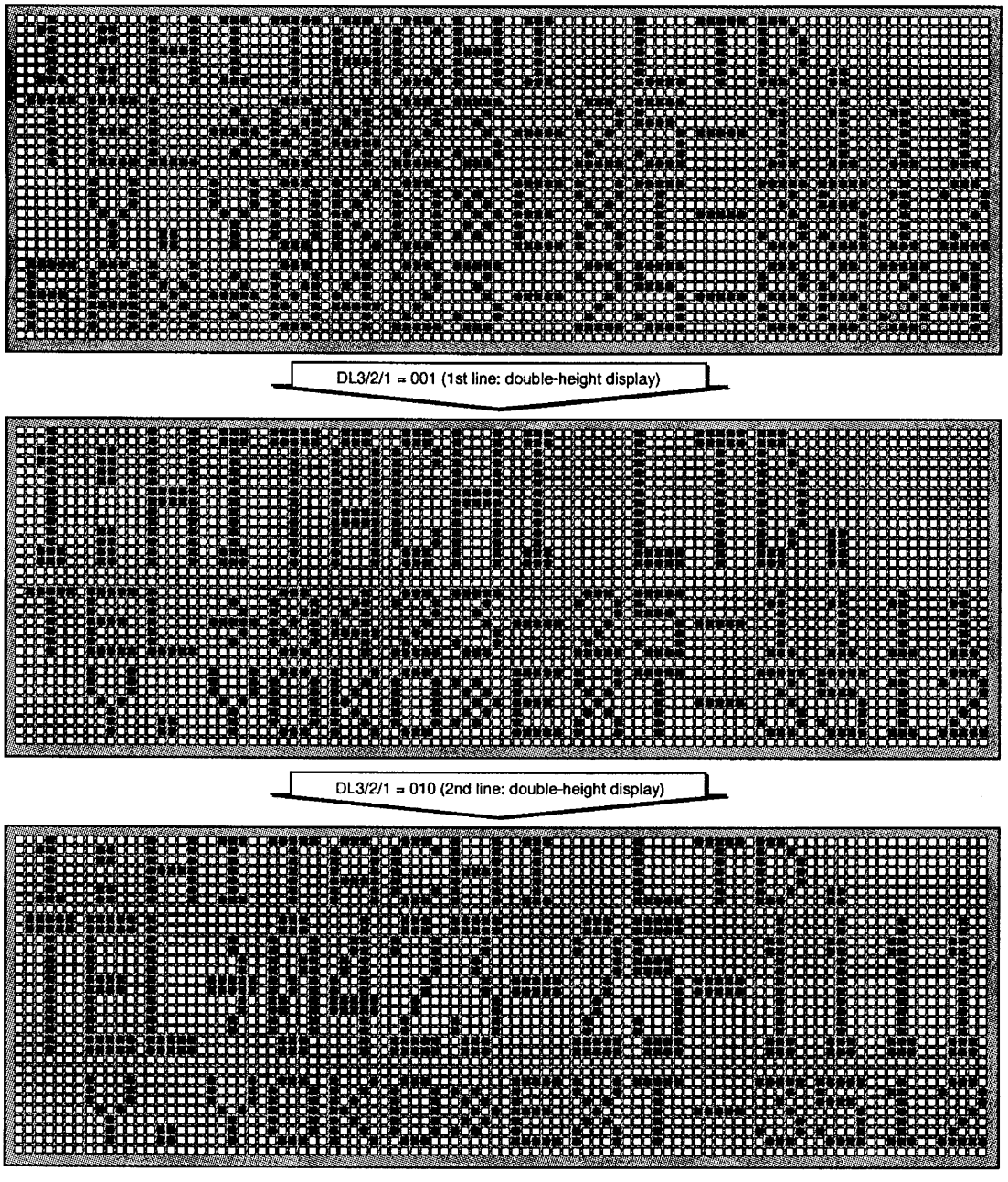


Figure 51 Double-height Display Control

Reversed Display Function

The HD66726 can display character/graphics display sections by black-white reversal except for the segment/icon display sections. Black-white reversal can be easily displayed when REV is set to 1.

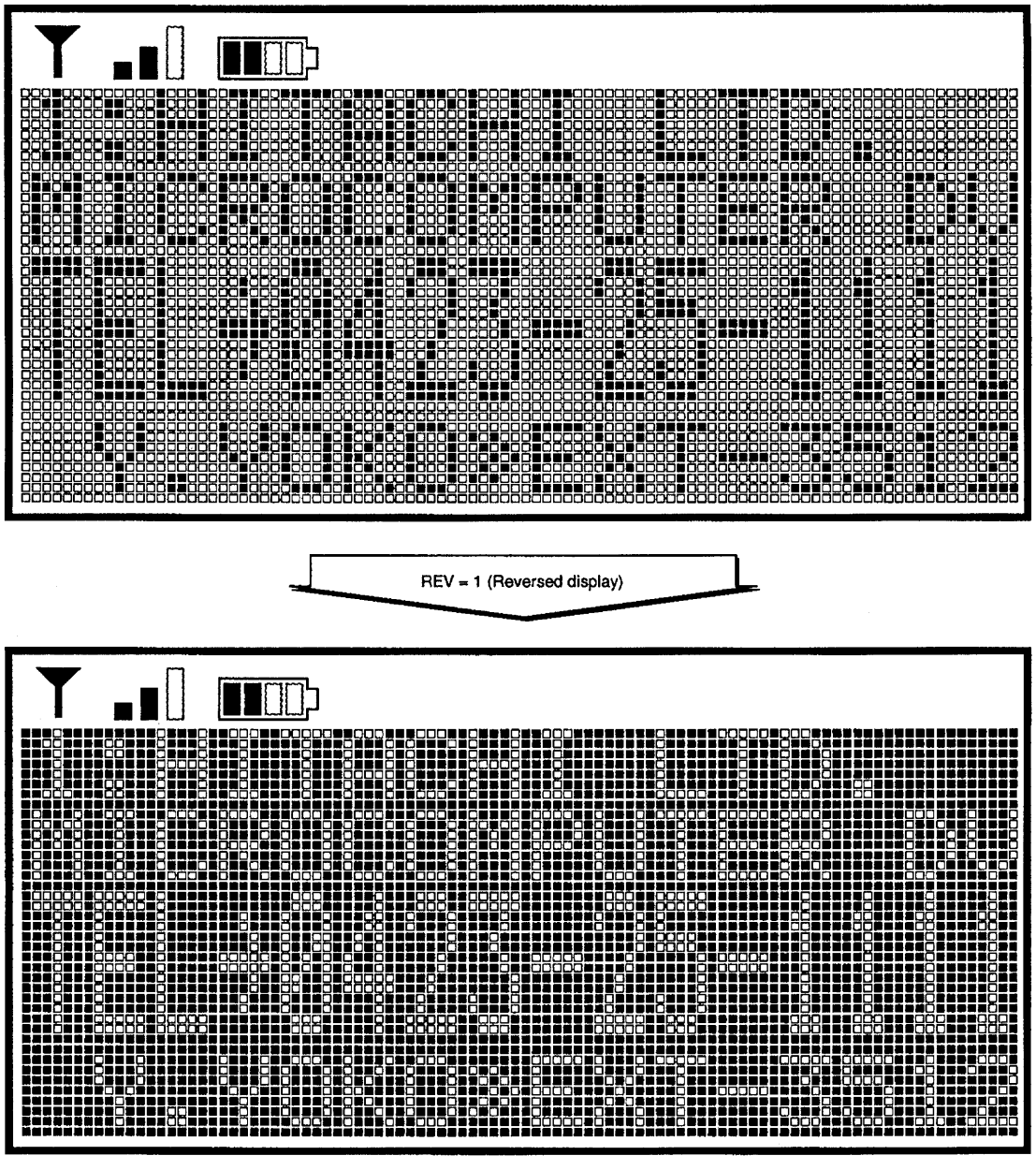


Figure 52 Reversed Display

Blink Mark Display

The HD66726 has a grayscale display and blink display based on 192 individual segments (marks). Sixty-four of these are for grayscale display and the remainder are for blink display.

These 64 segments can also control a grayscale display, providing simple grayscale on specific pictograms or marks. The above display uses a curtailed frame grayscale system, and flicker may result in quick-response liquid crystal materials. Table 43 shows the relationship between set data in SEGRAM and effective applied voltage during frame curtailing operation.

The remaining 128 segments are responsible for normal blinking and double-speed blinking. Normal blinking (black and white) is achieved by repeatedly turning on each segment for 32 frames and turning it off for the next 32 frames. Double-speed blinking (black and white) is achieved by repeatedly turning on each segment for 16 frames and turning it off for the next 16 frames, that is, double the speed of normal blinking.

Table 42 Relationship between Segment Driver Output Pin and Segment Display Function

When SGS = 0	When SGS = 1	Segment Output Control
SEG1/96, SEG4/93, SEG7/90, SEG10/87, SEG13/84, SEG16/81, SEG19/78, SEG22/75, SEG25/72, SEG28/69, SEG31/66, SEG34/63, SEG37/60, SEG40/57, SEG43/54, SEG46/51, SEG49/48, SEG52/45, SEG55/42, SEG58/39, SEG61/36, SEG64/33, SEG67/30, SEG70/27, SEG73/24, SEG76/21, SEG79/18, SEG82/15, SEG85/12, SEG88/9, SEG91/6, SEG94/3	SEG96/1, SEG93/4, SEG90/7, SEG87/10, SEG84/13, SEG81/16, SEG78/19, SEG75/22, SEG72/25, SEG69/28, SEG66/31, SEG63/34, SEG60/37, SEG57/40, SEG54/43, SEG51/46, SEG48/49, SEG45/52, SEG42/55, SEG39/58, SEG36/61, SEG33/64, SEG30/67, SEG27/70, SEG24/73, SEG21/76, SEG18/79, SEG15/82, SEG12/85, SEG9/88, SEG6/91, SEG3/94	Grayscale segment display allowed
Output pins other than above	Output pins other than above	Segment blinking allowed

Table 43 Relationship between SEGRAM Data and Grayscale Segment Display (Grayscale Control Segment Driver)

SEGRAM Data Setting				Effective Applied Voltage	SEGRAM Data Setting				Effective Applied Voltage
DB3	DB2	DB1	DB0	for COMS1 Segment	DB7	DB6	DB5	DB4	for COMS2 Segment
0	0	0	0	0 (Always unlit)	0	0	0	0	0 (Always unlit)
0	0	0	1	1 (Always lit)	0	0	0	1	1 (Always lit)
0	0	1	0	0.34 (Grayscale display)	0	0	1	0	0.34 (Grayscale display)
0	0	1	1	0.38 (Grayscale display)	0	0	1	1	0.38 (Grayscale display)
0	1	0	0	0.41 (Grayscale display)	0	1	0	0	0.41 (Grayscale display)
0	1	0	1	0.44 (Grayscale display)	0	1	0	1	0.44 (Grayscale display)
0	1	1	0	0.47 (Grayscale display)	0	1	1	0	0.47 (Grayscale display)
0	1	1	1	0.50 (Grayscale display)	0	1	1	1	0.50 (Grayscale display)
1	0	0	0	(Blink display) *	1	0	0	0	(Blink display) *
1	0	0	1	0.53 (Grayscale display)	1	0	0	1	0.53 (Grayscale display)
1	0	1	0	0.56 (Grayscale display)	1	0	1	0	0.56 (Grayscale display)
1	0	1	1	0.59 (Grayscale display)	1	0	1	1	0.59 (Grayscale display)
1	1	0	0	0.63 (Grayscale display)	1	1	0	0	0.63 (Grayscale display)
1	1	0	1	0.66 (Grayscale display)	1	1	0	1	0.66 (Grayscale display)
1	1	1	0	0.69 (Grayscale display)	1	1	1	0	0.69 (Grayscale display)
1	1	1	1	0.72 (Grayscale display)	1	1	1	1	0.72 (Grayscale display)

Note: Blinking is achieved by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.

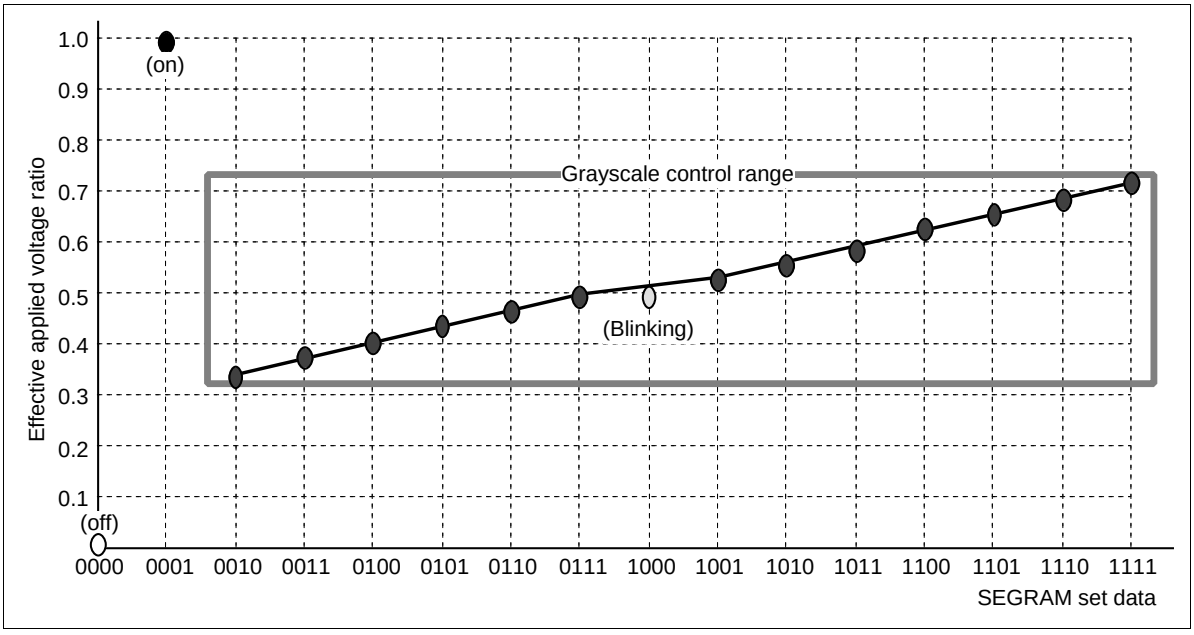


Figure 53 Relationship between SEGRAM Set Data and Effective Applied Voltage

Table 44 Relationship between SEGRAM Data and Blinking Control Segment Display (Blinking Control Segment Driver)

SEGRAM Data Setting				LCD Display Control for	SEGRAM Data Setting				LCD Display Control for
DB3	DB2	DB1	DB0	COMS1 Segment	DB7	DB6	DB5	DB4	COMS2 Segment
0	*1	*1	0	0 (Always unlit)	0	*1	*1	0	0 (Always unlit)
0	*1	*1	1	1 (Always lit)	0	*1	*1	1	1 (Always lit)
1	*1	*1	0	Blinking display *2	1	*1	*1	0	Blinking display *2
1	*1	*1	1	Double-speed blinking display *3	1	*1	*1	1	Double-speed blinking display *3

Notes: 1. 0 or 1.

2. Blinking is achieved by repeatedly turning on the segment for 32 frames and turning it off for the next 32 frames.
3. Double-speed blinking is achieved by repeatedly turning on the segment for 16 frames and turning it off for the next 16 frames.

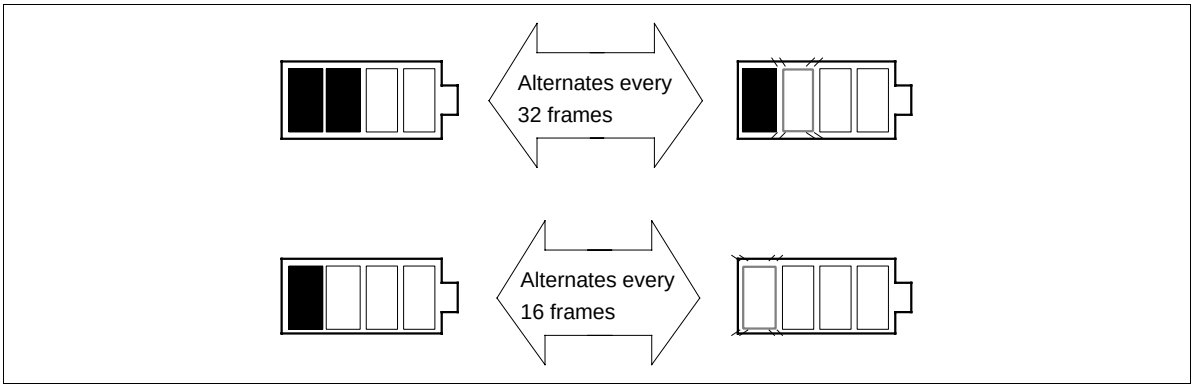


Figure 54 Blinking Control Segment Display

Line-cursor Display

The HD66726 can assign a cursor attribute to an entire line corresponding to the address counter value by setting the LC bit to 1. One of three line-cursor modes can be selected: a black-white reversed cursor (B/W = 1), an underline cursor (C = 1), and a blink cursor (B = 1). The cycle for a blink cursor is 32 frames. These line-cursors are suitable for highlighting an index and/or marker, or for indicating an item in a menu with a cursor or an underline.

However, the black-white reversed display described above does not perform black-white blinking.

Table 45 Address Counter Value and Line Cursor

Address Counter Value (AC)	Selected Line for Line Cursor
00H to 0FH	Entire 1st line (16 characters)
10H to 1FH	Entire 2nd line (16 characters)
20H to 2FH	Entire 3rd line (16 characters)
30H to 3FH	Entire 4th line (16 characters)
40H to 4FH	Entire 5th line (16 characters)

Black-white Reversed Cursor (LC = 1, B/W = 1)

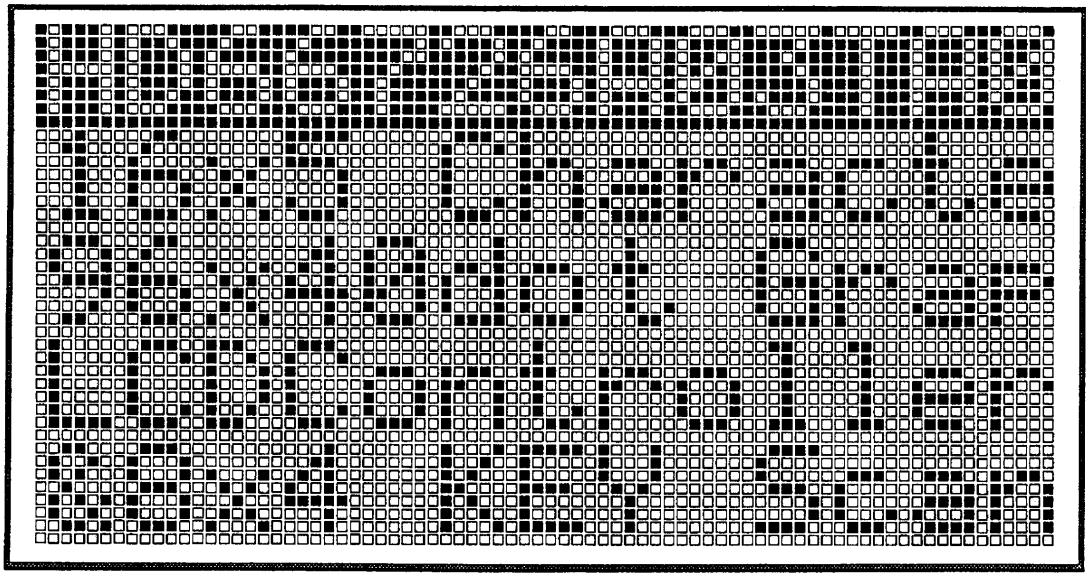


Figure 55 Black-white Reversed Cursor

Underline Cursor (LC = 1, C = 1)

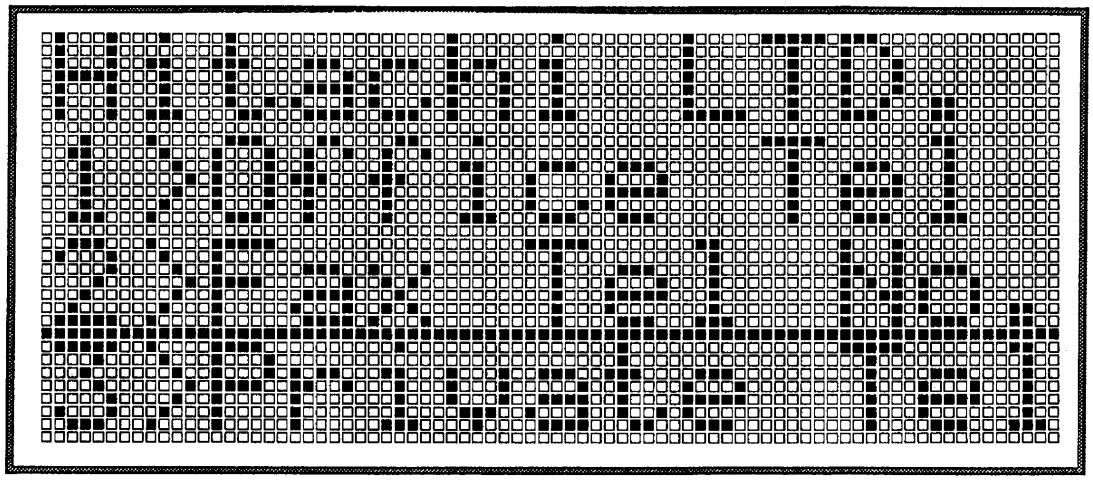


Figure 56 Underline Cursor

Blink Cursor (LC = 1, B = 1)

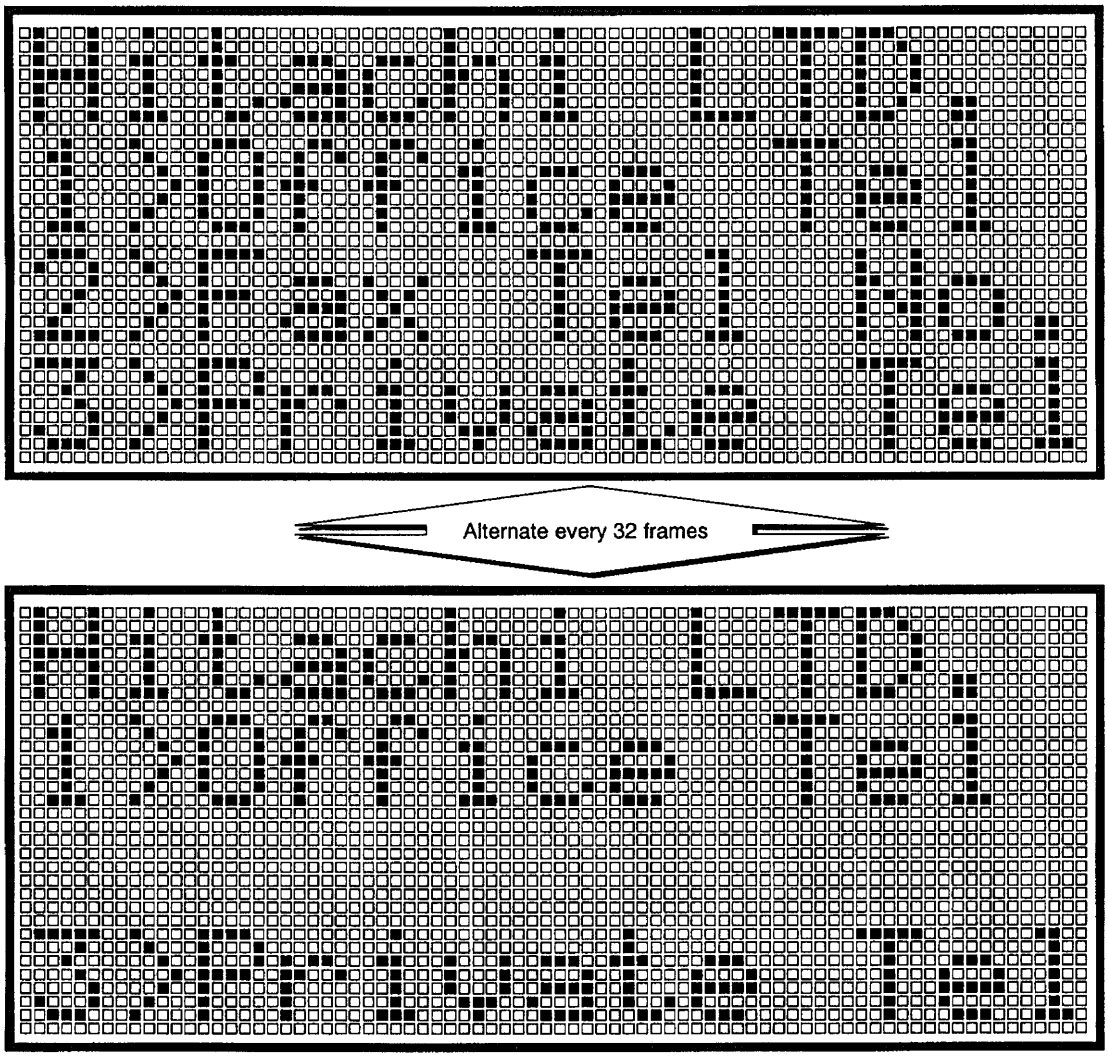


Figure 57 Blink Cursor

Partial-display-on Function

The HD66726 can program the liquid crystal display drive duty ratio setting (NL2-0 bits), liquid crystal display drive bias value selection (BS2-0 bits), boost output level selection (BT1/0 bit) and contrast adjustment (CT4-0 bits). For example, in the four-line display mode (1/34 duty ratio), the HD66726 can drive only two lines in the center of the screen by combining these register functions and the centering display (CEN bit) function. This is called partial-display-on. Lowering the liquid crystal display drive duty ratio as required saves the liquid crystal display drive voltage, thus reducing internal current consumption. This is suitable for calendar or time display, which needs to be continuous in the system standby state with minimal current consumption. Here, the non-displayed lines are constantly driven by the unselected level voltage, thus turning off the LCD for the lines.

In general, lowering the liquid crystal display drive duty ratio decreases the optimum liquid crystal display drive voltage and liquid crystal display drive bias value.

Table 46 Partial-display-on Function (4-line Display)

Item	Normal 4-line Display	Partial-on Display	
Character display	4th line displayed	Only one line in the center of the screen	Only two lines in the center of the screen
Segment display	Possible	Possible	Possible
Centering display	Not necessary (CEN = 0)	Possible (CEN = 1)	Possible (CEN = 1)
LCD drive duty ratio	1/34 (NL2/1/0 = 100)	1/10 (NL2/1/0 = 001) possible	1/18 (NL2/1/0 = 010) possible
LCD drive bias value (optimum)	1/6 (BS2-0 = 010)	1/4 (BS2-0 = 110)	1/5 (BS2-0 = 100)
LCD drive voltage	Adjustable using BT1/0 and CT4-0	Adjustable using BT1/0 and CT4-0	Adjustable using BT1/0 and CT4-0
Frame frequency (fosc = 50 kHz)	74 Hz	74 Hz	73 Hz

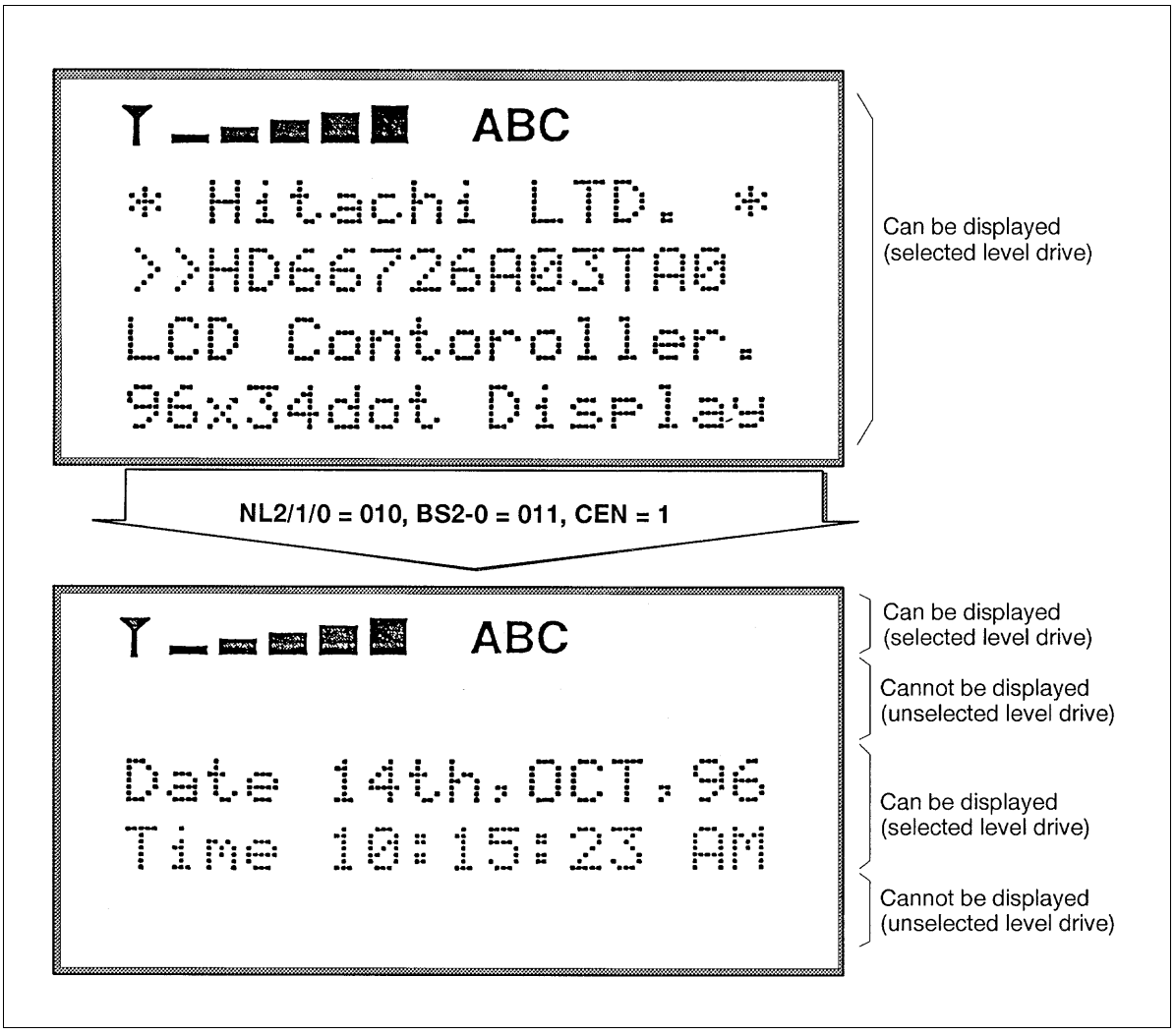


Figure 58 Partial-on Display (Date and Time Indicated)

Sleep Mode

Setting the sleep mode bit (SLP) to 1 puts the HD66726 in the sleep mode, where the device stops all internal display operations except for key scan operations, thus reducing current consumption. Specifically, LCD drive is completely halted. Here, all the SEG (SEG1 to SEG96 and COM (COM1 to COM40, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the sleep mode, the LCD drive power supply can be turned off, reducing the total current consumption of the LCD module.

The key scan circuit operates normally in the sleep mode, thus allowing normal key scan and key scan interrupt generation. For details, see the Key Scan Control section and Key Scan Interrupt (Wake-up Function) section.

Table 47 Comparison of Sleep Mode and Standby Mode

Function	Sleep Mode (SLP = 1)	Standby Mode (STB = 1)
Character display	Turned off	Turned off
Segment display	Turned off	Turned off
R-C oscillation circuit	Operates normally	Halted
Key scan circuit	Can operate normally	Halted but IRQ* can be generated

Standby Mode

Setting the standby mode bit (STB) to 1 puts the HD66726 in the standby mode, where the device stops completely, halting all internal operations including the R-C oscillation circuit, thus further reducing current consumption compared to that in the sleep mode. Specifically, character and segment displays, which are controlled by the multiplexing drive method, are completely halted. Here, all the SEG (SEG1 to SEG96) and COM (COM1 to COM40, COMS1/2) pins output the GND level, resulting in no display. If the AMP bit is set to 0 in the standby mode, the LCD drive power supply can be turned off.

During the standby mode, no instructions can be accepted other than those for the start-oscillation instruction and the key scan interrupt generation enable instruction. To cancel the standby mode, issue the start-oscillation instruction to stabilize R-C oscillation before setting the STB bit to 0.

Although key scan is halted in the standby mode, the HD66726 can detect key inputs, thus generating key scan interrupt (IRQ*). This means, the system can be activated from a completely inactive state. For details, see the Key Scan Interrupt (Wake-up Function) section.

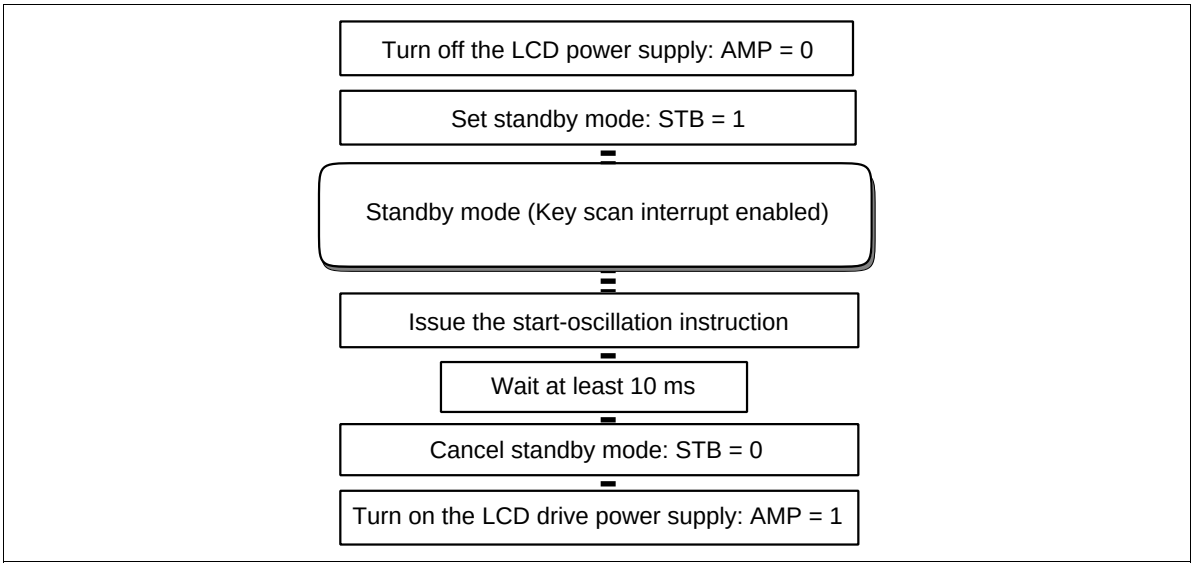


Figure 59 Procedure for Setting and Canceling Standby Mode

Absolute Maximum Ratings *

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	V_{CC}	V	–0.3 to +7.0	1
Power supply voltage (2)	V_{LCD} – GND	V	–0.3 to +15.0	1, 2
Input voltage	Vt	V	–0.3 to V_{CC} + 0.3	1
Operating temperature	Topr	°C	–40 to +85	
Storage temperature	Tstg	°C	–55 to +110	4

Note: If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristics limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage	V_{IH}	0.7 V_{CC}	—	V_{CC}	V		5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 1.8 to 2.7 V	5, 6
Input low voltage	V_{IL}	–0.3	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V	5, 6
Output high voltage (1) (SDA, DB0-7 pins)	V_{OH1}	0.75 V_{CC}	—	—	V	I_{OH} = –0.1 mA	5, 7
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.2 V_{CC}	V	V_{CC} = 1.8 to 2.7 V, I_{OL} = 0.1 mA	5
Output low voltage (1) (SDA, DB0-7 pins)	V_{OL1}	—	—	0.15 V_{CC}	V	V_{CC} = 2.7 to 5.5 V, I_{OL} = 0.1 mA	5
Output high voltage (2) (KST0-7, IRQ* pins)	V_{OH2}	0.7 V_{CC}	—	—	V	$–I_{OH}$ = 0.5 µA, V_{CC} = 3 V	5
Output low voltage (2) (KST0-7, IRQ* pins)	V_{OL2}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1 mA	5
Output high voltage (3) (PORT0-2 pins)	V_{OH3}	0.75 V_{CC}	—	—	V	$-I_{OH}$ = 0.1mA	5
Output low voltage (3) (PORT0-2 pins)	V_{OL3}	—	—	0.2 V_{CC}	V	I_{OL} = 0.1mA	5
Driver ON resistance (COM pins)	R_{COM}	—	3	20	kΩ	±Id = 0.05 mA, V_{LCD} = 8 V	8
Driver ON resistance (SEG pins)	R_{SEG}	—	3	30	kΩ	±Id = 0.05 mA, V_{LCD} = 8 V	8
I/O leakage current	I_{Li}	–1	—	1	µA	Vin = 0 to V_{CC}	9
Pull-up MOS current (KIN0-7, DB0-7, SDA pins)	$-I_p$	1	10	40	µA	V_{CC} = 3 V, Vin = 0 V	5
Current consumption during normal operation (V_{CC}–GND)	I_{OP}	—	25	50	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 50 kHz (1/42 duty)	10, 11
Current consumption during sleep mode (V_{CC}–GND)	I_{SL}	—	15	—	µA	R-C oscillation, V_{CC} = 3 V, f_{OSC} = 50 kHz (1/42 duty)	10, 11
Current consumption during standby mode (V_{CC}–GND)	I_{ST}	—	0.1	5	µA	No R-C oscillation, V_{CC} = 3 V, Ta = 25°C	10, 11
LCD drive power supply current (V_{LCD}–GND)	I_{EE}	—	15	30	µA	V_{LCD} – GND = 8 V, f_{OSC} = 50 kHz, 1/7 Bias, VTEST3 = "V_{CC}"	11
LCD drive voltage (V_{LCD} – GND)	V_{LCD}	4.5	—	13.0	V		12

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Double-boost output voltage (VLOUT pin)	V_{UP2}	5.5	5.9	—	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 50 kHz, Ta = 25°C	15
Triple-boost output voltage (VLOUT pin)	V_{UP3}	8.5	8.9	—	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 50 kHz, Ta = 25°C	15
Quadruple-boost output voltage (VLOUT pin)	V_{UP4}	11.5	11.8	—	V	V_{CC} = Vci = 3.0 V, I_O = 0.03 mA, C = 1 µF, f_{OSC} = 50 kHz, Ta = 25°C	15
Use range of boost output voltage	V_{UP2} V_{UP3} V_{UP4}	V_{CC}	—	13.0	V		15, 16

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

AC Characteristics (V_{CC} = 1.8 to 5.5 V, Ta = –40 to +85°C*[3])

Clock Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
External clock frequency	fcp	15	50	100	kHz		13
External clock duty ratio	Duty	45	50	55	%		13
External clock rise time	trcp	—	—	0.2	µs		13
External clock fall time	tfcp	—	—	0.2	µs		13
Internal Rf oscillation frequency	t_{OSC}	38	48	58	kHz	Rf = 390 kΩ, V_{CC} = 3 V	14

Note: For the numbered notes, refer to the Electrical Characteristics Notes section following these tables.

68-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	600	—	—	ns	Figure 66
	Read		800	—	—		
Enable high-level pulse width	Write	PW_{EH}	120	—	—	ns	Figure 66
	Read		350	—	—		
Enable low-level pulse width	Write	PW_{EL}	300	—	—	ns	Figure 66
	Read		300	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 66
Setup time (RS, R/W, CS* to E)		t_{ASE}	50	—	—	ns	Figure 66
Address hold time		t_{AHE}	20	—	—	ns	Figure 66
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 66
Write data hold time		t_{HE}	20	—	—	ns	Figure 66
Read data delay time		t_{DDRE}	—	—	300	ns	Figure 66
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 66

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	Write	t_{CYCE}	380	—	—	ns	Figure 66
	Read		500	—	—		
Enable high-level pulse width	Write	PW_{EH}	70	—	—	ns	Figure 66
	Read		250	—	—		
Enable low-level pulse width	Write	PW_{EL}	150	—	—	ns	Figure 66
	Read		150	—	—		
Enable rise/fall time		t_{Er}, t_{Ef}	—	—	25	ns	Figure 66
Setup time (RS, R/W, CS* to E)		t_{ASE}	50	—	—	ns	Figure 66
Address hold time		t_{AHE}	20	—	—	ns	Figure 66
Write data setup time		t_{DSWE}	60	—	—	ns	Figure 66
Write data hold time		t_{HE}	20	—	—	ns	Figure 66
Read data delay time		t_{DDRE}	—	—	200	ns	Figure 66
Read data hold time		t_{DHRE}	5	—	—	ns	Figure 66

80-system Bus Interface Timing Characteristics

(Vcc = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	600	—	—	ns	Figure 67
	Read	t_{CYCR}	800	—	—	ns	Figure 67
Write low-level pulse width		PW_{LW}	120	—	—	ns	Figure 67
Read low-level pulse width		PW_{LR}	350	—	—	ns	Figure 67
Write high-level pulse width		PW_{HW}	300	—	—	ns	Figure 67
Read high-level pulse width		PW_{HR}	300	—	—	ns	Figure 67
Write/Read rise/fall time		t_{WRr} , $_{WRf}$	—	—	25	ns	Figure 67
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 67
Address hold time		t_{AH}	20	—	—	ns	Figure 67
Write data setup time		t_{DSW}	60	—	—	ns	Figure 67
Write data hold time		t_{H}	20	—	—	ns	Figure 67
Read data delay time		t_{DDR}	—	—	300	ns	Figure 67
Read data hold time		t_{DHR}	5	—	—	ns	Figure 67

(Vcc = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Bus cycle time	Write	t_{CYCW}	380	—	—	ns	Figure 67
	Read	t_{CYCR}	500	—	—	ns	Figure 67
Write low-level pulse width		PW_{LW}	70	—	—	ns	Figure 67
Read low-level pulse width		PW_{LR}	250	—	—	ns	Figure 67
Write high-level pulse width		PW_{HW}	150	—	—	ns	Figure 67
Read high-level pulse width		PW_{HR}	150	—	—	ns	Figure 67
Write/Read rise/fall time		$t_{WRr, WRf}$	—	—	25	ns	Figure 67
Setup time (RS to CS*, WR*, RD*)		t_{AS}	50	—	—	ns	Figure 67
Address hold time		t_{AH}	20	—	—	ns	Figure 67
Write data setup time		t_{DSW}	60	—	—	ns	Figure 67
Write data hold time		t_{H}	20	—	—	ns	Figure 67
Read data delay time		t_{DDR}	—	—	200	ns	Figure 67
Read data hold time		t_{DHR}	5	—	—	ns	Figure 67

Clock-synchronized Serial Interface Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

(V_{CC} = 1.8 to 2.7 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.5	—	20	µs	Figure 68
	Read	t_{SCYC}	1	—	20	µs	Figure 68
Serial clock high-level width	Write	t_{SCH}	230	—	—	ns	Figure 68
	Read	t_{SCH}	480	—	—	ns	Figure 68
Serial clock low-level width	Write	t_{SCL}	230	—	—	ns	Figure 68
	Read	t_{SCL}	480	—	—	ns	Figure 68
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	50	ns	Figure 68
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 68
Chip select hold time		t_{CH}	200	—	—	ns	Figure 68
Serial input data setup time		t_{SISU}	100	—	—	ns	Figure 68
Serial input data hold time		t_{SIH}	100	—	—	ns	Figure 68
Serial output data delay time		t_{SOD}	—	—	400	ns	Figure 68
Serial output data hold data		t_{SOH}	5	—	—	ns	Figure 68

Reset Timing Characteristics (V_{CC} = 1.8 to 5.5 V)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	1	—	—	ms	Figure 69

(V_{CC} = 2.7 to 5.5 V)

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	Write	t_{SCYC}	0.2	—	20	µs	Figure 68
	Read	t_{SCYC}	0.5	—	20	µs	Figure 68
Serial clock high-level width	Write	t_{SCH}	80	—	—	ns	Figure 68
	Read	t_{SCH}	230	—	—	ns	Figure 68
Serial clock low-level width	Write	t_{SCL}	80	—	—	ns	Figure 68
	Read	t_{SCL}	230	—	—	ns	Figure 68
Serial clock rise/fall time		t_{scf}, t_{scr}	—	—	20	ns	Figure 68
Chip select setup time		t_{CSU}	60	—	—	ns	Figure 68
Chip select hold time		t_{CH}	200	—	—	ns	Figure 68
Serial input data setup time		t_{SISU}	40	—	—	ns	Figure 68
Serial input data hold time		t_{SIH}	40	—	—	ns	Figure 68
Serial output data delay time		t_{SOD}	—	—	200	ns	Figure 68
Serial output data hold data		t_{SOH}	5	—	—	ns	Figure 68

Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the given electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristics are exceeded, the LSI may malfunction or exhibit poor reliability.
2. VLCD > GND must be maintained.
3. For bare die products, specified at 85˚C.
4. For bare die products, specified by the common die shipment specification.
5. The following three circuits are I/O pin configurations (figure 60).

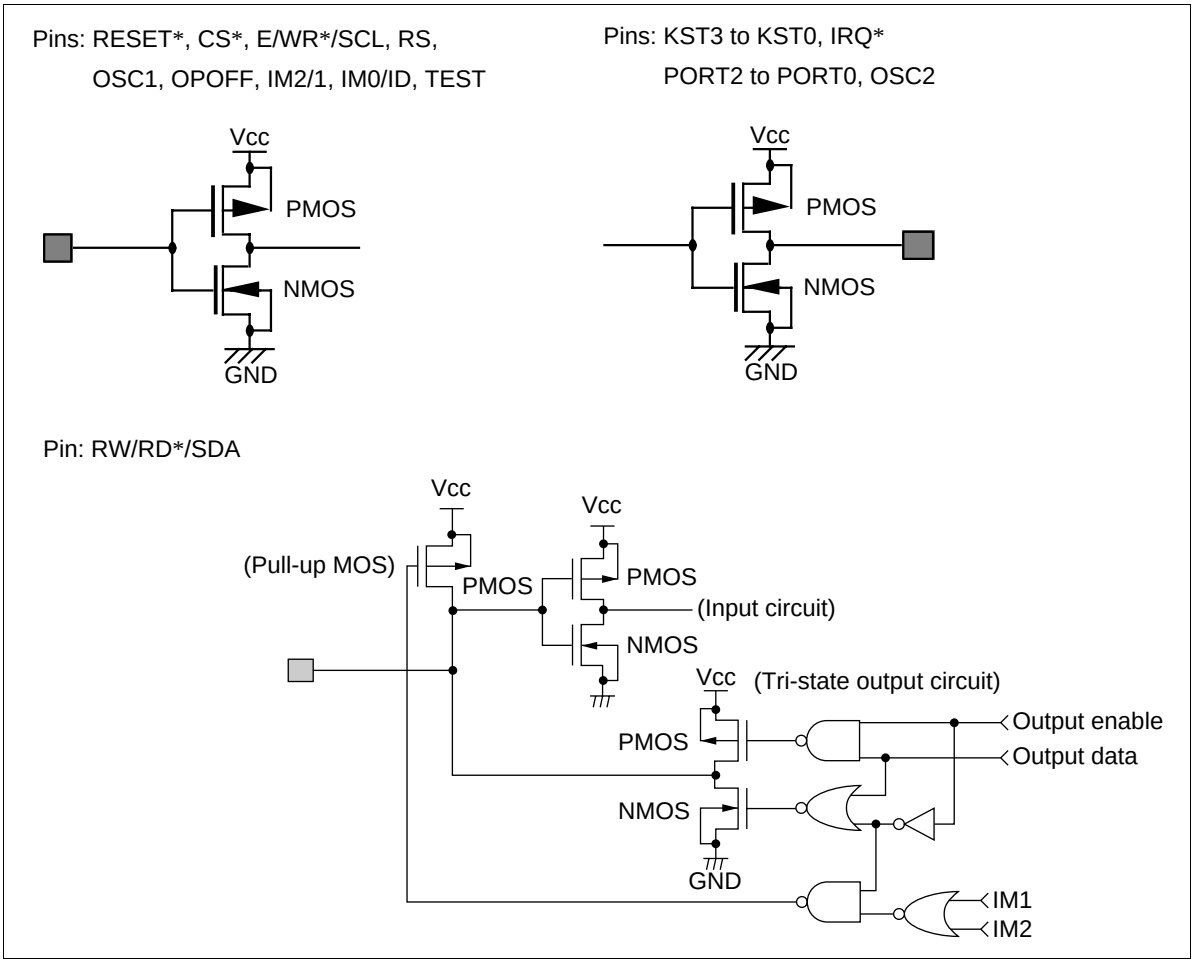


Figure 60 I/O Pin Configuration

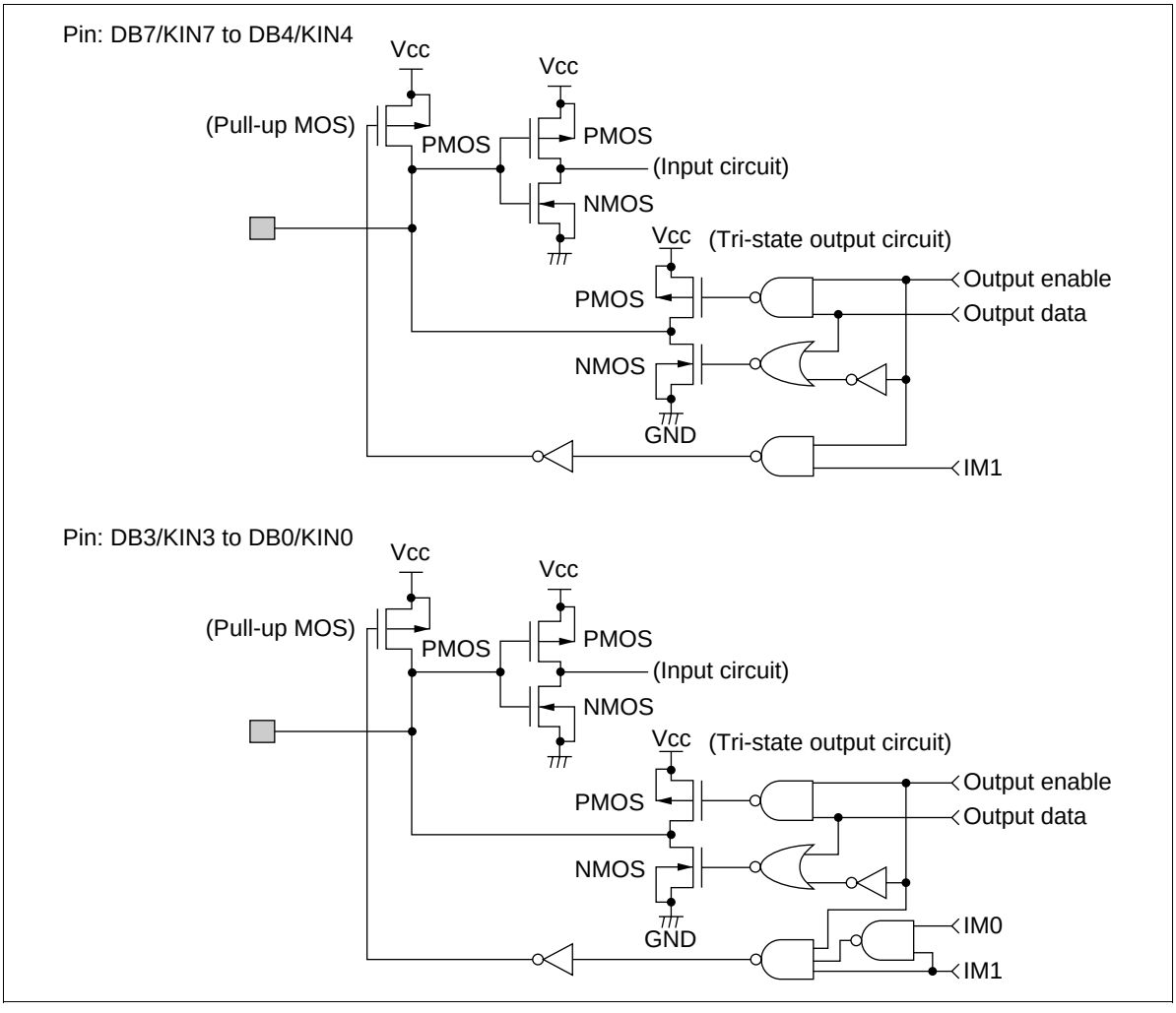


Figure 60 I/O Pin Configuration (cont)

6. The TEST pin must be grounded and the IM2/1, IM0/ID, and OPOFF pins must be grounded or connected to Vcc.
7. Corresponds to the high output for clock-synchronized serial interface.
8. Applies to the resistor value (RCOM) between power supply pins V1OUT, V2OUT, V5OUT, GND and common signal pins (COM1 to COM40, COMS1 and COMS2), and resistor value (RSEG) between power supply pins V1OUT, V3OUT, V4OUT, GND and segment signal pins (SEG1 to SEG96), when current Id is flown through all driver output pins.
9. This excludes the current flowing through pull-up MOSs and output drive MOSs.
10. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating.
11. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc) (figure 61).

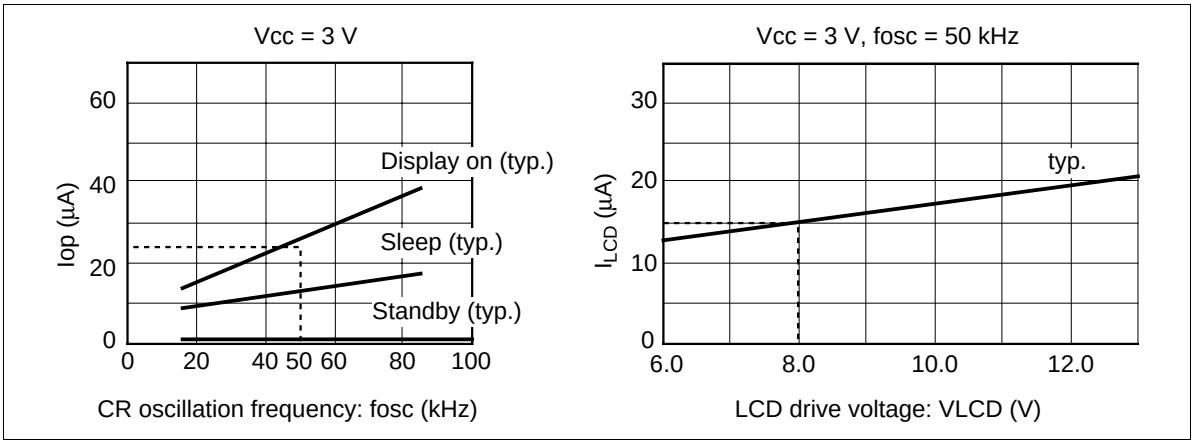


Figure 61 Relationship between the Operation Frequency and Current Consumption

12. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (Vcc, V1, V2, V3, V4, V5) when there is no load.

13. Applies to the external clock input (figure 62).

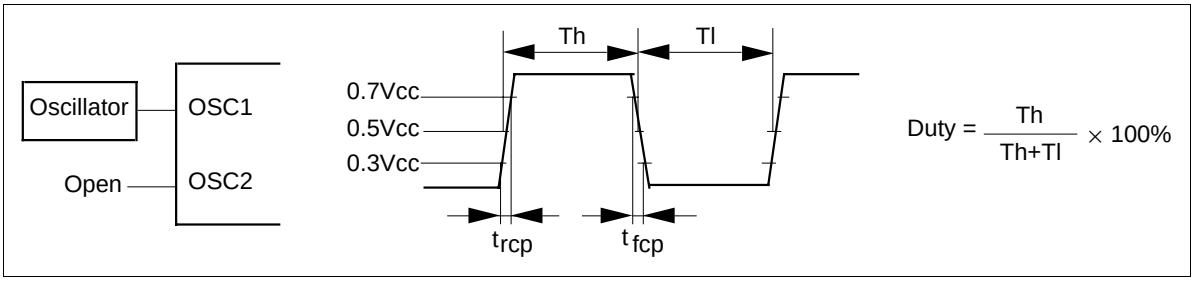
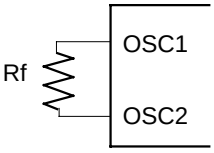


Figure 62 External Clock Supply

14. Applies to the internal oscillator operations using oscillation resistor Rf (figure 63).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

External resistance (Rf)	CR oscillation frequency : fosc				
	Vcc = 1.8 V	Vcc = 2.2 V	Vcc = 3.0 V	Vcc = 4.0 V	Vcc = 5.0 V
180 kΩ	73 kHz	84 kHz	92 kHz	96 kHz	98 kHz
240 kΩ	67 kHz	67 kHz	73 kHz	78 kHz	81 kHz
300 kΩ	50 kHz	56 kHz	60 kHz	62 kHz	63 kHz
330 kΩ	46 kHz	52 kHz	56 kHz	58 kHz	59 kHz
390 kΩ	40 kHz	45 kHz	48 kHz	50 kHz	51 kHz
470 kΩ	34 kHz	37 kHz	40 kHz	42 kHz	43 kHz

Figure 63 Internal Oscillation

15. Booster characteristics test circuits are shown in figure 64.

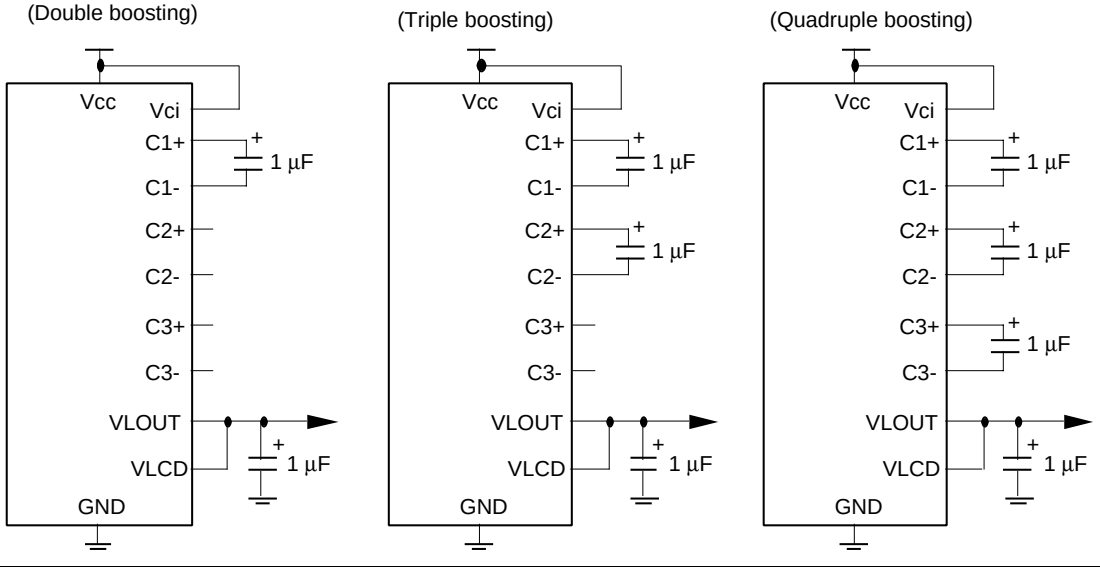
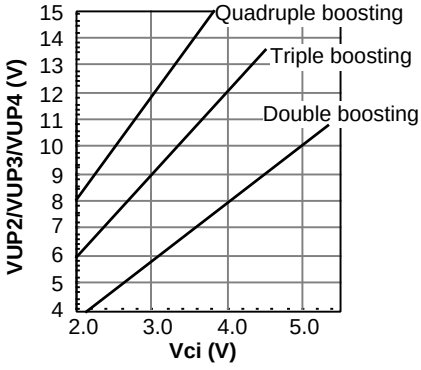


Figure 64 Booster

Referential data

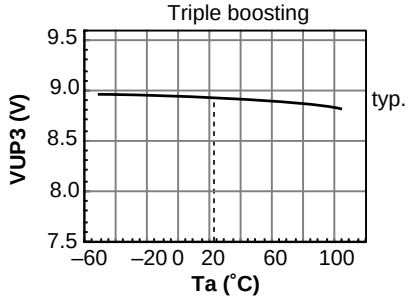
VUP2 = VLCD – GND; VUP3 = VLCD – GND; VUP4 = VLCD – GND

(i) Relation between the obtained voltage and input voltage



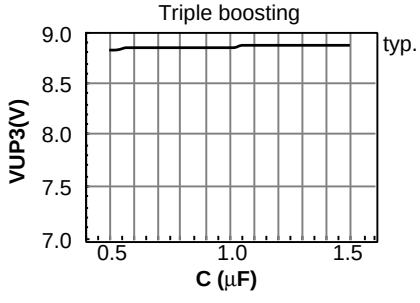
Vci = Vcc, fcp = 50 kHz, Ta = 25˚C

(ii) Relation between the obtained voltage and temperature <T.B.D.>

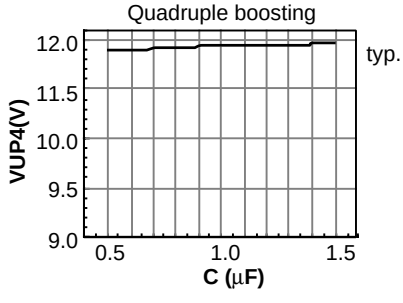


Vci = Vcc = 3.0 V, fosc = 50 kHz, Io = 30 µA

(iii) Relation between the obtained voltage and capacitance

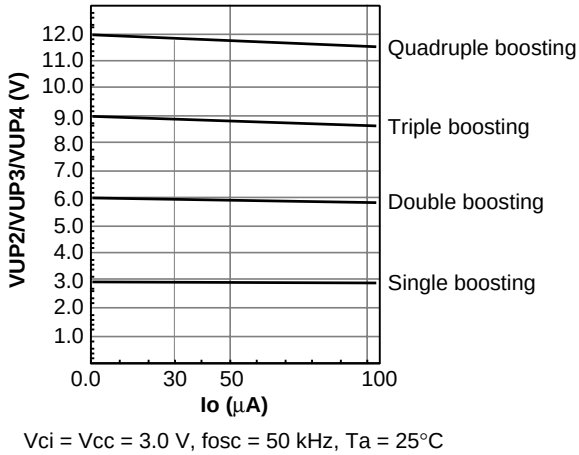


Vci = Vcc = 3.0 V, fosc = 50 kHz, Io = 30 µA



Vci = Vcc = 3.0 V, fosc = 50 kHz, Io = 30 µA

(iv) Relation between the obtained voltage and current <T.B.D.>



Vci = Vcc = 3.0 V, fosc = 50 kHz, Ta = 25°C

Figure 64 Booster (cont)

16. Vcc ≥ Vci must be maintained. The booster must be used in a range between 1.0 V ≤ Vci ≤ 4.0 V.

Load Circuits

AC Characteristics Test Load Circuits

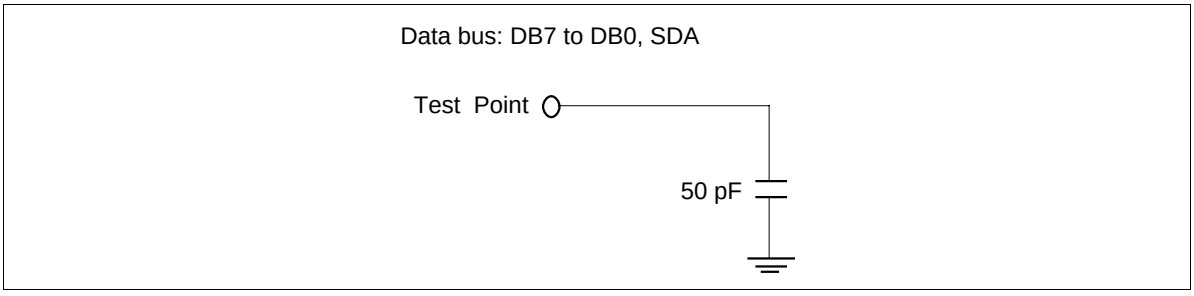


Figure 65 Load Circuit

Timing Characteristics

68-system Bus Operation

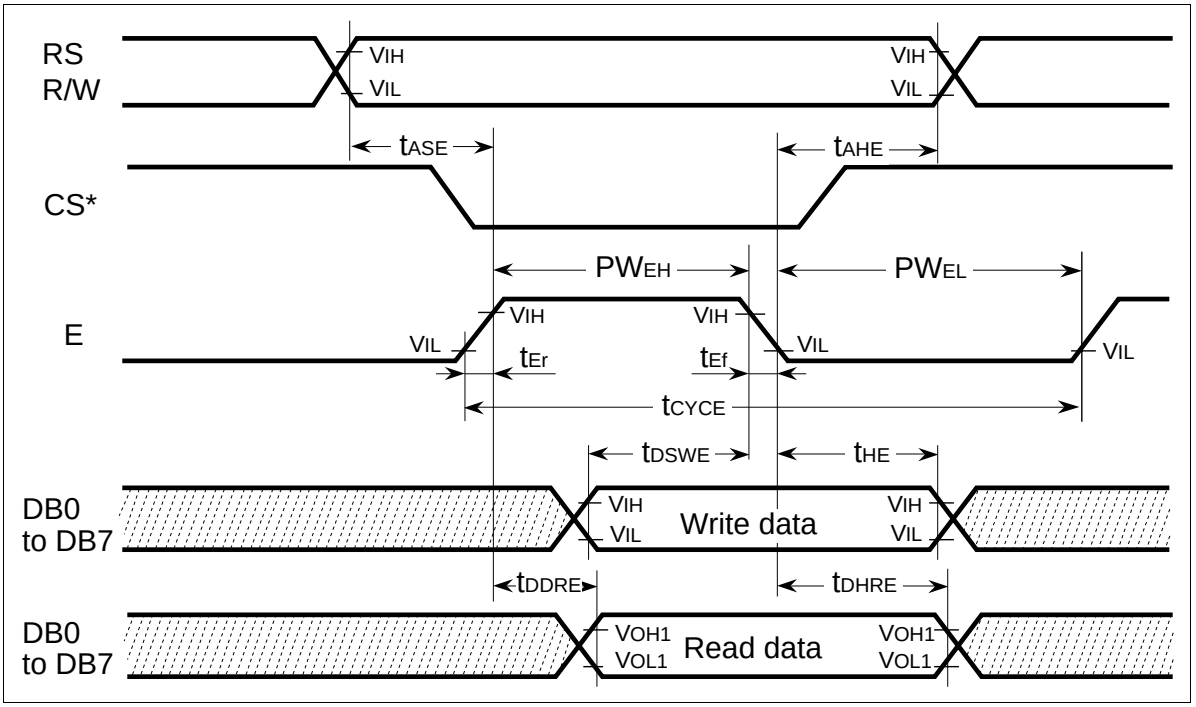


Figure 66 68-system Bus Timing

80-system Bus Operation

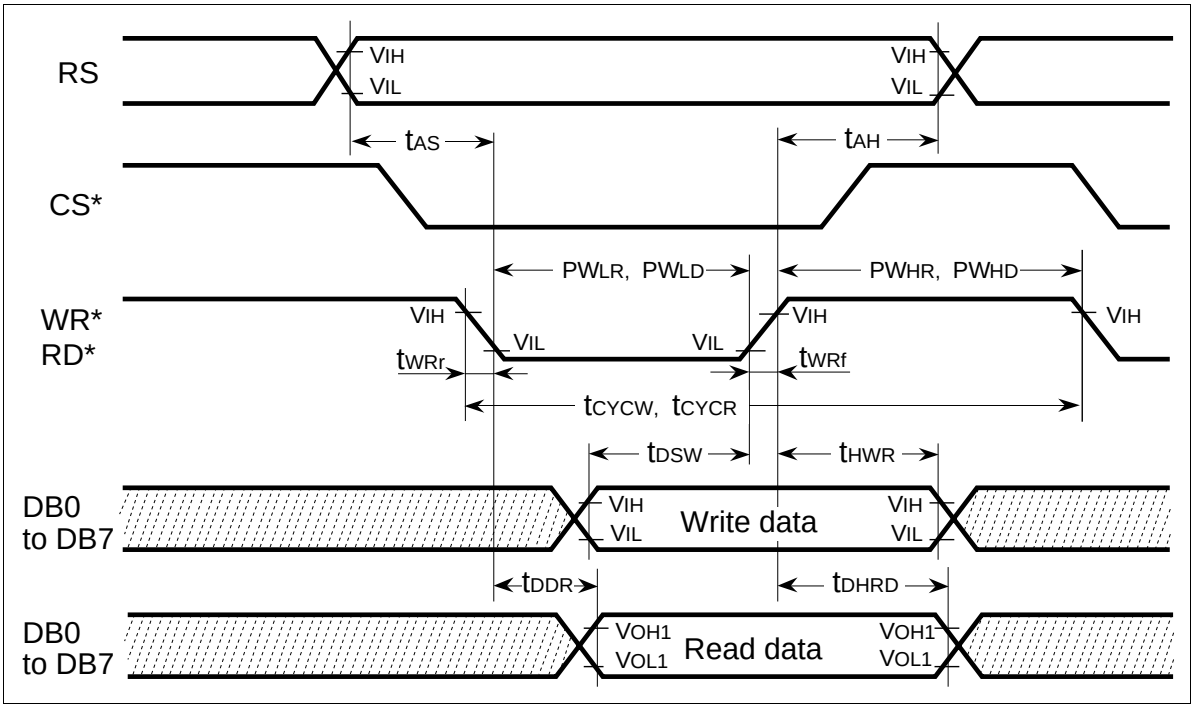


Figure 67 80-system Bus Timing

Clock-synchronized Serial Operation

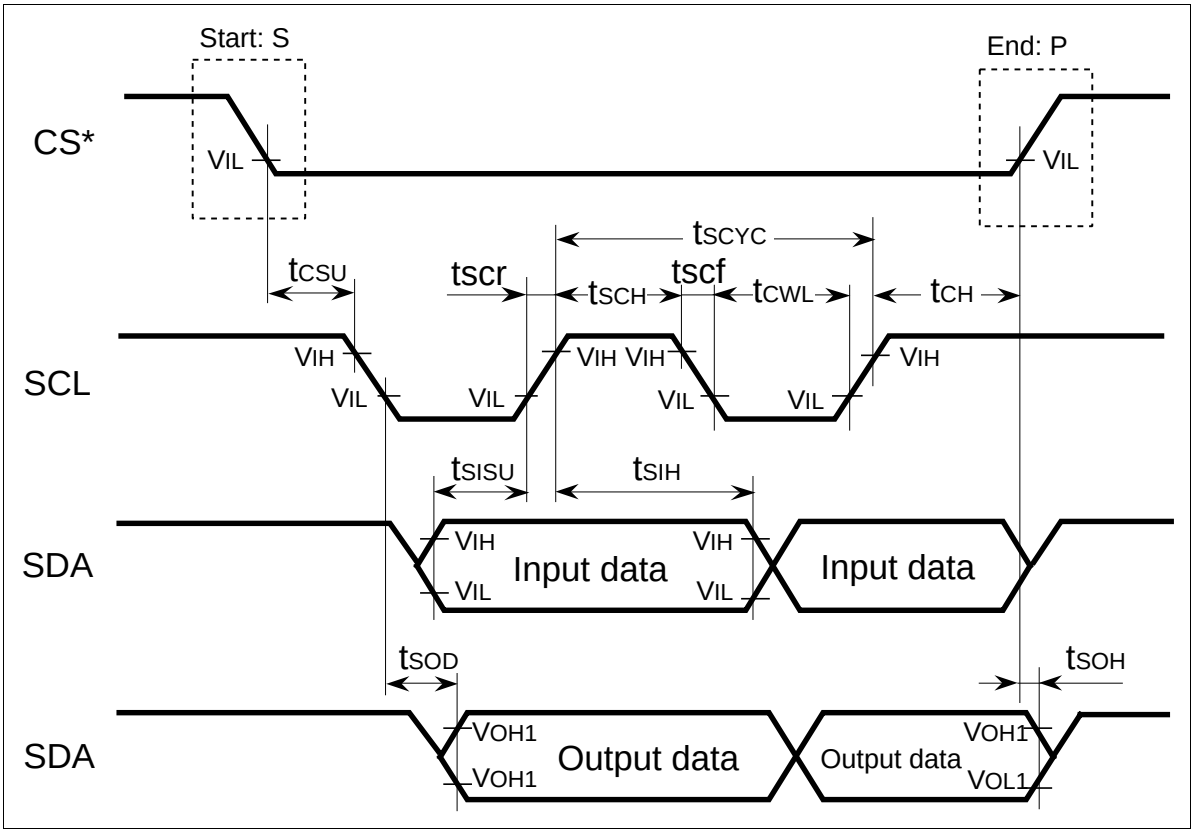


Figure 68 Clock-synchronized Serial Interface Timing

Reset Operation

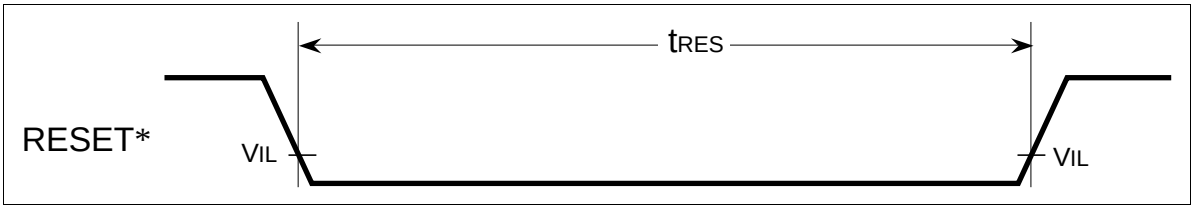


Figure 69 Reset Timing

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