HD66730 (LCD-II/J6)

(Dot-Matrix Liquid Crystal Display Controller/Driver Supporting Japanese Kanji Display)

Preliminary

HITACHI

Description

The HD66730 is a dot-matrix liquid crystal display controller (LCD) and driver LSI that displays Japanese characters consisting of kanji, hiragana and katakana according to the Japanese Industrial Standard (JIS) Level-1 Kanji Set. The HD66730 incorporates the following five functions on a single chip: (1) display control function for the dot matrix LCD, (2) a display RAM to store character codes, (3) ROM fonts to support kanji, (4) liquid crystal driver, and (5) a booster to drive the LCD. A 2-line 6-character kanji display can easily be achieved by receiving character codes (2 bytes/character) from the MPU.

The font ROM includes 2,965 kanji from the JIS Level-1 Kanji Set, 524 JIS non-kanji characters, and 128 half-size alphanumeric characters and symbols. Full-size fonts such as Japanese kanji and half-size of fonts such as alphanumeric characters can be displayed together.

In addition, display control equivalent to full bit mapping can be performed through horizontal and vertical dot-by-dot smooth scroll functions for each display line. To help make systems more compact, a three-line clock synchronous serial transfer method is adopted in addition to an 8-bit bus for interfacing with a microcomputer.

Features

- Dot-matrix liquid crystal display controller/driver supporting the display of kanji according to JIS Level-1 Kanji Set
- Large character generator ROM: 510 kbits
  - — Kanji according to JIS Level-1 Kanji Set (11 × 12 dots): 2,965-character font
  - — JIS non-kanji (11 × 12 dots): 524-character font
  - — Half-size alphanumeric characters and symbols (5 × 12 dots): 128-character font
- Display of 11 × 12 dots for full-size fonts consisting of kanji and kana, 5 × 12 dots for half-size fonts of alphanumeric characters and symbols in the same display
- 2-line 6-character full-size font display with a single chip (1/27 duty)
- Expansion driver interface: maximum 2-line 20-character (or 4-line 10-character) display
- Dot matrix font and 71 marks and icons (96 at extension)
- Various display control functions: horizontal smooth scroll (in dot units), vertical smooth scroll, white black inversion/blinking/white black inversion blinking character display, cursor display, display on/off
- Display data RAM: 40 × 2 bytes (stores codes to support 40 characters in a full-size font)
- Character generator RAM: 8 × 26 bytes (displays 8 characters of a 12 × 13 dot user font)
- 16-byte 96-segment RAM
- Three-line clock synchronous serial bus, 8-bit bus interface
- Built-in double/triple liquid-crystal voltage booster circuit and built-in oscillator (operating frequency can be adjusted through external resistors)
- Operating power supply voltage: 2.7 V to 5.5 V; liquid crystal display voltage: 3.0 V to 13.0 V
- QFP 1420-128 (0.5-mm pitch), bare-chip

Hitachi semiconductor

List 1 Programmable Duty Cycles

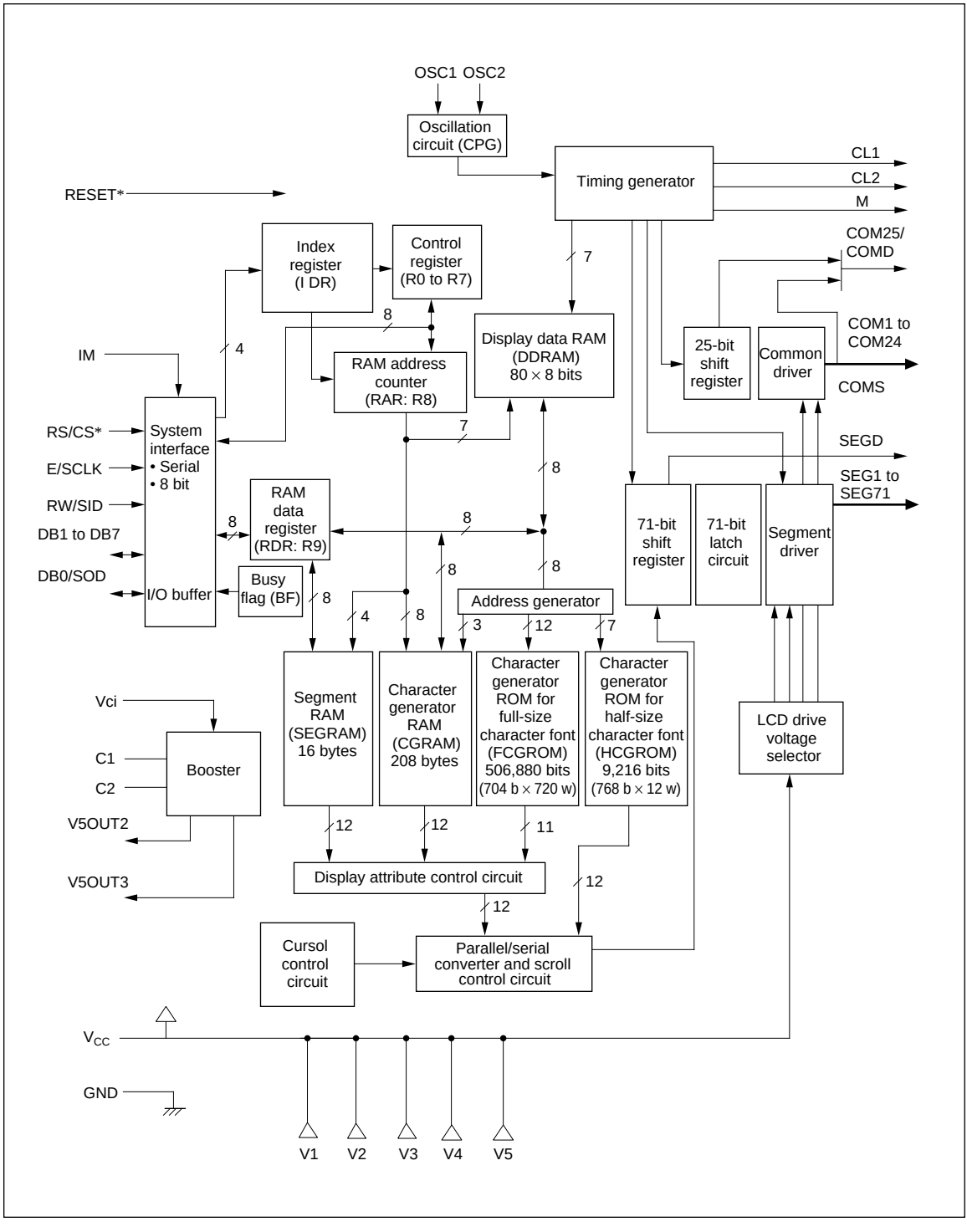
Duty Drive Setting	Number of Display Characters in Full-Size Font (Number of Segments/Marks)			Display Line Setting
	1-Chip Operation	Extension Display	Extension Drivers*	
1/14	1-line 6 characters (71)	1-line 40 characters (96)	10 drivers	1line, 2 lines
1/27	2-line 6 characters (71)	2-line 20 characters (96)	5 drivers	2 lines, 4 lines
1/40	—	3-line 10 characters (96)	3 drivers	4 lines
1/53	—	4-line 10 characters (96)	3 drivers	4 lines

Note: Number of extension driver with 40 outputs (HD44100R)

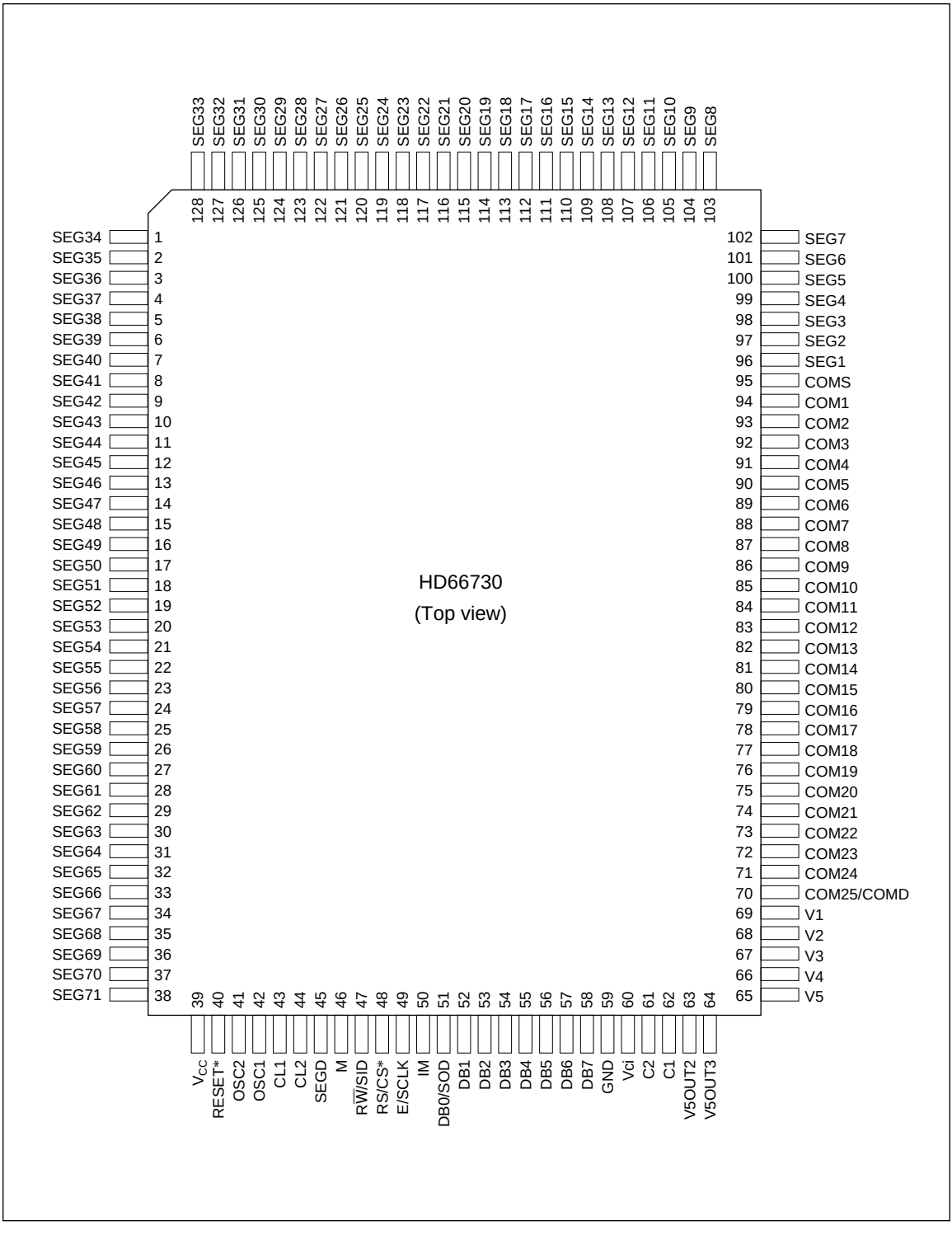
Ordering Information

Type No.	Package	CGROM
HD66730A00FS	FP-128	Japanese Kanji standard
HCD66730A00	Chip	

Block Diagram

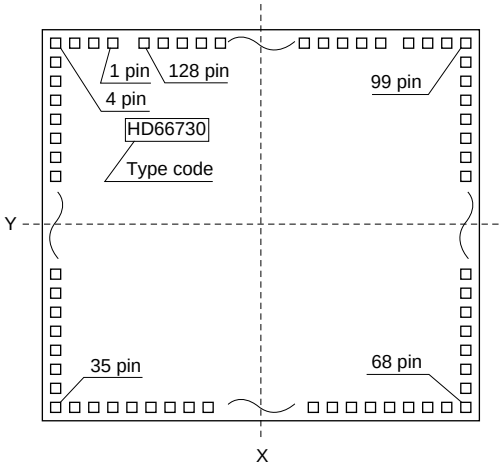


Pin Arrangement



The Location of Bonding Pads

HCD66730



Chip size (X × Y): 7.48 × 6.46 mm^2
Coordinate: Pad center
Origin: Chip center
Pad size (X × Y): 100 × 100 µm^2

(unit: µm)

Pin No.	Function	Coordinate X	Coordinate Y
1	SEG34	–2602	3012
2	SEG35	–2984	3012
3	SEG36	–3263	3012
4	SEG37	–3522	3012
5	SEG38	–3522	2782
6	SEG39	–3522	2582
7	SEG40	–3522	2341
8	SEG41	–3522	2161
9	SEG42	–3522	1981
10	SEG43	–3522	1801
11	SEG44	–3522	1621
12	SEG45	–3522	1440
13	SEG46	–3522	1260
14	SEG47	–3522	1030
15	SEG48	–3522	800
16	SEG49	–3522	620
17	SEG50	–3522	439
18	SEG51	–3522	259
19	SEG52	–3522	79
20	SEG53	–3522	–101
21	SEG54	–3522	–281
22	SEG55	–3522	–462
23	SEG56	–3522	–642
24	SEG57	–3522	–822
25	SEG58	–3522	–1002
26	SEG59	–3522	–1182
27	SEG60	–3522	–1363
28	SEG61	–3522	–1543
29	SEG62	–3522	–1723
30	SEG63	–3522	–1939
31	SEG64	–3522	–2183
32	SEG65	–3522	–2364
33	SEG66	–3522	–2544
34	SEG67	–3522	–2774
35	SEG68	–3522	–2984
36	SEG69	–3160	–2984
37	SEG70	–2860	–2984
38	SEG71	–2660	–2984
39	V_{CC}	–2435	–2984
40	RESET*	–2233	–2984
41	OSC2	–2063	–2984
42	OSC1	–1859	–2984
43	CL1	–1689	–2984
44	CL2	–1519	–2984
45	SEGD	–1349	–2984
46	M	–1179	–2984
47	RW/SID	–975	–2984
48	RS/CS*	–771	–2984
49	E/SCLK	–567	–2984
50	IM	–363	–2984
51	DB0/SOD	–146	–2984
52	DB1	71	–2984
53	DB2	287	–2984
54	DB3	504	–2984
55	DB4	721	–2984
56	DB5	938	–2984
57	DB6	1154	–2984
58	DB7	1371	–2984
59	GND	1533	–2984
60	Vci	1730	–2959
61	C2	1896	–2959
62	C1	2057	–2959
63	V5OUT2	2219	–2959
64	V5OUT3	2478	–2959
65	V5	2782	–2984
66	V4	3016	–2984
67	V3	3253	–2984
68	V2	3522	–2984
69	V1	3522	–2806
70	COM25/D	3522	–2626
71	COM24	3522	–2445
72	COM23	3522	–2265
73	COM22	3522	–2085
74	COM21	3522	–1855
75	COM20	3522	–1625
76	COM19	3522	–1444
77	COM18	3522	–1264
78	COM17	3522	–1084
79	COM16	3522	–854
80	COM15	3522	–624
81	COM14	3522	–443
82	COM13	3522	–263
83	COM12	3522	–83
84	COM11	3522	97
85	COM10	3522	277
86	COM9	3522	458
87	COM8	3522	638
88	COM7	3522	818
89	COM6	3522	998
90	COM5	3522	1178

Pin No.	Function	Coordinate X	Coordinate Y
91	COM4	3522	1409
92	COM3	3522	1639
93	COM2	3522	1819
94	COM1	3522	1999
95	COMS	3522	2179
96	SEG1	3522	2410
97	SEG2	3522	2590
98	SEG3	3522	2819
99	SEG4	3522	3012
100	SEG5	3222	3012
101	SEG6	2942	3012
102	SEG7	2662	3012
103	SEG8	2332	3012
104	SEG9	2152	3012
105	SEG10	1972	3012
106	SEG11	1791	3012
107	SEG12	1611	3012
108	SEG13	1431	3012
109	SEG14	1251	3012
110	SEG15	1071	3012
111	SEG16	890	3012
112	SEG17	710	3012
113	SEG18	530	3012
114	SEG19	350	3012
115	SEG20	170	3012
116	SEG21	–11	3012
117	SEG22	–191	3012
118	SEG23	–371	3012
119	SEG24	–551	3012
120	SEG25	–731	3012
121	SEG26	–912	3012
122	SEG27	–1092	3012
123	SEG28	–1272	3012
124	SEG29	–1452	3012
125	SEG30	–1632	3012
126	SEG31	–1813	3012
127	SEG32	–1993	3012
128	SEG33	–2173	3012

Pin Function

Table 1 Pin Functional Description

Signal	Number of Pins	I/O	Device Interfaced with	Function
RESET*	1	I	—	Acts as a reset input pin. The LSI is initialized during low level. Refer to Reset Function.
IM	1	I	—	Selects interface mode with the MPU; Low: Serial mode High: 8-bit bus mode
RS/CS*	1	I	MPU	Selects registers during bus mode: Low: Index register (write); Status register (read) High: Control register (write); RAM data (read/write) Acts as chip-select during serial mode: Low: Select (access enable) High: Not selected (access disable)
R$\overline{W}$/SID	1	I	MPU	Selects read/write during bus mode; Low: Write High: Read Inputs serial data during serial mode.
E/SCLK	1	I	MPU	Starts data read/write during bus mode; Inputs (Receives) serial clock during serial mode.
DB_1 to DB_7	7	I/O	MPU	Seven high-order bidirectional tristate data bus pins. Used for data transfer between the MPU and the HD66730. DB7 can be used as a busy flag. Open these pins during serial mode since these signals are not used.
DB0/ SOD	1	I/O /O	MPU	The lowest bidirectional data bit (DB0) during bus mode. Outputs (transmits) serial data during serial mode. Open this pin if reading (transmission) is not performed.
SEG_1 to SEG_{71}	71	O	LCD	Display data output signals for the segment extension driver.
COMS	1	O	LCD	Acts as a common output signal for segment display. Used to display icon and marks beside the character display.
COM_1 to COM_{24}	24	O	LCD	Acts as common output signals for character display. COM_{15} toCOM_{24} become non-selective waveforms when the duty ratio is 1/14.
COM_{25}/ COMD	1	O	LCD/ extension driver	Acts as common output signal (COM25) for character display when EXT2 bit is 0. Acts as a common extension pulse signal (COMD) when EXT2 bit is 1. The pin is grounded after RESET input is cleared.

Table 1 Pin Functional Description (cont)

Signal	Number of Pins	I/O	Device Interfaced with	Function
CL1	1	O	Extension driver	Outputs the latch pulse of segment extension driver. Can also be used as a shift clock of common extension driver. Enters tristate when both EXT1 and EXT2 are 0.
CL2	1	O	Extension driver	Outputs shift clock of segment extension driver. Can also be used as a common extension driver latch clock. Enters tristate when both EXT1 and EXT2 are 0.
SEGD	1	O	Extension driver	Outputs data of extension driver. Data after the 72nd dot is output. Enters tristate when EXT1 bit is 0.
M	1	O	Extension driver	Acts as an alternating current signal of extension driver. Enters tristate when both EXT1 and EXT2 bits are 0.
V1 to V5	5	—	Power supply	Power supply for LCD drive V_{CC} – V5 = 15 V (max)
V_{CC}/GND	2	—	Power supply	V_{CC}: +2.7 V to +5.5 V, GND: 0 V
OSC1/ OSC2	2	—	Oscillation resistor/ clock	When crystal oscillation is performed, an external resistor must be connected. When the pin input is an external clock, it must be input to OSC1.
Vci	1	I	—	Inputs voltage to the booster to generate the liquid crystal display drive voltage. Vci is reference voltage and power supply for the booster. Vci: 2.0 V to 5.0 V ≤ V_{CC}.
V5OUT2	1	O	V5 pin/ booster capacitor	Voltage input to the Vci pin is boosted twice and output. When the voltage is boosted three times, a capacitor with the same capacitance as that of C1–C2 should be connected here.
V5OUT3	1	O	V5 pin	Voltage input to the Vci pin is boosted three times and output.
C1/C2	2	—	Booster capacitor	External capacitor should be connected here when using the booster.

Function Description

System Interface

The HD66730 has two system interfaces: a synchronized serial one and an 8-bit bus. Both are selected by the IM pin.

The HD66730 has five types of 8-bit registers: an index register (IDR), status register (STR), various control registers, RAM address register (RAR), and RAM data register (RDR).

The index register (IDR) selects control registers, the RAM address register (RAR) or the RAM data register (RDR) for performing data transfer.

The status register (STR) indicates the internal state of the system. Various control registers store display control data here.

The RAM address register (RAR) stores the address data of display data RAM (DD RAM), character generator RAM (CG RAM), and segment RAM (SEG RAM).

The RAM data register (RDR) temporarily stores data to be written into DD RAM, CG RAM, or SEG RAM. Data written into the RDR from the MPU is automatically written into DD RAM, CG RAM, or SEG RAM by internal operations. The RDR is also used for data storage when reading data from DD RAM, CG RAM, or SEG RAM. Here, when address information is written into the RAR, data is read and then stored into the RDR from DD RAM, CG RAM, or SEG RAM by internal operations.

Data transfer between the MPU is then completed when the MPU reads the RDR. After this read, data in DD RAM, CG RAM, or SEG RAM stored at the next address is sent to the RDR at the next data read from the MPU.

These registers can be selected by the register select signal (RS) and the read/write signal (R/W) in the 8-bit bus interface, and by the RS bit and R/W bit of start-byte data in the synchronized serial interface.

Busy Flag

When the busy flag is 1, the HD66730 is in internal operation mode, and only the status register (STR) can be accessed. The busy flag (BF) is output from bit 7 (DB7). Access of other registers can be performed only after confirming that the busy flag is 0.

RAM Address Counter (RAR)

The RAM address counter (RAR) provides addresses for accessing DD RAM, CG RAM, or SEG RAM. When an initial address value is written into the RAM counter (RAR), the RAR is automatically incremented or decremented by 1. Note that a control register specifies which RAM (DD RAM, CG RAM, SEG RAM) to select.

Table 2 Register Selection

RS	R/$\overline{W}$	Operation
0	0	IDR write
0	1	STR read
1	0	Control register write, RAM address register (RAR) write, and RAM data register (RDR) write
1	1	RAM data register (RDR) read

Display Data RAM (DD RAM)

Display data RAM (DD RAM) stores character codes and display attribute codes for displaying data.

A full-size font is displayed using two bytes, and a half-size font is displayed using one byte. Since the RAM capacity is 80 bytes, 40 full-size characters or 80 half-size characters can be stored.

DD RAM displays only that data stored within the range corresponding to the number of display columns. Data stored outside the range is ignored. Refer to Combined Display of Full-Size and Half-Size characters for details on character codes stored in DD RAM. The relationship between DD RAM addresses and LCD display position depends on the number of display lines (1 line/2 lines/4 lines).

Execution of the display-clear instruction writes H'A0 corresponding to the half-size character for “space” throughout DD RAM.

Note: The HD66730 performs display by reading character codes from the DD RAM according to the number of display columns set by the control register. In particular, reading from the DD RAM begins at the position corresponding to the rightmost character as set by the maximum number of display columns. This means that one byte of a two-byte full-size character code should not be set in a position exceeding the maximum number of display columns. For example, do not write a full-size code (2 bytes) in the 12th and 13th byte when the display is set for six characters.

- 1-line display (NL1/0 = 00)

  80 bytes of consecutive addresses from H'00 to H'4F are allocated for DD RAM addresses. When there are fewer than 40 display characters (at full size), only the number of display characters specified by NC1/0 are displayed starting from H'00 in the DD RAM. For example, 12 bytes of addresses from H'00 to H'0B are used when a 6-character display (NC1/0 = 00) is performed using one HD66730; addresses from H'0C on are ignored. In this case, do not write a full-size code into bytes H'0B and H'0C because a half-size character may be displayed. See figure 1 for a 1-line display.

- 2-line display (NL1/0 = 01)

  The first line in the DD RAM address is displayed for the 40 bytes of addresses from H'00 to H'27, and the second line is displayed for the 40 bytes of addresses from H'40 to H'67. When there are fewer than 20 display characters (at full size), only the number of display characters specified by NC1/0 will be displayed starting from the leftmost address of the DD RAM. For example, 24 bytes of addresses from H'00 to H'0B and H'40 to H'4B are used when a 6-character display (NC1/0 = 00) is performed using one HD66730. Addresses from H'0C and H'4C on are ignored. See figure 2 for a 2-line display.

- 4-line display (NL1/0 = 11)

  The first line in the DD RAM address is displayed from H'00 to H'13, the second line from H'20 to H'33, the third line from H'40 to H'53, and the fourth line from H'60 to H'73. For a 6-character display (NC1/0 = 00) (at full-size), only 12 bytes from the leftmost address of DD RAM are displayed. See figure 3 for a 4-line display.

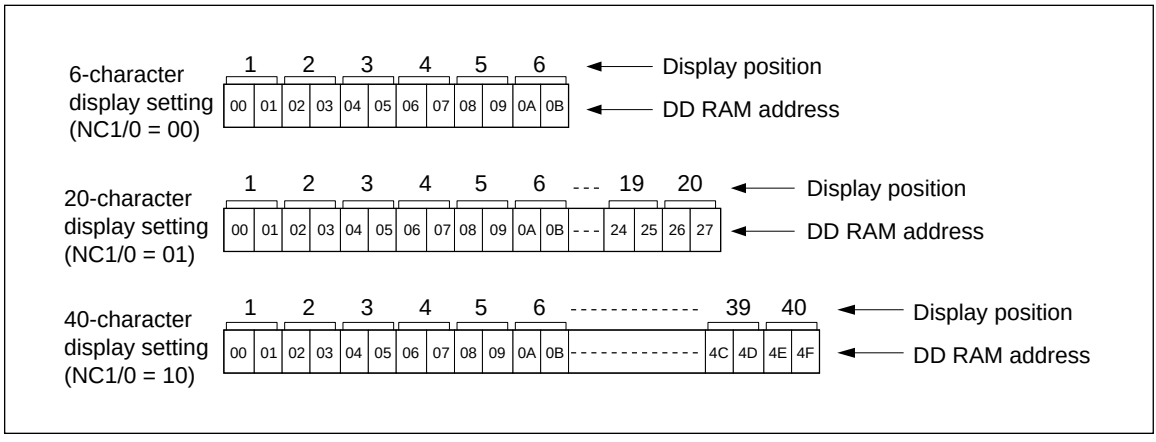


Figure 1 1-Line Display (NL1/0 = 00)

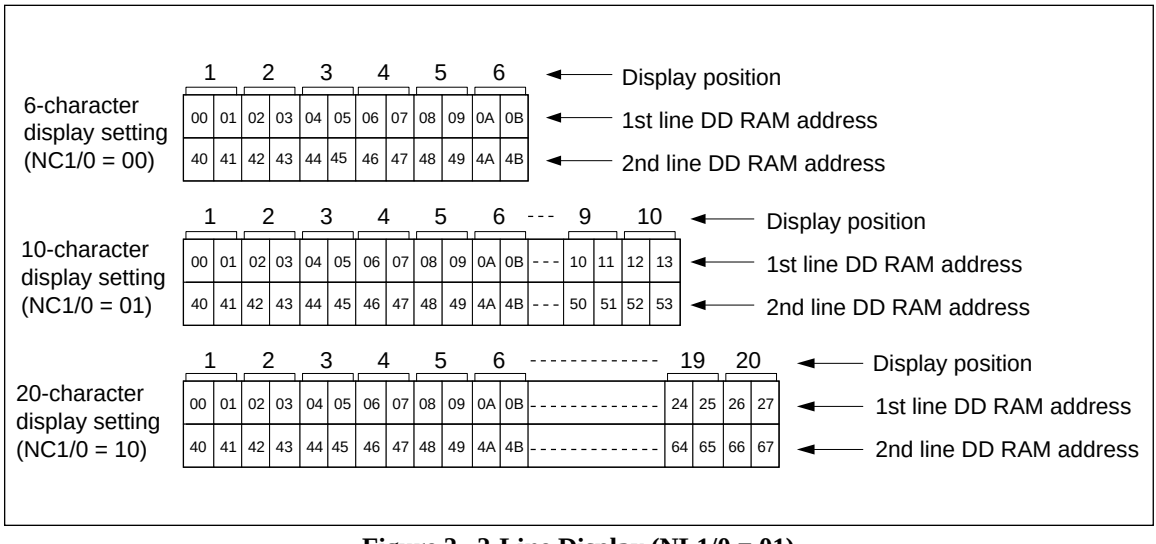


Figure 2 2-Line Display (NL1/0 = 01)

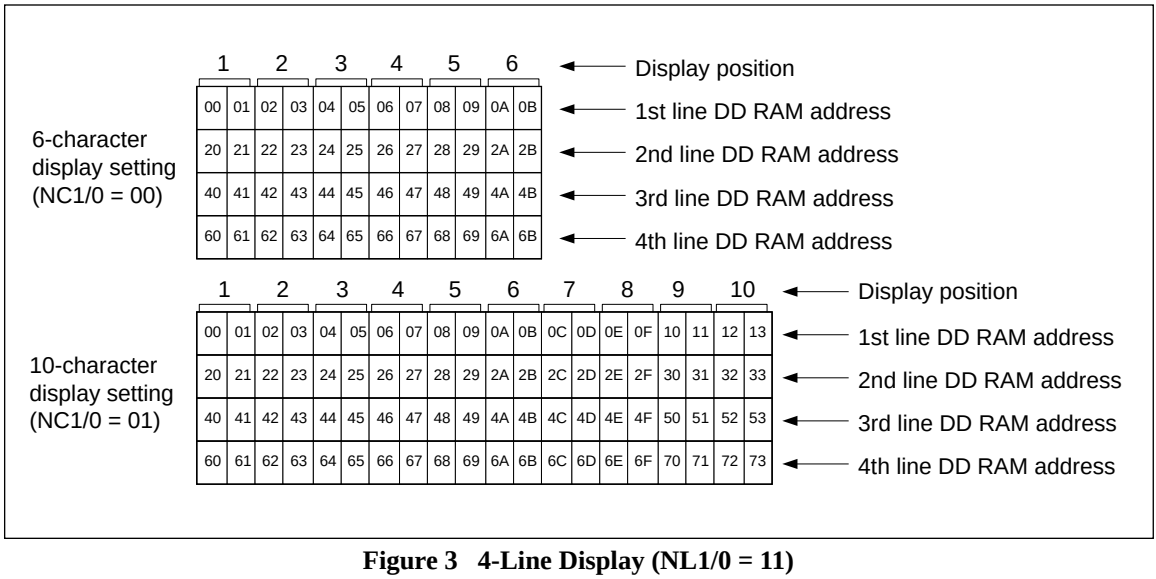


Figure 3 4-Line Display (NL1/0 = 11)

Character Generator ROM for a Full-Size Font (FCG ROM)

The character generator ROM for a full-size font (FCG ROM) generates 3,840 11 × 12 dot full-size character patterns from a 12-bit character code. This includes 2,965 kanji according to the JIS Level-1 Kanji Set and 524 JIS non-kanji. Table 3 shows the relationship between character codes set in DD RAM and full-size font patterns. Refer to Combined Display of Full-Size and Half-Size Characters for the relationship between JIS codes and the character codes to be set in the DD RAM.

Character Generator ROM for a Half-Size Font (HCG ROM)

The character generator ROM for a half-size font (HCG ROM) generates 128 5 × 12 dot character patterns from 7-bit character codes. A half-size font (alphanumeric characters and symbols) can be displayed together with a full-size font. Refer to Combined Display of Full-Size and Half-Size Characters for details.

Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to display arbitrary full-size font patterns. It can display 8 12 × 13 dot fonts.

This RAM can also display double-size characters and figures by combining multiple CG RAM fonts. Specify character codes from H'000 to H'007 in a full size of character code when displaying font patterns stored in the CG RAM.

Segment RAM (SEG RAM)

The segment RAM (SEG RAM) is used to control icons and marks in segment units by the user program. Bits in SEG RAM corresponding to segments to be displayed are directly set by the MPU, regardless of the contents of DD RAM and CG RAM. The SEG RAM is read and displayed when the COMS output pin is selected.

Up to 71 icons can be displayed using a single HD66730. Up to 96 icons can be displayed by expanding the drivers on the segment side. SEG RAM data is stored in eight bits. The lower six bits control the display of each segment, and the upper two bits control segment blinking.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as DD RAM, FCG ROM, HCG ROM, CG RAM, and SEG RAM. RAM read timing for display and internal operation timing for MPU access are generated separately to avoid interference. This prevents undesirable interferences, such as flickering, in areas other than the display area when writing data to DD RAM, for example.

The timing generator generates interface control signals CL1, CL2, M, and COMD-output of extension drivers for a extension configuration.

Display Attribute Controller

The display attribute controller displays white/black inverse, blinking, and white/black inverse blinking for a full size font in FCG ROM according to the attribute code set in the DD RAM. Refer to Display Attribute Designation for details.

Fonts in CG RAM and bit patterns in SEG RAM control display attributes using the upper two bits (bits 7 and 6) in each display-pattern data.

Cursor Control Circuit

The cursor control circuit is used to produce a cursor on a displayed character corresponding to the DD RAM address set in the RAM address counter (RAR). Cursors can be chosen from three types: 12th raster-row cursor that is displayed only on the 12th raster-row of each font; blink cursor that periodically displays the whole font in black and white and black inverted cursor that periodically displays the font in white and black (see

figure 9). Note that when the RAM address counter (RAR) is selecting CG RAM or SEG RAM, a cursor would be generated at that address, however, it does not have any meaning.

Note: One display line consists of 13 raster-rows.

Smooth Scroll Control Circuit

The smooth scroll control circuit is used to perform a smooth-scroll in units of dots.

When the number of characters to be displayed is greater than that possible at one time in the liquid crystal module, this horizontal smooth scroll can be used to display characters in an easy-to-read manner for each line. Refer to Horizontal Smooth Scroll for details for each line.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 26 common signal drivers and 71 segment signal drivers. When the liquid crystal driver duty ratio is set by a program, the necessary common signal drivers output drive waveforms and the remaining common drivers output non-selected waveforms. In addition, drivers can be expanded on the common and segment sides through register settings.

Display pattern data is sent serially through a 71-bit shift register and latched when all needed data has arrived. The latched data then enables the LCD driver to generate drive waveform outputs. This serial data is sent from the display pattern that corresponds to the last address of the DD RAM and is latched when the character pattern of the display data corresponding to the first address enters the internal shift register.

Booster

The booster outputs a voltage that is two or three times higher than the reference voltage input from pin Vci. Since the LCD voltage can be generated from the LSI operation power supply, this circuit can operate with a single power supply. Refer to Power Supply for Liquid Crystal Display Drive for details.

Oscillator

The HD66730 performs R-C oscillation by adding a single external oscillation resistor. The oscillation frequency corresponding to display size and frame frequency can be adjusted by changing the oscillation resistor. Refer to Oscillator for details.

Table 3 Relationship between Full-Size Character Code and Kanji

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0 2		亜	唖	娃	阿	哀	愛	挨	姶	逢	葵	茜	穐	悪	握	渥
0 3	旭	葦	芦	鯵	梓	圧	斡	扱	宛	姐	虻	飴	絢	綾	鮎	或
0 4	粟	袷	安	庵	按	暗	案	闇	鞍	杏	以	伊	位	依	偉	囲
0 5	夷	委	威	尉	惟	意	慰	易	椅	為	畏	異	移	維	緯	胃
0 6	萎	衣	謂	違	遺	医	井	亥	域	育	郁	磯	一	壱	溢	逸
0 7	稲	茨	芋	鰯	允	印	咽	員	因	姻	引	飲	淫	胤	蔭	
0 A		院	陰	隠	韻	吋	右	宇	烏	羽	迂	雨	卯	鵜	窺	丑
0 B	碓	臼	渦	嘘	唄	鬱	蔚	鰻	姥	厩	浦	瓜	閏	噂	云	運
0 C	雲	荏	餌	叡	営	嬰	影	映	曳	栄	永	泳	洩	瑛	盈	穎
0 D	頴	英	衛	詠	鋭	液	疫	益	駅	悦	謁	越	閲	榎	厭	円
0 E	園	堰	奄	宴	延	怨	掩	援	沿	演	炎	焔	煙	燕	猿	縁
0 F	艶	苑	薗	遠	鉛	鴛	塩	於	汚	甥	凹	央	奥	往	応	
1 2		押	旺	横	欧	殴	王	翁	襖	鴬	鴎	黄	岡	沖	荻	億
1 3	屋	憶	臆	桶	牡	乙	俺	卸	恩	温	穏	音	下	化	仮	何
1 4	伽	価	佳	加	可	嘉	夏	嫁	家	寡	科	暇	果	架	歌	河
1 5	火	珂	禍	禾	稼	箇	花	苛	茄	荷	華	菓	蝦	課	嘩	貨
1 6	迦	過	霞	蚊	俄	峨	我	牙	画	臥	芽	蛾	賀	雅	餓	駕
1 7	介	会	解	回	塊	壊	廻	快	怪	悔	恢	懐	戒	拐	改	
1 A		魁	晦	械	海	灰	界	皆	絵	芥	蟹	開	階	貝	凱	劾
1 B	外	咳	害	崖	慨	概	涯	碍	蓋	街	該	鎧	骸	浬	馨	蛙
1 C	垣	柿	蛎	鈎	劃	嚇	各	廓	拡	撹	格	核	殻	獲	確	穫
1 D	覚	角	赫	較	郭	閣	隔	革	学	岳	楽	額	顎	掛	笠	樫
1 E	橿	梶	鰍	潟	割	喝	恰	括	活	渇	滑	葛	褐	轄	且	鰹
1 F	叶	椛	樺	鞄	株	兜	竃	蒲	釜	鎌	噛	鴨	栢	茅	萱	
2 2		粥	刈	苅	瓦	乾	侃	冠	寒	刊	勘	勧	巻	喚	堪	姦
2 3	完	官	寛	干	幹	患	感	慣	憾	換	敢	柑	桓	棺	款	歓
2 4	汗	漢	澗	潅	環	甘	監	看	竿	管	簡	緩	缶	翰	肝	艦
2 5	莞	観	諌	貫	還	鑑	間	閑	関	陥	韓	館	舘	丸	含	岸
2 6	厳	玩	癌	眼	岩	翫	贋	雁	頑	顔	願	企	伎	危	喜	器
2 7	基	奇	嬉	寄	岐	希	幾	忌	揮	机	旗	既	期	棋	棄	
2 A		機	帰	毅	気	汽	畿	祈	季	稀	紀	徽	規	記	貴	起
2 B	軌	輝	飢	騎	鬼	亀	偽	儀	妓	宜	戯	技	擬	欺	犠	疑
2 C	祇	義	蟻	誼	議	掬	菊	鞠	吉	吃	喫	桔	橘	詰	砧	杵
2 D	黍	却	客	脚	虐	逆	丘	久	仇	休	及	吸	宮	弓	急	救
2 E	朽	求	汲	泣	灸	球	究	窮	笈	級	糾	給	旧	牛	去	居
2 F	巨	拒	拠	挙	渠	虚	許	距	鋸	漁	禦	魚	亨	享	京	
3 2		供	侠	僑	兇	競	共	凶	協	匡	卿	叫	喬	境	峡	強
3 3	彊	怯	恐	恭	挟	教	橋	況	狂	狭	矯	胸	脅	興	蕎	郷
3 4	鏡	響	饗	驚	仰	凝	尭	暁	業	局	曲	極	玉	桐	粁	僅
3 5	勤	均	巾	錦	斤	欣	欽	琴	禁	禽	筋	緊	芹	菌	衿	襟
3 6	謹	近	金	吟	銀	九	倶	句	区	狗	玖	矩	苦	躯	駆	駈
3 7	駒	具	愚	虞	喰	空	偶	寓	遇	隅	串	櫛	釧	屑	屈	
3 A		掘	窟	沓	靴	轡	窪	熊	隈	粂	栗	繰	桑	鍬	勲	君
3 B	薫	訓	群	軍	郡	卦	袈	祁	係	傾	刑	兄	啓	圭	珪	型
3 C	契	形	径	恵	慶	慧	憩	掲	携	敬	景	桂	渓	畦	稽	系
3 D	経	継	繋	罫	茎	荊	蛍	計	詣	警	軽	頚	鶏	芸	迎	鯨
3 E	劇	戟	撃	激	隙	桁	傑	欠	決	潔	穴	結	血	訣	月	件
3 F	倹	倦	健	兼	券	剣	喧	圏	堅	嫌	建	憲	懸	拳	捲	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4 2		検	権	牽	犬	献	研	硯	絹	県	肩	見	謙	賢	軒	遣
4 3	鍵	険	顕	験	鹸	元	原	厳	幻	弦	減	源	玄	現	絃	舷
4 4	言	諺	限	乎	個	古	呼	固	姑	孤	己	庫	弧	戸	故	枯
4 5	湖	狐	糊	袴	股	胡	菰	虎	誇	跨	鈷	雇	顧	鼓	五	互
4 6	伍	午	呉	吾	娯	後	御	悟	梧	檎	瑚	碁	語	誤	護	醐
4 7	乞	鯉	交	佼	侯	候	倖	光	公	功	効	勾	厚	口	向	
4 A		后	喉	坑	垢	好	孔	孝	宏	工	巧	巷	幸	広	庚	康
4 B	弘	恒	慌	抗	拘	控	攻	昂	晃	更	杭	校	梗	構	江	洪
4 C	浩	港	溝	甲	皇	硬	稿	糠	紅	紘	絞	綱	耕	考	肯	肱
4 D	腔	膏	航	荒	行	衡	講	貢	購	郊	酵	鉱	砿	鋼	閤	降
4 E	項	香	高	鴻	剛	劫	号	合	壕	拷	濠	豪	轟	麹	克	刻
4 F	告	国	穀	酷	鵠	黒	獄	漉	腰	甑	忽	惚	骨	狛	込	
5 2		此	頃	今	困	坤	墾	婚	恨	懇	昏	昆	根	梱	混	痕
5 3	紺	艮	魂	些	佐	叉	唆	嵯	左	差	査	沙	瑳	砂	詐	鎖
5 4	裟	坐	座	挫	債	催	再	最	哉	塞	妻	宰	彩	才	採	栽
5 5	歳	済	災	采	犀	砕	砦	祭	斎	細	菜	裁	載	際	剤	在
5 6	材	罪	財	冴	坂	阪	堺	榊	肴	咲	崎	埼	碕	鷺	作	削
5 7	詐	搾	昨	朔	柵	窄	策	索	錯	桜	鮭	笹	匙	冊	刷	
5 A		察	拶	撮	擦	札	殺	薩	雑	皐	鯖	捌	錆	鮫	皿	晒
5 B	三	傘	参	山	惨	撒	散	桟	燦	珊	産	算	纂	蚕	讃	賛
5 C	酸	餐	斬	暫	残	仕	仔	伺	使	刺	司	史	嗣	四	士	始
5 D	姉	姿	子	屍	市	師	志	思	指	支	孜	斯	施	旨	枝	止
5 E	死	氏	獅	祉	私	糸	紙	紫	肢	脂	至	視	詞	詩	試	誌
5 F	諮	資	賜	雌	飼	歯	事	似	侍	児	字	寺	慈	持	時	
6 2		次	滋	治	爾	璽	痔	磁	示	而	耳	自	蒔	辞	汐	鹿
6 3	式	識	鴫	竺	軸	宍	雫	七	叱	執	失	嫉	室	悉	湿	漆
6 4	疾	質	実	蔀	篠	偲	柴	芝	屡	蕊	縞	舎	写	射	捨	赦
6 5	斜	煮	社	紗	者	謝	車	遮	蛇	邪	借	勺	尺	杓	灼	爵
6 6	酌	釈	錫	若	寂	弱	惹	主	取	守	手	朱	殊	狩	珠	種
6 7	腫	趣	酒	首	儒	受	呪	寿	授	樹	綬	需	囚	収	周	
6 A		宗	就	州	修	愁	拾	洲	秀	秋	終	繍	習	臭	舟	蒐
6 B	衆	襲	讐	蹴	輯	週	酋	酬	集	醜	什	住	充	十	従	戎
6 C	柔	汁	渋	獣	縦	重	銃	叔	夙	宿	淑	祝	縮	粛	塾	熟
6 D	出	術	述	俊	峻	春	瞬	竣	舜	駿	准	循	旬	楯	殉	淳
6 E	準	潤	盾	純	巡	遵	醇	順	処	初	所	暑	曙	渚	庶	緒
6 F	署	書	薯	藷	諸	助	叙	女	序	徐	恕	鋤	除	傷	償	
7 2		勝	匠	升	召	哨	商	唱	嘗	奨	妾	娼	宵	将	小	少
7 3	尚	庄	床	廠	彰	承	抄	招	掌	捷	昇	昌	昭	晶	松	梢
7 4	樟	樵	沼	消	渉	湘	焼	焦	照	症	省	硝	礁	祥	称	章
7 5	笑	粧	紹	肖	菖	蒋	蕉	衝	裳	訟	証	詔	詳	象	賞	醤
7 6	鉦	鍾	鐘	障	鞘	上	丈	丞	乗	冗	剰	城	場	壌	嬢	常
7 7	情	擾	条	杖	浄	状	畳	穣	蒸	譲	醸	錠	嘱	埴	飾	
7 A		拭	植	殖	燭	織	職	色	触	食	蝕	辱	尻	伸	信	侵
7 B	唇	娠	寝	審	心	慎	振	新	晋	森	榛	浸	深	申	疹	真
7 C	神	秦	紳	臣	芯	薪	親	診	身	辛	進	針	震	人	仁	刃
7 D	塵	壬	尋	甚	尽	腎	訊	迅	陣	靱	笥	諏	須	酢	図	厨
7 E	逗	吹	垂	帥	推	水	炊	睡	粋	翠	衰	遂	酔	錐	錘	随
7 F	瑞	髄	崇	嵩	数	枢	趨	雛	据	杉	椙	菅	頗	雀	裾	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
8 2		澄	摺	寸	世	瀬	畝	是	凄	制	勢	姓	征	性	成	政
8 3	整	星	晴	棲	栖	正	清	牲	生	盛	精	聖	声	製	西	誠
8 4	誓	請	逝	醒	青	静	斉	税	脆	隻	席	惜	戚	斥	昔	析
8 5	石	積	籍	績	脊	責	赤	跡	蹟	碩	切	拙	接	摂	折	設
8 6	窃	節	説	雪	絶	舌	蝉	仙	先	千	占	宣	専	尖	川	戦
8 7	扇	撰	栓	梅	泉	浅	洗	染	潜	煎	煽	旋	穿	箭	線	
8 A		繊	羨	腺	舛	船	薦	詮	賤	践	選	遷	銭	銑	閃	鮮
8 B	前	善	漸	然	全	禅	繕	膳	糎	噌	塑	岨	措	曾	曽	楚
8 C	狙	疏	踈	礎	祖	租	粗	素	組	蘇	訴	阻	遡	鼠	僧	創
8 D	双	叢	倉	喪	壮	奏	爽	宋	層	匝	惣	想	捜	掃	挿	掻
8 E	操	早	曹	巣	槍	槽	漕	燥	争	痩	相	窓	糟	総	綜	聡
8 F	草	荘	葬	蒼	藻	装	走	送	遭	鎗	霜	騒	像	増	憎	
9 2		臓	蔵	贈	造	促	側	則	即	息	捉	束	測	足	速	俗
9 3	属	賊	族	続	卒	袖	其	揃	存	孫	尊	損	村	遜	他	多
9 4	太	汰	詑	唾	堕	妥	惰	打	柁	舵	楕	陀	駄	騨	体	堆
9 5	対	耐	岱	帯	待	怠	態	戴	替	泰	滞	胎	腿	苔	袋	貸
9 6	退	逮	隊	黛	鯛	代	台	大	第	醍	題	鷹	滝	瀧	卓	啄
9 7	宅	托	択	拓	沢	濯	琢	託	鐸	濁	諾	茸	凧	蛸	只	
9 A		叩	但	達	辰	奪	脱	巽	竪	辿	棚	谷	狸	鱈	樽	誰
9 B	丹	単	嘆	坦	担	探	旦	歎	淡	湛	炭	短	端	箪	綻	耽
9 C	胆	蛋	誕	鍛	団	壇	弾	断	暖	檀	段	男	談	値	知	地
9 D	弛	恥	智	池	痴	稚	置	致	蜘	遅	馳	築	畜	竹	筑	蓄
9 E	逐	秩	窒	茶	嫡	着	中	仲	宙	忠	抽	昼	柱	注	虫	衷
9 F	註	酎	鋳	駐	樗	瀦	猪	苧	著	貯	丁	兆	凋	喋	寵	
A 2		帖	帳	庁	弔	張	彫	徴	懲	挑	暢	朝	潮	牒	町	眺
A 3	聴	脹	腸	蝶	調	諜	超	跳	銚	長	頂	鳥	勅	捗	直	朕
A 4	沈	珍	賃	鎮	陳	津	墜	椎	槌	追	鎚	痛	通	塚	栂	掴
A 5	槻	佃	漬	柘	辻	蔦	綴	鍔	椿	潰	坪	壺	嬬	紬	爪	吊
A 6	釣	鶴	亭	低	停	偵	剃	貞	呈	堤	定	帝	底	庭	廷	弟
A 7	悌	抵	挺	提	梯	汀	碇	禎	程	締	艇	訂	諦	蹄	逓	
A A		邸	鄭	釘	鼎	泥	摘	擢	敵	滴	的	笛	適	鏑	溺	哲
A B	徹	撤	轍	迭	鉄	典	填	天	展	店	添	纏	甜	貼	転	顛
A C	点	伝	殿	澱	田	電	兎	吐	堵	塗	妬	屠	徒	斗	杜	渡
A D	登	菟	賭	途	都	鍍	砥	砺	努	度	土	奴	怒	倒	党	冬
A E	凍	刀	唐	塔	塘	套	宕	島	嶋	悼	投	搭	東	桃	梼	棟
A F	盗	淘	湯	涛	灯	燈	当	痘	祷	等	答	筒	糖	統	到	
B 2		董	蕩	藤	討	謄	豆	踏	逃	透	鐙	陶	頭	騰	闘	働
B 3	動	同	堂	導	憧	撞	洞	瞳	童	胴	萄	道	銅	峠	鴇	匿
B 4	得	徳	涜	特	督	禿	篤	毒	独	読	栃	橡	凸	突	椴	届
B 5	鳶	苫	寅	酉	瀞	噸	屯	惇	敦	沌	豚	遁	頓	呑	曇	鈍
B 6	奈	那	内	乍	凪	薙	謎	灘	捺	鍋	楢	馴	縄	畷	南	楠
B 7	軟	難	汝	二	尼	弐	迩	匂	賑	肉	虹	廿	日	乳	入	
B A		如	尿	韮	任	妊	忍	認	濡	禰	祢	寧	葱	猫	熱	年
B B	念	捻	撚	燃	粘	乃	廼	之	埜	嚢	悩	濃	納	能	脳	膿
B C	農	覗	蚤	巴	把	播	覇	杷	波	派	琶	破	婆	罵	芭	馬
B D	俳	廃	拝	排	敗	杯	盃	牌	背	肺	輩	配	倍	培	媒	梅
B E	楳	煤	狽	買	売	賠	陪	這	蝿	秤	矧	萩	伯	剥	博	拍
B F	柏	泊	白	箔	粕	舶	薄	迫	曝	漠	爆	縛	莫	駁	麦	

Table 3 Relationship between Full-Size Character Code and Kanji (cont)

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
C 2		函	箱	硲	箸	肇	筈	櫨	幡	肌	畑	畠	八	鉢	溌	発
C 3	醗	髪	伐	罰	抜	筏	閥	鳩	噺	塙	蛤	隼	伴	判	半	反
C 4	叛	帆	搬	斑	板	氾	汎	版	犯	班	畔	繁	般	藩	販	範
C 5	釆	煩	頒	飯	挽	晩	番	盤	磐	蕃	蛮	匪	卑	否	妃	庇
C 6	彼	悲	扉	批	披	斐	比	泌	疲	皮	碑	秘	緋	罷	肥	被
C 7	誹	費	避	非	飛	樋	簸	備	尾	微	枇	毘	琵	眉	美	
C A		鼻	柊	稗	匹	疋	髭	彦	膝	菱	肘	弼	必	畢	筆	逼
C B	桧	姫	媛	紐	百	謬	俵	彪	標	氷	漂	瓢	票	表	評	豹
C C	廟	描	病	秒	苗	錨	鋲	蒜	蛭	鰭	品	彬	斌	浜	瀕	貧
C D	賓	頻	敏	瓶	不	付	埠	夫	婦	富	冨	布	府	怖	扶	敷
C E	斧	普	浮	父	符	腐	膚	芙	譜	負	賦	赴	阜	附	侮	撫
C F	武	舞	葡	蕪	部	封	楓	風	葺	蕗	伏	副	復	幅	服	
D 2		福	腹	複	覆	淵	弗	払	沸	仏	物	鮒	分	吻	噴	墳
D 3	憤	扮	焚	奮	粉	糞	紛	雰	文	聞	丙	併	兵	塀	幣	平
D 4	弊	柄	並	蔽	閉	陛	米	頁	僻	壁	癖	碧	別	瞥	蔑	箆
D 5	偏	変	片	篇	編	辺	返	遍	便	勉	娩	弁	鞭	保	舗	鋪
D 6	圃	捕	歩	甫	補	輔	穂	募	墓	慕	戊	暮	母	簿	菩	倣
D 7	俸	包	呆	報	奉	宝	峰	峯	崩	庖	抱	捧	放	方	朋	
D A		法	泡	烹	砲	縫	胞	芳	萌	蓬	蜂	褒	訪	豊	邦	鋒
D B	飽	鳳	鵬	乏	亡	傍	剖	坊	妨	帽	忘	忙	房	暴	望	某
D C	棒	冒	紡	肪	膨	謀	貌	貿	鉾	防	吠	頬	北	僕	卜	墨
D D	撲	朴	牧	睦	穆	釦	勃	没	殆	堀	幌	奔	本	翻	凡	盆
D E	摩	磨	魔	麻	埋	妹	昧	枚	毎	哩	槙	幕	膜	枕	鮪	柾
D F	鱒	桝	亦	俣	又	抹	末	沫	迄	侭	繭	麿	万	慢	満	
E 2		漫	蔓	味	未	魅	巳	箕	岬	密	蜜	湊	蓑	稔	脈	妙
E 3	粍	民	眠	務	夢	無	牟	矛	霧	鵡	椋	婿	娘	冥	名	命
E 4	明	盟	迷	銘	鳴	姪	牝	滅	免	棉	綿	緬	面	麺	摸	模
E 5	茂	妄	孟	毛	猛	盲	網	耗	蒙	儲	木	黙	目	杢	勿	餅
E 6	尤	戻	籾	貰	問	悶	紋	門	匁	也	冶	夜	爺	耶	野	弥
E 7	矢	厄	役	約	薬	訳	躍	靖	柳	薮	鑓	愉	愈	油	癒	
E A		諭	輸	唯	佑	優	勇	友	宥	幽	悠	憂	揖	有	柚	湧
E B	涌	猶	猷	由	祐	裕	誘	遊	邑	郵	雄	融	夕	予	余	与
E C	誉	輿	預	傭	幼	妖	容	庸	揚	揺	擁	曜	楊	様	洋	溶
E D	熔	用	窯	羊	耀	葉	蓉	要	謡	踊	遥	陽	養	慾	抑	欲
E E	沃	浴	翌	翼	淀	羅	螺	裸	来	莱	頼	雷	洛	絡	落	酪
E F	乱	卵	嵐	欄	濫	藍	蘭	覧	利	吏	履	李	梨	理	璃	
F 2		痢	裏	裡	里	離	陸	律	率	立	葎	掠	略	劉	流	溜
F 3	琉	留	硫	粒	隆	竜	龍	侶	慮	旅	虜	了	亮	僚	両	凌
F 4	寮	料	梁	涼	猟	療	瞭	稜	糧	良	諒	遼	量	陵	領	力
F 5	緑	倫	厘	林	淋	燐	琳	臨	輪	隣	鱗	麟	瑠	塁	涙	累
F 6	類	令	伶	例	冷	励	嶺	怜	玲	礼	苓	鈴	隷	零	霊	麗
F 7	齢	暦	歴	列	劣	烈	裂	廉	恋	憐	漣	煉	簾	練	聯	
F A		蓮	連	錬	呂	魯	櫓	炉	賂	路	露	労	婁	廊	弄	朗
F B	楼	榔	浪	漏	牢	狼	篭	老	聾	蝋	郎	六	麓	禄	肋	録
F C	論	倭	和	話	歪	賄	脇	惑	枠	鷲	亙	亘	鰐	詫	藁	蕨
F D	椀	湾	碗	腕												
F E																
F F																

Table 4 Relationship between Full-Size Character Code and Non-Kanji

Upper/Lower	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
4 8			、	。	,	.	・	:	;	?	!	゛	゜	´	`	¨
4 9	^	―	_	ヽ	ヾ	ゝ	ゞ	〃	仝	々	〆	〇	―	―	-	／
8 8	＼	～	∥	｜	…	‥	‘	’	“	”	(	)	〔	〕	[	]
8 9	｜	｜	〈	〉	《	》	「	」	『	』	【	】	＋	－	±	×
C 8	÷	＝	≠	＜	＞	≦	≧	∞	∴	♂	♀	°	′	″	℃	¥
C 9	$	¢	£	%	#	&	*	@	§	☆	★	○	●	◎	◇	
5 0		◆	□	■	△	▲	▽	▼	※	〒	→	←	↑	↓	＝	
5 1											∈	∋	⊆	⊇	⊂	⊃
9 0	∪	∩									∧	∨	¬	⇒	⇔	∀
9 1	∃												∠	⊥	⌒	∂
D 0	∇	≡	≒	≪	≫	√	∽	∝	∵	∫	∬					
D 1			Å	‰	♯	♭	♪	†	‡	¶					◯	
5 8																
5 9	0	1	2	3	4	5	6	7	8	9						
9 8		A	B	C	D	E	F	G	H	I	J	K	L	M	N	O
9 9	P	Q	R	S	T	U	V	W	X	Y	Z					
D 8		a	b	c	d	e	f	g	h	i	j	k	l	m	n	o
D 9	p	q	r	s	t	u	v	w	x	y	z					
6 0		ぁ	あ	ぃ	い	ぅ	う	ぇ	え	ぉ	お	か	が	き	ぎ	く
6 1	ぐ	け	げ	こ	ご	さ	ざ	し	じ	す	ず	せ	ぜ	そ	ぞ	た
A 0	だ	ち	ぢ	っ	つ	づ	て	で	と	ど	な	に	ぬ	ね	の	は
A 1	ば	ぱ	ひ	び	ぴ	ふ	ぶ	ぷ	へ	べ	ぺ	ほ	ぼ	ぽ	ま	み
E 0	む	め	も	ゃ	や	ゅ	ゆ	ょ	よ	ら	り	る	れ	ろ	ゎ	わ
E 1	ゐ	ゑ	を	ん												
6 8		ァ	ア	ィ	イ	ゥ	ウ	ェ	エ	ォ	オ	カ	ガ	キ	ギ	ク
6 9	グ	ケ	ゲ	コ	ゴ	サ	ザ	シ	ジ	ス	ズ	セ	ゼ	ソ	ゾ	タ
A 8	ダ	チ	ヂ	ッ	ツ	ヅ	テ	デ	ト	ド	ナ	ニ	ヌ	ネ	ノ	ハ
A 9	バ	パ	ヒ	ビ	ピ	フ	ブ	プ	ヘ	ベ	ペ	ホ	ボ	ポ	マ	ミ
E 8	ム	メ	モ	ャ	ヤ	ュ	ユ	ョ	ヨ	ラ	リ	ル	レ	ロ	ヮ	ワ
E 9	ヰ	ヱ	ヲ	ン	ヴ	ヵ	ヶ									
7 0		A	B	Γ	Δ	E	Z	H	Θ	I	K	Λ	M	N	Ξ	O
7 1	Π	P	Σ	T	ϒ	Φ	X	Ψ	Ω							
B 0		α	β	γ	δ	ε	ζ	η	θ	ι	κ	λ	μ	ν	ξ	ο
B 1	π	ρ	σ	τ	υ	φ	χ	ψ	ω							
F 0																
F 1																
7 8		А	Б	В	Г	Д	Е	Ё	Ж	З	И	Й	К	Л	М	Н
7 9	О	П	Р	С	Т	У	Ф	Х	Ц	Ч	Ш	Щ	Ъ	Ы	Ь	Э
B 8	Ю	Я														
B 9		а	б	в	г	д	е	ё	ж	з	и	й	к	л	м	н
F 8	о	п	р	с	т	у	ф	х	ц	ч	ш	щ	ъ	ы	ь	э
F 9	ю	я														
4 0		─	│	┌	┐	┘	└	├	┬	┤	┴	┼	━	┃	┏	┓
4 1	┛	┗	┣	┳	┫	┻	╋	┠	┯	┨	┷	┿	┝	┰	┥	┸
8 0	╂															
8 1																
C 0																
C 1																

Table 5 Relationship between Half-Size Character Code and Character Pattern (ROM Code: A00)

Lower (3 bits) \ Upper (4 bits)	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx 000					(Space)											
xxxx 001																
xxxx 010																
xxxx 011																
xxxx 100																
xxxx 101																
xxxx 110																
xxxx 111																

Relationship between Character Codes (DD RAM), CG RAM Addresses, and Display Characters

Full size character codes H'000 to H'007 can be used to access 8 character patterns in the CG RAM. Since each character pattern can be displayed up to 12 × 13 dots, CG RAM patterns can be displayed immediately next to each other (to the right, left, top, or bottom) without any character spaces between them. Table 6 shows the correspondence between CG RAM addresses and full-size character codes for access of the CG RAM by the MPU.

Table 6 Relationship between Character Codes (DD RAM), CG RAM Addresses, and Display Characters

Character Code				CGRAM Address							CGRAM Data														
											$A_0 = 0$								$A_0 = 1$						
C_{11} ---------- C_3	C_2	C_1	C_0	A_7	A_6	A_5	A_4	A_3	A_2	A_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0 0 0 0 0 0 0 0 0 0	0	0	0	0	0	0	0	0	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							0	0	0	1	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	0	1	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	0	1	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	0	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	0	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							0	1	1	0	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	1	1	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	0	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	0	1	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	1	0	A	A	0	1	0	0	0	0	A	A	0	0	0	1	0	0
							1	0	1	1	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
0 0 0 0 0 0 0 0 0 1	0	0	1	0	0	1	0	0	0	0	A	A	0	0	0	0	0	1	A	A	0	0	0	0	0	0
							0	0	0	1	A	A	0	0	0	0	0	0	A	A	1	0	0	0	0	0
							0	0	1	0	A	A	0	1	1	1	1	1	A	A	1	1	1	1	0	0
							0	0	1	1	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							0	1	0	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	0	1	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	1	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	1	1	1	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	0	0	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	0	1	A	A	0	0	0	1	0	0	A	A	0	1	0	0	0	0
							1	0	1	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
							1	0	1	1	A	A	1	1	1	1	1	1	A	A	1	1	1	1	1	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0
0 0 0 0 0 0 0 0 0 0	1	1	1	1	1	1	0	0	0	0	A	A	0	0	1	0	0	0	A	A	0	0	1	0	0	0
							0	0	0	1	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							0	0	1	0	A	A	0	1	0	0	1	1	A	A	0	0	0	1	0	0
							0	0	1	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	0	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	0	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	1	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							0	1	1	1	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							1	0	0	0	A	A	1	0	0	0	0	1	A	A	0	0	0	0	1	0
							1	0	0	1	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							1	0	1	0	A	A	0	1	0	0	0	1	A	A	0	0	0	1	0	0
							1	0	1	1	A	A	0	0	1	0	1	1	A	A	1	0	1	0	0	0
							1	1	0	0	A	A	0	0	0	0	0	0	A	A	0	0	0	0	0	0

Character pattern (1)

Character pattern (2)

Character pattern (8)

Notes:
1. CG RAM is selected when the upper 9 bits (C3 to C11) of the full size character codes are 0. In this case, the lower 3 bits (C0 to C2) of the character code correspond to bits 5 to 7 (A5 to A7) (3 bits: 8 types) in the CG RAM address.
2. CG RAM address bits 1 to 4 (A1 to A4) designate the character pattern line position. The 12th line is the cursor position and its display is formed by a logical OR with the cursor.
3. CG RAM address 0 (A0) corresponds to the left-half and right-half of a full-size character pattern.
4. The character data is stored with the rightmost character element in bit 0 (LSB), as shown in the table above. Pattern produced by bits 0 to 5 is displayed and 13 raster-rows are displayed together. Thus, an arbitrary character pattern consisting of 12×13 dots can be displayed.
5. A set bit in the CG RAM data corresponds to display selection, and 0 to non-selection.
6. The upper two bits (AA) of CG RAM data indicate the display attribute for the lower 6-bit pattern. In this case, display attributes specified for the DD RAM during full-size character display is disabled. When these upper two bits are 00, the CG RAM pattern is simply displayed as set; when 01, the pattern reverses (black/white), when 10, the pattern blinks; and when 11, the pattern reverses and blinks.

Relationship between SEG RAM Addresses and Display Patterns

SEG RAM data is displayed when the select level of the COMS pin is output. Since SEG RAM data does not depend on character code data in DD RAM, and does not undergo horizontal smooth scroll, it can be used to display icon and marks. The following shows the relationship between SEG RAM addresses and segment output pins.

Table 7 Relationship between SEG RAM Addresses and Display Patterns

SEGRAM Address				SEGRAM Data							
A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	0	0	0	B1	B0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6
0	0	0	1	B1	B0	SEG7	SEG8	SEG9	SEG10	SEG11	SEG12
0	0	1	0	B1	B0	SEG13	SEG14	SEG15	SEG16	SEG17	SEG18
0	0	1	1	B1	B0	SEG19	SEG20	SEG21	SEG22	SEG23	SEG24
0	1	0	0	B1	B0	SEG25	SEG26	SEG27	SEG28	SEG29	SEG30
0	1	0	1	B1	B0	SEG31	SEG32	SEG33	SEG34	SEG35	SEG36
0	1	1	0	B1	B0	SEG37	SEG38	SEG39	SEG40	SEG41	SEG42
0	1	1	1	B1	B0	SEG43	SEG44	SEG45	SEG46	SEG47	SEG48
1	0	0	0	B1	B0	SEG49	SEG50	SEG51	SEG52	SEG53	SEG54
1	0	0	1	B1	B0	SEG55	SEG56	SEG57	SEG58	SEG59	SEG60
1	0	1	0	B1	B0	SEG61	SEG62	SEG63	SEG64	SEG65	SEG66
1	0	1	1	B1	B0	SEG67	SEG68	SEG69	SEG70	SEG71	SEG72
1	1	0	0	B1	B0	SEG73	SEG74	SEG75	SEG76	SEG77	SEG78
1	1	0	1	B1	B0	SEG79	SEG80	SEG81	SEG82	SEG83	SEG84
1	1	1	0	B1	B0	SEG85	SEG86	SEG87	SEG88	SEG89	SEG90
1	1	1	1	B1	B0	SEG91	SEG92	SEG93	SEG94	SEG95	SEG96

Blinking control — Pattern on/off

Notes:
1. SEG1 to SEG71 are pin numbers of the segment output driver of the HD66730. Pin SEG1 is positioned on the left edge of the display. Segments from SEG72 on are displayed by extension drivers. After SEG 96, display is performed from SEG1 again.
2. The lower six bits (D0 to D5) indicate display on/off for of each segment. A bit setting of 1 selects display while 0 selects no display.
3. Pattern blinking of the lower six bits is controlled by the upper two bits (D6 and D7) of SEG RAM data. When the upper two bits (B0 and B1) are 10, segments whose corresponding bits in the lower 6 bits are set to 1 will blink on the display. When the upper two bits (B0 and B1) are 01, only the bit-5 pattern can blink. Do not attempt to set the upper two bits (B0 and B1) to 11 (setting is prohibited).

Register Functions

Outline

Data can be written from the MPU to the internal control registers and internal RAM of the HD66730 via an 8-bit bus interface or a serial interface. There are five types of internal control registers, as follows (details are described later):

- Index register: Selects and designates which control register the MPU is to access
- Status register: Indicates the internal state
- Control registers: Designates display control
- RAM address register: Sets an address for accessing the various RAMs
- RAM data register: Receives and transmits data to and from the various RAMs

Table 17 shows the instruction list and the number of execution cycles of each instruction after performing register setting. Instructions that perform data transfer with the RAM data register tend to be used the most. However, auto-incrementation by 1 (or auto decrementation by 1) of internal HD66730 RAM addresses after each data write can lighten the program load on the MPU. Note that when an instruction is being executed (internal operations are being performed), only the busy flag in the status register can be read.

Since the busy flag is 1 during execution, the MPU should check this value before accessing a register. When accessing a register without checking the busy flag, an interval longer than the instruction execution time is needed before the next access. Refer to table 17 Instruction Registers, for instruction execution times.

When rewriting DD RAM, character display will momentarily breakdown if the data (character codes) that is being rewritten is also being read by the system for display. For this reason, check the display read line position (NF) and the display read raster-row position (LF) in the status register (SR), and rewrite a DD RAM line that is not being read and displayed.

Functional Description

Index Register (IR)

The index register (figure 4) designates control registers (R0 to R7), RAM address register (RAR: R8), and RAM data register (RDR: R9). The register number must be set between addresses 0000 to 1001 in binary digits. Note that if address 1111 is set, the test register will be selected. Addresses 1010 to 1110 are ignored.

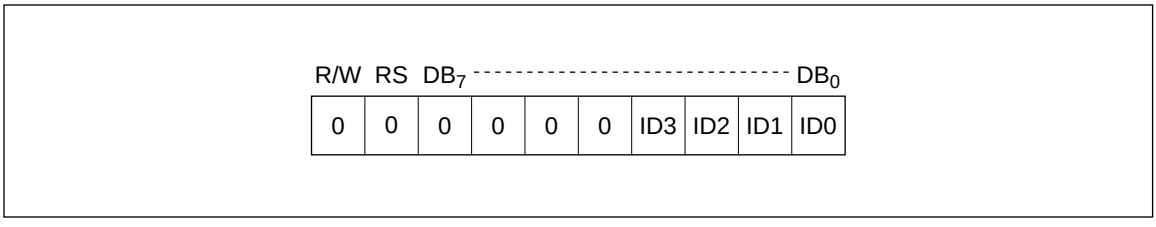


Figure 4 Index Register

Status Register (ST)

The status register (figure 5) includes the busy flag (BF), display line bits (NF1/0), and display raster-row bits (LF0 to LF3). If BF is 1, an instruction is being executed, and another instruction will not be accepted during this time. Any attempt to write data to a register at this time is ignored.

Rasters-rows are driven one at a time according to specific timing to perform liquid crystal display. Bits NF1 and NF0 indicate display lines, and bits LF3 to LF0 indicate the raster-row in a line. If character display degenerates when rewriting DD RAM, rewrite only those display lines that are not currently being read out by the system for display. During segment display, the next state of the last raster-row in the character display is read out.

Table 8 Display State According to NF1 and NF0

NF1	NF0	Display State
00	0	Displaying the first line
0	1	Displaying the second line
1	0	Displaying the third line
1	1	Displaying the fourth line

Table 9 Display State According to LF3 to LF0

LF3	LF2	LF1	LF0	Display State
0	0	0	0	Displaying the first raster-row
0	0	0	1	Displaying the second raster-row
0	0	1	0	Displaying the third raster-row
0	0	1	1	Displaying the fourth raster-row
•				•
•				•
•				•
1	1	0	0	Displaying the 13th raster-row

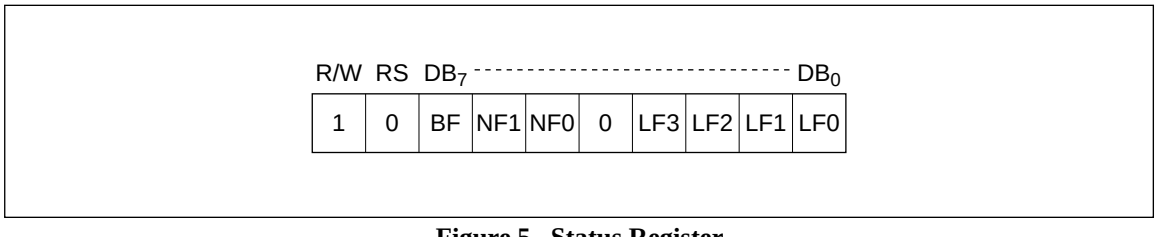


Figure 5 Status Register

Entry Mode Register (R0)

The entry mode register (figure 6) includes bits I/D, RM1, and RM0.

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read out from the DD RAM. When the DD RAM address is incremented by 1, the cursor or blinking will also shift to the right. This applies to both CG RAM and SEG RAM.

RM1/0: Selects DD RAM, CG RAM, or SEG RAM for access (table 10).

Table 10 RAM Selection by RM1 and RM0

RM1	RM0	Selected RAM
0	0/1	Display data RAM (DD RAM)
1	0	Character generator RAM (CG RAM)
1	1	Segment RAM (SEG RAM)

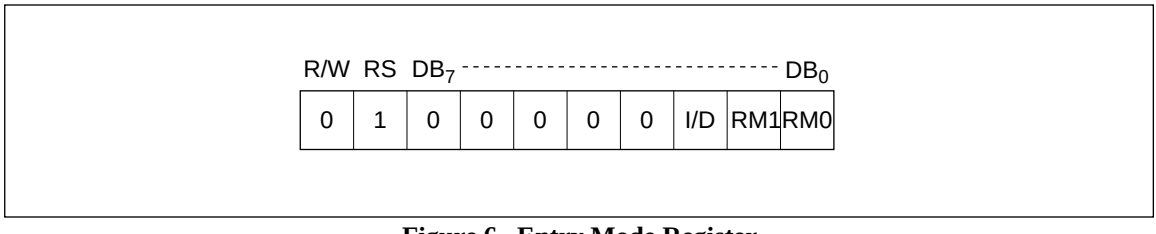


Figure 6 Entry Mode Register

Function Set Register (R1)

The function set register (figure 7) includes bits BST, EXT2, EXT1, DT1, DT0, and DCL.

BST: When BST is 1, the booster starts to operate. When the LCD voltage is external, set BST to 0 to stop operation of the internal booster. In addition, the consumption current can be suppressed by stopping the booster when entering standby mode without display.

EXT2/1: Extends the common driver and segment driver. Set EXT2 to 1 to extend the driver to the common side if the duty ratio is 1/40 or 1/53. Extend the driver to the segment side by setting EXT1 to 1 when displaying 7 or more digits (of full size) in the horizontal direction. DD RAM capacity is 80 bytes.

DT1/0: Selects the duty ratio of the LCD (table 11). Although this bit can be set separately from the display line designation (NL1/0), the duty ratio must be selected so that it will be smaller than the number of display lines.

DCL: When DCL is 1, the display is cleared by writing the code for half-size space (H'A0) into all DD RAM addresses. Then H'00 is written into the RAM address counter (RAR) and the DD RAM is selected. The character code for character code H'A0 must be a blank pattern when rewriting HCG ROM used for half-size characters.

Cursor Control Register (R2)

The cursor control register includes bits CHM, C, CM1, and CM0.

CHM: When CHM is set to 1, DD RAM is selected, the RAM address counter (RAR) is set to 0, and the cursor home instruction is executed. The contents of DD RAM do not change. The cursor or blinking moves to the left edge of the display (the left edge of the first line if two lines are displayed).

C: When C = 1, cursor display is turned on. The cursor is displayed at the position corresponding to the count value of the RAM address counter (RAR). To set data in the RAR, set the index register (IDR) to 1000 to select it, and modify the data in the RAR. Note that the RAM address counter (RAR) automatically increments (decrements) when the RAM is accessed, and the cursor will move accordingly.

CM1/0: Selects cursor display mode (table 12 and figure 9). The blinking frequency (cycle) of the blink cursor and the white/black inverted cursor has 64 frames.

Table 11 Duty Drive Ratio

DT1	DT0	Duty Drive Ratio
0	0	1/14 duty drive
0	1	1/27 duty drive
1	0	1/40 duty drive
1	1	1/53 duty drive

Table 12 Cursor Mode Selection

CM1	CM0	Selected Cursor Mode
0	0	12th raster-row cursor
0	1	Blink cursor
1	0/1	White/black inverted cursor

R/W	RS	DB_7						DB_0
0	1	0	BST	EXT2	EXT1	DT1	DT0	0	DCL

Figure 7 Function Set Register

R/W	RS	DB_7						DB_0
0	1	0	0	0	0	CHM	C	CM1	CM0

Figure 8 Cursor Control Register

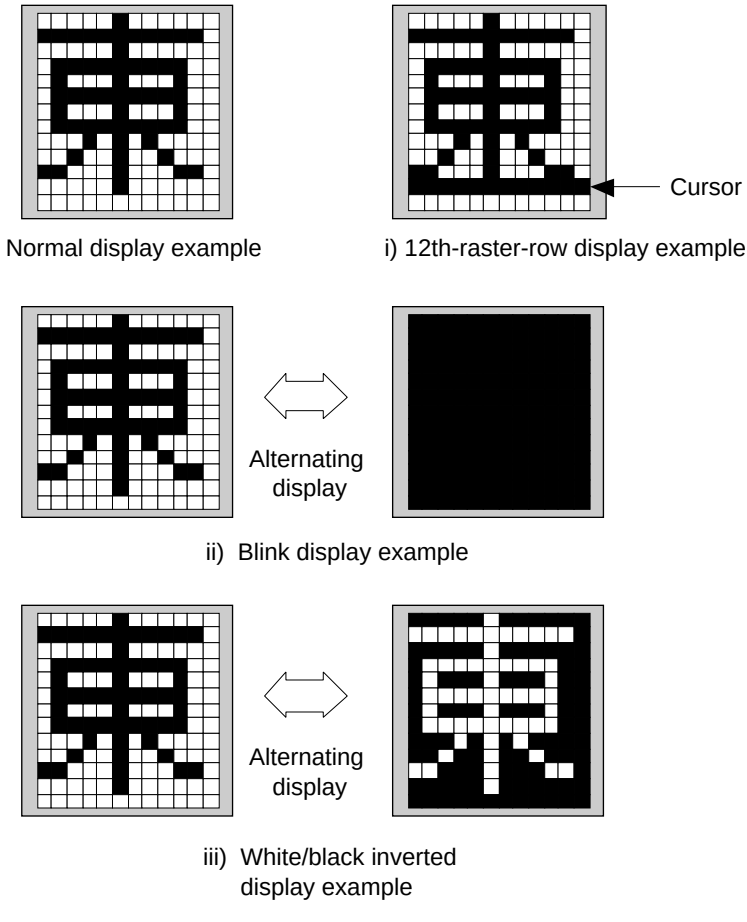


Figure 9 Cursor Display Examples

Display Control Register 1 (R3)

The display control register 1 (figure 10) includes bits ST, DC, and DS.

ST: When ST is 1, the display control register 1 enters the standby mode. The internal operation clock is divided into 32. Data cannot be displayed on the LCD panel, however, the consumption current can be suppressed during the standby mode. Note that the register setting value and the data inside the RAM are maintained.

DC: When DC is 1, the character display is turned on.

DS: When DS is 1, the segment display is turned on. Bit DS can selectively display marks.

Display Control Register 2 (R4)

NC1/0: Selects the display character in the horizontal direction. When performing a horizontal smooth scroll, set the number of display characters larger than the actual number of liquid crystal drive characters. When the frame frequency (cycle) is stable, the operation frequency is proportional to the display characters. Operation frequency must be suppressed by setting the number of display character as small as possible because the consumption current is proportional to the operation frequency. Refer to Oscillator for details.

N/L1/0: Sets the number of display lines. Set the number of display lines larger than the duty drive ratio (DT1/0). Do not set 10 to these bits. Table 13 indicates the settings of the display lines.

Table 13 Display Control Register 2 Setting

Display Lines NL1/0	Display Characters: NC1/0		
	00	**01**	**10**
00	1-line 6 characters	1-line 20 characters	1-line 40 characters
01	2-line 6 characters	2-line 10 characters	2-line 20 characters
10	Setting is inhibited.		
11	4-line 6 characters	4-line 10 characters	4-line 10 characters

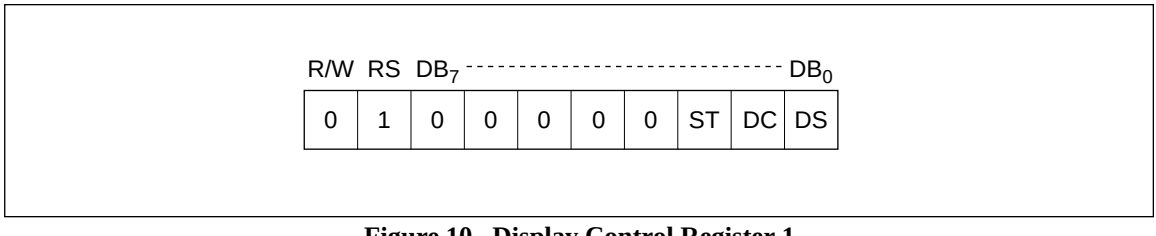


Figure 10 Display Control Register 1

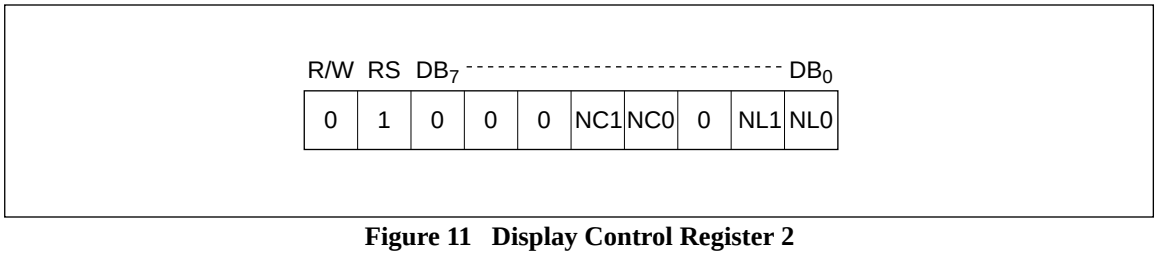


Figure 11 Display Control Register 2

Scroll Control Register 1 (R5)

The scroll control register 1 (figure 12) includes bits SN1, SN0, SL3, SL2, SL1, and SL0.

SN1/0: Selects the starting line to be displayed. When SN1/0 shows 00, display begins from the first line. When SN1/0 shows 01, 10, 11, display begins from the second, third, or fourth line, respectively. Use these bits within the display line setting (NL1/0). SN can be used to display a smooth scroll and DD RAM memory bank switching.

SL0 to SL3: Selects the scroll starting raster-row of the line set by the start display line (SL1/0). When these bits show 0000, a display line starting from the head raster-row (first raster-row) is displayed and can be set to 1100 (13th raster-row) showing the last raster-row. A vertical smooth scroll can be performed by sequentially incrementing the first raster-row. Refer to Vertical Smooth Scroll for details. Note that bits SL0 to SL3 that are set to a value above 1100 will not operate correctly.

Scroll Control Register 2 (R6)

The scroll control register 2 (figure 13) includes bits PS1, PS0, SE4, SE3, SE2, and SE1.

PS1/0: Selects the partial smooth scroll mode. When PS1/0 bits are 00, all characters scroll horizontally across the display. When bits PS1/0 are 01, only the leftmost character is fixed and the remaining characters perform horizontal smooth scroll display. When bits PS1/0 are 10, the two leftmost bits, and when 11, the three leftmost characters are fixed and the remaining characters perform horizontal smooth scroll Refer to Partial Smooth Scroll for details.

SE1 to SE4: These bits enable a dot scroll in display lines designated by scroll control register 3 (R7). When bit SE is 1, the first line is scrolled according to scroll control register 3 (R7). When SE2 is 1, the second line scrolls independently, when SE3 is 1, the third line scrolls independently, when SE4 is 1, the fourth line scrolls independently. Scrolling multiple lines at the same time is also possible.

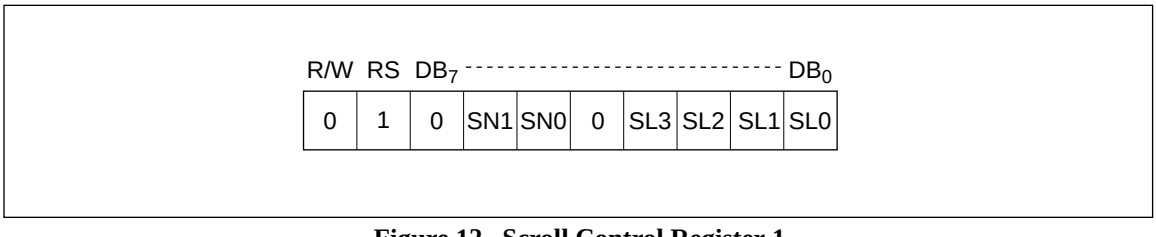


Figure 12 Scroll Control Register 1

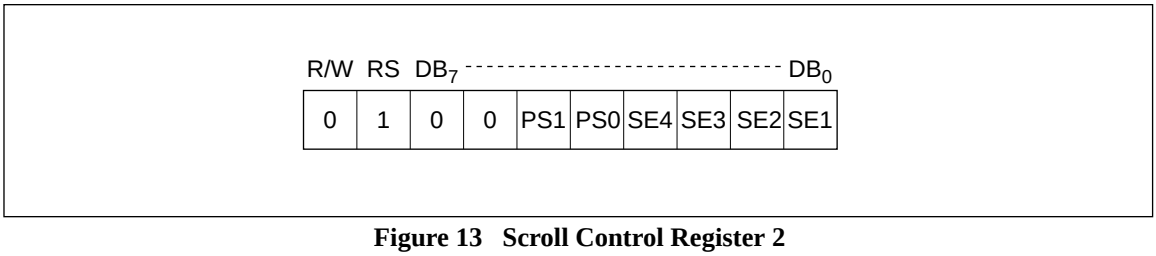


Figure 13 Scroll Control Register 2

Scroll Control Register 3 (R7)

The scroll control register 3 (figure 14) includes bits SQ5, SQ4, SQ3, SQ2, SQ1, and SQ0.

SQ0 to SQ5: These bits designate the number of dots to be horizontally scrolled to the left on the panel. Horizontal smooth scroll can be performed for any number of dots between 1 and 48 inclusive by using the non-display DD RAM area. When these bits are 000000, scrolling is not performed. When these bits are 110000, 48 dots are scrolled to the left. If these bits are set to a value above 110000, 48 dots are still scrolled. Refer to Horizontal Smooth Scroll for details.

RAM Address Register (R8)

The RAM address register (figure15) initially contains the RAM address at which incrementation (decrementation) starts. RAM selection bits (RM1/0) in the entry mode register (R0) select which RAM to access (DD RAM/CG RAM/SEG RAM). When DD RAM (RM1/0 = 00) is selected, address allocation differs according to the number of display lines, but in all cases the most significant bit (RA7) is ignored. During a 1-line display (NL1/0 = 00), addresses H'00 to H'4F are allocated to that line. During a 2-line display, addresses H'00 to H'27 are allocated to the first line, and addresses H'40 to H'67 are allocated to the second line. During a 4-line display, addresses H'00 to H'13 are allocated to the first line, H'20 to H'33 to the second , H'40 to H'53 to the third, and H'60 to H'73 to the fourth. See table 14.

When CG RAM (RM1/0 = 10) is selected, addresses H'00 to H'19 are allocated to the first character and addresses H'20 to H'39 are allocated to the second character, and so on (table 15). The setting of addresses between characters (example: H'1A to H'1F) is ignored here. When SEG RAM is selected (RM1/0 = 11), addresses H'0 to H'F are allocated to the RAM and the upper four bits (R4 to R7) are ignored (table 16).

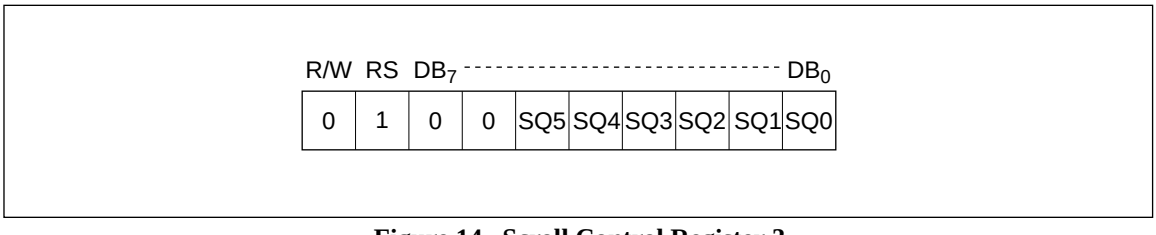


Figure 14 Scroll Control Register 3

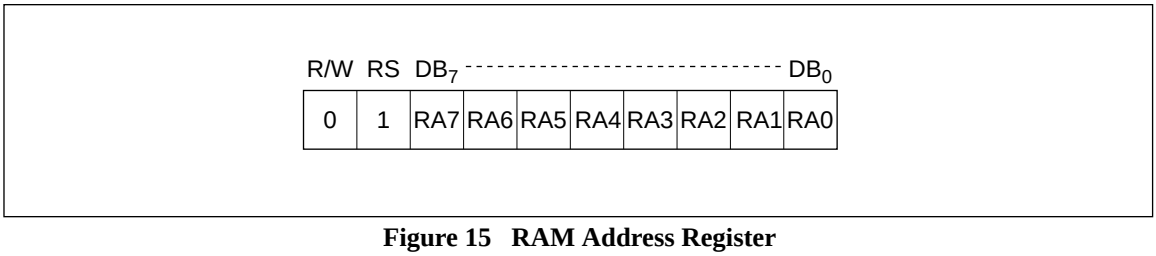


Figure 15 RAM Address Register

Table 14 DD RAM Address Allocation

Displayed Lines	1-Line Display (NL1/0 = 00)	2-Line Display (NL1/0 = 01)	4-Line Display (NL1/0 = 00)
First line	H'00 to H'4F	H'00 to H'27	H'00 to H'13
Second line	—	H'40 to H'67	H'20 to H'33
Third line	—	—	H'40 to H'53
Fourth line	—	—	H'60 to H'73

Table 15 CG RAM Address Allocation

Displayed Character	CG RAM Address
First character	H'00 to H'19
Second character	H'20 to H'39
Third character	H'40 to H'59
Fourth character	H'60 to H'79
Fifth character	H'80 to H'99
Sixth character	H'A0 to H'B9
Seventh character	H'C0 to H'D9
Eighth character	H'E0 to H'F9

Table 16 SEG RAM Address Allocation

Displayed Segment	SEG RAM Address	Displayed Segment	SEG RAM Address
SEG1 to SEG6	H'0	SEG49 to SEG54	H'8
SEG7 to SEG12	H'1	SEG55 to SEG60	H'9
SEG13 to SEG18	H'2	SEG61 to SEG66	H'A
SEG19 to SEG24	H'3	SEG67 to SEG72	H'B
SEG25 to SEG30	H'4	SEG73 to SEG78	H'C
SEG31 to SEG36	H'5	SEG79 to SEG84	H'D
SEG37 to SEG42	H'6	SEG85 to SEG90	H'E
SEG43 to SEG48	H'7	SEG91 to SEG96	H'F

Note: SEG72 to SEG96 are driven by extension drivers.

RAM Data Register (R9)

This register (figure 16) stores 8-bit data that is written to or read from the DD RAM, CG RAM, or SEG RAM at the address indicated by the RAM address counter (RAC). The RAM selection bit (RM1/0) selects the RAM (DD RAM, CG RAM, SEG RAM). After the said RAM is accessed, RAM address is automatically incremented (decremented) by 1 according to the I/D bit.

Note that RAM selection bits (RM1/0) and RAM address register (R8) must be set before reading. If not, the first data read is invalid. If read instructions continue to be executed, however, data will be read correctly from the second read.

Test Register (RF)

This is a test register (figure 17) and must be set to H'00 at all times. This register is automatically cleared (H'00) by reset input; however, it must be cleared by software after power-on if the reset pin is not used.

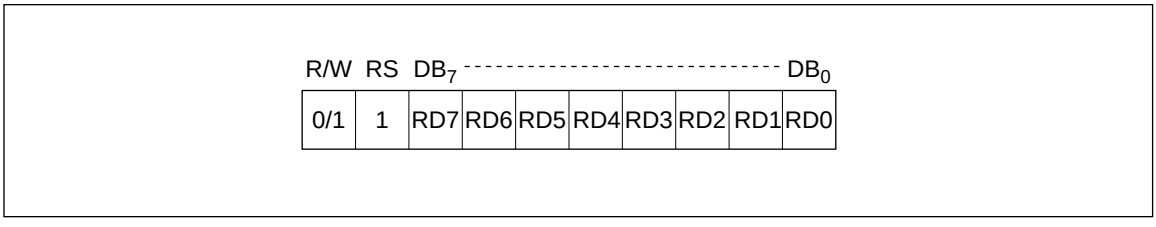


Figure 16 RAM Data Register

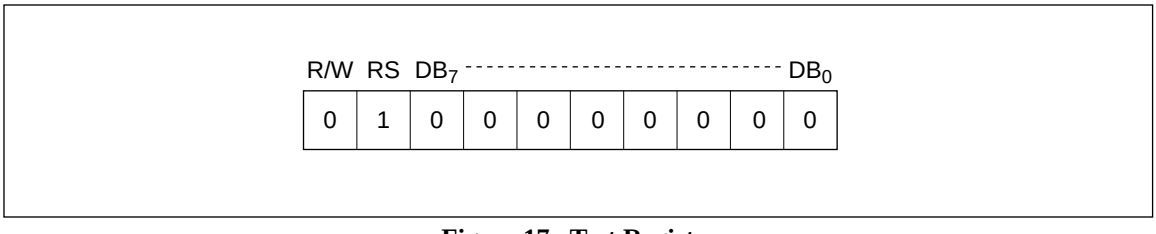


Figure 17 Test Register

Table 17 Instruction Registers

Reg. No.	Index (Hex)	Register	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Clock Cycle
IR	—	Index (IDR)	0	0	—	—	—	—	ID3	ID2	ID1	ID0	Designates the register number of the instruction register to access. ID = 0000: R0 to 1001: R9	12
SR	—	Status (STR)	1	0	BF	NF1	NF0	—	LF3	LF2	LF1	LF0	Indicates the busy flag (BF), display read line position (NF1/0), display read raster-row position (NL0 to NL3).	0
R0	0	Entry mode (EMR)	0	1	0	0	0	0	0	I/D	RM1	RM0	Designates RAM address incrementation or decrementation (I/D) and RAM selection (RM1/0).	12
R1	1	Function set (FSR)	0	1	0	BST	EXT2	EXT1	DT1	DT0	0	DCL	Clears display (DCL) and initializes the DDRAM address. Selects duty drive ratio (DT1/0), enables extension driver (EXT2/1) and sets the booster operation on.	DCL = 1: 492 Other: 12
R2	2	Cursor control (CCR)	0	1	0	0	0	0	CHM	C	CM1	CM0	Designates cursor-on (C) and cursor display mode (CM1/0). Executes cursor home (CHM) instruction.	12
R3	3	Display control 1 (DCR1)	0	1	0	0	0	0	0	ST	DC	DS	Designates standby mode (ST), character display on (DC), and segment display on (DS).	12
R4	4	Display control 2 (DCR2)	0	1	0	0	NC1	NC0	0	0	NL1	NL0	Sets the number of display characters (NC1/0) and display lines (NL1/0).	12
R5	5	Scroll control 1 (SCR1)	0	1	0	SN1	SN0	0	SL3	SL2	SL1	SL0	Sets the display start line (SN1/0) and start raster-row (ST0 to ST3).	12
R6	6	Scroll control 2 (SCR2)	0	1	0	0	PS1	PS0	SE4	SE3	SE2	SE1	Designates partial scroll columns (PS1/0) and scroll display line enable (SE1 to SE4).	12
R7	7	Scroll control 3 (SCR3)	0	1	0	0	SQ5	SQ4	SQ3	SQ2	SQ1	SQ0	Sets the number of dots to be scrolled (SQR0 to SQR5).	12

Table 17 Instruction Registers (cont)

Reg. No.	Index (Hex)	Register	Code R/W	RS	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Clock Cycle
R8	8	RAM address (RAR)	0	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	Resets the address counter for DD RAM/CG RAM/SEG RAM. RAM is selected by RM1/0.	12
R9	9	RAM data (RDR)	0/1	1	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	Writes or reads data to and from DD RAM/CG RAM/SEG RAM. RAM is selected by RM1/0.	12
RF	F	Test (TSR)	0	1	0	0	0	0	0	0	0	0	This is a test register. Set 00 in this register.	12

Note: The execution time depends on the input or oscillation frequency.

BF = 1: Internal processing being performed
NF1/0: Position of display read line
LF0 to LF3: Position of display read raster-row
ID = 1: Address increment
= 0: Address decrement
RM1/0: RAM selection (00/01: DD RAM. (10: GG RAM, 11: SEG RAM)
BST = 1: Booster on
EXT2 = 1: Common driver extension enable
EXT1 = 1: Segment driver extension enable
DT1/0: Duty ratio (00: 1/14, 01: 1/27, 10: 1/40, 11: 1/53)
DCL = 1: Executes display-clear instruction
CHM = 1: Executes cursor-home instruction
C = 1: Cursor on
CM1/0: Designates cursor mode (00: 12th raster-row, 01: blinking, 10: white/black inverse)
ST = 1: Standby mode
DC = 1: Character display on
DS = 1: Segment display on

NC1/0: Sets the number of display characters (6 to 40 characters)
NL1/0: Sets the number of display lines (00: 1 line, 01: 2 lines, 11: 4 lines)
SN1/0: Designates the line to start displaying (00: first line, 01: second line, 10: third line, 11: fourth line)
SL0 to SL3: Designates scroll starting raster-row (0000: first raster-row, 1100: 13th raster-row)
PS1/0: Designates partial scroll (00: all columns scroll. 01: the leftmost column fixed, 10: the two leftmost columns fixed, 11: the three leftmost columns fixed)
SE1 to SE4: Designates which line to scroll (SE = 1: enables the first line to be scrolled, etc.)
SQ0 to SQ5: Number of dots to scroll (0 to 48 dots)
RA0 to RA7: RAM address
RD0 to RD7: RAM data

Reset Function

The HD66730 is reset by setting the RESET pin to low level. During reset, the system performs next-control-register setting and executes instructions. The busy flag (BF) therefore indicates a busy state (BF = 1) at this time, which means that only the index register and status register can be accessed.

Display clear (DD RAM reset) is performed automatically by reset input. Since more than 500 clocks of execution cycles are needed to initialize the DD RAM, the reset period must be set to more than this number. Note that if the reset input conditions specified in Electrical Characteristics are not satisfied, the HD66730 will not operate correctly, and reset should be performed by software.

Initialization of Instruction Register Function

1. Index Register: IR

   The index register cannot be initialized by reset. After reset release, the index register must be set to access a control register.

2. Status register: SR

   BF = 1: Busy state

3. Entry mode register: R0

   I/D = 1: +1 (incrementation)
   RM1/0 = 00: DD RAM selection

4. Function set register: R1

   BST = 0: Booster off
   EXT2/1 = 11: Driver extension enable
   DT1/0 = 11: 1/53 duty drive
   DCL = 1: Display-clear execution

Note: At least 500 clock cycles of execution time is needed to clear the DD RAM.

5. Cursor control register: R2

   CHM = 1: Cursor home execution
   C = 0: Cursor display off
   CM1/0 = 00: 12th raster-row cursor display mode

6. Display control register 1: R3

   ST = 0: Standby mode clear
   DC = 0: Character display off
   DS = 0: Segment display off

7. Display control register 2: R4

   NC1/0 = 00: 6-column display mode
   NL1/0 = 00: 1-line display mode

8. Scroll control register 1: R5

   SN1/0 = 00: Starts displaying from the first line.
   SL3 to SL0 = 0000: Starts displaying from the first raster-row.

9. Scroll control register 2: R6

   PS1/0 = 00: Partial scroll release
   SE4 to SE1 = 0000: Disables dot scrolling for all lines.

10. Scroll control register 3: R7

    SQ5 to SQ0 = 000000: Number of dots to be scrolled = 0

11. RAM address register: R8

    RAM address register is automatically incremented during reset when display-clear is executed. Note that after reset is released, this register must be reset by software before accessing RAM.

Initial Setting of Pin Functions

1. Bus/serial interface

   The input level of pin IM selects the 8-bit bus or serial interface. For an 8-bit bus interface, data is written into the index register or read from the status register according to the level of pin R/W. Note that pin RS must be held low during this time. For serial interface, data is written into the index register according to bit R/W. Note that bit RS must be 0 during this time. During reset, only the index register and status register can be set and RAM cannot be accessed.

2. LCD driver output

   Since segment drivers (pins SEG1 to SEG71) are in a display-off state during reset, they output non-selective levels (V2/V3 level) during reset. At this time, a 4-line 6-character display alternates its current. Common drivers (pins COM1 to COM24 and COMS) output non-selective levels (V1/V4 level) during reset, and alternate its current for a 4-line 6-character display.

Note: Pins COM25/COMD are grounded (0V) during reset. When pin COM25 is used without expanding drivers to the common side, display may be performed using the liquid crystal drive voltage. In this case, adjust the liquid crystal voltage during reset.

3. Extension driver interface output

   Since bits EXT2/1 are 11 during reset, extension is performed to both segment side and common side. Pin CL2 outputs the oscillation (operation) frequency clock. Pins CL1 and M output signals in a cycle corresponding to a 4-line 6-character display size. In addition, pins SEGD and COM25/COMD output low (ground level) since the display is turned off.

4. Booster output

   The operation of the internal booster stops because bit BST becomes 0 during reset.

Note: The potential of pins V5OUT2 and V5OUT3 increases by about +0.7 V with respect to GND level when the booster stops. When using external polarized capacitors, make sure that no reverse bias occurs.

Interfacing to the MPU

The HD66730 enters 8-bit bus interface mode when the IM pin is set high. The HD66730 can interface with the MPU via an I/O port. Use the serial interface when there are restraints in the bus wiring width.

Instruction is executed when data is written into the control register. In this case, only the status register can be read (busy check, etc.). In this case, check the busy flag when accessing (polling), or insert an interval considering the execution time and perform the next access when the internal process has completely finished. The instruction execution time depends on the HD66730 operation frequency. When using the internal oscillation circuit of the HD66730, the instruction time will change as the oscillation frequency does. Figure 18 shows an example of an 8-bit data transfer timing sequence. Figure 19 shows an example of interface between HD66730 and 8-bit microcomputers.

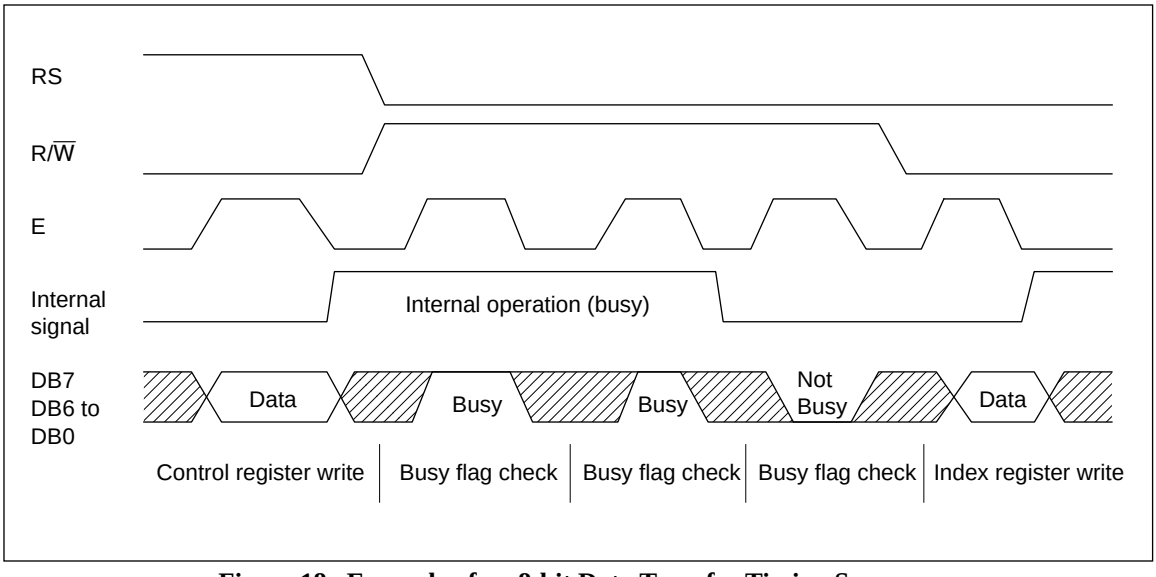
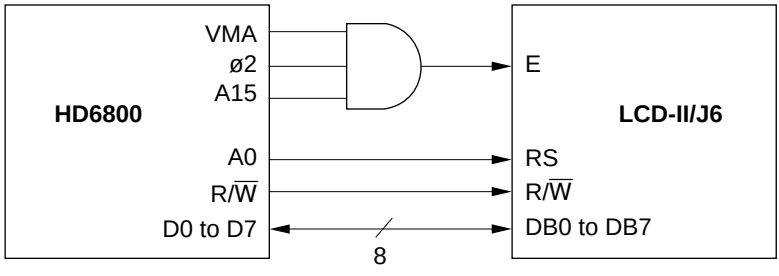
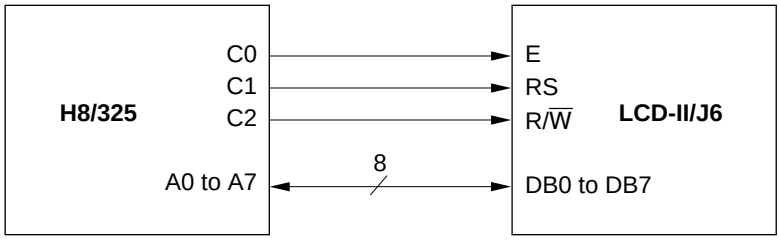


Figure 18 Example of an 8-bit Data Transfer Timing Sequence



a) Bus line interface



b) I/O port interface

Figure 19 Example of Interfacing with 8-Bit Microcomputers

Transferring Serial Data

The HD66730 enters serial interface mode when the IM pin is set low. A three-line clock-synchronous transfer method is used. The HD66730 receives serial input data (SID) and transmits serial output data (SOD) by synchronizing with a transfer clock (SCLK) sent from the master side.

When the HD66730 interfaces with several chips, chip select pin (CS*) must be used. The transfer clock (SCLK) input is activated by making chip select (CS*) low. In addition, the transfer counter of the HD66730 can be reset and serial transfer synchronized by making chip select (CS*) high. Here, since the data which was being sent at reset is cleared, restart the transfer from the first bit of this data. In a minimum system where a single HD66730 interfaces to a single MPU, an interface can be constructed from the transfer clock (SCLK) and serial input data (SID). In this case, chip select (CS*) should be fixed to low.

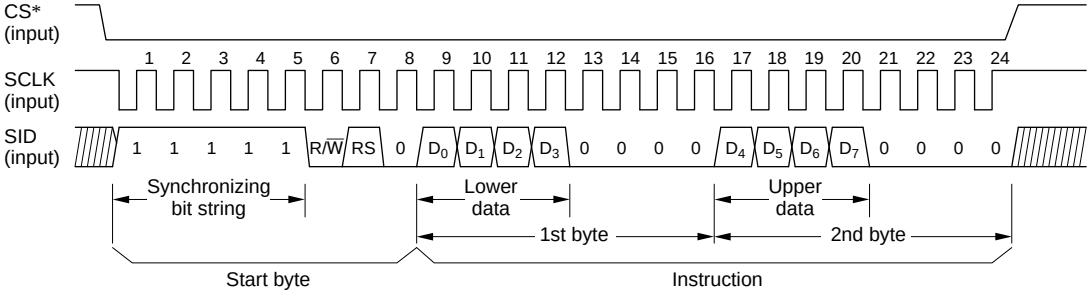
The transfer clock (SCLK) is independent of operational clock (CLK) of the HD66730. However, when several instructions are continuously transferred, the instruction execution time determined by the operational clock (CLK) (see Continuous Transfer) must be considered since the HD66730 does not have an internal transmit/receive buffer.

Figure 20 shows the basic procedure for transferring serial data. To begin with, transfer the start byte. By receiving five consecutive bits of 1 (synchronizing bit string) at the beginning of the start byte, the transfer counter of the HD66730 is reset and serial transfer is synchronized. The 2 bits following the synchronizing bit string (5 bits) specify transfer direction (R/$\overline{W}$ bit) and register select (RS bit). Be sure to transfer 0 in the 8th bit.

After receiving the start byte, instructions are received and the data/busy flag is transmitted. When the transfer direction and register select remain the same, data can be continuously transmitted or received.

The transfer protocol is described in detail in the following.

a) Serial data input (receiving)



b) Serial data output (transmitting)

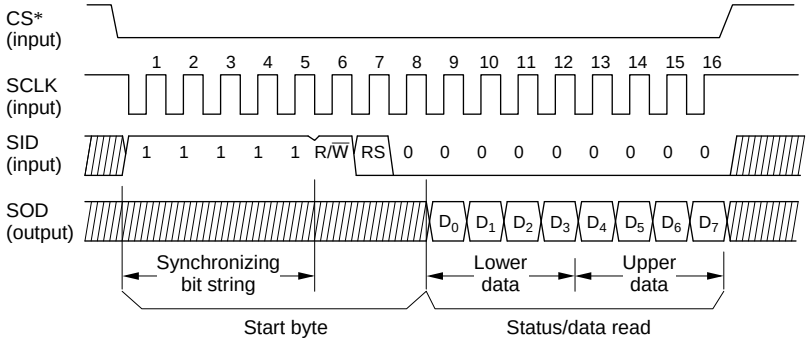


Figure 20 Basic Procedure for Transferring Serial Data

- Receiving (write)

  After receiving the start synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, an 8-bit instruction is received in 2 bytes: the lower 4 bits of the instruction are placed in the LSB of the first byte, and the higher 4 bits of the instruction are placed in the LSB of the second byte. Be sure to transfer 0 in the following 4 bits of each byte. When instructions are received with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

- Transmitting (read)

  After receiving the synchronizing bit string, the R/W bit (= 0), and the RS bit in the start byte, 8-bit read data is transmitted from pin SOD in the same way as receiving. When read data is transmitted with R/W bit and RS bit unchanged, continuous transfer is possible (see Continuous Transfer in the following).

  The status register (SR) is read when the RS bit is 0. RAM data is read out when the RS bit is set to 1 after designating RAM data register (R9) with the index register (IR). Bits RM1/0 of entry mode register (R0) select the RAM. When reading RAM data, an interval longer than the RAM reading time must be taken after the start byte has been accepted and before the first data has been read out. During transmission (data output), the SID input is continuously monitored for a start synchronizing bit string (11111). Once this has been detected, the R/$\overline{W}$ and RS bits are received. Accordingly, 0 must always be input to SID when transmitting data continuously.

- Continuous Transfer

  When instructions are received with the R/W bit and RS bit unchanged, continuous receive is possible without inserting a start byte between instructions.

  After receiving the last bit (the 8th bit in the 2nd byte) of an instruction, the system begins to execute it. To execute the next instruction, the instruction execution time of the HD66730 must be considered. If the last bit (the 8th bit in the 2nd byte) of the next instruction is received during execution of the previous instruction, the instruction will be ignored.

  In addition, if the next unit of data is read before read execution of previous data is completed for RAM data, normal data is not sent. To transfer data normally, the busy flag must be checked. However, if the amount of wiring used for transmission needs to be reduced, or if the burden of polling on the CPU needs to be lightened, transfer can be performed without reading the busy flag. In this case, insert a transfer wait between instructions so that the current instruction has time to complete execution. Figure 21 shows the procedure for continuous data transfer.

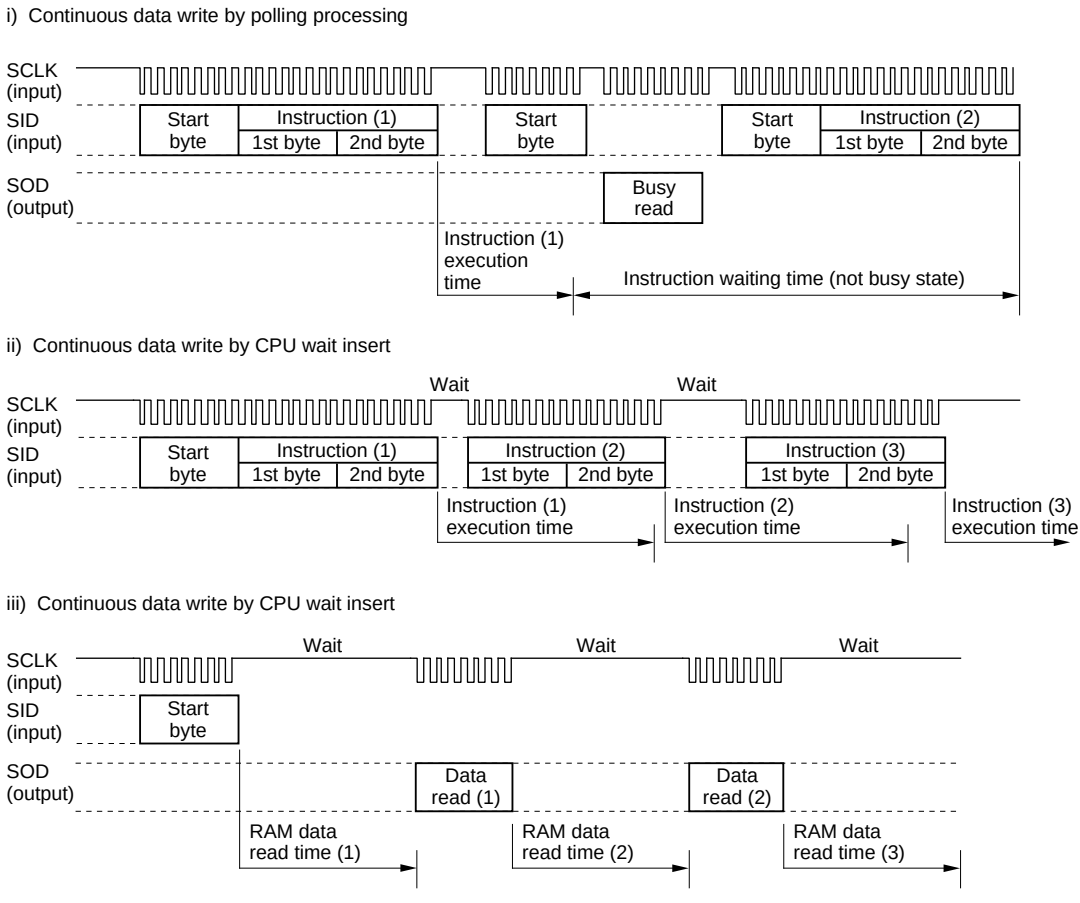


Figure 21 Procedure for Continuous Data Transfer

Combined Display of Full-Size and Half-Size Characters

The HD66730 performs display from the left edge of the display combining 12-dot full-size (character size: 11 × 12 dots) and 6-dot half-size characters (character size: 5 × 12 dots). There will be a one-dot space between these fonts.

The most significant bit in the data (8 bits) in DD RAM is allocated to the designation bit indicating a full-size or half-size character. When this MSB is 0, the full-size character is selected, and when 1, the half-size character is selected.

When the full-size character is selected, 2 bytes of DD RAM are linked and used as a 16-bit code (figure 22). In this case, the lower byte is written into the smaller DD RAM address. 12 bits of this 16-bit code are used as character codes. Up to 4096 character codes can be specified. In addition, two of the remaining four bits can be allocated to a display-attribute code and can designate white/black inverted display for individual characters (refer to Display Attribute Designation). Table 18 shows the relationship between the 16-bit designated JIS code and the HD66730 12-bit character code. 8-bit data designating half-size characters are used as an 8-bit code (figure 23). Specifically, 7 bits of the 8-bit half-size characters become the character codes, so that a total of 128 characters can be displayed (alphanumeric characters and symbols can be displayed as half-size characters).

User fonts can be displayed using the CG RAM. Special symbols not included in the internal CG ROM or the JIS Level-2 Kanji Set can be displayed as needed. Since the display font size of the CG RAM is 12 × 13 dots, CG RAM fonts can be displayed to the right, left, top or bottom, in order to be used to display double-size characters or graphics. Note that the display-attribute code (A1/A0) designation that is to be written into the DD RAM is ignored when the CG RAM is used. In this case, bits 6 and 7 in the CG RAM are used for display-attribute-code designation. Refer to CG RAM for details.

Table 18 Relationship between JIS Codes and HD66730 Character Codes

- JIS first byte code: b1 to b7 (7 bits)
- JIS second byte code: a1 to a7 (7 bits)
- CG RAM address for user fonts: u0 to u2 (3 bits)

				Character Code Arrangement of HD66730											
JIS	**b7**	**b6**	**b5**	**C11**	**C10**	**C9**	**C8**	**C7**	**C6**	**C5**	**C4**	**C3**	**C2**	**C1**	**C0**
Non-kanji	0	1	0	a7	a6	b3	b2	b1	0	0	a5	a4	a3	a2	a1
Level 1 kanji	0	1	1	b7	b6	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
Level 1 kanji	1	0	0	b7	b6	b3	b2	b1	a7	a6	a5	a4	a3	a2	a1
User font	—	—	—	0	0	0	0	0	0	0	0	0	u2	u1	u0
				Upper byte				Lower byte							

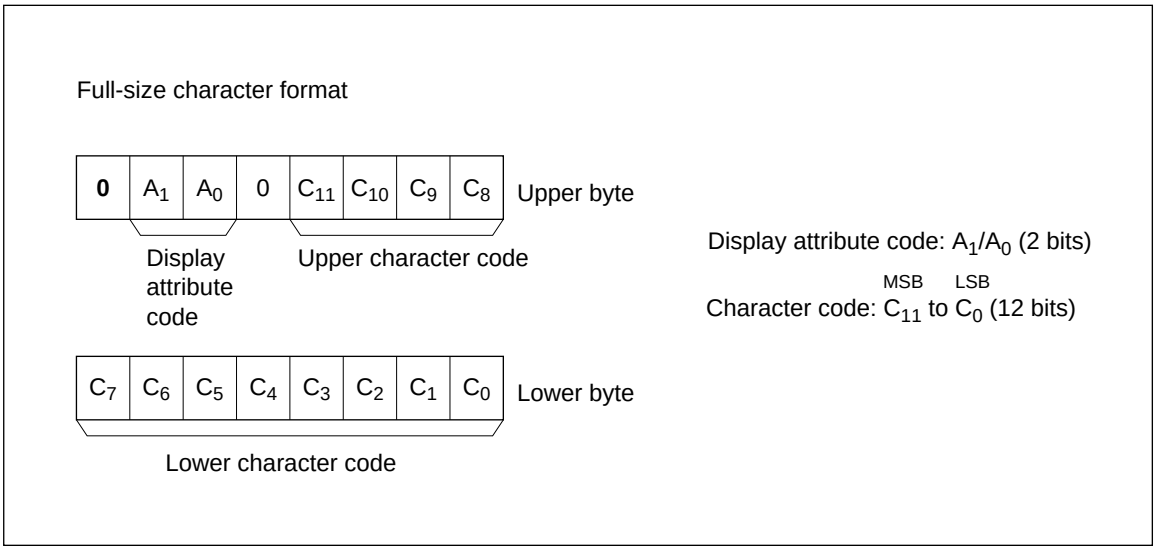


Figure 22 Full-Size Character Codes

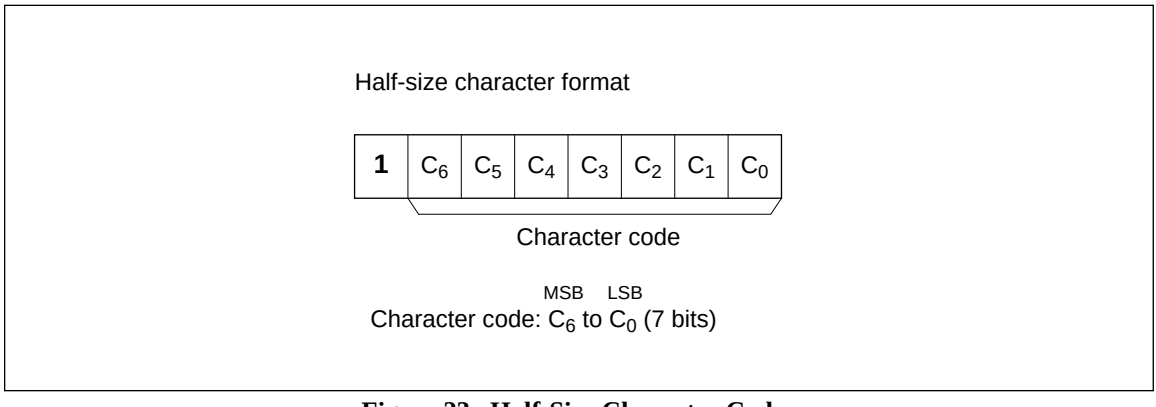


Figure 23 Half-Size Character Codes

An example of displaying full-size and half-size characters together is described here.

Full-size character display conforms to JIS (16 bits). Perform code conversion (16 bits → 12 bits) according to the relationship between the 16-bit JIS code and the HD66730 12-bit character code and write two-byte character data to the DD RAM (write the lower byte to the smaller DD RAM address). The example is shown in table 19. When displaying a half-size character, refer to table 5 the HD66730 Half-size Font List and write one-byte character data into the DD RAM. The example is shown in table 20.

Figure 24 shows how to set data to the DD RAM when performing a 2-line display and figure 25 shows the resulting liquid crystal display.

Table 19 Example of Full-Size Font Conversion

Displayed Character	JIS Code (First/Second Byte)	Character Code (C11 to C0)
東	45/6C (Hex)	AEC (Hex)
京	35/7E (Hex)	2FE (Hex)
都	45/54 (Hex)	AD4 (Hex)
小	3E/2E (Hex)	72E (Hex)
平	4A/3F (Hex)	D3F (Hex)
市	3B/54 (Hex)	5D4 (Hex)
本	4B/5C (Hex)	DDC (Hex)
町	44/2E (Hex)	A2C (Hex)
の	24/4E (Hex)	A0E (Hex)

Table 20 Example of Half-Size Font Code

Display Character	Character Code (C0 to C11)
1	31 (Hex)
2	32 (Hex)
0	30 (Hex)
,	2C (Hex)
M	4D (Hex)
C	43 (Hex)

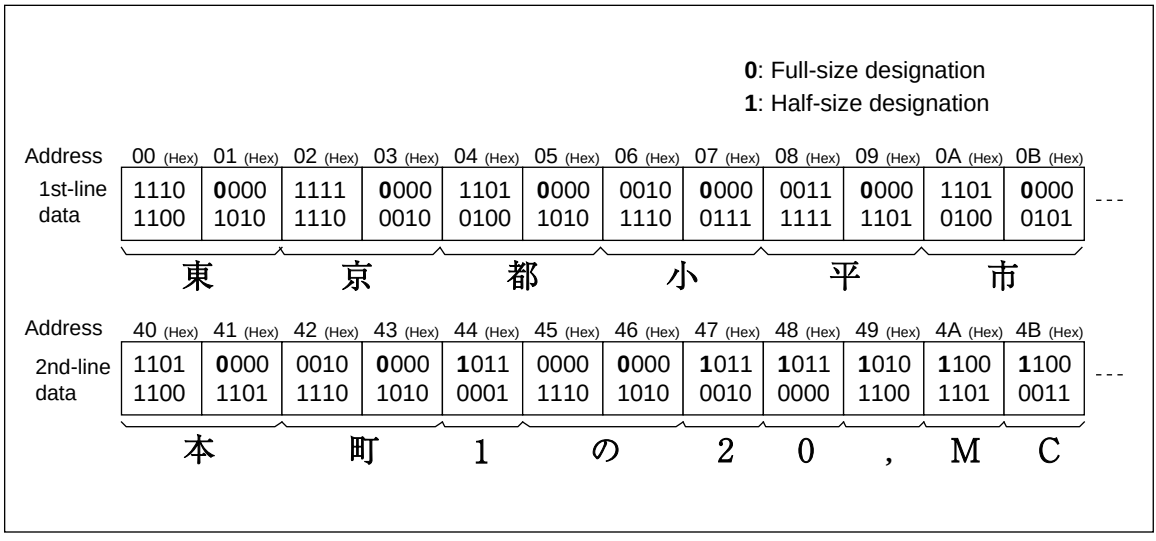


Figure 24 Example of DD RAM Character Code (2-Line Display Mode)

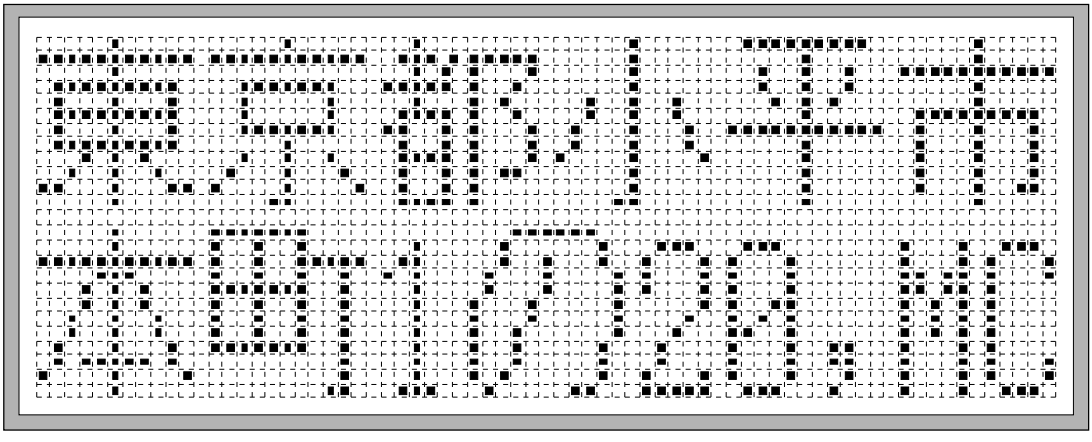


Figure 25 Example of Liquid Crystal Display

Display Attribute Designation

The HD66730 allocates 12 bits of the full-size 16-bit code character to an abbreviated character code and 2 bits to a display-attribute code (figure 26). White/black inverted display, blinking display, and white/black inverted blinking display can be designated for each full-size character (table 21). Display attribute control is performed for a 12×13 dot matrix unit that includes a 11×12 dot full-size character and a column of dots to the right and a row of dots to the bottom (figure 27). The blinking cycle for blinking display and white/black inverted blinking display is 64 frames. Blinking display is performed by changing the display pattern every 32 frames. Since the 8-bit code designated for half-size characters cannot accommodate a display attribute, they will always be displayed normally.

Table 21 Display Attribute Designation

A1	A0	Display State
0	0	Normal display
0	1	White/black inverted display
1	0	Blinking display
1	1	White/black inverted blinking display

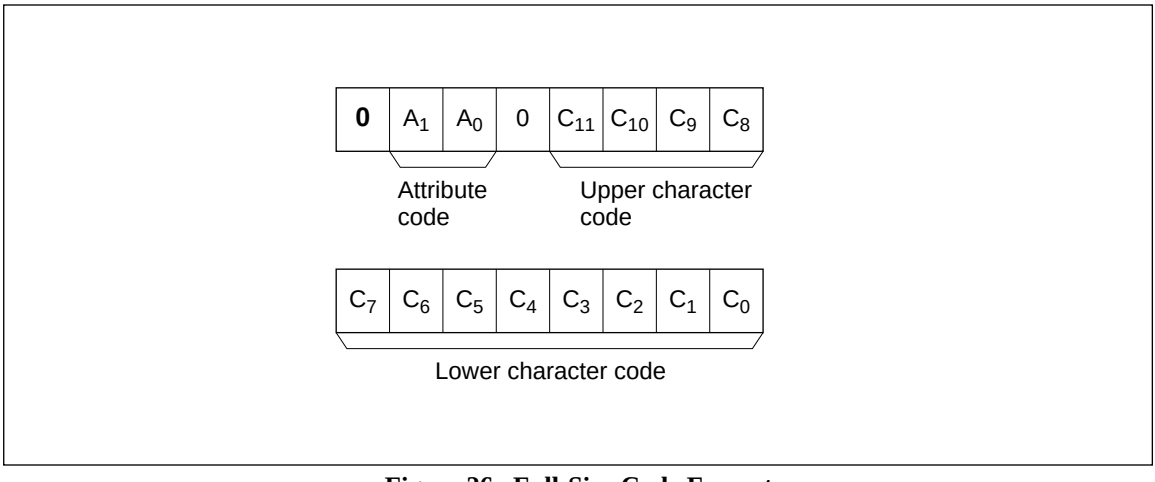
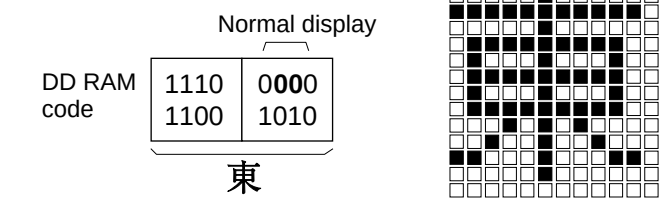
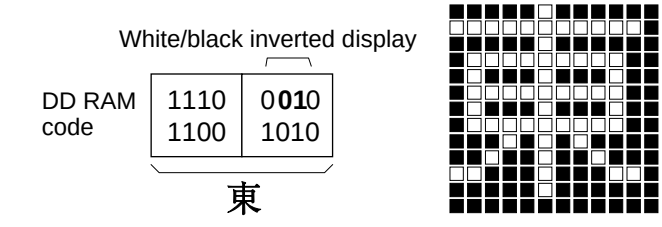


Figure 26 Full-Size Code Format

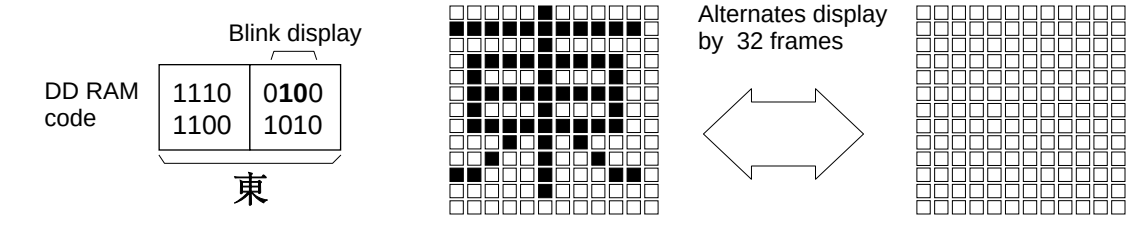
a) Example of normal display



b) Example of white/black inverted display



c) Example of blinking display



d) Example of white/black inverted blinking display

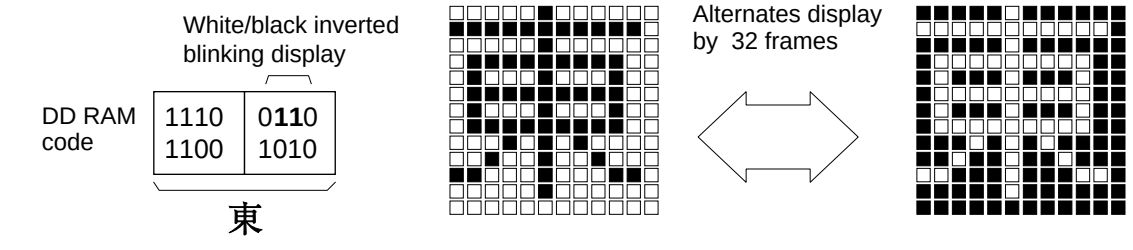


Figure 27 Setting Codes in the DD RAM and Display Examples

Horizontal Smooth Scroll

Data shown on the display can be scrolled horizontally to the left for a specified number of dots (figure 28). The number of dots are set in scroll control register 3 (SCR3: R7), and the display lines to be scrolled are designated by the display line enable bits (SE1/SE2/SE3/SE4) in scroll control register 2 (SCR2: R6). Because the number of dots that can be set for scrolling here is 48, scrolling for more than this number can be achieved by shifting to the left by four characters of character code data in DD RAM for the scroll display line in question, rewriting the characters, and then scrolling again. When rewriting DD RAM while displaying characters, however, character output will momentarily breakdown, and the display may flicker. In this case, first check which display lines are currently being displayed by referring to NF1/0 (line 1 to the line 4) and display raster-rows LF0 to LF3 (raster-row 1 to raster-row 13) in the status register, and then rewrite a DD RAM line that is not being displayed. Keep in mind that scroll display line enable bits (SE1 to SE4) can be used to designate those display lines for which horizontal smooth scroll is desired.

In partial scroll, one to three leftmost characters on the display as specified by the partial scroll bits (PS1/0) of the scroll control register 2 (SCR: R6) are fixed and the remaining characters undergo a smooth scroll to perform partial smooth scroll.

When performing horizontal smooth scroll, the number of characters to be displayed (NC1/0: R4) must be at least 4 characters more than the number of characters actually displayed on the liquid crystal display. For example, set 10 or more display characters (NC1/0) for a single-chip 6-character display.

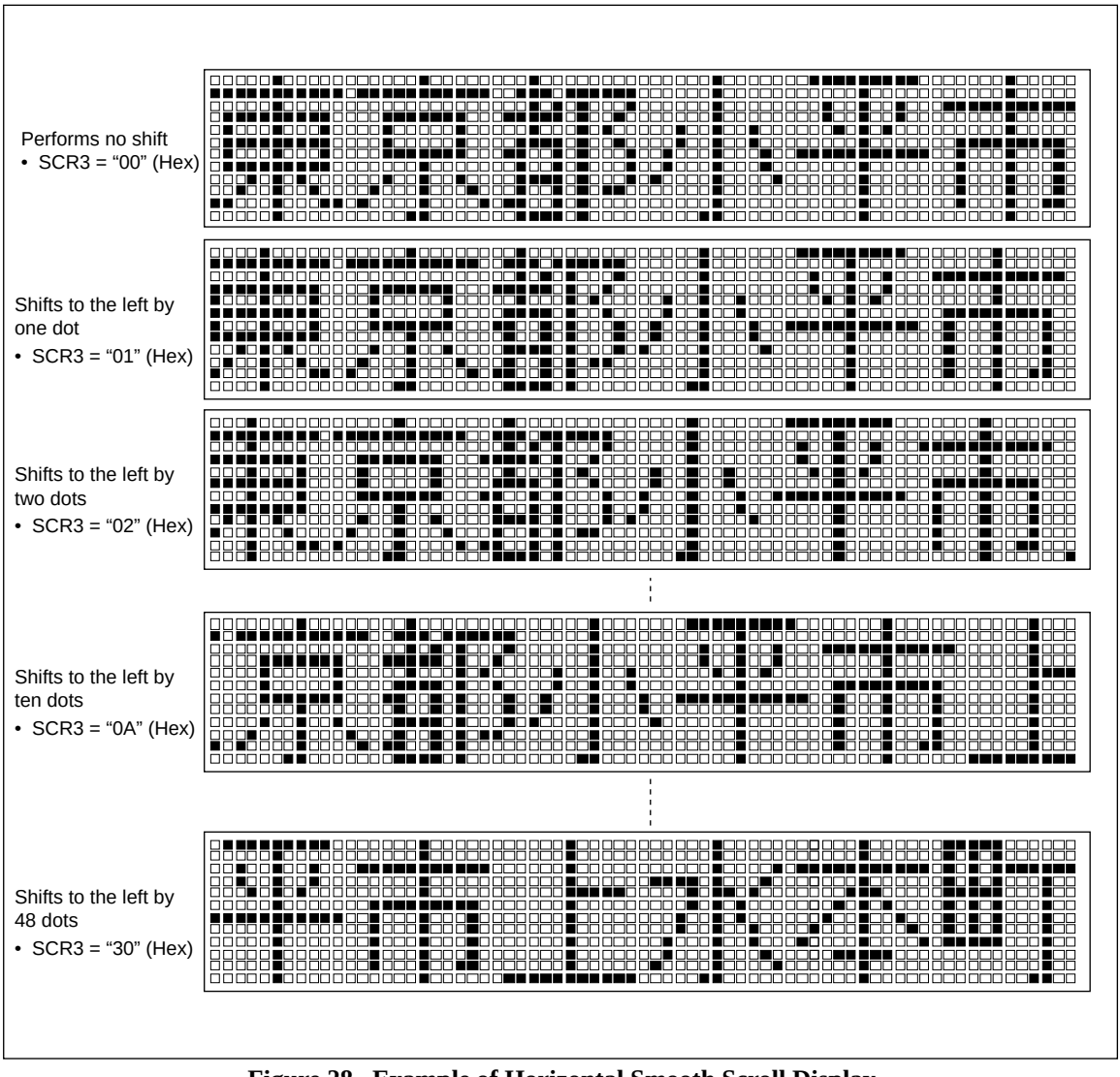
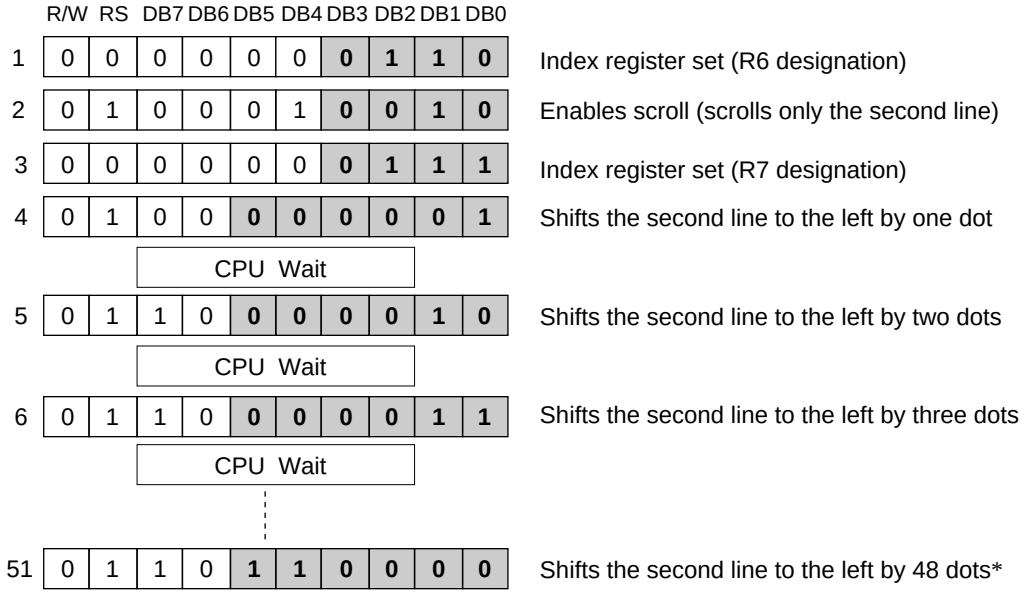


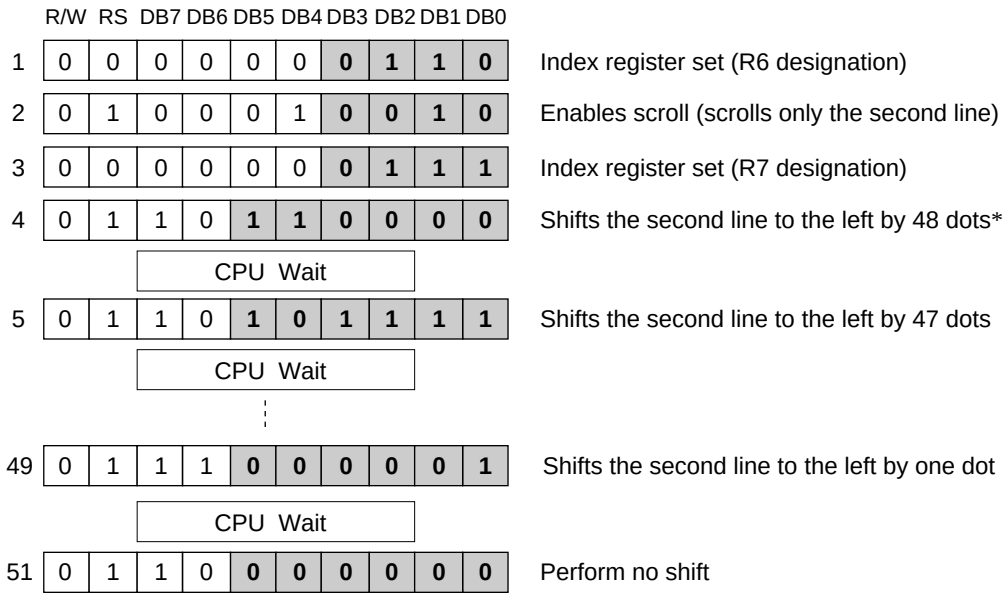
Figure 28 Example of Horizontal Smooth Scroll Display

Examples of Register Setting



Note: The number of dots that can be specified for scrolling is 48. Scrolling for more than this number can be achieved by rewriting DD RAM data and scrolling again from dot 0. Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode: 40 characters, 2-line display mode: 20 characters, 4-line display mode: 10 characters).

Figure 29 Example of Executing Smooth Scroll to the Left



Note: The number of dots that can be specified for scrolling is 48. Rewrite 48 dots (4 characters) of data inside the DD RAM and shift them to the right before scrolling. Scrolling for more than this number can be achieved by rewriting the data of DD RAM and begin scrolling from dot 48 again. Note that the number of characters shown on the LCD and the number of scroll characters must be less than the number of maximum display characters (1-line display mode: 40 characters, 2-line display mode: 20 characters, 4-line display mode: 10 characters).

Figure 30 Example of Executing Smooth Scroll to the Right

Partial Smooth Scroll

Partial smooth scroll displays one to three leftmost characters as fixed while the remaining ones undergo a horizontal smooth scroll in the left and right direction. Specifically, the number of leftmost characters to be fixed is specified by the partial scroll bits (PS1/0) in the scroll control register 2 (SCR2: R6). For example, when bits PS1/0 are 10, the two leftmost characters are fixed; when 11, the three leftmost characters are fixed.

Although half-size characters can be displayed in a fixed display area, they must be displayed in even-numbered groups of two, four or six characters. Figure 31 shows an example of smooth scroll performed in a display when bits PS1/0 are set to 10. The two leftmost characters (住所) are displayed as fixed, and the remaining four characters undergo a smooth scroll.

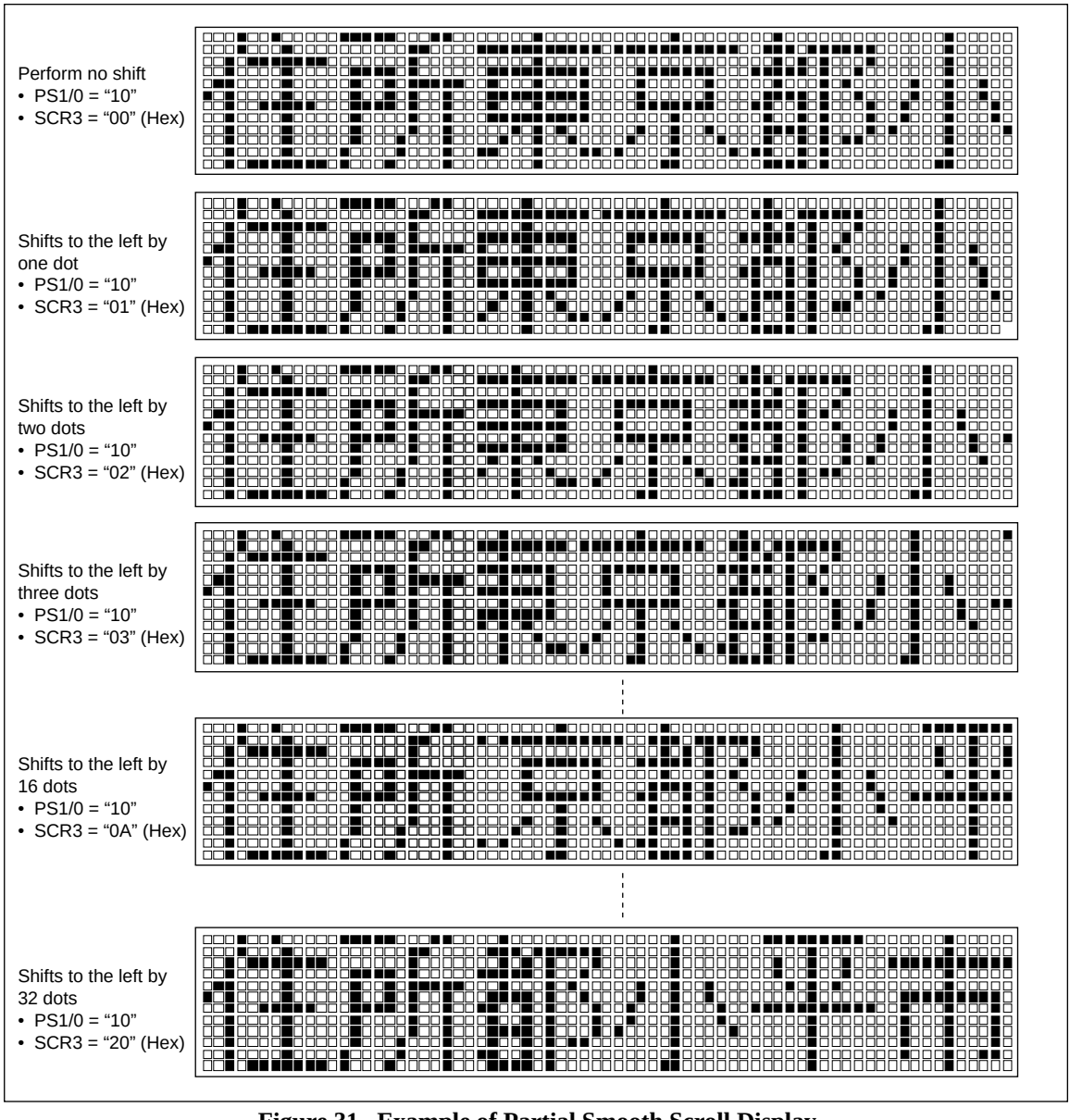


Figure 31 Example of Partial Smooth Scroll Display

Vertical Smooth Scroll

Vertical smooth scroll up and down can be performed by setting the number of display lines (NL1/0: R4) to a value greater than the actual number of liquid crystal display lines, which can be set by the duty drive ratio (DT1/0: R1) to 1/14 (1-line display), 1/27 (2-line display), 1/40 (3-line display), or 1/53 (4-line display). The display line setting (NL1/0: R4), which controls the display, can select 1-line display mode, 2-line display mode, or 4-line display mode.

For example, to perform normal vertical smooth scroll for a 3-line liquid crystal display with a duty ratio of 1/40, set the number of display lines (NL1/0: R4) to 4 lines. Note that if vertical smooth scroll is performed when the number of actual liquid display lines is the same as the number of set display lines, the display line that has scrolled out of the display will appear again from the bottom (or the top) (this function is called lap-around). In a 4-line crystal liquid display, only the lap-around function can be performed. Vertical smooth scroll is controlled by incrementing or decrementing the display line (SN1/0), which indicates which line to start from, and the display raster-row (SL0 to SL3). For example, when performing smooth scroll up, the display raster-row (SL0 to SL3) is incremented from 0000 to 1100 in order to scroll 12 raster-rows. Moreover, by incrementing the display line (SN1/0) and then incrementing the display raster-row from 0000 to 1100 again, a total of 25 raster-rows can be scrolled. Since the DD RAM is only 80 bytes, its data must be rewritten when performing continuous scroll exceeding this capacity.

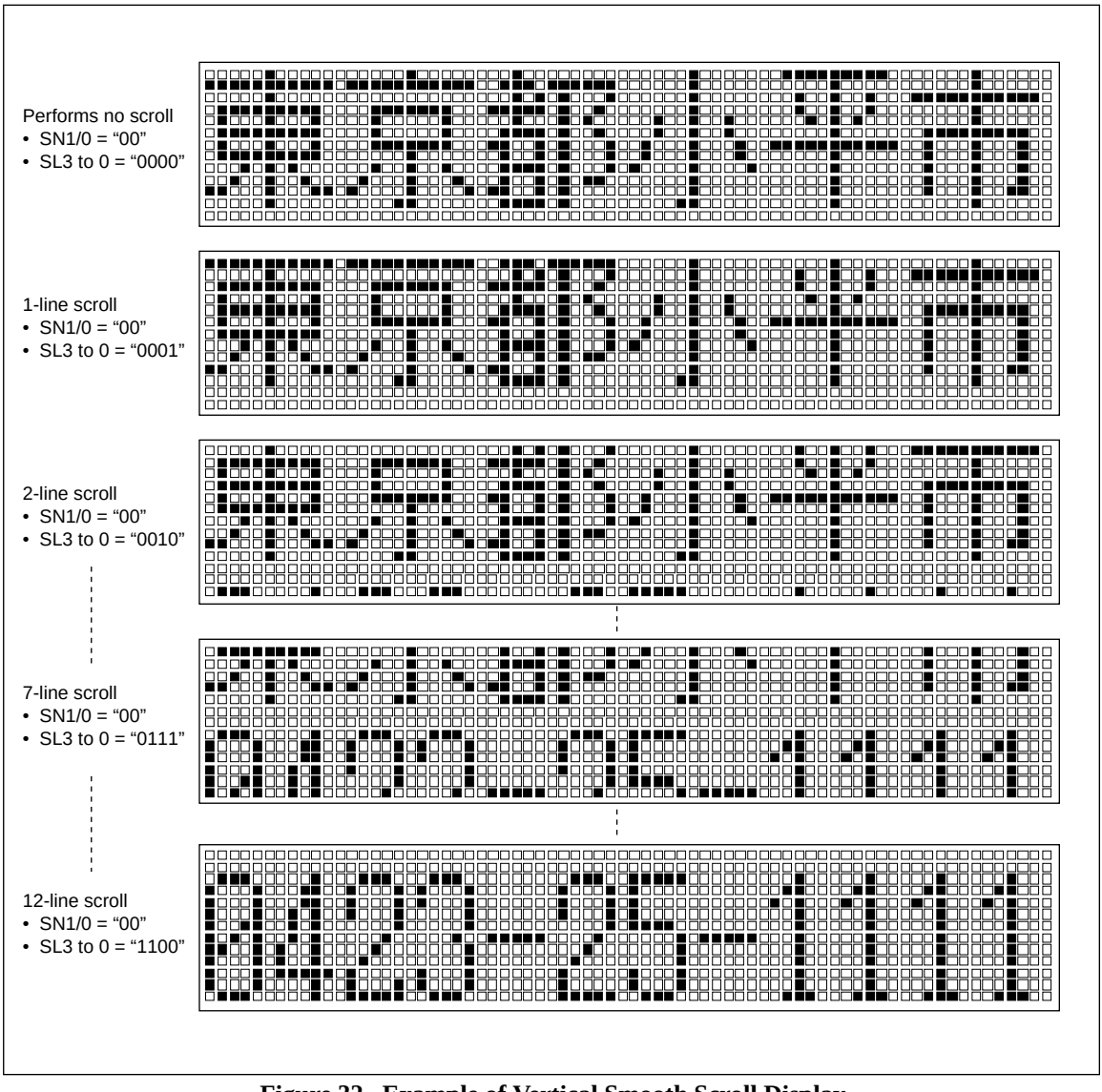
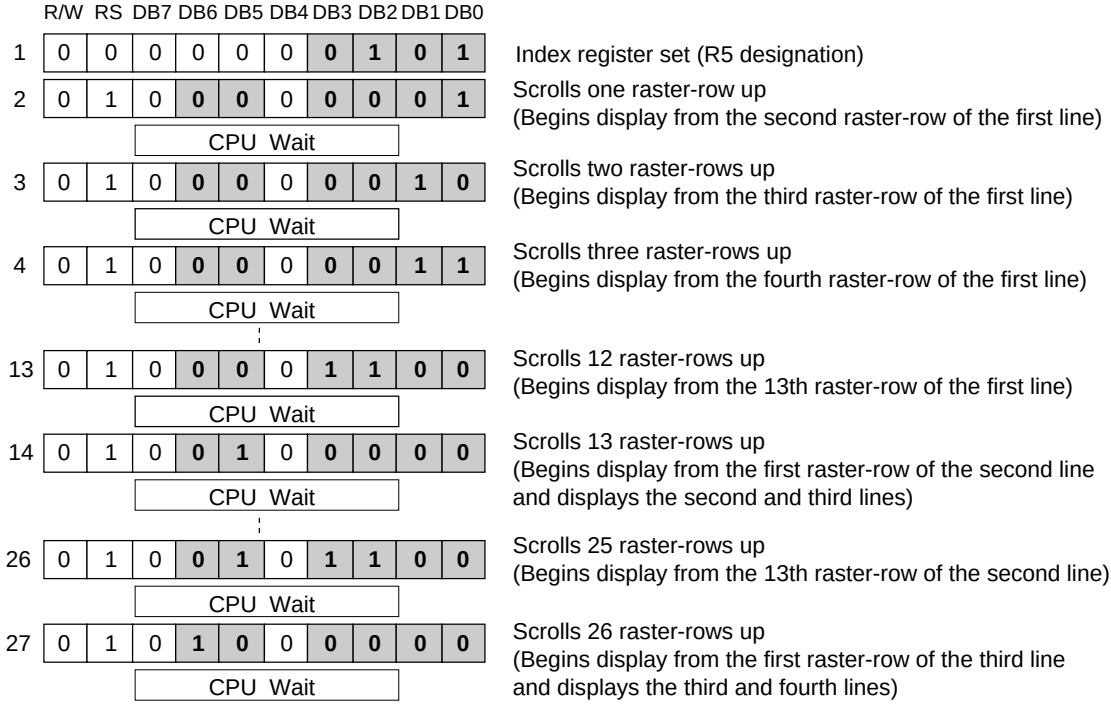


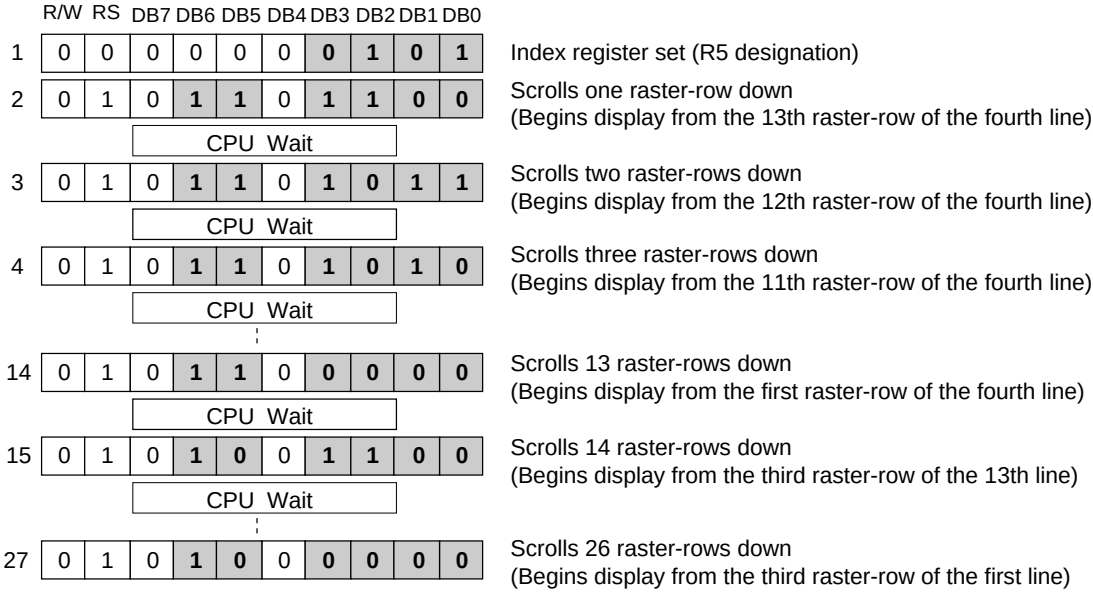
Figure 32 Example of Vertical Smooth Scroll Display

Examples of Register Setting (2-Line Liquid Crystal Drive: DT1/0 = 01, 4-Line Display Mode: NL1/0 = 11)



Note: The DD RAM has 80 bytes. For a 4-line display mode, a 4-line 10-character/line display can therefore be performed. Although the line and raster-row for scrolling can be designated as desired, the first raster-row of the first line will be displayed after displaying raster-row 13 of line 4.

Figure 33 Example of Performing Smooth Scroll Up



Note: The DD RAM has 80 bytes. For a 4-line display mode, a 4-line 10-character/line display can therefore be performed. Although the line and raster-row for scrolling can be designated as desired, the first raster-row of the first line will be displayed after displaying raster-row 13 of line 4.

Figure 34 Example of Performing Smooth Scroll Down

Extension Driver LSI Interface

The HD66730 can interface with extension drivers using extension driver interface signals CL1, CL2, D, and M output from the HD66730, increasing the number of display characters (figure 35). Although the liquid crystal driver voltage that drives the booster of the HD66730 can also be used as the driver power supply of extension drivers, the output voltage drop of the booster increases as the load of the booster increases.

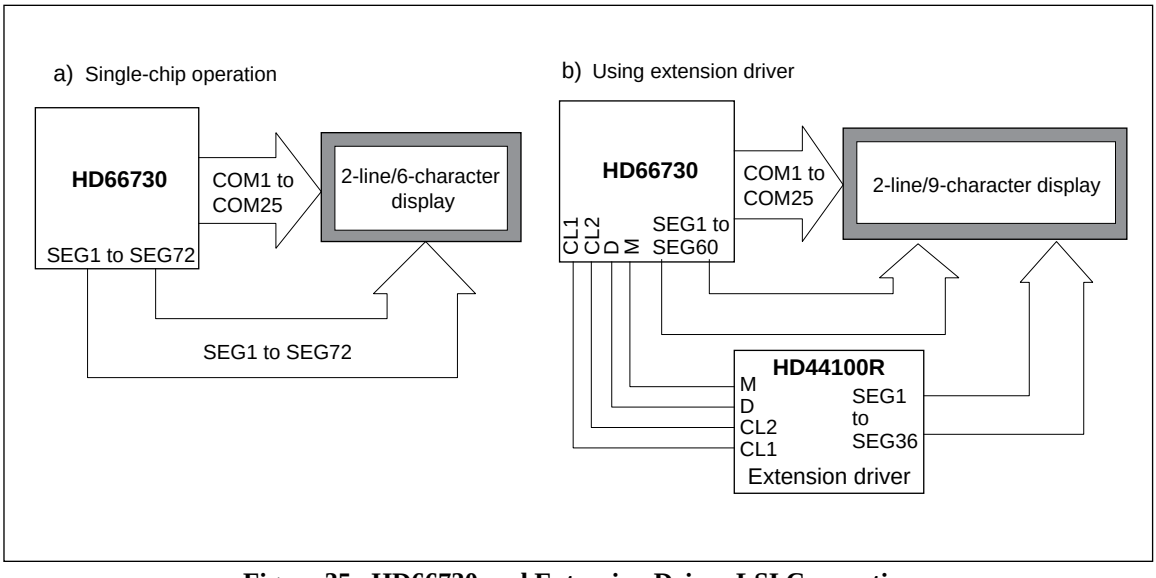


Figure 35 HD66730 and Extension Driver LSI Connection

Relationship between the Display Position at Extension Display and the Display Data RAM (DD RAM) Address

During 1-line display mode, up to 40 characters can be displayed by using extension drivers. In this case, DD RAM addresses H'00 to H'4F are allocated to each display position. During 2-line display, up to 20 characters can be displayed by using extension drivers. DD RAM addresses H'00 to H'27 are allocated to the first line and H'40 to H'67 to the second. See figure 36.

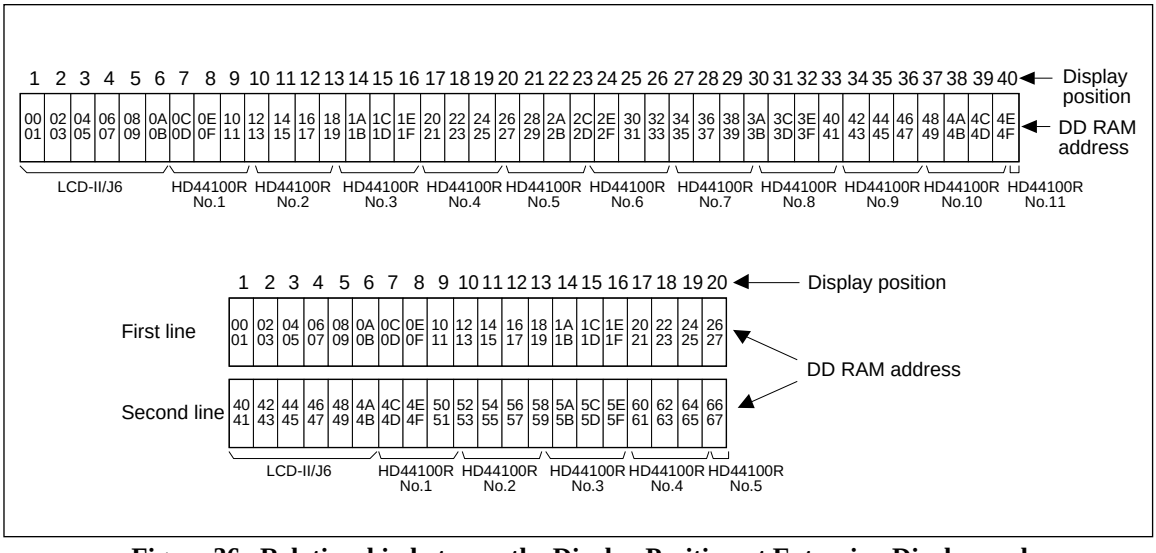


Figure 36 Relationship between the Display Position at Extension Display and the Display Data RAM (DD RAM) Address

Interfacing with the Liquid Crystal Panel

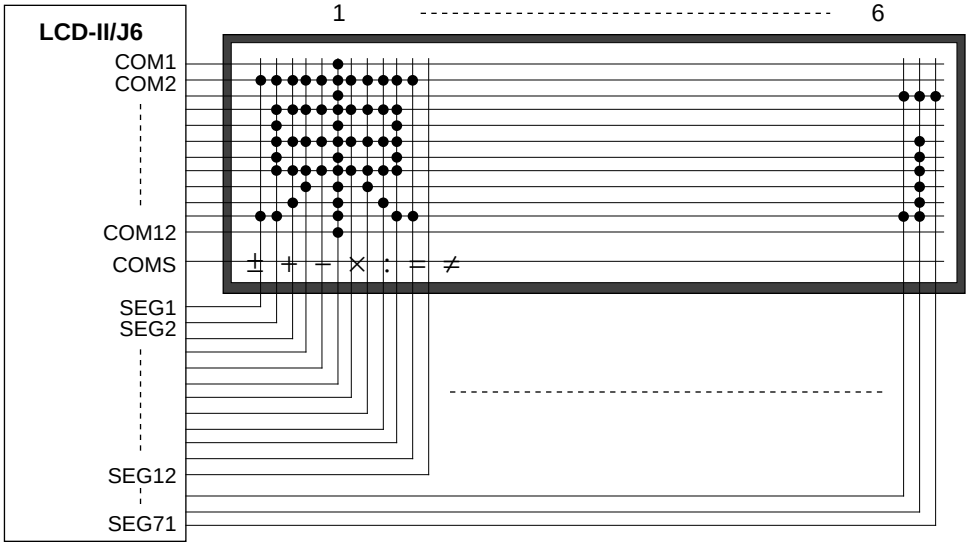
By connecting the HD66730 to extension drivers, the display can be expanded up to a 1-line/40-character, 2-line/20-character, or a 4-line/10-character display configuration. Bits DT1/0 set the duty drive ratio and bits NC1/0 set the number of characters per line. In addition, bits NL1/0 sets the number of display lines during display read control. Table 22 shows the relationship between the number of characters actually displayed on the liquid crystal panel and the corresponding number of extension drivers needed.

Table 22 Relationship between the Number of Liquid Crystal Display Characters and Extension Drivers

	Number of Display Characters per Line						
Display Lines	**6 Characters**	**10 Characters**	**12 Characters**	**16 Characters**	**20 Characters**	**40 Characters**	**Duty Drive**
1 line	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	(11/0)	1/14
2 lines	(0/0)	(2/0)	(2/0)	(3/0)	(5/0)	Display disabled	1/27
3 lines	(0/1)	(2/1)	Display disabled	Display disabled	Display disabled	Display disabled	1/40
4 lines	(0/1)	(2/1)	Display disabled	Display disabled	Display disabled	Display disabled	1/53

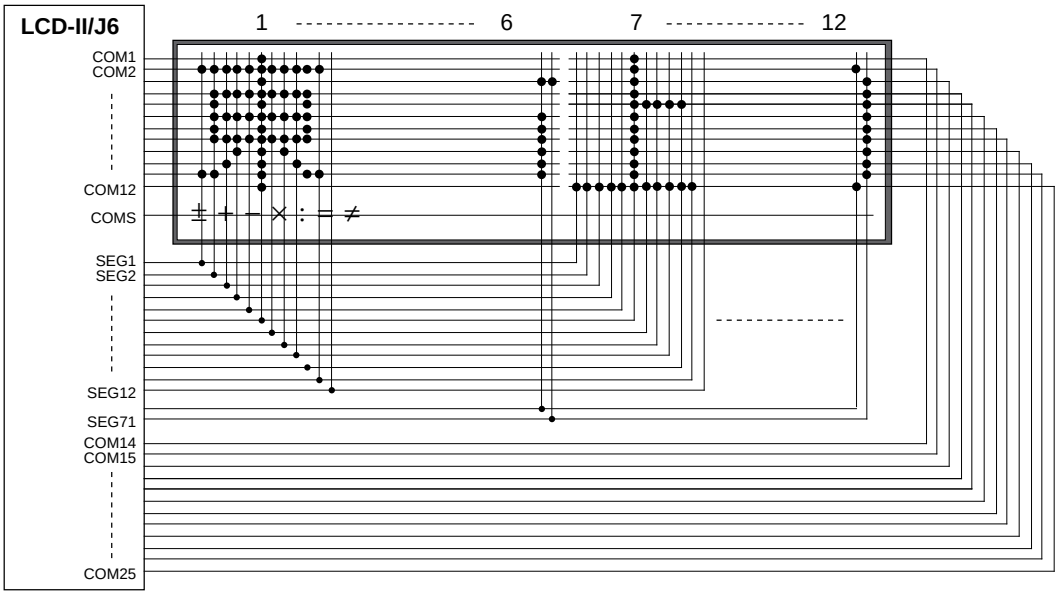
Notes:
1. Numbers in parentheses = (number of extension segment drivers/number of common drivers)
2. This is an example when using the HD44100R (40 output extension drivers), and when Nh represents display characters and Nd extension driver outputs, the number of extension drivers needed can generally be calculated as follows:
   [Number of extension drivers] = (12 * Nh – 71 – 1)/Nd] ↑
3. The right-edge segment (space between characters) is not displayed in 6-character or 16-character display.
4. Horizontal smooth scroll cannot be performed during an 1-line/40-character, 2-line/20-character, 3-line/10-character, or 4-line/10-character display.

Example of Interfacing with a 1-Line Display Panel



Note: The rightmost dot-column space of the 6th character cannot be displayed.

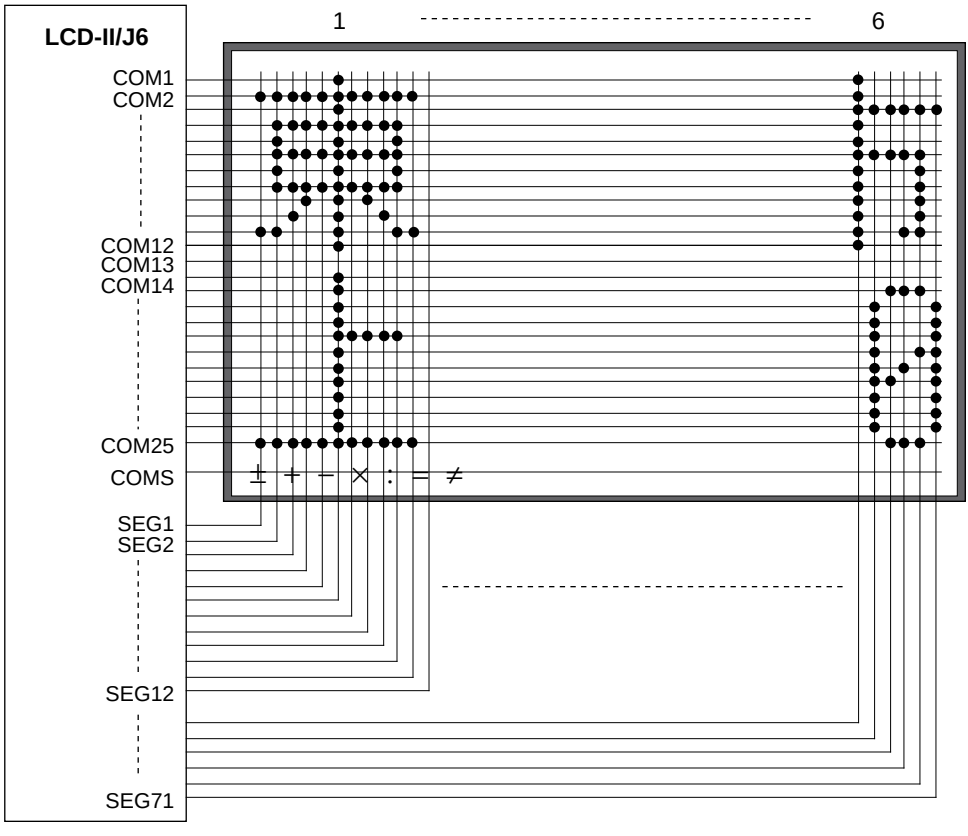
Figure 37 Example of 1-Line/6-Character + 71-Segment Display (Using 1/14 Duty)



Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.
2. The above figure shows how a liquid crystal panel can be arranged into a 1-line/12-character display while operating the HD66730 in 2-line/6-character display mode. Although the duty ratio becomes high, extension drivers will not be needed. COM13 for spaces between display lines will not be needed.

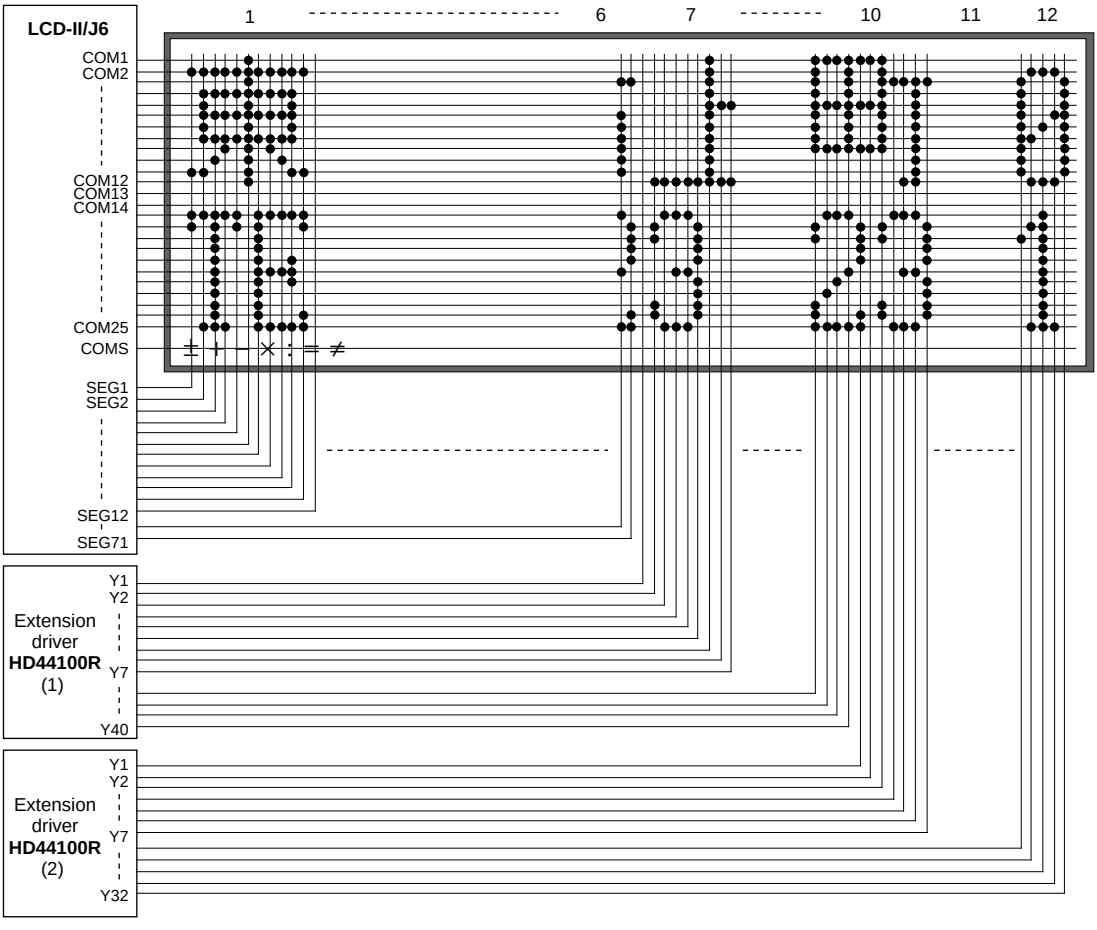
Figure 38 Example of 1-Line/12-Character + 71-Segment Display (Using 1/27 Duty)

Example of Interfacing with a 2-Line Display Panel



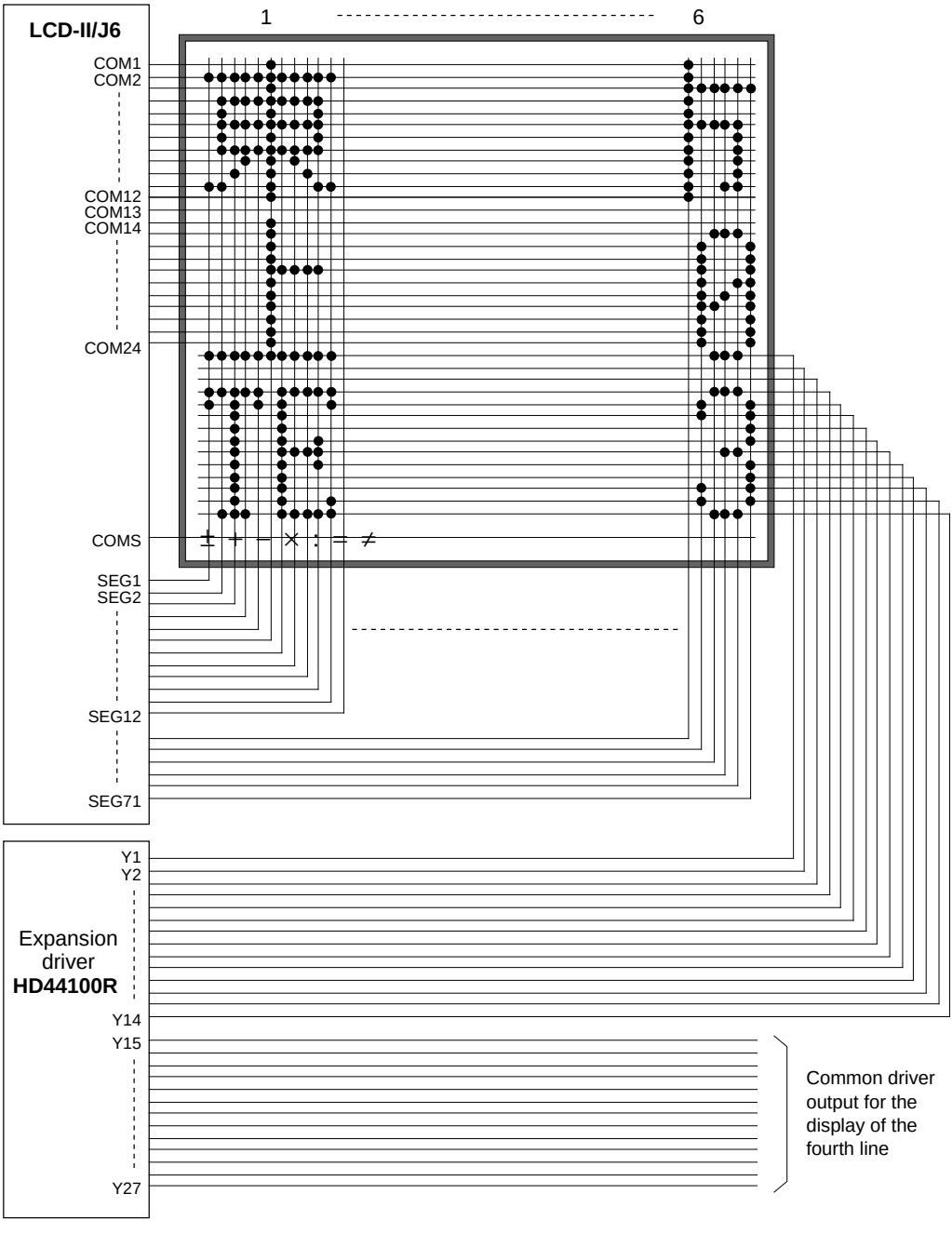
Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.
2. When performing vertical smooth scroll, or displaying double-size characters or graphic figures by the CG RAM, COM13 can be used for spaces between lines. Display can be performed continuously vertically.

Figure 39 Example of 2-Line/6-Character + 71-Segment Display (Using 1/27 Duty)



Note: COM13 is used for the space between the first line and the second line.

Figure 40 Example of 2-Line/12-Character + 96-Segment Display (Using 1/27 Duty)



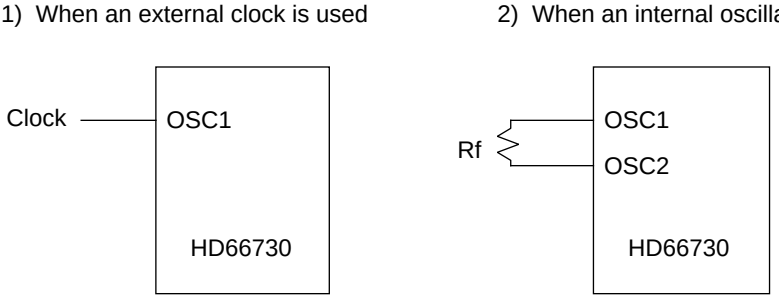
Notes: 1. The rightmost dot-column space of the 6th character cannot be displayed.

2. When performing vertical smooth scroll, or displaying double-size characters or graphic figures by the CG RAM, COM13 is used for spaces between lines. Display can be performed continuously vertically.
3. HD44100 output usage: Y1 = 12th raster-row of the second line, Y2 = space between lines, Y3 to Y4 = third-line characters, Y15 = space between lines, Y16 to Y27 = fourth-line characters

Figure 41 Example of 3-Line/6-Character + 71-Segment Display (Using 1/40 Duty) (Example of 4-Line/6-Character + 71-Segment Display (Using 1/53 Duty))

Oscillator

Figure 42 shows the optimal value of the oscillation frequency or the external clock frequency depends on the duty drive ratio setting (DT1/0), number of display lines (NL1/0), and the number of display characters (NC1/0) in the HD66730. The oscillation frequency or the external clock frequency must be adjusted according to the frame frequency of the liquid crystal drive.



Note: The oscillator frequency can be adjusted by an oscillator resistor (Rf). Refer to Electrical Characteristics for the relationship between the oscillator resistor (Rf) and the oscillator frequency. If Rf is increased or power supply voltage is decreased, the oscillator frequency decreases.

Figure 42 Oscillator Connections

Relationship between the Oscillation Frequency and the Liquid Crystal Display Frame Frequency

Figures 43 to 46 and tables 23 to 26 show the oscillation frequency and the external clock frequency for various registor settings when the frame frequency is 80 Hz.

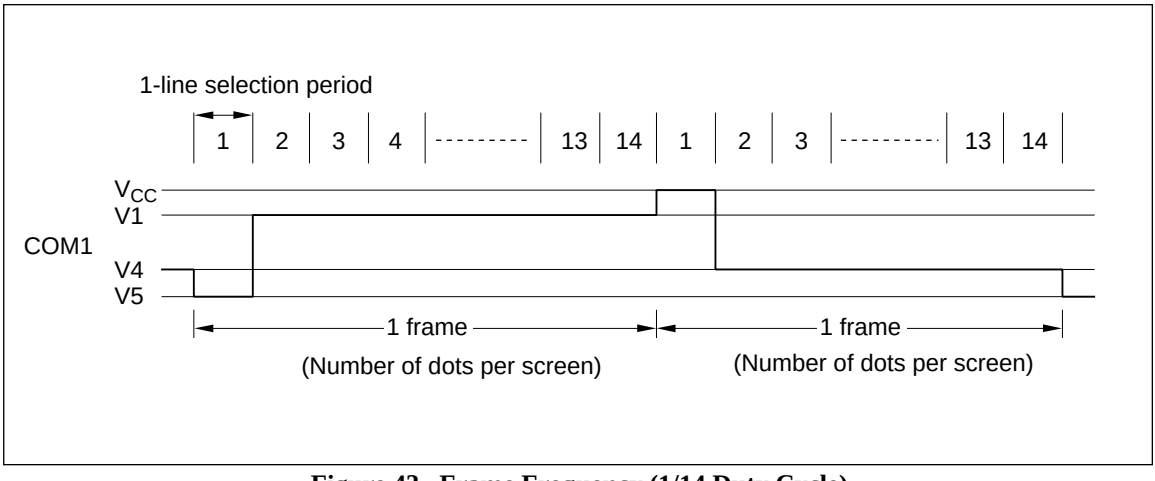


Figure 43 Frame Frequency (1/14 Duty Cycle)

Table 23 1/14 Duty Drive

Number of Display Lines:	**1-Line Display**		
(NL1/0 Set Value):	**(00)**		
Number of display characters	6 characters	20 characters	40 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	240 dots	480 dots
Number of dots per screen (kHz)	1008 dots	3360 dots	6720 dots
Oscillation frequency (kHz)*	80	270	540

Number of Display Lines:	**2-line Display**		
(NL1/0 Set Value):	**(01)**		
Number of display characters	6 characters	20 characters	40 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (kHz)	1008 dots	1680 dots	3360 dots
Oscillation frequency (kHz)*	80	270	540

Number of Display Lines:	**4-Line Display**	
(NL1/0 Set Value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	1008 dots	1680 dots
Oscillation frequency (kHz)*	80	270

Note: * The frequencies in table 23 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that a optimum frame frequency can be obtained.

1/27 Duty Cycle (DT1/0 = 01: 2-Line Drive)

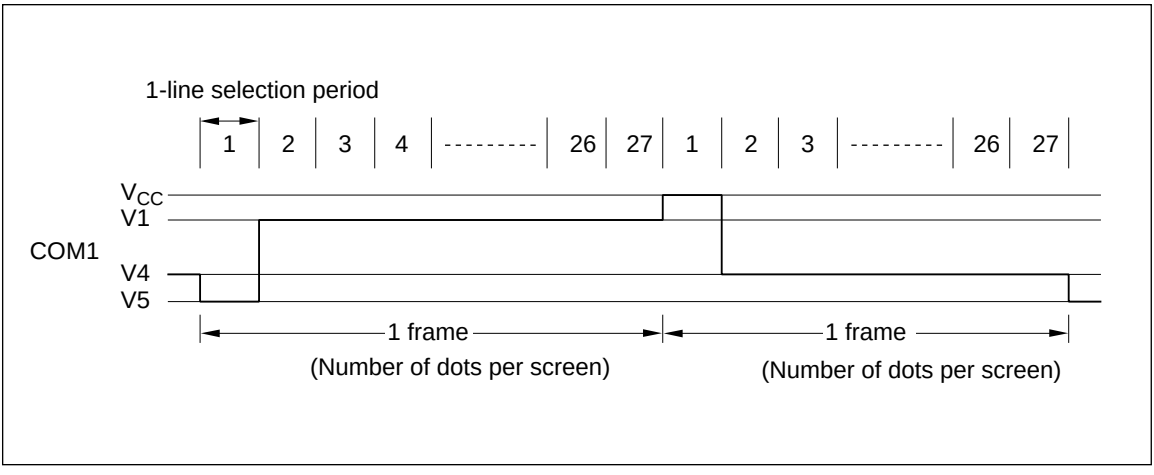


Figure 44 Frame Frequency (1/27 Duty Cycle)

Table 24 1/27 Duty Drive

Number of Display Lines:	**2-Line Display**		
(NL1/0 Set Value):	**(01)**		
Number of display characters	6 characters	10 characters	20 characters
(NC1/0 set value)	(00)	(01)	(11)
1-line selection period (dot)	72 dots	120 dots	240 dots
Number of dots per screen (kHz)	1944 dots	3240 dots	6480 dots
Oscillation frequency (kHz)*	155	260	520

Number of Display Lines:	**4-Line Display**	
(NL1/0 Set Value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	1944 dots	3240 dots
Oscillation frequency (kHz)*	155	260

Note: * The frequencies in table 24 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

1/40 Duty Cycle (DT1/0 = 10: 3-Line Drive)

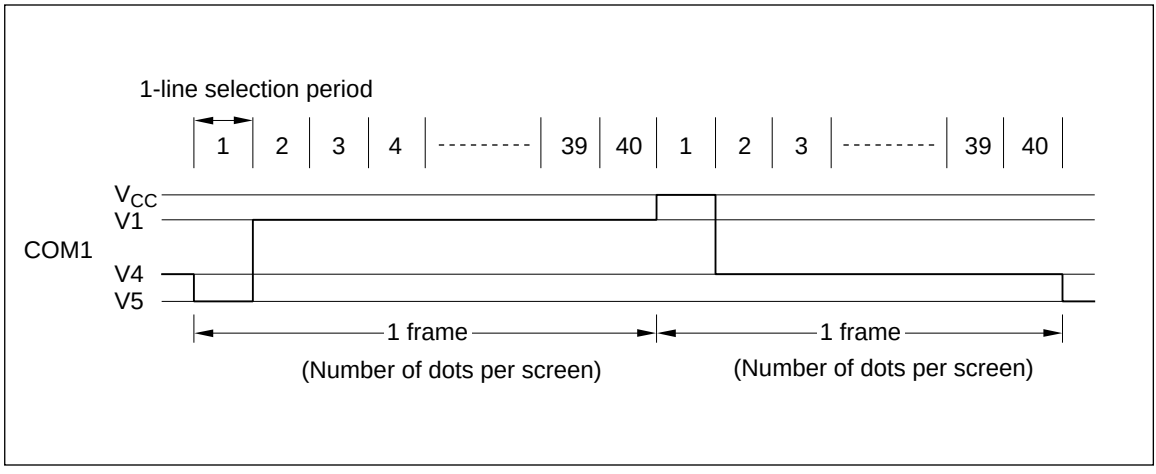


Figure 45 Frame Frequency (1/40 Duty Cycle)

Table 25 1/40 Duty Drive

Number of Display Lines:	**4-Line Display**	
(NL1/0 set value):	**(11)**	
Number of display characters	6 characters	10 characters
(NC1/0 set value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	2880 dots	4800 dots
Oscillation frequency (kHz)*	230	385

Note: * The frequencies in table 25 are examples when the frame frequency is set to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

1/53 Duty Cycle (DT1/0 = 11: 4-Line Drive)

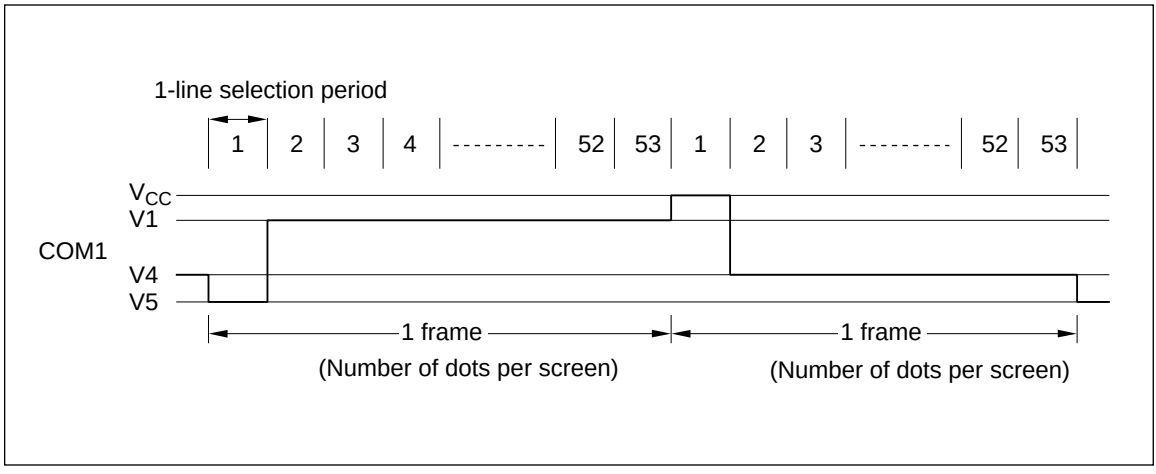


Figure 46 Frame Frequency (1/53 Duty Cycle)

Table 26 1/53 Duty Drive

Number of Display Lines:	**4-line Display (11)**	
(NL1/0 Setting Value):	**(00)**	**(01)**
Number of display characters	6 characters	10 characters
(NC1/0 setting value)	(00)	(01)
1-line selection period (dot)	72 dots	120 dots
Number of dots per screen (kHz)	3816 dots	6360 dots
Oscillation frequency (kHz)*	305	510

Note: * The frequencies in table 26 are examples when the frame frequency was is to 80 Hz. Adjust the oscillation frequency so that an optimum frame frequency can be obtained.

Power Supply for Liquid Crystal Display Drive

The HD66730 incorporates a booster for raising the LCD voltage two or three times that of the reference voltage input below V_{CC} (figure 47). A two or three times boosted voltage can be obtained by externally attaching two or three 1-µF capacitors.

If the LCD panel is large and needs a large amount of drive current, the values of bleeder resistors that generate the V1 to V5 potential are made smaller. However, the load current in the booster and the voltage drop increases in this case.

We recommend setting the resistance value of each bleeder larger than 4.7 kW and to hold down the DC load current to 0.4 mA if using a booster circuit. An external power supply should supply LCD voltage if the DC load current exceeds 0.7 mA (figure 48). Refer to Electrical Characteristics showing the relationship between the load current and booster voltage output. Table 27 shows the duty factor and bleeder resistor value for power supply for liquid crystal display drive.

Table 27 Duty Factor and Bleeder Resistor Value for Power Supply for Liquid Crystal Display Drive

Item		Data			
Drive lines (DT1/0 setting value)		1	2	3	4
Duty factor		1/14	1/27	1/40	1/53
Bias		1/4.7	1/6.2	1/7.3	1/8.3
Bleeder resistance value	R1	R	R	R	R
	R0	R*0.7	R*2.2	R*3.3	R*4.3

Note: * R changes depending on the size of a liquid crystal panel. Normally, R must be 5 kΩ to 10 kΩ. Adjust R to the optimum value with the consumption current and display picture quality.

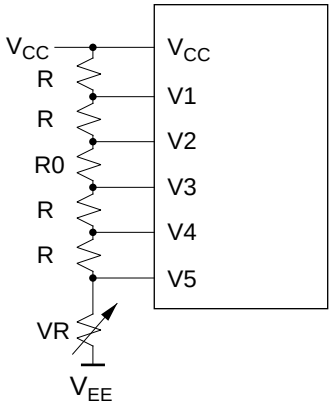
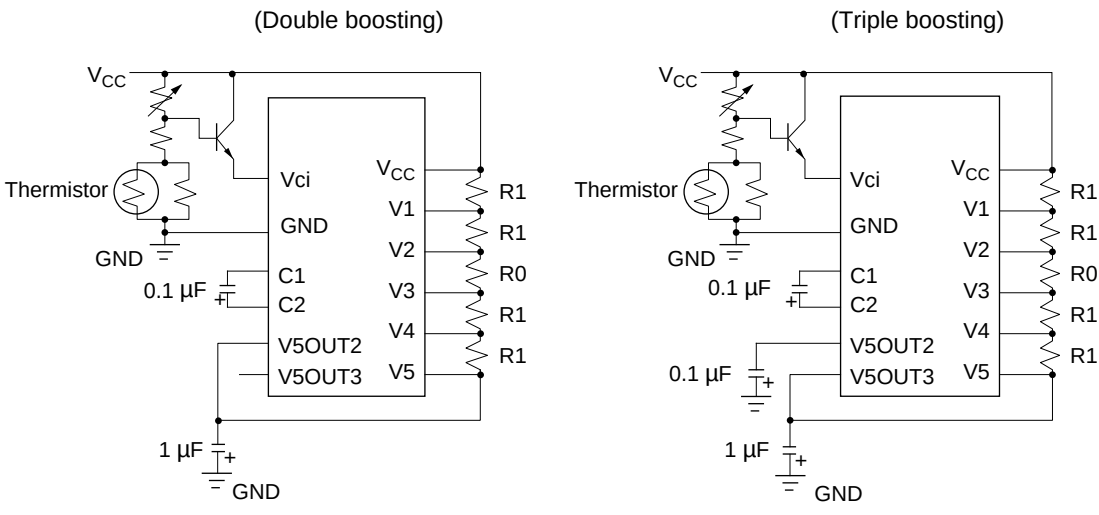


Figure 47 Example of Power Supply for Liquid Crystal Display Drive (with External Power Supply)



Notes:
1. The reference voltage input (Vci) must be set below the power supply (V_{CC}).
2. Current that flows into reference voltage input (Vci) is 2-3 times larger than the load current flowing through bleeder resistors. Note that a reference voltage drop occurs due to the current flowing into the Vci input when a reference voltage (Vci) is generated by resistor division.
3. The amount of output voltage (V5OUT2/V5OUT3) drop of a booster circuit also increases as the load current flowing through bleeder resistors increases. Thus, set the bleeder resistance as large as possible (4.7 kW or greater) without affecting display picture quality.
4. Adjust the reference voltage input (Vci) according to the fluctuation of booster characteristics because the output voltage (V5OUT2/V5OUT3) drop depends on the load current, operation temperature, operation frequency, capacitance of external capacitors, and manufacturing tolerance. Refer to Electrical Characteristics for details.
5. Adjust the reference voltage input (Vci) so that the output voltage (V5OUT2/V5OUT3) after boosting will not exceed the absolute maximum rating of liquid crystal power supply voltage (15 V).
6. Make sure that you connect polarized capacitors correctly.

Figure 48 Example of Power Supply for Liquid Crystal Display Drive (with Internal Booster)

Absolute Maximum Ratings*

Item	Symbol	Value	Unit	Notes
Power supply voltage (1)	V_{CC}	–0.3 to +7.0	V	1
Power supply voltage (2)	V_{CC}–V5	–0.3 to +17.0	V	1, 2
Input voltage	V_t	–0.3 to V_{CC} + 0.3	V	1
Operating temperature	T_{opr}	–20 to +75	°C	3
Storage temperature	T_{stg}	–55 to +125	°C	4

Note: * If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

DC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes
Input high voltage (1) (except OSC1)	V_{IH1}	$0.7V_{CC}$	—	V_{CC}	V		5, 6
Input low voltage (1) (except OSC1)	V_{IL1}	–0.3	—	$0.2V_{CC}$	V	V_{CC} = 2.7 to 3.0 V	5, 6
		–0.3	—	0.6	V	V_{CC} = 3.0 to 4.5 V	
Input high voltage (2) (OSC1)	V_{IH2}	$0.7V_{CC}$	—	V_{CC}	V		15
Input low voltage (2) (OSC1)	V_{IL2}	—	—	$0.2V_{CC}$	V		15
Output high voltage (1) (D0–D7)	V_{OH1}	$0.75V_{CC}$	—	—	V	$–I_{OH}$ = 0.1 mA	7
Output low voltage (1) (D0–D7)	V_{OL1}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.1 mA	7
Output high voltage (2) (except D0–D7)	V_{OH2}	$0.8V_{CC}$	—	—	V	$–I_{OH}$ = 0.04 mA	8
Output low voltage (2) (except D0–D7)	V_{OL2}	—	—	$0.2V_{CC}$	V	I_{OL} = 0.04 mA	8
Driver ON resistance (COM)	R_{COM}	—	—	20	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
Driver ON resistance (SEG)	R_{SEG}	—	—	30	kΩ	±Id = 0.05 mA, V_{LCD} = 4 V	13
I/O leakage current	I_{LI}	–1	—	1	µA	V_{IN} = 0 to V_{CC}	9
Pull-up MOS current (RESET* pin)	$–I_p$	5	50	120	µA	V_{CC} = 3 V Vin = 0 V	
Power supply current	I_{CC}	—	0.15	0.30	mA	R_f oscillation, external clock V_{CC} = 3 V, f_{OSC} = 270 kHz	10, 14
LCD voltage	V_{LCD}	3.0	—	15.0	V	V_{CC}–V5, 1/4.7 bias	16

Booster Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
Output voltage (V5OUT2 pin)	V_{UP2}	7.5	8.7	—	V	$V_{CC} = V_{ci} = 4.5$ V, $I_o = 0.25$ mA, C = 1 µF, $f_{OSC} = 270$ kHz, $T_a = 25°C$	18
Output voltage (V5OUT3 pin)	V_{UP3}	7.0	7.7	—	V	$V_{CC} = V_{ci} = 2.7$ V, $I_o = 0.25$ mA, C = 1 µF, $f_{OSC} = 270$ kHz, $T_a = 25°C$	18
Input voltage	V_{Ci}	2.0	—	5.0	V		18, 19

AC Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Clock Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C*3)

Item		Symbol	Min	Typ	Max	Unit	Test Condition	Notes*
External clock operation	External clock frequency	f_{cp}	80	270	700	kHz		11
	External clock duty	Duty	45	50	55	%		
	External clock rise time	t_{rcp}	—	—	0.2	µs		
	External clock fall time	t_{rcp}	—	—	0.2	µs		
R_f oscillation	Clock oscillation frequency	f_{OSC}	180	240	300	kHz	$R_f = 75$ kΩ, $V_{CC} = 3$ V	12

System Interface Timing Characteristics (1) (V_{CC} = 2.7 V to 4.5 V, T_a = –20 to +75°C*3)

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	1000	—	—	ns	Figure 49
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	0 (T.B.D.)	—	—		
Address hold time	t_{AH}	0 (T.B.D.)	—	—		
Data set-up time	t_{DSW}	195	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	1000	—	—	ns	Figure 50
Enable pulse width (high level)	PW_{EH}	450	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	25		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	0 (T.B.D.)	—	—		
Address hold time	t_{AH}	0 (T.B.D.)	—	—		
Data delay time	t_{DDR}	—	—	360		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 51
Serial clock (high level width)	t_{SCH}	400	—	—	ns	
Serial clock (low level width)	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{scr}, t_{scf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		
Serial output data delay time	t_{SOD}	—	—	360		
Serial output data hold time	t_{SOH}	5	—	—		

System Interface Timing Characteristics (2) (V_{CC} = 4.5 V to 5.5 V, T_a = –20 to +75°C[*3])

Bus Write Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 49
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data set-up time	t_{DSW}	80	—	—		
Data hold time	t_H	10	—	—		

Bus Read Operation

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Enable cycle time	t_{CYCE}	500	—	—	ns	Figure 50
Enable pulse width (high level)	PW_{EH}	230	—	—		
Enable rise/fall time	t_{Er}, t_{Ef}	—	—	20		
Address set-up time (RS, R/$\overline{W}$ to E)	t_{AS}	40	—	—		
Address hold time	t_{AH}	10	—	—		
Data delay time	t_{DDR}	—	—	160		
Data hold time	t_{DHR}	5	—	—		

Serial Interface Sequence

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	0.5	—	20	µs	Figure 51
Serial clock (high level width)	t_{SCH}	200	—	—	ns	
Serial clock (low level width)	t_{SCL}	200	—	—		
Serial clock rise/fall time	t_{scr}, t_{scf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	20	—	—		
Serial input data set-up time	t_{SISU}	100	—	—		
Serial input data hold time	t_{SIH}	100	—	—		
Serial output data delay time	t_{SOD}	—	—	160		
Serial output data hold time	t_{SOH}	5	—	—		

Segment Extension Signal Timing Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item		Symbol	Min	Typ	Max	Unit	Test Condition
Clock pulse width	High level	t_{CWH}	800	—	—	ns	Figure 52
	Low level	t_{CWL}	800	—	—		
Clock set-up time		t_{CSU}	500	—	—		
Data set-up time		t_{SU}	300	—	—		
Data hold time		t_{DH}	300	—	—		
M delay time		t_{DM}	–1000	—	1000		
COMD set-up time		t_{DSU}	300				
Clock rise/fall time	COMD	t_{ct1}	—	—	700		
	Pins except COMD	t_{ct2}	—	—	200		

Reset Timing Characteristics (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Reset low-level width	t_{RES}	10	—	—	ms	Figure 53

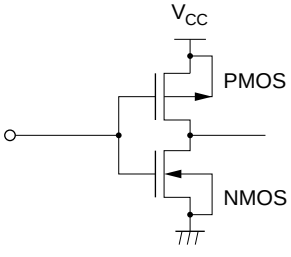
Power Supply Conditions (V_{CC} = 2.7 V to 5.5 V, T_a = –20 to +75°C[*3])

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Power supply rise time	t_{rcc}	0.1	—	10	ms	Figure 54
Power supply off time	t_{OFF}	1	—	—		

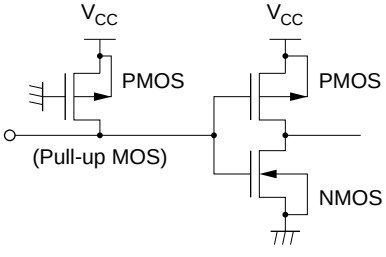
Electrical Characteristics Notes

1. All voltage values are referred to GND = 0 V. If the LSI is used above the absolute maximum ratings, it may become permanently damaged. Using the LSI within the electrical characteristic is strongly recommended to ensure normal operation. If these electrical characteristic are exceeded, the LSI may malfunction or exhibit poor reliability.
2. $V_{CC} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$ must be maintained.
3. For die products, specified up to 75°C.
4. For die products, specified by the die shipment specification.
5. The following four circuits are I/O pin configurations except for liquid crystal display output.

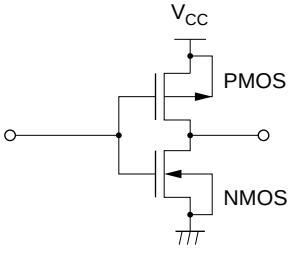
Input pin
Pin: E/SCLK, RS/CS*, RW/SID, IM,



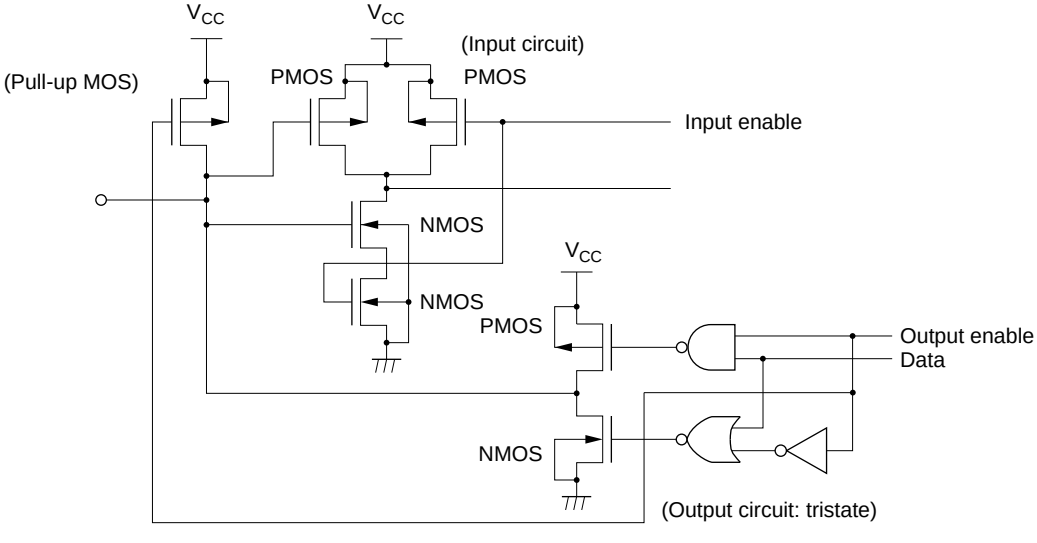
Input pin
Pins: RESET*



Output pin
Pins: CL1, CL2, M, SEGD



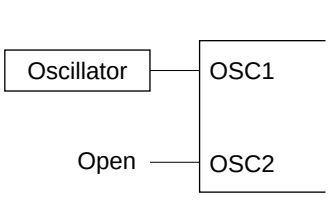
I/O Pin
Pins: DB0/SOD to DB7

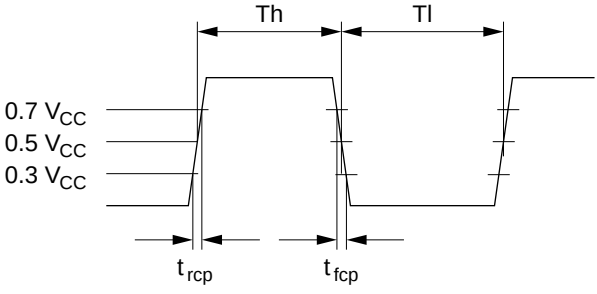


6. Applies to input pins and I/O pins, excluding the OSC1 pin.
7. Applies to I/O pins.
8. Applies to output pins.
9. Current flowing through pull-up MOSs, excluding output drive MOSs.

10. Input/output current is excluded. When input is at an intermediate level with CMOS, the excessive current flows through the input circuit to the power supply. To avoid this from happening, the input level must be fixed high or low.

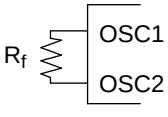
11. Applies only to external clock operation.





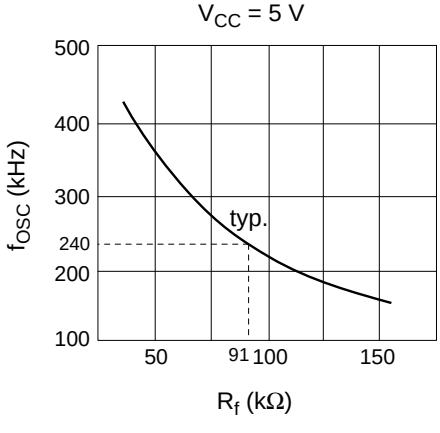
$$\text{Duty} = \frac{Th}{Th + Tl} \times 100\%$$

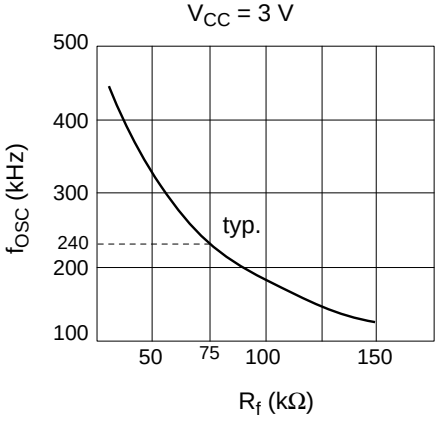
12. Applies only to the internal oscillator operation using oscillation resistor R_f.



Since the oscillation frequency varies depending on the I = OSC2 pin capacitance, the wiring length to these pins should be minimized.

Referential data

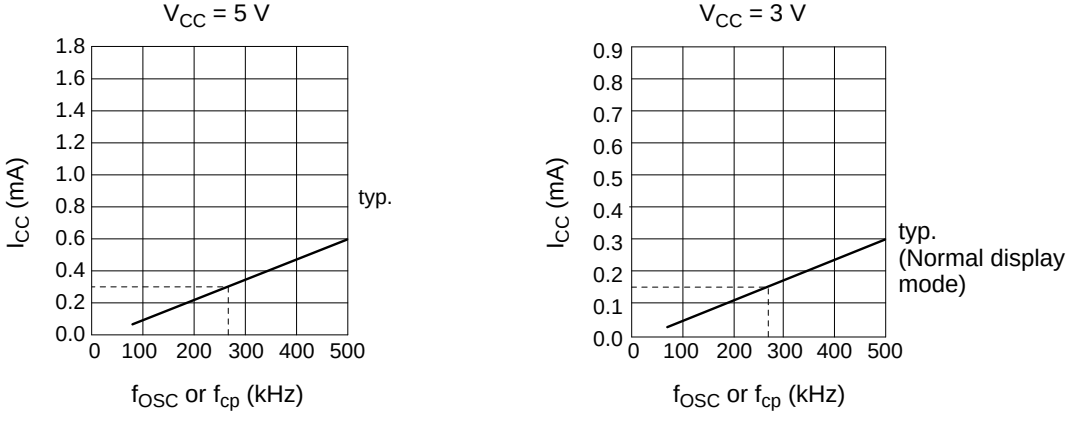




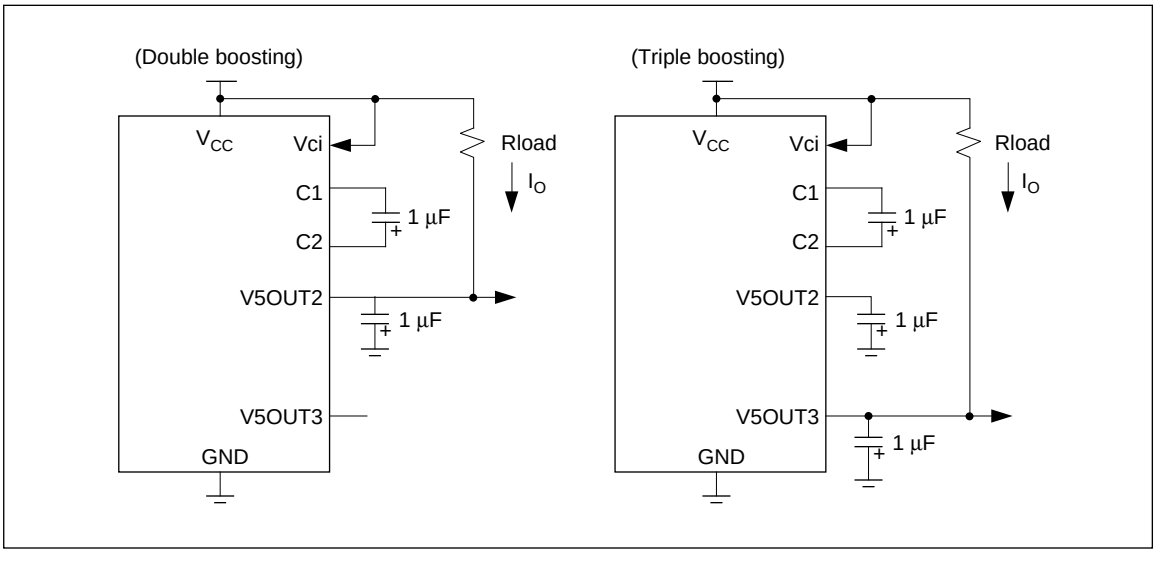
13. RCOM is the resistance between the power supply pins (V_{CC}, V1, V4, V5) and each common signal pin (COM0 to COM25).

    RSEG is the resistance between the power supply pins (V_{CC}, V2, V3, V5) and each segment signal pin (SEG1 to SEG71).

14. The following graphs show the relationship between operation frequency and current consumption (referential data).



15. Applies to the OSC1 pin.
16. Each COM and SEG output voltage is within ±0.15 V of the LCD voltage (V_{CC}, V1, V2, V3, V4, V5) when there is no load.
17. The TEST pin must be fixed to ground, and the IM pin must also be connected to V_{CC} or ground.
18. Booster characteristics test circuits are shown below.

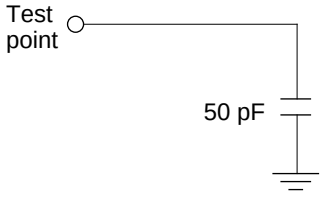


19. Vci ≤ V_{CC} must be maintained.

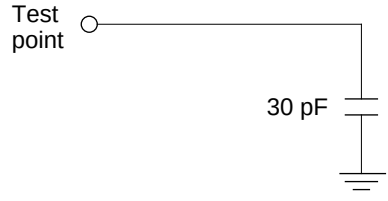
Load Circuits

AC Characteristics Test Load Circuits

Data bus: DB0 to DB7, SOD



Segment extension signals: CL1, CL2, SEGD, M, COM



Timing Characteristics

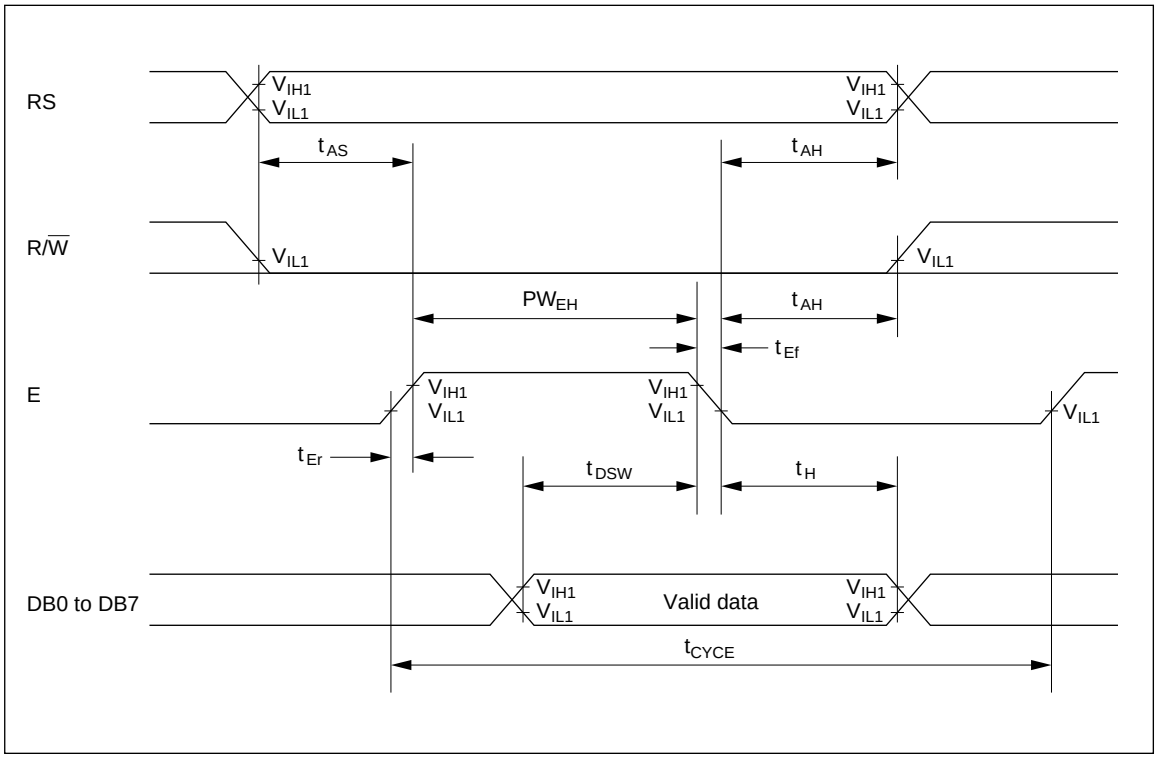


Figure 49 Bus Write Operation

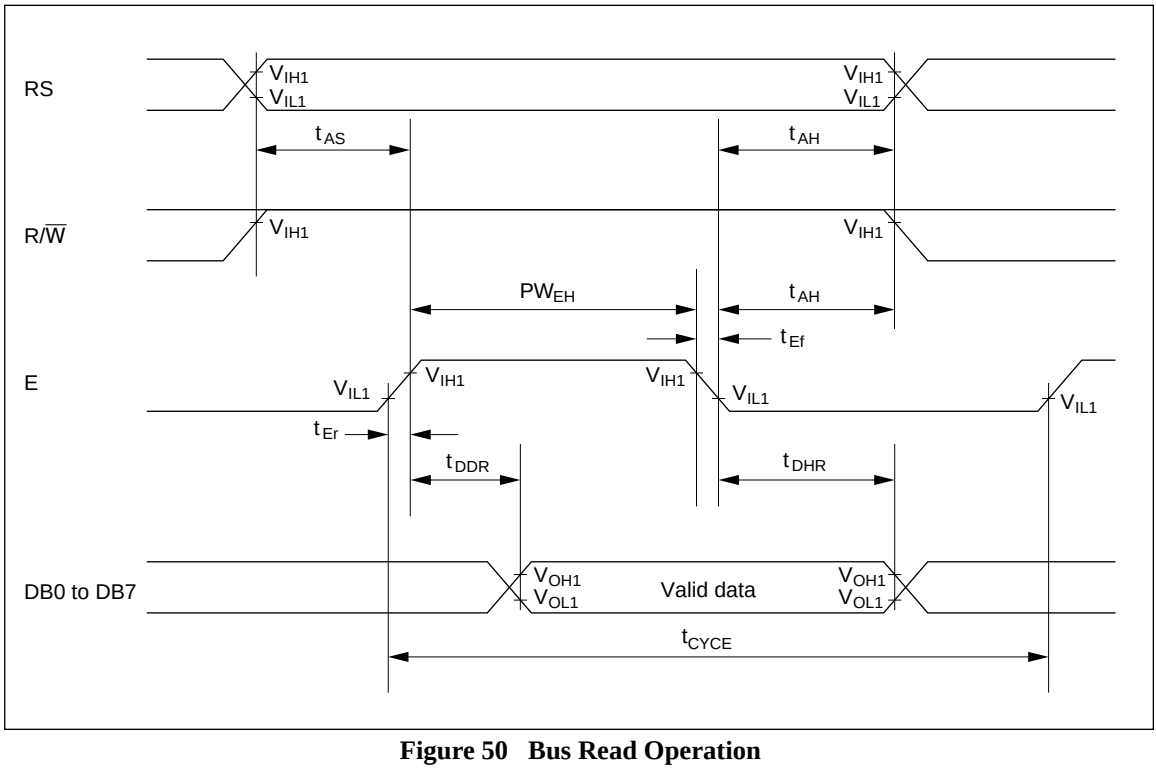


Figure 50 Bus Read Operation

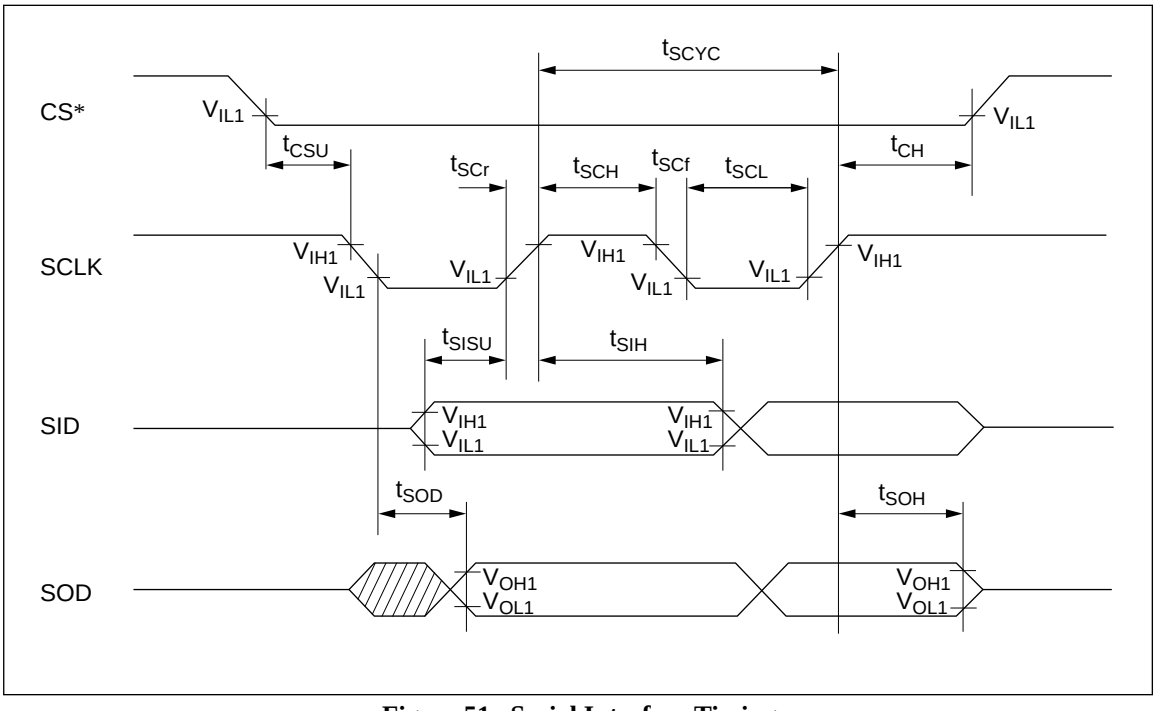


Figure 51 Serial Interface Timing

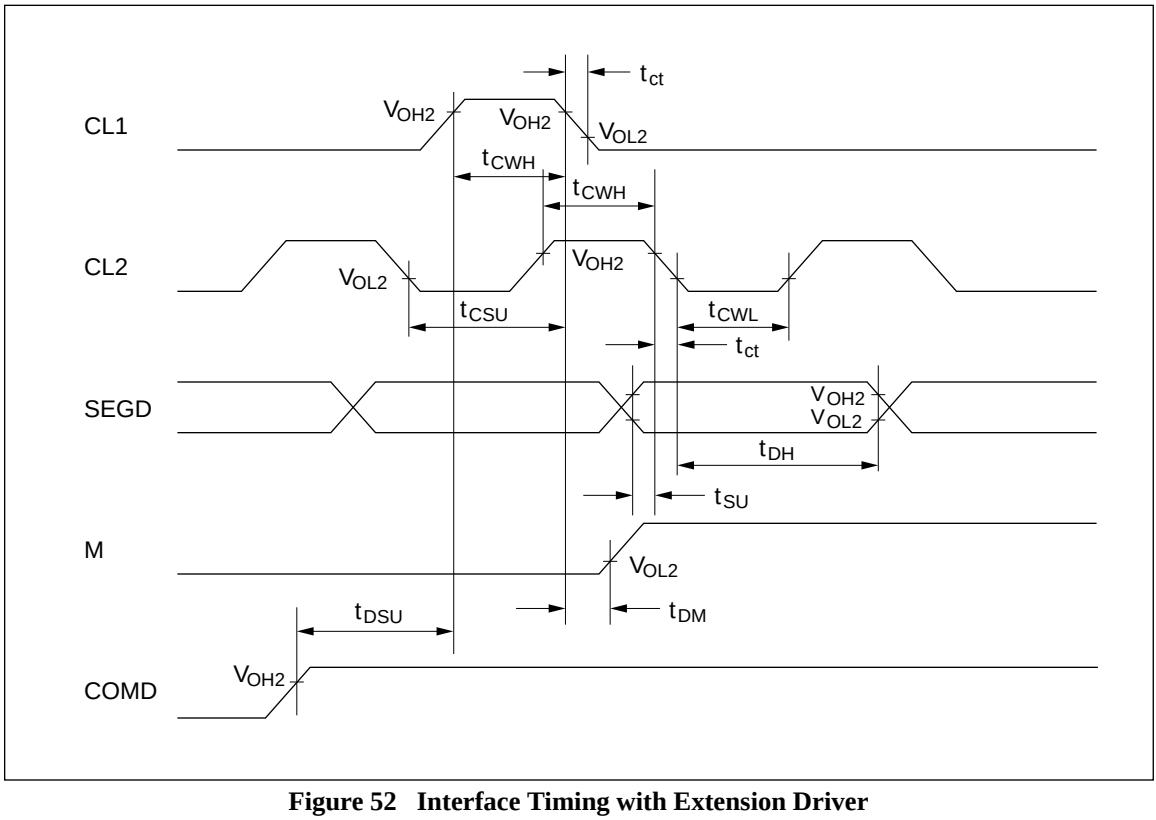
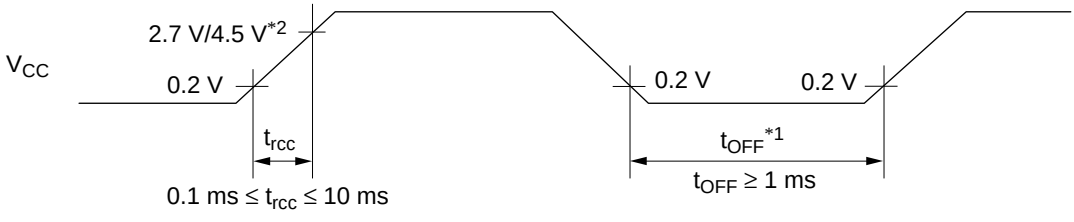


Figure 52 Interface Timing with Extension Driver

Figure 53 Reset Timing



Notes: 1. t_{OFF} compensates for the power oscillation period caused by momentary power supply oscillations.
2. Specified at 4.5 V for 5-volt operation, and at 2.7 V for 3-volt operation.

Figure 54 Power Supply Sequemce