HD66770

396-channel Source Driver with Internal RAM for TFT 65536-color Displays

HITACHI

Rev.1.1
April 2002

Description

The HD66770, 396-channel source driver LSI, displays 132RGB-by-176 dot graphics on TFT displays in 65,536 colors. It is for driving TFT color LCD displays to a maximum of 132RGB by 176 dots, in combination with the gate driver, HD66771 and Power supply IC, HD667P00. The HD66770's bit-operation functions, 16-bit high-speed bus interface, and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the graphics RAM.

The HD66770, HD66771 and HD667P00 have various functions for reducing the power consumption of a LCD system. HD66770 has a low-voltage operation (1.8 V min.) and an internal RAM to display a maximum of 132RGB-by-176 dot color, and the HD66771 has 288 pins of TFT gate wiring driver circuit. Also, HD667P00 has the internal booster that generates the liquid crystal voltage, breeder resistance and the voltage follower circuit for liquid crystal driver. HD66770 incorporates a circuit that interfaces with the HD66771/HD667P00, it can set instructions for HD66771/HD667P00. In addition, precise power control can be achieved by combining these hardware functions with software functions, such as an 8-color display and standby and sleep mode. This LSI is suitable for any medium-sized or small portable battery-driven product requiring long-term driving capabilities, such as digital cellular phones supporting a WWW browser, bi-directional pagers, and small PDAs.

Features

- 132RGB x 176-dot graphics display LCD controller/driver for 65,536 TFT colors (when HD66771/HD667P00 are used)
- 16-/8-bit high-speed bus interface and serial peripheral interface (SPI)
- High-speed burst-RAM write function
- Writing to a window-RAM address area by using a window-address function
- Bit-operation functions for graphics processing:
- Write-data mask function in bit units
- Logical operation in pixel unit and conditional write function
- Various color-display control functions:
- 65,536 colors can be displayed at the same time (gamma adjust included)
- Vertical scroll display function in raster-row units

- Low-power operation supports:
  - Vcc = 1.8 to 3.3 V (low-voltage range)
  - DDVDH = 4.5 to 5.5 V (liquid crystal drive voltage)
  - Power-save functions such as the standby mode and sleep mode
  - Partial LCD drive of two screens in any position
  - Maximum 12-times step-up circuit for liquid crystal drive voltage (HD667P00)
  - Voltage followers to decrease direct current flow in the LCD drive bleeder-resistors (HD66770)
- Built-in circuit for interfacing with the gate driver, HD66771 and Power supply IC, (HD667P00)
- Maximum 132RGB-by-176-dot display in combination with the HD66771 and HD667P00
- Internal RAM capacity: 46,464 bytes
- 396-source liquid crystal display driver
- n-raster-row inversion drive (It is possible to LCD driving voltage inversion reverse the polarity in every selected raster-row.)
- Internal oscillation and hardware reset
- Shift change of source driver

Type Numbers

Type Number	External Appearance
HCD667A70BP	Die with gold bump (Straight output arrangement)
HCD667B70BP	Die with gold bump (Laced output arrangement)

HD66770 Block Diagram Description

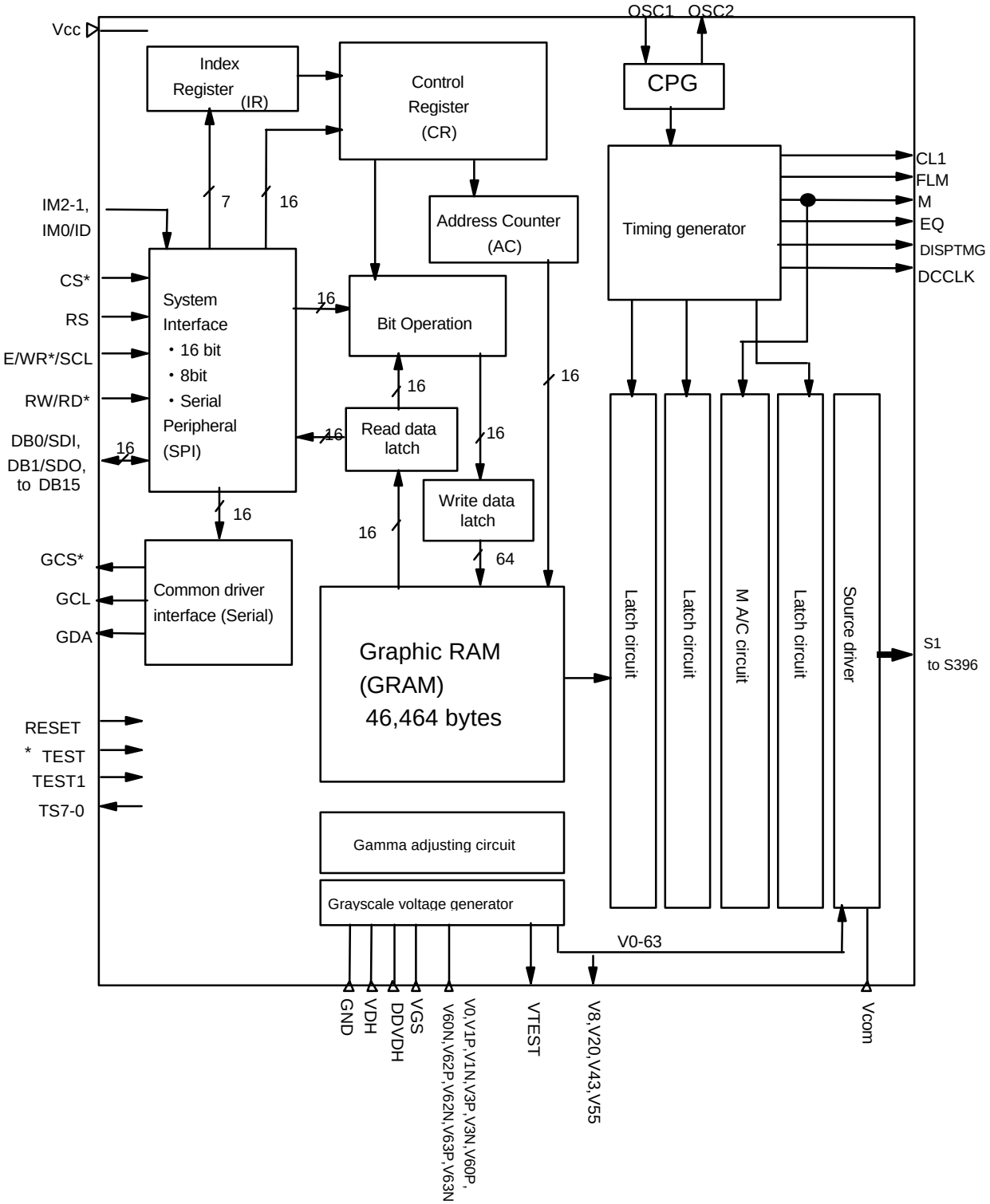


Figure 1: HD66770 Block Diagram Description

Pin Functions

Table 1 Pin Functional Description

Signals	Number of Pins	I/O	Connected to	Functions
IM2-1, IM0/ID	3	I	GND or V_{CC}	Selects the MPU interface mode: IM2 IM1 IM0/I MPU interface mode "GND" "GND" "GND" 68-system 16-bits bus interface "GND" "GND" "Vcc" 68-system 8-bit bus interface "GND" "Vcc" "GND" 80-system 16-bit bus interface "GND" "Vcc" "Vcc" 80-system 8-bit bus interface "Vcc "GND" ID Serial peripheral interface (SPI) When a serial interface is selected, the IM0 pin is used as the ID setting for a device code.
CS*	1	I	MPU	Selects the HD66770: Low: HD66770 is selected and can be accessed High: HD66770 is not selected and cannot be accessed Must be fixed at GND level when not in use.
RS	1	I	MPU	Selects the register. Low: Index/status High: Control
E/WR*/SCL	1	I	MPU	For a 68-system bus interface, serves as an enable signal to activate data read/write operation. For an 80-system bus interface, serves as a write strobe signal and writes data at the low level. For a synchronous clock interface, serves as the synchronous clock signal.
RW/RD*	1	I	MPU	For a 68-system bus interface, serves as a signal to select data read/write operation. Low: Write High: Read For an 80-system bus interface, serves as a read strobe signal and reads data at the low level.
DB0/SDI	1	I/O	MPU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as the serial data input pin (SDI). The input level is read on the rising edge of the SCL signal.
DB1/SDO	1	I/O	MCU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level. For a clock-synchronous serial interface, serves as a serial data output pin (SDO). Successive bit values are output on the falling edge of the SCL signal.
DB2-DB15	14	I/O	MPU	Serves as a 16-bit bi-directional data bus. For an 8-bit bus interface, data transfer uses DB15-DB8; fix unused DB7-DB0 to the Vcc or GND level.

(Continue to the Next page)

Signals	Number of Pins	I/O	Connected to	Functions
S1–S396	396	O	LCD	Output signals are for liquid crystal voltage. The SS bit can change the shift direction of the source signal. For example, if SS = 0, RAM address 0000 is output from S1. If SS = 1, it is output from S396. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
CL1	1	O	HD66771	The one-raster-row-cycle pulse is output.
M	1	O	HD667P00	The AC-cycle signal is output.
FLM	1	O	HD66771	The frame-start pulse is output.
EQ	1	O	HD667P00	Indicate setting of the Vcom output to its high-impedance state during transitions of Vcom when Vcom is being AC-cycled. Low: VcomH or VcomL is being output on the Vcom pin. High: Vcom pin is in high-impedance state
DISPTMG	1	O	HD66771	Gate off signal in the partial display “Low” : Output Voff signal “High” : Output normal signal
DCCLK	1	O	HD667P00	Outputs clock for the step-up circuit of HD667P00.
GCL	1	O	HD66771 HD667P00	Clock signal for a serial transfer of register setting values to the gate driver and the power supply IC. Data is output on the falling edge of this clock.
GDA	1	O	HD66771 HD667P00	Data signal for serial transfer as register setting values to the gate driver and The power supply IC.
GCS*	1	O	HD66771 HD667P00	Chip-select for the HD66771 and HD667P00. Low: the HD66771/HD667P00 are selected and can receive a serial transfer data. High: the HD66771/HD667P00 are not selected and cannot receive a serial transfer data.
DDVDH	1	I	HD667P00	Input power supply for LCD drive circuit, which can be provided by HD667P00. DDVDH : +4.5 to +5.5 V
VDH	1	I	HD667P00	This is the standard level of grayscale voltage generator, which can be provided by HD667P00. VDH (max.) : DDVDH – 0.5 V
Vcom	1	I	HD667P00	It is a signal for equalizing function. All LCD driver’s outputs (S1 to S396) are short to Vcom level (Hi-Z) in EQ = ”High” period. Must be left disconnected when VcomL < 0 V.
V_{CC}, GND	2	—	Power supply	V_{CC}: + 1.8 V to + 3.6 V; GND (logic): 0 V
OSC1, OSC2	2	I or O	Oscillation-resistor	Connect an external resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2.
RESET1* RESET2*	2	I	MPU or external R-C circuit	Reset pin. Initializes the LSI when low. Must be reset after power-on.

(Continue to the Next page)

Signals	Number of Pins	I/O	Connected to	Functions
VccDUM		O	Input pins	Outputs the internal V_{CC} level; shorting this pin sets the adjacent input pin to the V_{CC} level.
GNDDUM		O	Input pins	Outputs the internal GND level; shorting this pin sets the adjacent input pin to the GND level.
Dummy		—	—	Dummy pad. Must be left disconnected.
TEST	1	I	GND	Test pin. Must be fixed at GND level.
V0, V1P, V3P, V60P, V62P, V63P	6	I/O	Stabilized capacitor	When built-in op-amp is on (SAP2-0=”001”, “010”, “011”, “100”, “101”), it is for outputs of positive polar (V0 is for positive/negative polar) built-in op-amp. Connect condenser and stabilize the condition.
V1N, V3N, V60N, V62N, V63N	5	I/O	Stabilized capacitor	When built-in op-amp is on (SAP2-0=”001”, “010”, “011”, “100”, “101”), it is for outputs of negative polar built-in op-amp. Connect condenser and stabilize the condition.
V8, V20, V43, V55	4	O	Open	Test pin. Must be left disconnected.
VGS	1	I	GND or External resistor	This is the standard level of grayscale voltage generator. Connect external variable resistor when the level is adjusted for every panel with the source driver.
VTEST	1	O	Open	Test pin. Must be left disconnected.
TS0-TS7	8	O	Open	Test pin. Must be left disconnected.
TEST1	1	I	GND or Vcc	Test pin. Must be connected at GND or Vcc.

2001.2.28

HD667A70 PAD Arrangement

(Straight Output Arrangement)

- Chip Size: 15.06mm x 2.68mm
- Chip thickness: 550um (typ.)
- PAD coordinate: PAD center
- Coordinate origin: Chip center

- Au bump size:

(1) 80 um x 80 um

DUMMY1, DUMMY2, DUMMY3, DUMMY4
RESET1* to TS7
RESET1* to TS7

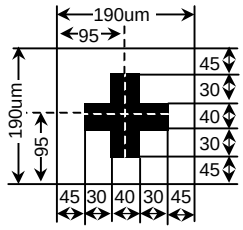
(2) 30 um x 80um
S338 to S59

(3) 80um x 35um
S396 to S355, S42 to S1

(4) 45um x 80um
S354 to S339, S58 to S43

- Au bump pitch: Refer to PAD coordinate
- Au bump height: 15 um (typ.)
- Number in the diagram refers to number on the PAD coordinate.
- Cross hairs

(1) Figure



(2) Arrangement: 2 places
(3) Coordinates (X, Y)
(7151, -1161) (-7151, -1161)

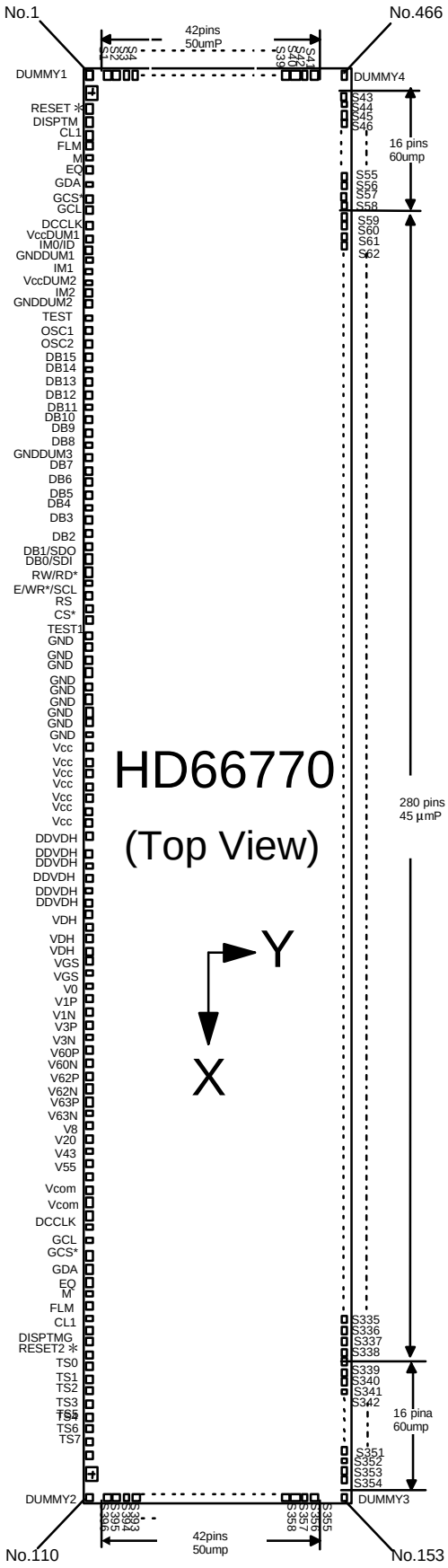


Figure 2: PAD Arrangement

HD66770PAD Coordinate (Straight) 2001.02.28 REV0.0

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-7398	-1208	66	DDVDH	1326	-1208	131	S376	7398	-25	196	S312	5108	1208
2	RESET1*	-6931	-1208	67	DDVDH	1426	-1208	132	S375	7398	25	197	S311	5063	1208
3	DISPTMG	-6780	-1208	68	VDH	1576	-1208	133	S374	7398	75	198	S310	5018	1208
4	CL1	-6630	-1208	69	VDH	1676	-1208	134	S373	7398	125	199	S309	4973	1208
5	FLM	-6480	-1208	70	VDH	1776	-1208	135	S372	7398	175	200	S308	4928	1208
6	M	-6330	-1208	71	VDH	1877	-1208	136	S371	7398	225	201	S307	4883	1208
7	EQ	-6180	-1208	72	VGS	2027	-1208	137	S370	7398	275	202	S306	4838	1208
8	GDA	-6030	-1208	73	VGS	2127	-1208	138	S369	7398	325	203	S305	4793	1208
9	GCS*	-5880	-1208	74	V0	2277	-1208	139	S368	7398	375	204	S304	4748	1208
10	GCL	-5730	-1208	75	V1P	2427	-1208	140	S367	7398	425	205	S303	4703	1208
11	DCCLK	-5579	-1208	76	V1N	2577	-1208	141	S366	7398	475	206	S302	4658	1208
12	VCCDUM1	-5429	-1208	77	V3P	2727	-1208	142	S365	7398	525	207	S301	4613	1208
13	IM0/ID	-5329	-1208	78	V3N	2877	-1208	143	S364	7398	575	208	S300	4568	1208
14	GNDDUM1	-5229	-1208	79	V60P	3027	-1208	144	S363	7398	626	209	S299	4523	1208
15	IM1	-5129	-1208	80	V60N	3178	-1208	145	S362	7398	676	210	S298	4478	1208
16	VCCDUM2	-5029	-1208	81	V62P	3328	-1208	146	S361	7398	726	211	S297	4433	1208
17	IM2	-4929	-1208	82	V62N	3478	-1208	147	S360	7398	776	212	S296	4388	1208
18	GNDDUM2	-4829	-1208	83	V63P	3628	-1208	148	S359	7398	826	213	S295	4343	1208
19	TEST	-4729	-1208	84	V63N	3778	-1208	149	S358	7398	876	214	S294	4298	1208
20	OSC1	-4579	-1208	85	V8	3928	-1208	150	S357	7398	926	215	S293	4253	1208
21	OSC2	-4429	-1208	86	V20	4028	-1208	151	S356	7398	976	216	S292	4208	1208
22	DB15	-4278	-1208	87	V43	4128	-1208	152	S355	7398	1026	217	S291	4163	1208
23	DB14	-4128	-1208	88	V55	4228	-1208	153	DUMMY3	7398	1208	218	S290	4118	1208
24	DB13	-3978	-1208	89	VTEST	4328	-1208	154	S354	7232	1208	219	S289	4073	1208
25	DB12	-3828	-1208	90	VCOM	4479	-1208	155	S353	7172	1208	220	S288	4028	1208
26	DB11	-3678	-1208	91	VCOM	4579	-1208	156	S352	7112	1208	221	S287	3983	1208
27	DB10	-3528	-1208	92	DCCLK	4729	-1208	157	S351	7052	1208	222	S286	3938	1208
28	DB9	-3378	-1208	93	GCL	4879	-1208	158	S350	6991	1208	223	S285	3893	1208
29	DB8	-3228	-1208	94	GCS*	5029	-1208	159	S349	6931	1208	224	S284	3848	1208
30	GNDDUM3	-3077	-1208	95	GDA	5179	-1208	160	S348	6871	1208	225	S283	3803	1208
31	DB7	-2927	-1208	96	EQ	5329	-1208	161	S347	6811	1208	226	S282	3758	1208
32	DB6	-2777	-1208	97	M	5479	-1208	162	S346	6751	1208	227	S281	3713	1208
33	DB5	-2627	-1208	98	FLM	5630	-1208	163	S345	6691	1208	228	S280	3668	1208
34	DB4	-2477	-1208	99	CL1	5780	-1208	164	S344	6631	1208	229	S279	3623	1208
35	DB3	-2327	-1208	100	DISPTMG	5930	-1208	165	S343	6571	1208	230	S278	3578	1208
36	DB2	-2177	-1208	101	RESET2*	6080	-1208	166	S342	6510	1208	231	S277	3533	1208
37	DB1/SDO	-2027	-1208	102	TS0	6230	-1208	167	S341	6450	1208	232	S276	3488	1208
38	DB0/SDI	-1877	-1208	103	TS1	6330	-1208	168	S340	6390	1208	233	S275	3443	1208
39	RW/RD*	-1726	-1208	104	TS2	6430	-1208	169	S339	6330	1208	234	S274	3398	1208
40	E/WR*/SCL	-1576	-1208	105	TS3	6530	-1208	170	S338	6278	1208	235	S273	3353	1208
41	RS	-1426	-1208	106	TS4	6630	-1208	171	S337	6233	1208	236	S272	3308	1208
42	CS*	-1276	-1208	107	TS5	6730	-1208	172	S336	6188	1208	237	S271	3263	1208
43	TEST1	-1126	-1208	108	TS6	6830	-1208	173	S335	6143	1208	238	S270	3218	1208
44	GND	-976	-1208	109	TS7	6931	-1208	174	S334	6098	1208	239	S269	3173	1208
45	GND	-876	-1208	110	DUMMY2	7398	-1208	175	S333	6053	1208	240	S268	3128	1208
46	GND	-776	-1208	111	S396	7398	-1026	176	S332	6008	1208	241	S267	3083	1208
47	GND	-676	-1208	112	S395	7398	-976	177	S331	5963	1208	242	S266	3038	1208
48	GND	-575	-1208	113	S394	7398	-926	178	S330	5918	1208	243	S265	2993	1208
49	GND	-475	-1208	114	S393	7398	-876	179	S329	5873	1208	244	S264	2948	1208
50	GND	-375	-1208	115	S392	7398	-826	180	S328	5828	1208	245	S263	2903	1208
51	GND	-275	-1208	116	S391	7398	-776	181	S327	5783	1208	246	S262	2858	1208
52	GND	-175	-1208	117	S390	7398	-726	182	S326	5738	1208	247	S261	2813	1208
53	GND	-75	-1208	118	S389	7398	-676	183	S325	5693	1208	248	S260	2768	1208
54	VCC	75	-1208	119	S388	7398	-626	184	S324	5648	1208	249	S259	2723	1208
55	VCC	175	-1208	120	S387	7398	-575	185	S323	5603	1208	250	S258	2678	1208
56	VCC	275	-1208	121	S386	7398	-525	186	S322	5558	1208	251	S257	2633	1208
57	VCC	375	-1208	122	S385	7398	-475	187	S321	5513	1208	252	S256	2588	1208
58	VCC	475	-1208	123	S384	7398	-425	188	S320	5468	1208	253	S255	2543	1208
59	VCC	575	-1208	124	S383	7398	-375	189	S319	5423	1208	254	S254	2498	1208
60	VCC	676	-1208	125	S382	7398	-325	190	S318	5378	1208	255	S253	2453	1208
61	DDVDH	826	-1208	126	S381	7398	-275	191	S317	5333	1208	256	S252	2408	1208
62	DDVDH	926	-1208	127	S380	7398	-225	192	S316	5288	1208	257	S251	2363	1208
63	DDVDH	1026	-1208	128	S379	7398	-175	193	S315	5243	1208	258	S250	2318	1208
64	DDVDH	1126	-1208	129	S378	7398	-125	194	S314	5198	1208	259	S249	2273	1208
65	DDVDH	1226	-1208	130	S377	7398	-75	195	S313	5153	1208	260	S248	2228	1208

HD66770 PAD Coordinate (Straight)

No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y	No.	pad name	X	Y
261	S247	2183	1208	326	S182	-743	1208	391	S117	-3668	1208	456	S52	-6691	1208
262	S246	2138	1208	327	S181	-788	1208	392	S116	-3713	1208	457	S51	-6751	1208
263	S245	2093	1208	328	S180	-833	1208	393	S115	-3758	1208	458	S50	-6811	1208
264	S244	2048	1208	329	S179	-878	1208	394	S114	-3803	1208	459	S49	-6871	1208
265	S243	2003	1208	330	S178	-923	1208	395	S113	-3848	1208	460	S48	-6931	1208
266	S242	1958	1208	331	S177	-968	1208	396	S112	-3893	1208	461	S47	-6991	1208
267	S241	1913	1208	332	S176	-1013	1208	397	S111	-3938	1208	462	S46	-7052	1208
268	S240	1868	1208	333	S175	-1058	1208	398	S110	-3983	1208	463	S45	-7112	1208
269	S239	1823	1208	334	S174	-1103	1208	399	S109	-4028	1208	464	S44	-7172	1208
270	S238	1778	1208	335	S173	-1148	1208	400	S108	-4073	1208	465	S43	-7232	1208
271	S237	1733	1208	336	S172	-1193	1208	401	S107	-4118	1208	466	DUMMY4	-7398	1208
272	S236	1688	1208	337	S171	-1238	1208	402	S106	-4163	1208	467	S42	-7398	1026
273	S235	1643	1208	338	S170	-1283	1208	403	S105	-4208	1208	468	S41	-7398	976
274	S234	1598	1208	339	S169	-1328	1208	404	S104	-4253	1208	469	S40	-7398	926
275	S233	1553	1208	340	S168	-1373	1208	405	S103	-4298	1208	470	S39	-7398	876
276	S232	1508	1208	341	S167	-1418	1208	406	S102	-4343	1208	471	S38	-7398	826
277	S231	1463	1208	342	S166	-1463	1208	407	S101	-4388	1208	472	S37	-7398	776
278	S230	1418	1208	343	S165	-1508	1208	408	S100	-4433	1208	473	S36	-7398	726
279	S229	1373	1208	344	S164	-1553	1208	409	S99	-4478	1208	474	S35	-7398	676
280	S228	1328	1208	345	S163	-1598	1208	410	S98	-4523	1208	475	S34	-7398	626
281	S227	1283	1208	346	S162	-1643	1208	411	S97	-4568	1208	476	S33	-7398	575
282	S226	1238	1208	347	S161	-1688	1208	412	S96	-4613	1208	477	S32	-7398	525
283	S225	1193	1208	348	S160	-1733	1208	413	S95	-4658	1208	478	S31	-7398	475
284	S224	1148	1208	349	S159	-1778	1208	414	S94	-4703	1208	479	S30	-7398	425
285	S223	1103	1208	350	S158	-1823	1208	415	S93	-4748	1208	480	S29	-7398	375
286	S222	1058	1208	351	S157	-1868	1208	416	S92	-4793	1208	481	S28	-7398	325
287	S221	1013	1208	352	S156	-1913	1208	417	S91	-4838	1208	482	S27	-7398	275
288	S220	968	1208	353	S155	-1958	1208	418	S90	-4883	1208	483	S26	-7398	225
289	S219	923	1208	354	S154	-2003	1208	419	S89	-4928	1208	484	S25	-7398	175
290	S218	878	1208	355	S153	-2048	1208	420	S88	-4973	1208	485	S24	-7398	125
291	S217	833	1208	356	S152	-2093	1208	421	S87	-5018	1208	486	S23	-7398	75
292	S216	788	1208	357	S151	-2138	1208	422	S86	-5063	1208	487	S22	-7398	25
293	S215	743	1208	358	S150	-2183	1208	423	S85	-5108	1208	488	S21	-7398	-25
294	S214	698	1208	359	S149	-2228	1208	424	S84	-5153	1208	489	S20	-7398	-75
295	S213	653	1208	360	S148	-2273	1208	425	S83	-5198	1208	490	S19	-7398	-125
296	S212	608	1208	361	S147	-2318	1208	426	S82	-5243	1208	491	S18	-7398	-175
297	S211	563	1208	362	S146	-2363	1208	427	S81	-5288	1208	492	S17	-7398	-225
298	S210	518	1208	363	S145	-2408	1208	428	S80	-5333	1208	493	S16	-7398	-275
299	S209	473	1208	364	S144	-2453	1208	429	S79	-5378	1208	494	S15	-7398	-325
300	S208	428	1208	365	S143	-2498	1208	430	S78	-5423	1208	495	S14	-7398	-375
301	S207	383	1208	366	S142	-2543	1208	431	S77	-5468	1208	496	S13	-7398	-425
302	S206	338	1208	367	S141	-2588	1208	432	S76	-5513	1208	497	S12	-7398	-475
303	S205	293	1208	368	S140	-2633	1208	433	S75	-5558	1208	498	S11	-7398	-525
304	S204	248	1208	369	S139	-2678	1208	434	S74	-5603	1208	499	S10	-7398	-575
305	S203	203	1208	370	S138	-2723	1208	435	S73	-5648	1208	500	S9	-7398	-626
306	S202	158	1208	371	S137	-2768	1208	436	S72	-5693	1208	501	S8	-7398	-676
307	S201	113	1208	372	S136	-2813	1208	437	S71	-5738	1208	502	S7	-7398	-726
308	S200	68	1208	373	S135	-2858	1208	438	S70	-5783	1208	503	S6	-7398	-776
309	S199	23	1208	374	S134	-2903	1208	439	S69	-5828	1208	504	S5	-7398	-826
310	S198	-23	1208	375	S133	-2948	1208	440	S68	-5873	1208	505	S4	-7398	-876
311	S197	-68	1208	376	S132	-2993	1208	441	S67	-5918	1208	506	S3	-7398	-926
312	S196	-113	1208	377	S131	-3038	1208	442	S66	-5963	1208	507	S2	-7398	-976
313	S195	-158	1208	378	S130	-3083	1208	443	S65	-6008	1208	508	S1	-7398	-1026
314	S194	-203	1208	379	S129	-3128	1208	444	S64	-6053	1208				
315	S193	-248	1208	380	S128	-3173	1208	445	S63	-6098	1208		Cross hairs	-7151	-1161
316	S192	-293	1208	381	S127	-3218	1208	446	S62	-6143	1208			7151	-1161
317	S191	-338	1208	382	S126	-3263	1208	447	S61	-6188	1208				
318	S190	-383	1208	383	S125	-3308	1208	448	S60	-6233	1208				
319	S189	-428	1208	384	S124	-3353	1208	449	S59	-6278	1208				
320	S188	-473	1208	385	S123	-3398	1208	450	S58	-6330	1208				
321	S187	-518	1208	386	S122	-3443	1208	451	S57	-6390	1208				
322	S186	-563	1208	387	S121	-3488	1208	452	S56	-6450	1208				
323	S185	-608	1208	388	S120	-3533	1208	453	S55	-6510	1208				
324	S184	-653	1208	389	S119	-3578	1208	454	S54	-6571	1208				
325	S183	-698	1208	390	S118	-3623	1208	455	S53	-6631	1208				

2001.2.28

HD667B70 PAD Arrangement

(Laced Output Arrangement)

- Chip Size: 15.06mm x 2.68mm
- Chip thickness: 550um (typ.)
- PAD coordinate: PAD center
- Coordinate origin: Chip center

- Au bump size:

(1) 80 um x 80 um

DUMMY1, DUMMY2, DUMMY3, DUMMY4
RESET1* to TS7
RESET1* to TS7

(2) 30 um x 80um

S338 to S59

(3) 80um x 35um

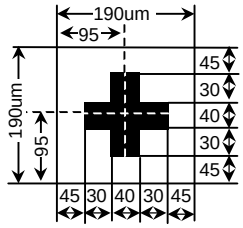
S396 to S355, S42 to S1

(4) 45um x 80um

S354 to S339, S58 to S43

- Au bump pitch: Refer to PAD coordinate
- Au bump height: 15 um (typ.)
- Number in the diagram refers to number on the PAD coordinate.
- Cross hairs

(1) Figure



(2) Arrangement: 2 places

(3) Coordinates (X, Y)

(7151, -1161) (-7151, -1161)

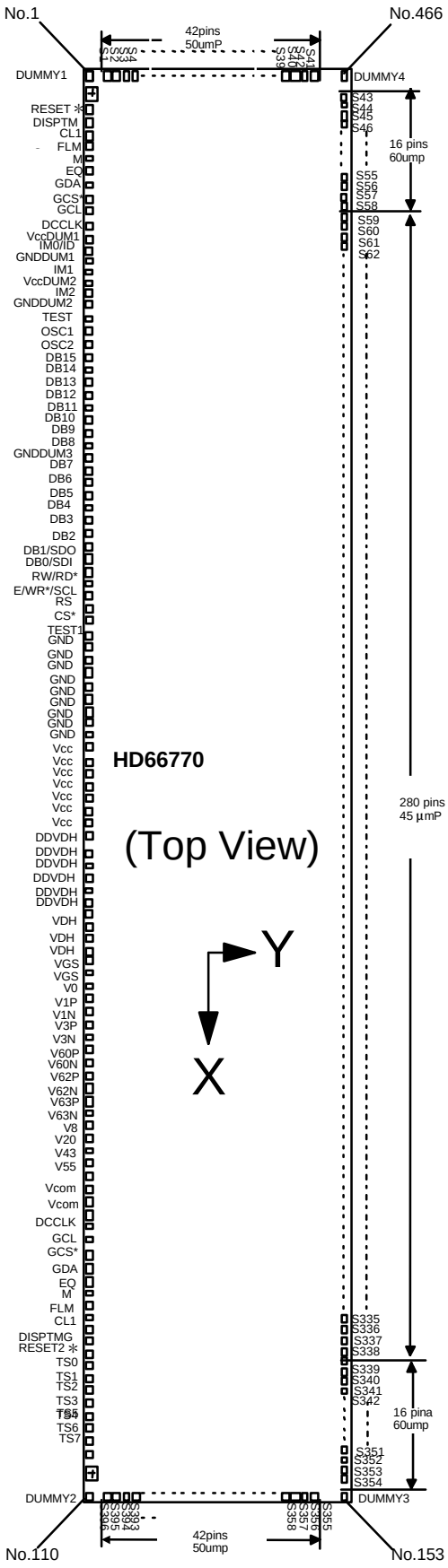


Figure 3: PAD Arrangement

HD66770 PAD Coordinate (Laced Coordinate) 2001.2.28 REV0.0

No.	padname	X	Y	No.	padname	X	Y	No.	padname	X	Y	No.	padname	X	Y
1	DUMMY1	-7398	-1208	66	DDVDH	1326	-1208	131	S376	7283	-25	196	S312	5108	1093
2	RESET1*	-6931	-1208	67	DDVDH	1426	-1208	132	S375	7398	25	197	S311	5063	1208
3	DISPTMG	-6780	-1208	68	VDH	1576	-1208	133	S374	7283	75	198	S310	5018	1093
4	CL1	-6630	-1208	69	VDH	1676	-1208	134	S373	7398	125	199	S309	4973	1208
5	FLM	-6480	-1208	70	VDH	1776	-1208	135	S372	7283	175	200	S308	4928	1093
6	M	-6330	-1208	71	VDH	1877	-1208	136	S371	7398	225	201	S307	4883	1208
7	EQ	-6180	-1208	72	VGS	2027	-1208	137	S370	7283	275	202	S306	4838	1093
8	GDA	-6030	-1208	73	VGS	2127	-1208	138	S369	7398	325	203	S305	4793	1208
9	GCS*	-5880	-1208	74	V0	2277	-1208	139	S368	7283	375	204	S304	4748	1093
10	GCL	-5730	-1208	75	V1P	2427	-1208	140	S367	7398	425	205	S303	4703	1208
11	DCCLK	-5579	-1208	76	V1N	2577	-1208	141	S366	7283	475	206	S302	4658	1093
12	VCCDUM1	-5429	-1208	77	V3P	2727	-1208	142	S365	7398	525	207	S301	4613	1208
13	IM0/ID	-5329	-1208	78	V3N	2877	-1208	143	S364	7283	575	208	S300	4568	1093
14	GNDDUM1	-5229	-1208	79	V60P	3027	-1208	144	S363	7398	626	209	S299	4523	1208
15	IM1	-5129	-1208	80	V60N	3178	-1208	145	S362	7283	676	210	S298	4478	1093
16	VCCDUM2	-5029	-1208	81	V62P	3328	-1208	146	S361	7398	726	211	S297	4433	1208
17	IM2	-4929	-1208	82	V62N	3478	-1208	147	S360	7283	776	212	S296	4388	1093
18	GNDDUM2	-4829	-1208	83	V63P	3628	-1208	148	S359	7398	826	213	S295	4343	1208
19	TEST	-4729	-1208	84	V63N	3778	-1208	149	S358	7283	876	214	S294	4298	1093
20	OSC1	-4579	-1208	85	V8	3928	-1208	150	S357	7398	926	215	S293	4253	1208
21	OSC2	-4429	-1208	86	V20	4028	-1208	151	S356	7283	976	216	S292	4208	1093
22	DB15	-4278	-1208	87	V43	4128	-1208	152	S355	7398	1026	217	S291	4163	1208
23	DB14	-4128	-1208	88	V55	4228	-1208	153	DUMMY3	7398	1208	218	S290	4118	1093
24	DB13	-3978	-1208	89	VTEST	4328	-1208	154	S354	7232	1093	219	S289	4073	1208
25	DB12	-3828	-1208	90	VCOM	4479	-1208	155	S353	7172	1208	220	S288	4028	1093
26	DB11	-3678	-1208	91	VCOM	4579	-1208	156	S352	7112	1093	221	S287	3983	1208
27	DB10	-3528	-1208	92	DCCLK	4729	-1208	157	S351	7052	1208	222	S286	3938	1093
28	DB9	-3378	-1208	93	GCL	4879	-1208	158	S350	6991	1093	223	S285	3893	1208
29	DB8	-3228	-1208	94	GCS*	5029	-1208	159	S349	6931	1208	224	S284	3848	1093
30	GNDDUM3	-3077	-1208	95	GDA	5179	-1208	160	S348	6871	1093	225	S283	3803	1208
31	DB7	-2927	-1208	96	EQ	5329	-1208	161	S347	6811	1208	226	S282	3758	1093
32	DB6	-2777	-1208	97	M	5479	-1208	162	S346	6751	1093	227	S281	3713	1208
33	DB5	-2627	-1208	98	FLM	5630	-1208	163	S345	6691	1208	228	S280	3668	1093
34	DB4	-2477	-1208	99	CL1	5780	-1208	164	S344	6631	1093	229	S279	3623	1208
35	DB3	-2327	-1208	100	DISPTMG	5930	-1208	165	S343	6571	1208	230	S278	3578	1093
36	DB2	-2177	-1208	101	RESET2*	6080	-1208	166	S342	6510	1093	231	S277	3533	1208
37	DB1/SDO	-2027	-1208	102	TS0	6230	-1208	167	S341	6450	1208	232	S276	3488	1093
38	DB0/SDI	-1877	-1208	103	TS1	6330	-1208	168	S340	6390	1093	233	S275	3443	1208
39	RW/RD*	-1726	-1208	104	TS2	6430	-1208	169	S339	6330	1208	234	S274	3398	1093
40	E/WR*/SCL	-1576	-1208	105	TS3	6530	-1208	170	S338	6278	1093	235	S273	3353	1208
41	RS	-1426	-1208	106	TS4	6630	-1208	171	S337	6233	1208	236	S272	3308	1093
42	CS*	-1276	-1208	107	TS5	6730	-1208	172	S336	6188	1093	237	S271	3263	1208
43	TEST1	-1126	-1208	108	TS6	6830	-1208	173	S335	6143	1208	238	S270	3218	1093
44	GND	-976	-1208	109	TS7	6931	-1208	174	S334	6098	1093	239	S269	3173	1208
45	GND	-876	-1208	110	DUMMY2	7398	-1208	175	S333	6053	1208	240	S268	3128	1093
46	GND	-776	-1208	111	S396	7283	-1026	176	S332	6008	1093	241	S267	3083	1208
47	GND	-676	-1208	112	S395	7398	-976	177	S331	5963	1208	242	S266	3038	1093
48	GND	-575	-1208	113	S394	7283	-926	178	S330	5918	1093	243	S265	2993	1208
49	GND	-475	-1208	114	S393	7398	-876	179	S329	5873	1208	244	S264	2948	1093
50	GND	-375	-1208	115	S392	7283	-826	180	S328	5828	1093	245	S263	2903	1208
51	GND	-275	-1208	116	S391	7398	-776	181	S327	5783	1208	246	S262	2858	1093
52	GND	-175	-1208	117	S390	7283	-726	182	S326	5738	1093	247	S261	2813	1208
53	GND	-75	-1208	118	S389	7398	-676	183	S325	5693	1208	248	S260	2768	1093
54	VCC	75	-1208	119	S388	7283	-626	184	S324	5648	1093	249	S259	2723	1208
55	VCC	175	-1208	120	S387	7398	-575	185	S323	5603	1208	250	S258	2678	1093
56	VCC	275	-1208	121	S386	7283	-525	186	S322	5558	1093	251	S257	2633	1208
57	VCC	375	-1208	122	S385	7398	-475	187	S321	5513	1208	252	S256	2588	1093
58	VCC	475	-1208	123	S384	7283	-425	188	S320	5468	1093	253	S255	2543	1208
59	VCC	575	-1208	124	S383	7398	-375	189	S319	5423	1208	254	S254	2498	1093
60	VCC	676	-1208	125	S382	7283	-325	190	S318	5378	1093	255	S253	2453	1208
61	DDVDH	826	-1208	126	S381	7398	-275	191	S317	5333	1208	256	S252	2408	1093
62	DDVDH	926	-1208	127	S380	7283	-225	192	S316	5288	1093	257	S251	2363	1208
63	DDVDH	1026	-1208	128	S379	7398	-175	193	S315	5243	1208	258	S250	2318	1093
64	DDVDH	1126	-1208	129	S378	7283	-125	194	S314	5198	1093	259	S249	2273	1208
65	DDVDH	1226	-1208	130	S377	7398	-75	195	S313	5153	1208	260	S248	2228	1093

HD66770 PAD Coordinate (Laced Coordinate)

No.	padname	X	Y	No.	padname	X	Y	No.	padname	X	Y	No.	padname	X	Y
261	S247	2183	1208	326	S182	-743	1093	391	S117	-3668	1208	456	S52	-6691	1093
262	S246	2138	1093	327	S181	-788	1208	392	S116	-3713	1093	457	S51	-6751	1208
263	S245	2093	1208	328	S180	-833	1093	393	S115	-3758	1208	458	S50	-6811	1093
264	S244	2048	1093	329	S179	-878	1208	394	S114	-3803	1093	459	S49	-6871	1208
265	S243	2003	1208	330	S178	-923	1093	395	S113	-3848	1208	460	S48	-6931	1093
266	S242	1958	1093	331	S177	-968	1208	396	S112	-3893	1093	461	S47	-6991	1208
267	S241	1913	1208	332	S176	-1013	1093	397	S111	-3938	1208	462	S46	-7052	1093
268	S240	1868	1093	333	S175	-1058	1208	398	S110	-3983	1093	463	S45	-7112	1208
269	S239	1823	1208	334	S174	-1103	1093	399	S109	-4028	1208	464	S44	-7172	1093
270	S238	1778	1093	335	S173	-1148	1208	400	S108	-4073	1093	465	S43	-7232	1208
271	S237	1733	1208	336	S172	-1193	1093	401	S107	-4118	1208	466	DUMMY4	-7398	1208
272	S236	1688	1093	337	S171	-1238	1208	402	S106	-4163	1093	467	S42	-7283	1026
273	S235	1643	1208	338	S170	-1283	1093	403	S105	-4208	1208	468	S41	-7398	976
274	S234	1598	1093	339	S169	-1328	1208	404	S104	-4253	1093	469	S40	-7283	926
275	S233	1553	1208	340	S168	-1373	1093	405	S103	-4298	1208	470	S39	-7398	876
276	S232	1508	1093	341	S167	-1418	1208	406	S102	-4343	1093	471	S38	-7283	826
277	S231	1463	1208	342	S166	-1463	1093	407	S101	-4388	1208	472	S37	-7398	776
278	S230	1418	1093	343	S165	-1508	1208	408	S100	-4433	1093	473	S36	-7283	726
279	S229	1373	1208	344	S164	-1553	1093	409	S99	-4478	1208	474	S35	-7398	676
280	S228	1328	1093	345	S163	-1598	1208	410	S98	-4523	1093	475	S34	-7283	626
281	S227	1283	1208	346	S162	-1643	1093	411	S97	-4568	1208	476	S33	-7398	575
282	S226	1238	1093	347	S161	-1688	1208	412	S96	-4613	1093	477	S32	-7283	525
283	S225	1193	1208	348	S160	-1733	1093	413	S95	-4658	1208	478	S31	-7398	475
284	S224	1148	1093	349	S159	-1778	1208	414	S94	-4703	1093	479	S30	-7283	425
285	S223	1103	1208	350	S158	-1823	1093	415	S93	-4748	1208	480	S29	-7398	375
286	S222	1058	1093	351	S157	-1868	1208	416	S92	-4793	1093	481	S28	-7283	325
287	S221	1013	1208	352	S156	-1913	1093	417	S91	-4838	1208	482	S27	-7398	275
288	S220	968	1093	353	S155	-1958	1208	418	S90	-4883	1093	483	S26	-7283	225
289	S219	923	1208	354	S154	-2003	1093	419	S89	-4928	1208	484	S25	-7398	175
290	S218	878	1093	355	S153	-2048	1208	420	S88	-4973	1093	485	S24	-7283	125
291	S217	833	1208	356	S152	-2093	1093	421	S87	-5018	1208	486	S23	-7398	75
292	S216	788	1093	357	S151	-2138	1208	422	S86	-5063	1093	487	S22	-7283	25
293	S215	743	1208	358	S150	-2183	1093	423	S85	-5108	1208	488	S21	-7398	-25
294	S214	698	1093	359	S149	-2228	1208	424	S84	-5153	1093	489	S20	-7283	-75
295	S213	653	1208	360	S148	-2273	1093	425	S83	-5198	1208	490	S19	-7398	-125
296	S212	608	1093	361	S147	-2318	1208	426	S82	-5243	1093	491	S18	-7283	-175
297	S211	563	1208	362	S146	-2363	1093	427	S81	-5288	1208	492	S17	-7398	-225
298	S210	518	1093	363	S145	-2408	1208	428	S80	-5333	1093	493	S16	-7283	-275
299	S209	473	1208	364	S144	-2453	1093	429	S79	-5378	1208	494	S15	-7398	-325
300	S208	428	1093	365	S143	-2498	1208	430	S78	-5423	1093	495	S14	-7283	-375
301	S207	383	1208	366	S142	-2543	1093	431	S77	-5468	1208	496	S13	-7398	-425
302	S206	338	1093	367	S141	-2588	1208	432	S76	-5513	1093	497	S12	-7283	-475
303	S205	293	1208	368	S140	-2633	1093	433	S75	-5558	1208	498	S11	-7398	-525
304	S204	248	1093	369	S139	-2678	1208	434	S74	-5603	1093	499	S10	-7283	-575
305	S203	203	1208	370	S138	-2723	1093	435	S73	-5648	1208	500	S9	-7398	-626
306	S202	158	1093	371	S137	-2768	1208	436	S72	-5693	1093	501	S8	-7283	-676
307	S201	113	1208	372	S136	-2813	1093	437	S71	-5738	1208	502	S7	-7398	-726
308	S200	68	1093	373	S135	-2858	1208	438	S70	-5783	1093	503	S6	-7283	-776
309	S199	23	1208	374	S134	-2903	1093	439	S69	-5828	1208	504	S5	-7398	-826
310	S198	-23	1093	375	S133	-2948	1208	440	S68	-5873	1093	505	S4	-7283	-876
311	S197	-68	1208	376	S132	-2993	1093	441	S67	-5918	1208	506	S3	-7398	-926
312	S196	-113	1093	377	S131	-3038	1208	442	S66	-5963	1093	507	S2	-7283	-976
313	S195	-158	1208	378	S130	-3083	1093	443	S65	-6008	1208	508	S1	-7398	-1026
314	S194	-203	1093	379	S129	-3128	1208	444	S64	-6053	1093				
315	S193	-248	1208	380	S128	-3173	1093	445	S63	-6098	1208		Cross hairs	-7151	-1161
316	S192	-293	1093	381	S127	-3218	1208	446	S62	-6143	1093			7151	-1161
317	S191	-338	1208	382	S126	-3263	1093	447	S61	-6188	1208				
318	S190	-383	1093	383	S125	-3308	1208	448	S60	-6233	1093				
319	S189	-428	1208	384	S124	-3353	1093	449	S59	-6278	1208				
320	S188	-473	1093	385	S123	-3398	1208	450	S58	-6330	1093				
321	S187	-518	1208	386	S122	-3443	1093	451	S57	-6390	1208				
322	S186	-563	1093	387	S121	-3488	1208	452	S56	-6450	1093				
323	S185	-608	1208	388	S120	-3533	1093	453	S55	-6510	1208				
324	S184	-653	1093	389	S119	-3578	1208	454	S54	-6571	1093				
325	S183	-698	1208	390	S118	-3623	1093	455	S53	-6631	1208				

Block Function Description

System Interface

The HD66770 has five high-speed system interfaces: an 80-system 16-bit/8-bit bus, a 68-system 16-bit/8-bit bus, and a serial peripheral (SPI: Serial Peripheral Interface port). The interface mode is selected by the IM2-0 pins.

The HD66770 has three 16-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal. When a logic operation is performed inside of the HD66770 by using the display data set in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice nor to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Table 2 Register Selection (8/16 Parallel Interface)

80-system Bus		68-system Bus		
WR*	**RD***	**R/W**	**RS**	**Operations**
0	1	0	0	Writes indexes into IR
1	0	1	0	Reads internal status
0	1	0	1	Writes into control registers and GRAM through WDR
1	0	1	1	Reads from GRAM through RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start bytes		
R/W Bits	**RS Bits**	**Operations**
0	0	Writes indexes into IR
1	0	Reads internal status
0	1	Writes into control registers and GRAM through WDR
1	1	Reads from GRAM through RDR

Bit Operation

The HD66770 supports the following functions: a write data mask function that selects and writes data into the GRAM in bit units, and a logic operation function that performs logic operations or conditional determination on the display data set in the GRAM and writes into the GRAM. With the 16-bit bus interface, these functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

Address Counter (AC)

The address counter (AC) assigns address to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has 16 bits/pixel and stores the bit-pattern data of 132 x 176 bytes.

Grayscale Voltage Generator

The grayscale voltage circuit generates a LCD driver circuit that corresponds to the grayscale levels as specified in the grayscale gamma-adjusting resistor. 65,536 possible colors can be displayed at the same time. For details, see the gamma-adjusting resistor.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access are generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, CL1, EQ, DCCLK, DISPTMG) for the gate driver and The power supply IC.

Oscillation Circuit (OSC)

The HD66770 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulses can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 396 source drivers (S1 to S396).

Display pattern data is latched when 396-bit data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The shift direction of 396-bit data can be changed by the SS bit by selecting an appropriate direction for the device-mounting configuration.

Interface with Gate Driver

A serial interface circuit provides an interface with the HD66771 and HD667P00. When sending an instruction setting from the HD66770 to the HD66771 and HD667P00, a register setting value from within the HD66770 is transferred via the serial interface circuit. A transfer is started by setting a serial transfer enable of the HD66770. However, transfer to and reading from the HD66771 or HD667P00 is not possible during standby. For details, see the Gate Serial Transfer section

Table 4: Relationship between GRAM address and display position (SS = “0”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB 11	.... DB 0	DB 11	.... DB 0	DB 11	.... DB 0	DB 11	.... DB 0						DB 11	.... DB 0		DB 11	.... DB 0		DB 11	.... DB 0		DB 11	.... DB 0	
G1	G176	"0000"H		"0001"H		"0002"H		"0003"H						.....	"0080"H			"0081"H			"0082"H			"0083"H		
G2	G175	"0100"H		"0101"H		"0102"H		"0103"H						.....	"0180"H			"0181"H			"0182"H			"0183"H		
G3	G174	"0200"H		"0201"H		"0202"H		"0203"H						.....	"0280"H			"0281"H			"0282"H			"0283"H		
G4	G173	"0300"H		"0301"H		"0302"H		"0303"H						.....	"0380"H			"0381"H			"0382"H			"0383"H		
G5	G172	"0400"H		"0401"H		"0402"H		"0403"H						.....	"0480"H			"0481"H			"0482"H			"0483"H		
G6	G171	"0500"H		"0501 H		"0502"H		"0503"H						.....	"0580"H			"0581 H			"0582"H			"0583"H		
G7	G170	"0600"H		"0601"H		"0602"H		"0603"H						.....	"0680"H			"0681"H			"0682"H			"0683"H		
G8	G169	"0700"H		"0701"H		"0702"H		"0703"H						.....	"0780"H			"0781"H			"0782"H			"0783"H		
G9	G168	"0800"H		"0801"H		"0802"H		"0803"H						.....	"0880"H			"0881"H			"0882"H			"0883"H		
G10	G167	"0900"H		"0901"H		"0902"H		"0903"H						.....	"0980"H			"0981"H			"0982"H			"0983"H		
G11	G166	"0A00"H		"0A01"H		"0A02"H		"0A03"H						.....	"0A80"H			"0A81"H			"0A82"H			"0A83"H		
G12	G165	"0B00"H		"0B01"H		"0B02"H		"0B03"H						.....	"0B80"H			"0B81"H			"0B82"H			"0B83"H		
G13	G164	"0C00"H		"0C01"H		"0C02"H		"0C03"H						.....	"0C80"H			"0C81"H			"0C82"H			"0C83"H		
G14	G163	"0D00"H		"0D01"H		"0D02"H		"0D03"H						.....	"0D80"H			"0D81"H			"0D82"H			"0D83"H		
G15	G162	"0E00"H		"0E01"H		"0E02"H		"0E03"H						.....	"0E80"H			"0E81"H			"0E82"H			"0E83"H		
G16	G161	"0F00"H		"0F01"H		"0F02"H		"0F03"H						.....	"0F80"H			"0F81"H			"0F82"H			"0F83"H		
G17	G160	"1000"H		"1001"H		"1002"H		"1003"H						.....	"1080"H			"1081"H			"1082"H			"1083"H		
G18	G159	"1100"H		"1101"H		"1102"H		"1103"H						.....	"1180"H			"1181"H			"1182"H			"1183"H		
G19	G158	"1200"H		"1201"H		"1202"H		"1203"H						.....	"1280"H			"1281"H			"1282"H			"1283"H		
G20	G157	"1300"H		"1301"H		"1302"H		"1303"H						.....	"1380"H			"1381"H			"1382"H			"1383"H		
⋮	⋮	⋮		⋮		⋮		⋮							⋮			⋮			⋮			⋮		
G169	G8	"A800"H		"A801"H		"A802"H		"A803"H						.....	"A880"H			"A881"H			"A882"H			"A883"H		
G170	G7	"A900"H		"A901"H		"A902"H		"A903"H						.....	"A980"H			"A981"H			"A982"H			"A983"H		
G171	G6	"AA00"H		"AA01"H		"AA02"H		"AA03"H						.....	"AA80"H			"AA81"H			"AA82"H			"AA83"H		
G172	G5	"AB00"H		"AB01"H		"AB02"H		"AB03"H						.....	"AB80"H			"AB81"H			"AB82"H			"AB83"H		
G173	G4	"AC00"H		"AC01"H		"AC02"H		"AC03"H						.....	"AC80"H			"AC81"H			"AC82"H			"AC83"H		
G174	G3	"AD00"H		"AD01"H		"AD02"H		"AD03"H						.....	"AD80"H			"AD81"H			"AD82"H			"AD83"H		
G175	G2	"AE00"H		"AE01"H		"AE02"H		"AE03"H						.....	"AE80"H			"AE81"H			"AE82"H			"AE83"H		
G176	G1	"AF00"H		"AF01"H		"AF02"H		"AF03"H						.....	"AF80"H			"AF81"H			"AF82"H			"AF83"H		

Table 5: Relationship between GRAM address and output pin

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
RGB allotment	R					G						B				
output pin	S(3n+1)											S(3n+3)				

Table 6: Relationship between GRAM address and display position (SS = “1”)

S/G pin		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB0 ... DB11			DB0 ... DB11			DB0 ... DB11			DB0 ... DB11				DB0 ... DB11			DB0 ... DB11			DB0 ... DB11			DB0 ... DB11		
G1	G176	"0083"H			"0082"H			"0081"H			"0080"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G175	"0183"H			"0182"H			"0181"H			"0180"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G174	"0283"H			"0282"H			"0281"H			"0280"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G173	"0383"H			"0382"H			"0381"H			"0380"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G172	"0483"H			"0482"H			"0481"H			"0480"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G171	"0583"H			"0582"H			"0581 H			"0580"H			.....	"0503"H			"0502"H			"0501 H			"0500"H		
G7	G170	"0683"H			"0682"H			"0681"H			"0680"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G169	"0783"H			"0782"H			"0781"H			"0780"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G168	"0883"H			"0882"H			"0881"H			"0880"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G167	"0983"H			"0982"H			"0981"H			"0980"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G166	"0A83"H			"0A82"H			"0A81"H			"0A80"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G165	"0B83"H			"0B82"H			"0B81"H			"0B80"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G164	"0C83"H			"0C82"H			"0C81"H			"0C80"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G163	"0D83"H			"0D82"H			"0D81"H			"0D80"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G162	"0E83"H			"0E82"H			"0E81"H			"0E80"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G161	"0F83"H			"0F82"H			"0F81"H			"0F80"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G160	"1083"H			"1082"H			"1081"H			"1080"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G159	"1183"H			"1182"H			"1181"H			"1180"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G158	"1283"H			"1282"H			"1281"H			"1280"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G157	"1383"H			"1382"H			"1381"H			"1380"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮		⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G169	G8	"A883"H			"A882"H			"A881"H			"A880"H			.....	"A803"H			"A802"H			"A801"H			"A800"H		
G170	G7	"A983"H			"A982"H			"A981"H			"A980"H			.....	"A903"H			"A902"H			"A901"H			"A900"H		
G171	G6	"AA83"H			"AA82"H			"AA81"H			"AA80"H			.....	"AA03"H			"AA02"H			"AA01"H			"AA00"H		
G172	G5	"AB83"H			"AB82"H			"AB81"H			"AB80"H			.....	"AB03"H			"AB02"H			"AB01"H			"AB00"H		
G173	G4	"AC83"H			"AC82"H			"AC81"H			"AC80"H			.....	"AC03"H			"AC02"H			"AC01"H			"AC00"H		
G174	G3	"AD83"H			"AD82"H			"AD81"H			"AD80"H			.....	"AD03"H			"AD02"H			"AD01"H			"AD00"H		
G175	G2	"AE83"H			"AE82"H			"AE81"H			"AE80"H			.....	"AE03"H			"AE02"H			"AE01"H			"AE00"H		
G176	G1	"AF83"H			"AF82"H			"AF81"H			"AF80"H			.....	"AF03"H			"AF02"H			"AF01"H			"AF00"H		

Table 7: Relationship between GRAM address and output pin

GRAM data	DB 15	DB 14	DB 13	DB 12	DB 11	DB 10	DB 9	DB 8	DB 7	DB 6	DB 5	DB 4	DB 3	DB 2	DB 1	DB 0
RGB allotment	R					G						B				
output pin	S(396-3n)					S(395-3n)						S(394-3n)				

Instructions

Outline

The HD66770 uses the 16-bit bus architecture. Before the internal operation of the HD66770 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high-performance microcomputer. The internal operation of the HD66770 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB15 to DB0), make up the HD66770 instructions.
There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale gamma adjustment
- Interface with the gate driver and Power supply IC

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. Because instructions are executed in 0 cycles, they can be written in succession.

Instruction Descriptions

Index

The index instruction specifies the RAM control indexes (R00h to R3Fh). It sets the register number in the range of 00000 to 111111 in binary form. However, R40 to R44 are disabled since they are test registers.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Figure 4 Index Instruction

Status Read

The status read instruction reads the internal status of the HD66770.

L7–0: Indicate the driving raster-row position where the liquid crystal display is being driven.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Figure 5 Status Read Instruction

Start Oscillation (R00h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, *0770H is read.

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0

Figure 6 Start Oscillation Instruction

Driver Output Control (R01h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

Figure 7 Driver Output Control Instruction

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G228. When GS = 1, G228 shifts to G1

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S396. When SS = 1, S396 shifts to S1. When SS = 0, <R><G><B> color is assigned from S1. When SS = 1, <R><G><B> color is assigned from S396. Re-write to the RAM when intending to change the SS bit.

Note: The GS bit is for setting the gate driver. Control according to the bit's value is executed by the gate driver. For details, see the data sheet for the gate driver.

NL4–0: Specify number of lines for the LCD drive. Number of lines for the LCD drive can be adjusted for every eight raster-rows. GRAM address mapping does not depend on the setting value of the drive duty ratio. Select the set value for the panel size or higher.

Table 8: NL Bits and Drive Duty

NL4	NL3	NL2	NL1	NL0	Display Size	Number of LCD Driver Lines	Gate Driver Used
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	396 x 16 dots	16	G1 to G16
0	0	0	1	0	396 x 24 dots	24	G1 to G24
0	0	0	1	1	396 x 32 dots	32	G1 to G32
0	0	1	0	0	396 x 40 dots	40	G1 to G40
0	0	1	0	1	396 x 48 dots	48	G1 to G48
0	0	1	1	0	396 x 56 dots	56	G1 to G56
0	0	1	1	1	396 x 64 dots	64	G1 to G64
0	1	0	0	0	396 x 72 dots	72	G1 to G72
0	1	0	0	1	396 x 80 dots	80	G1 to G80
0	1	0	1	0	396 x 88 dots	88	G1 to G88
0	1	0	1	1	396 x 96 dots	96	G1 to G96
0	1	1	0	0	396 x 104 dots	104	G1 to G104
0	1	1	0	1	396 x 112 dots	112	G1 to G112
0	1	1	1	0	396 x 120 dots	120	G1 to G120
0	1	1	1	1	396 x 128 dots	128	G1 to G128
1	0	0	0	0	396 x 136 dots	136	G1 to G136
1	0	0	0	1	396 x 144 dots	144	G1 to G144
1	0	0	1	0	396 x 152 dots	152	G1 to G152
1	0	0	1	1	396 x 160 dots	160	G1 to G160
1	0	1	0	0	396 x 168 dots	168	G1 to G168
1	0	1	0	1	396 x 176 dots	176	G1 to G176

Note: Blank period (when all gates output Vgoff level) of 8H period will be inserted to the gates after all gates are scanned.

LCD-Driving-Waveform Control (R02h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

Figure 8 LCD-Driving-Waveform Control Instruction

FLD1-0: Set number of the field that the n field inter-laced driving. For details, see the "Inter-laced" drive section.

FLD1	FLD0	Number of field
0	0	Setting disabled
0	1	1 field
1	0	Setting disabled
1	1	3 field

Table 9

B/C: When B/C = 0, a B-pattern waveform is generated and alternates in every frame for LCD drive. When B/C = 1, a n raster-row waveform is generated and alternates in each raster-row specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register. For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive raster-row and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Note: FLD1-0 bits are for the gate driver. Control according to the bits' value executed by the gate driver. For details, see the data sheet for the gate driver.

Power Control 1 (R03h)

Power Control 2 (R04h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
W	1	CAD	0	0	VRN4	VRN3	VRN2	VRN1	VRN0	0	0	0	VRP4	VRP3	VRP2	VRP1	VRP0

Figure 9 Power Control Instruction

SAP2-0: The amount of fixed current from the operational amplifier for the source driver is adjusted. When the amount of fixed current is large, LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when SAP2-0 = "000", the current consumption can be reduced by halting the operational amplifier and step-up circuit operation.

SAP2	SAP1	SAP0	Op-amp Current
0	**0**	**0**	**Halt op-amp**
0	**0**	**1**	**Small**
0	**1**	**0**	**Small/medium**
0	**1**	**1**	**Medium**

Table 10

SAP2	SAP1	SAP0	Op-amp Current
1	**0**	**0**	**Medium/large**
1	**0**	**1**	**Large**
1	**1**	**0**	Setting disabled
1	**1**	**1**	Setting disabled

Table 11

BT2–0: The output factor of step-up circuit is selected. Adjust scale factor of the step-up circuit by the voltage used. Lower amplification of the step-up circuit consumes less current.

DC2-0: The operating frequency in the step-up circuit is selected. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

AP2–0: The amount of fixed current from operational amplifier for the power supply is adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = "000", the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

SLP: When SLP = 1, the HD66770 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only serial transfer to a gate driver/power-supply IC and the following instructions can be executed during the sleep mode.

Power control: (BT2–0, DC2–0, AP2–0, SLP, STB, VC2-0, CAD, VR3-0, VRL3-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits)

Common interface control: (TE, IDX)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained.

STB: When STB = 1, the HD66770 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

a. Standby mode cancel (STB = "0")

b. Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after the standby mode is canceled. Serial transfer to the common driver is possible when it is in standby mode. Transfer the data again after it has been released from standby mode.

CAD: Set up based on retention capacitor configuration of the TFT panel.

CAD = "0" Set this up when use Cst composition.

CAD = "1" Set this up when use Cadd composition.

VRP4-0: Control amplitude (positive polarity) of 64-grayscale. For details, see the amplitude adjusting circuit section.

VRN4-0: Control amplitude (negative polarity) of 64-grayscale. For details, see the Amplitude Adjusting Circuit section.

Note: BT2-0, DC2-0, AP2-0, SLP, CAD bits are for Power supply IC. Control according to the bits' values is executed by Power supply IC. For details, see the data sheet for the Power supply IC.

Power Control 3 (R0Ch)

Power Control 4 (R0Dh)

Power Control 5 (R0Eh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
W	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

Figure 10

VC2-0: Adjust reference voltage of VREG1OUT, VREG2OUT and VciOUT to optional rate of Vci. Also, when VC2 = "1", it is possible to stop the internal reference voltage generator. This leads to control for VREG1OUT/VciOUT with REGP and VREG2OUT with REGN externally.

VRL3-0: Set magnification of amplification for VREG2OUT voltage (voltage for the reference voltage, VREG2 while generating Vgoff.) It allows to magnify the amplification of REGN from -2 to -8.5 times.

PON: This is an operation starting bit for the booster circuit 3. PON = 0 is to stop and PON = 1 to start operation.

VRH3-0 : Set magnification of amplification for VREGOUT1 voltage(voltage for the reference voltage, VREG1 while generating VDH.) It allows to magnify the amplification of REGP from 1.45 to 2.85 times.

VCOMG: When VCOMG = 1, VcomL voltage can output to negative voltage (-5V).
When VCOMG = 0, VcomL voltage becomes GND and stops the amplifier of the negative voltage. Therefore, low power consumption is accomplished. Also, When VCOMG = 0 and when Vcom is driven in A/C, setting of the VDV4-0 is invalid. In this case, adjustment of Vcom/Vgoff A/C amplitude must be adjusted with VcomH using VCM4-0.

VDV4-0: Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. It is possible to set up from 0.6 to 1.23 times of VREG1. When Vcom is not driven in A/C, the set up is invalid.

VCM4-0: Set VcomH voltage (voltage of higher side when Vcom is driven in A/C.) It is possible to amplify from 0.4 to 0.98 times of VREG1 voltage. Also, when setting up VCM4-0 = 1111, stop the internal volume adjustment and adjust VcomH with external resistance from VcomR.

Note: VC2-0, VRL3-0, VRH4-0, VCOMG, VDV4-0, VCM4-0 bits are for Power supply IC. Control according to the bits' values is executed by Power supply IC. For details, see the data sheet for the Power supply IC.

Entry Mode (R05h)

Compare Register (R06h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

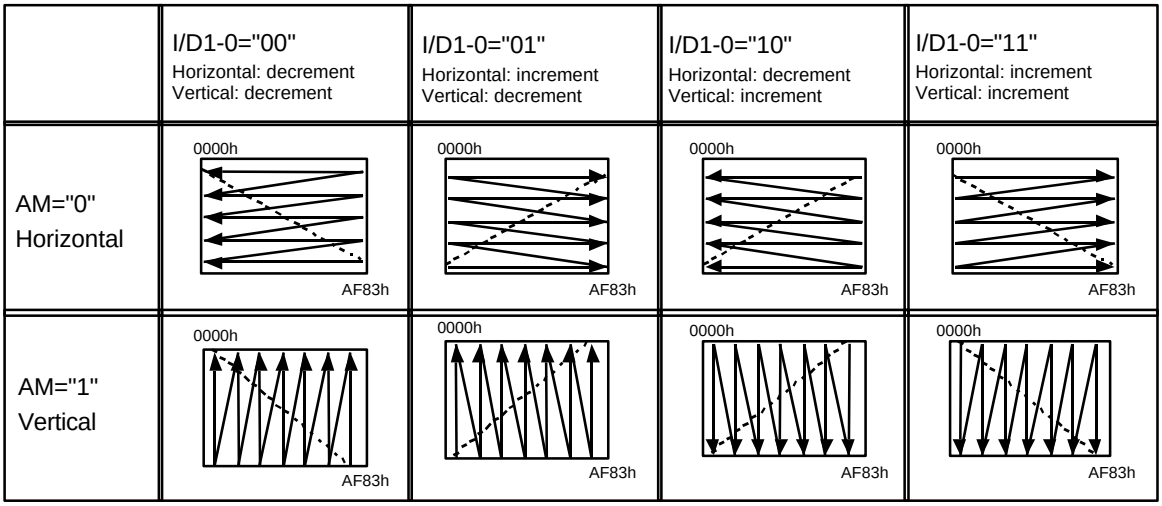
Figure 11

The write date sent from the microcomputer is modified in the HD66770 written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High Speed RAM Write Mode section.

I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD15-8) and lower (AD7-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.

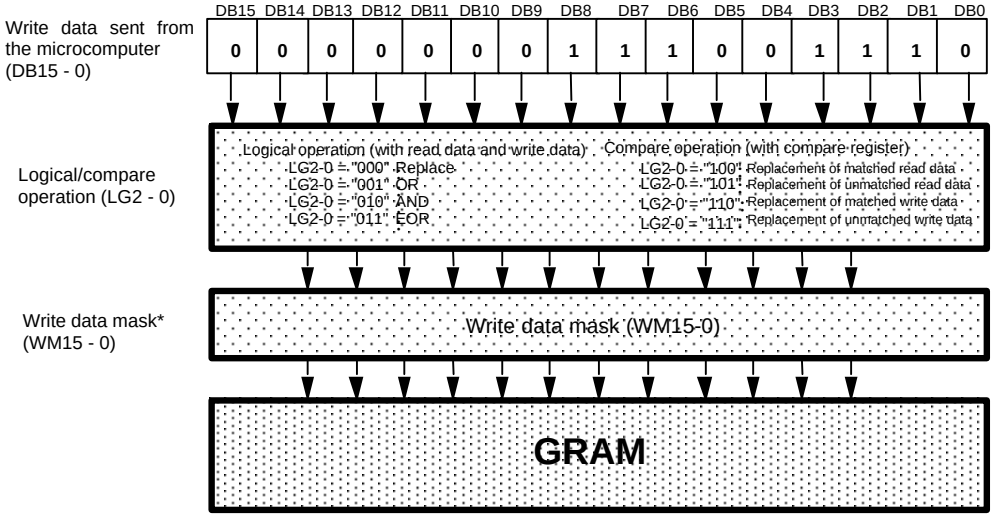


Note: When a window address range has been set the GRAM can only be written to within that range.

Figure 12 Address Direction Settings

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP11–0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.

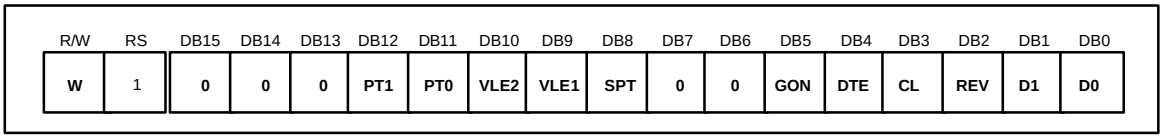
CP15–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer.



Note: The write data mask (WM11-0) is set by the register in the RAM Write Data Mask section.

Figure 13

Display Control (R07h)



R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

Figure 14 Display Control Instruction

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the Screen-division Driving Function section.

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll display
1	0	Scroll display	Fixed display
1	1	Setting disabled	

Table 12

CL: When CL = 1, number of colors is 8-color mode. For details, see the 8-color Display Mode section.

CL	Number of Display Colors
0	65,536
1	8

Table 13

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

REV: Displays all character and graphics display sections with reversal when REV = 1. Since the grayscale level can be reversed, display of the same data is enabled on normally-white and normally-black panels

i) Combination with the partial display

REV	GRAM data	Source output level							
		Display area		non-display area					
				PT1-0=(0.*)		PT1-0=(1.0)		PT1-0=(1.1)	
		VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"
0	16'h0000 ⋮ 16'hFFFF	V63 ⋮ V0	V0 ⋮ V63	V63	V0	GND	GND	Hi-z	Hi-z
1	16'h0000 ⋮ 16'hFFFF	V0 ⋮ V63	V63 ⋮ V0	V63	V0	GND	GND	Hi-z	Hi-z

Figure 15

ii) Combination with the D1-0

REV	GRAM data	Source output level							
		D1-0=(1.1)		D1-0=(1.0)		D1-0=(0.1)		D1-0=(0.0)	
		VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"	VCOM="L"	VCOM="H"
0	16'h0000 ⋮ 16'hFFFF	V63 ⋮ V0	V0 ⋮ V63	V63	V0	GND	GND	GND	GND
1	16'h0000 ⋮ 16'hFFFF	V0 ⋮ V63	V63 ⋮ V0	V63	V0	GND	GND	GND	GND

Figure 16

GON: Gate off level is GND when GON = 0.

DTE: DISPTMG output is fixed to GND when DTE = 0.

GON	Gate Output
0	Vgon/GND
1	Vgon/Vgoff

Table 14

DTE	DISPTMG Output
0	Halt (GND)
1	Operation (Vcc/GND)

Table 15

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be displayed instantly by setting D1 = 1. When D1 is 0, the display is off with all of the source outputs set to the GND level. Because of this, the HD66770 can control the charging current for the LCD with AC driving. Control the display on/off while control GON and DTE. For details, see the Instruction Set Up Flow.
When D1–0 = 01, the internal display of the HD66770 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.

Table 16 D Bits and Operation

D1	D0	Source Output	HD66770 Internal Display Operation	Control Signal (CL1, FLM, M)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Notes: 1. Writing from the microcomputer to the GRAM is independent from the state of D1–0.
2. In the sleep and standby modes, D1–0 = 00. However, the register contents of D1–0 are not modified.

Note: SPT and GON bits are for setting the gate driver. Control according to the bits' values is executed by the gate driver. For details, see the data sheet for the gate driver.

Gate Driver Interface Control (R0Ah)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0

Figure 17 Gate Driver Interface Control Instruction

IDX2-0: Index bits that select instructions for the gate driver/Power supply IC. The instruction that corresponds to the setting of gate driver and power supply IC is transferred, with the index, to the gate driver and the power supply IC via the serial interface. These instructions are transferred in bit rows as shown below. The upper 3 bits correspond to IDX2-0. The IDX2-0 setting at the time of transfer selects the instruction for the gate driver and the power supply IC as listed below.

To change an instruction setting on the gate driver and the power supply IC, first change the instruction bit on the HD66770 at first, then, select the instruction, which includes the changed instruction bit, from the list below, by setting IDX2-0 as required. The instruction is transferred to the gate driver/Power supply IC after TE bit is set to 1, and is executed**.**

TE: Serial transfer enable for the gate driver/power-supply IC. When 0 is read on TE bit, serial transfer is possible. Do not change the instruction during transfer. When 1 is written to TE bit, transfer starts. TE returning to 0 indicates the end of the transfer. Note that, serial transfer to the gate driver/Power supply IC requires 18 clock cycles at most. Do not change the instruction during the transfer.

* New instructions should be transferred to the gate driver / power supply IC soon after they have been set on the HD66770.

Table 17: the gate driver (HD 66770) instructions

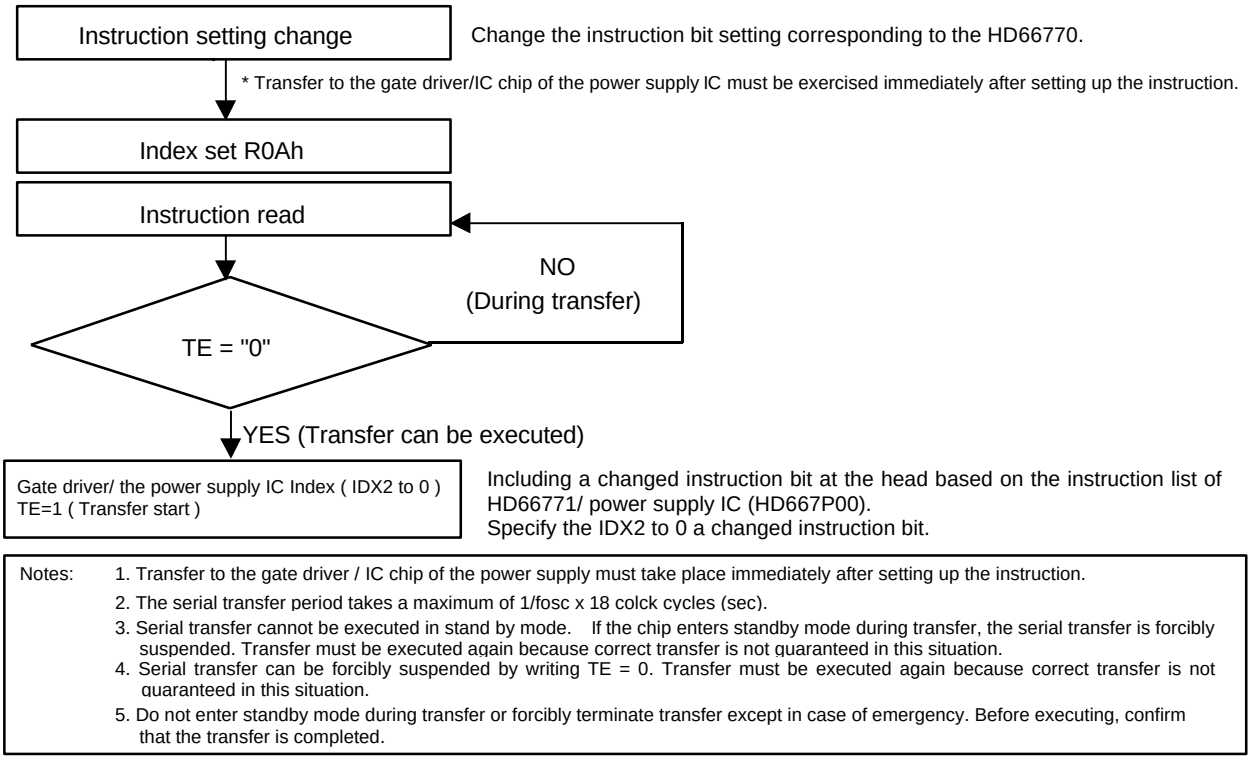
IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	*	GON	*	*	*	*	*	*	*	*	*	*	SLP
0	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*
0	1	0	*	*	*	*	*	*	*	*	*	*	*	*	*
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	0	0	GS	NL4	NL3	NL2	NL1	NL0	SCN4	SCN3	SCN2	SCN1	SCN0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	FLD1	FLD0

* Register for HD667P00

Table 18: Power supply IC (HD667P00) instructions

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	GON	VCOMG	BT2	BT1	BT0	DC2	DC1	DC	AP2	AP1	AP0	SLP
0	0	1	CAD	VRL3	VRL2	VRL1	VRL0	VRH4	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
0	1	0	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	VCM4	VCM3	VCM2	VCM1	VCM0
0	1	1	Setting disabled												
1	0	0	Setting disabled												
1	0	1	Setting disabled												
1	1	0	*	*	*	*	*	*	*	*	*	*	*	*	*
1	1	1	*	*	*	*	*	*	*	*	*	*	*	*	*

* Register for HD66771



Notes:
1. Transfer to the gate driver / IC chip of the power supply must take place immediately after setting up the instruction.
2. The serial transfer period takes a maximum of 1/fosc x 18 colck cycles (sec).
3. Serial transfer cannot be executed in stand by mode. If the chip enters standby mode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again because correct transfer is not guaranteed in this situation.
4. Serial transfer can be forcibly suspended by writing TE = 0. Transfer must be executed again because correct transfer is not guaranteed in this situation.
5. Do not enter standby mode during transfer or forcibly terminate transfer except in case of emergency. Before executing, confirm that the transfer is completed.

Figure 18 Gate Interface: Serial Transfer Sequence

Frame Cycle Control (R0Bh)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

Figure 19

RTN3-0: Set the 1H period.

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing drive line count, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

EQ1-0: EQ period can be set with EQ1-0.

Table 19

RTN3	RTN2	RTN1	RTN0	Clock cycles per Raster-row
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
	⋮			⋮
1	1	1	0	30
1	1	1	1	31

Table 20

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc = R-C oscillation frequency

Formula for the fram frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line + 8)}} \text{ [Hz]}$$

fosc: CR oscillation frequency
Line: Number of drive raster-row (NL bits)
Division ratio: DIV bit
Clock cycles per raster-row: RTN bits

Table 21

EQ1	EQ0	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle

SDT1-0: Set delay amount from the gate output signal falling edge of the source outputs.

Table 22

SDT1	SDT0	Delay amount of the source output
0	**0**	1 clock cycle
0	**1**	2 clock cycle
1	**0**	3 clock cycle
1	**1**	4 clock cycle

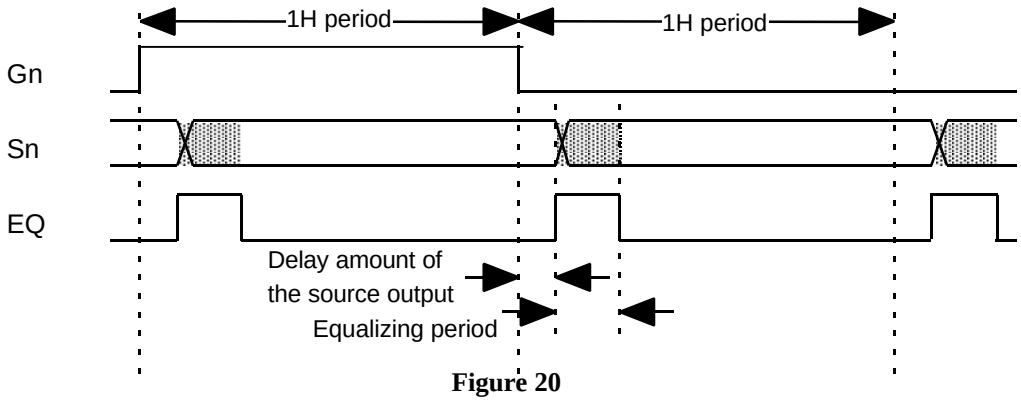


Figure 20

NO1-0: Set amount of non-overlap for the gate output.

Table 23

NO1	NO0	Amount of non-overlap
0	**0**	0 clock cycle
0	**1**	4 clock cycle
1	**0**	6 clock cycle
1	**1**	8 clock cycle

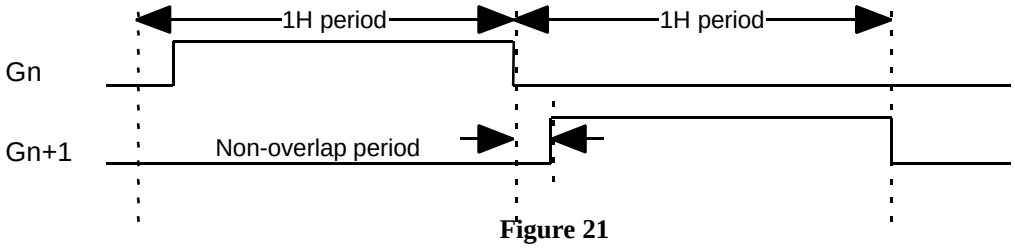


Figure 21

Gate Scan Position (R0Fh)

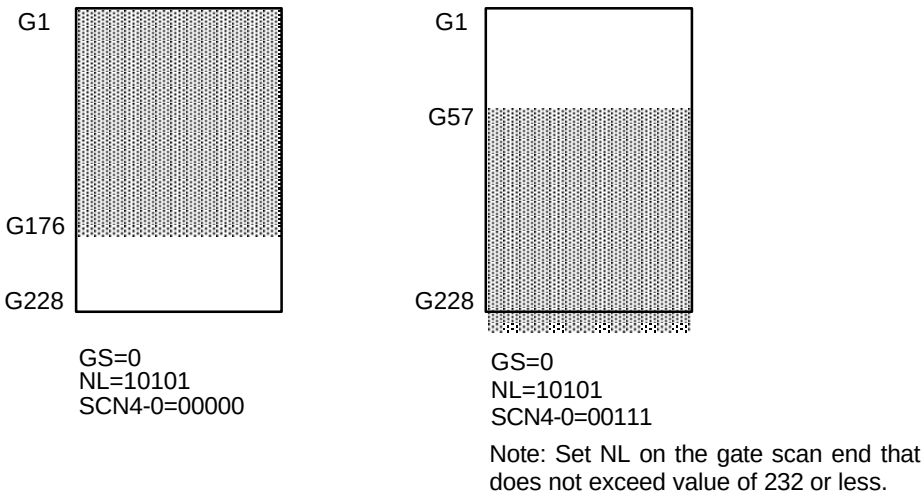
R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

Figure 22

SCN4-0 Set the scanning starting position of the gate driver.

SCN4	SCN3	SCN2	SCN1	SCN0	Scanning start position When GS=0	Scanning start position When GS=1
0	0	0	0	0	G1	G228
0	0	0	0	1	G9	G220
0	0	0	1	0	G17	G212
⋮					⋮	⋮
1	1	0	1	0	G209	G20
1	1	0	1	1	G217	G12

Table 24



Note: Set NL on the gate scan end that does not exceed value of 232 or less.

Figure 23: Relationship between NL and SCN set up value

Note: SCN4-0 bits are for setting the gate driver. Control according to the bits' values is executed by the gate driver. For details, see the data sheet for the gate driver.

Vertical Scroll Control (R11h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

Figure 24

VL7-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 176th can be scrolled for the number of the raster-row. After 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL7-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scroll length
0	0	0	0	0	0	0	0	0 raster-row
0	0	0	0	0	0	0	1	1 raster-row
0	0	0	0	0	0	1	0	2 raster-row
				⋮				⋮
1	0	1	0	1	1	1	0	174 raster-row
1	0	1	0	1	1	1	1	175 raster-row

Note: Do not set any higher raster-row than 175 ("AF"H)

Table 25

1st Screen Driving Position (R14h)

2nd Screen Driving Position (R15h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Figure 25

SS17–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver.

SE17–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS17–10 = 07H and SE17–10 = 10H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFH. For details, see the Screen-division Driving Function section.

SS27–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver. The second screen is driven when SPT = 1.

SE27–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SPT = 1, SS27–20 = 20H, and SE27–20 = AFH are set, the LCD driving is performed from G33 to G80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ AFH. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)

Vertical RAM Address Position (R17h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

Figure 26 Horizontal/Vertical RAM Address Position Instruction

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ 3Fh.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ AFh.

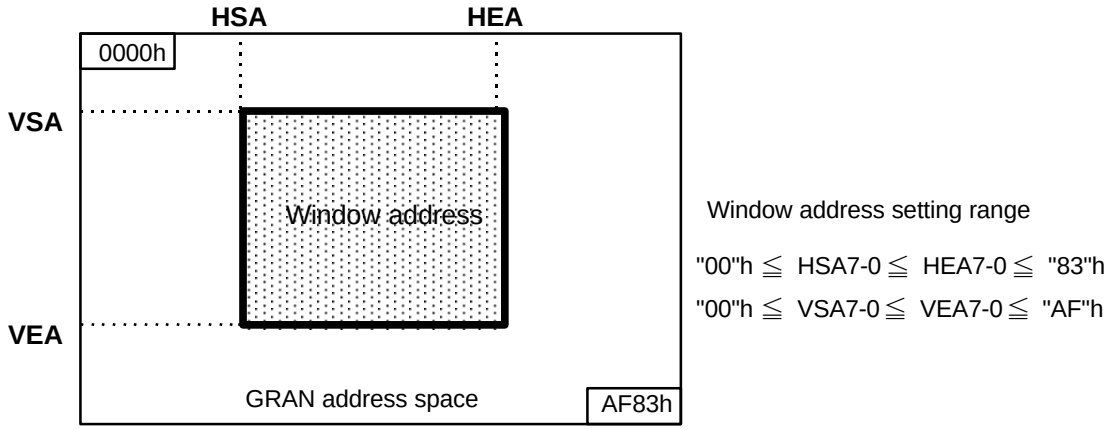


Figure 27 Window Address Setting Range

Note: 1. Ensure that the window address area is within the GRAM address space.
2. In high-speed write mode, data are written to GRAM in four-words. Thus, dummy write operations should be inserted depending on the window address area. For details, see the High-Speed Burst RAM Write Function section.
3. Set RAM address within the window address area. In high-speed write mode, set RAM address within the area containing dummy area. For details, see the High-Speed RAM Write Function section.

RAM Write Data Mask (R20h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

Figure 28 RAM Write Data Mask Instruction

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14 to 0 bits mask the write data of DB14 to 0 in a bit unit. For details, see the Graphics Operation Function section.

RAM Address Set (R21h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

Figure 29 RAM Address Set Instruction

AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

Table 26 GRAM Address Range in Eight-grayscale Mode

AD15 to AD0	GRAM Setting
"0000"H to "0083"H	Bitmap data for G1
"0100"H to "0183"H	Bitmap data for G2
"0200"H to "0283"H	Bitmap data for G3
"0300"H to "0383"H	Bitmap data for G4
⋮	⋮
"AC00"H to "AC83"H	Bitmap data for G173
"AD00"H to "AD83"H	Bitmap data for G174
"AE00"H to "AE83"H	Bitmap data for G175
"AF00"H to "AF83"H	Bitmap data for G176

Write Data to GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
W	1	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

Figure 30

WD15–0 : Write 16-bit data to the GRAM. This data selects the grayscale level. After a write, the address is automatically updated according to the AM and I/D bit settings. During the standby mode, the GRAM cannot be accessed.

	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
GRAM Write Data	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0
	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0

1 pixel

Figure 31

Table 27 GRAM Data and Grayscale Level

GRAM Data Set-up G	GRAM Data Set-up R/B	Selected Grayscale N	Selected Grayscale P	GRAM Data Set-up G	GRAM Data Set-up R/B	Selected Grayscal N	Selected Grayscal P	GRAM Data Set-up G	GRAM Data Set-up R/B	Selected Grayscal N	Selected Grayscal P	GRAM Data Set-up G	GRAM Data Set-up R/B	Selected Grayscal N	Selected Grayscal P
000000	00000	V0	V63	010000	01000	V16	V47	100000	-	V32	V31	110000	-	V48	V15
000001	-	V1	V62	010001	-	V17	V46	100001	10000	V33	V30	110001	11000	V49	V14
000010	00001	V2	V61	010010	01001	V18	V45	100010	-	V34	V29	110010	-	V50	V13
000011	-	V3	V60	010011	-	V19	V44	100011	10001	V35	V28	110011	11001	V51	V12
000100	00010	V4	V59	010100	01010	V20	V43	100100	-	V36	V27	110100	-	V52	V11
000101	-	V5	V58	010101	-	V21	V42	100101	10010	V37	V26	110101	11010	V53	V10
000110	00011	V6	V57	010110	01011	V22	V41	100110	-	V38	V25	110110	-	V54	V9
000111	-	V7	V56	010111	-	V23	V40	100111	10011	V39	V24	110111	11011	V55	V8
001000	00100	V8	V55	011000	01100	V24	V39	101000	-	V40	V23	111000	-	V56	V7
001001	-	V9	V54	011001	-	V25	V38	101001	10100	V41	V22	111001	11100	V57	V6
001010	00101	V10	V53	011010	01101	V26	V37	101010	-	V42	V21	111010	-	V58	V5
001011	-	V11	V52	011011	-	V27	V36	101011	10101	V43	V20	111011	11101	V59	V4
001100	00110	V12	V51	011100	01110	V28	V35	101100	-	V44	V19	111100	-	V60	V3
001101	-	V13	V50	011101	-	V29	V34	101101	10110	V45	V18	111101	11110	V61	V2
001110	00111	V14	V49	011110	01111	V30	V33	101110	-	V46	V17	111110	-	V62	V1
001111	-	V15	V48	011111	-	V31	V32	101111	10111	V47	V16	111111	11111	V63	V0

Read Data from GRAM (R22h)

R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R	1	RD 15	RD 14	RD 13	RD 12	RD 11	RD 10	RD 9	RD 8	RD 7	RD 6	RD 5	RD 4	RD 3	RD 2	RD 1	RD 0

Figure 32 Read Data from GRAM Instruction

RD15–0: Read 16-bit data from the GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB15–0) becomes invalid and the second-word read is normal.

When bit processing, such as a logical operation, is performed within the HD66770, only one read can be processed since the latched data in the first word is used.

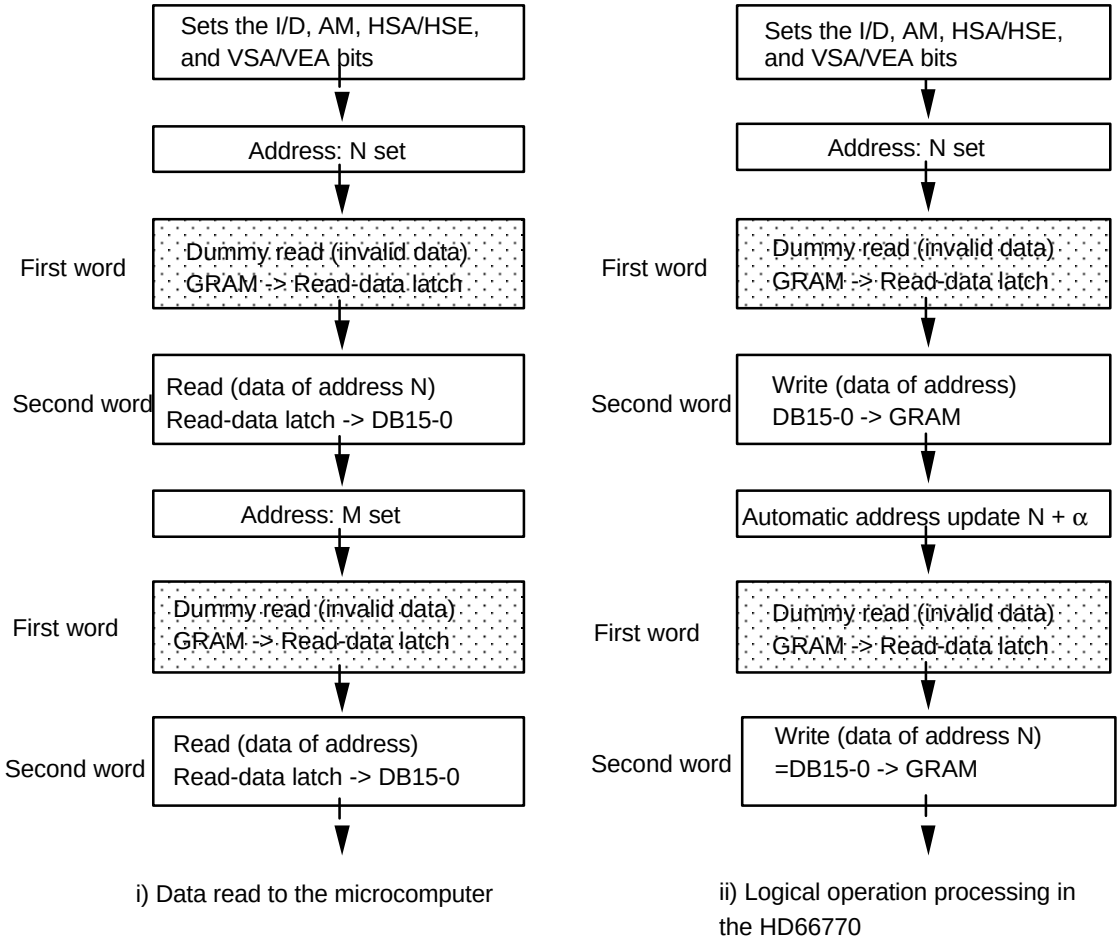


Figure 33 GRAM Read Sequence

Gamma Control (R30h to R37h, R3F)

	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R30	W	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00
R31	W	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20
R32	W	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40
R33	W	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00
R34	W	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00
R35	W	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20
R36	W	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40
R37	W	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00
R3F	W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VDR1	VDR0

Table 28

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

PRN12-00: Gradient adjustment register for the negative polarity output

VDR1-0: Adjustment register for the grayscale reference value.

For details, see the Gamma Adjustment Function.

Instruction List (HD66770)

Reg. No.	Register Name			Upper Code								Lower Code								Description	Execution cycle
		R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
IR	Index	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Sets the index register value.	0
SR	Status read	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	Reads the driving raster-row position (L7-0).	0
R00h	Start oscillation	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	Starts the oscillation mode.	10 ms
	Device code read	1	1	0	0	0	0	0	1	1	1	0	1	1	1	0	0	0	0	Reads 0770H.	0
R01h	Driver output control	0	1	0	0	0	0	0	0	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0	Sets the gate driver shift direction (GS), source driver shift direction (SS), and number of driving lines (NL4-0).	0
R02h	LCD-driving-waveform control	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	Sets the LCD drive AC waveform (B/C), number of interlaced field (FLD1-0), EOR output (EOR), and the number of n-raster-rows (NW5-0) at C-pattern AC drive.	0
R03h	Power control 1	0	1	0	0	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB	Sets the standby mode (STB), LCD power on (AP1-0), sleep mode (SLP), boosting cycle (DC2-0), boosting output multiplying factor (BT3-0), and source op-amp on (SAP2-0).	0
R04h	Power control 2	0	1	CAD	0	0	VRN4	VRN3	VRN2	VRN1	VRN0	0	0	0	VRP4	VRP3	VRP2	VRP1	VRP0	Sets the grayscale adjusting generator (VRN4-0, VRP4-0) and configuration of retention volume (CAD).	0
R05h	Entry mode	0	1	0	0	0	0	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	Specifies the logical operation (LG2-0), AC counter mode (AM), increment/decrement mode (I/D1-0) and high-speed-write mode (HWM).	0
R06h	Compare register	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	Sets the compare register (CP15-0).	0
R07h	Display control	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0	Specifies display on (D1-0), reversed display (REV), number of display colors (CL), DISPTMG enable (DTE), gate output on (GON), screen division driving (SPT), and vertical scroll (VLE2-1) and source output condition (PT1-0).	0
R0Ah	COM driver interface control	0	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0	Specifies the serial transfer enable (TE) and index for the power supply transfer instructions (IDX2-0).	0
		1	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0		0
R0Bh	Frame cycle control	0	1	NO1	NO0	STD1	STD0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	Sets the 1H period (RTN3-0) and operating clock frequency-division ratio (DIV1-0), the equalizing period (EQ1-0), delay volume of the source output (STD1-0), non-overlap volume of the gate output (NO1-0).	0
R0Ch	Power control 3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	Sets an adjustment factor for the Vci voltage (VC2-0).	0
R0Dh	Power control 4	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0	Sets the amplification factor for VREGOUT1 voltage (VRH4-0) and for VREGOUT2 voltage (VRL3-0).	0
R0Eh	Power control 5	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0	Sets VcomH voltage (VCM4-0), AC-cycle oscillation of Vcom and Vgoff (VDV3-0) and voltage of VCOM (VCOMG)	0
R0Fh	Gate scanning starting position	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0	Sets the scanning starting position (SCN4-0) of the gate driver.	0
R11h	Vertical scroll control	0	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Specifies the screen display scroll volume (VL7-0).	0
R14h	1st screen driving position	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	Sets 1st-screen driving start (SS17-10) and end (SE17-10).	0
R15h	2nd screen driving position	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	Sets 2nd-screen driving start (SS27-20) and end (SE27-20).	0
R16h	Horizontal RAM address position	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	Sets the start (HSA7-0) and end (HEA7-0) of the horizontal RAM address range.	0
R17h	Vertical RAM address position	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	Sets the start (VSA7-0) and end (VEA7-0) of the vertical RAM address range.	0
R20h	RAM write data mask	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	Specifies write data mask (WM15-0) at RAM write.	0
R21h	RAM address set	0	1	AD15-8 (upper)								AD7-0 (lower)								Initially sets the RAM address to the address counter (AC).	0
R22h	Write data to RAM	0	1	Write Data (upper)								Write Data (lower)								Write data to RAM.	0
	Write data from RAM	1	1	Read Data (upper)								Read Data (lower)								Read data from RAM.	0

R30h	Gamma control (1)	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	Adjust the Gamma control.	0
R31h	Gamma control (2)	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	Adjust the Gamma control.	0
R32h	Gamma control (3)	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	Adjust the Gamma control.	0
R33h	Gamma control (4)	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	Adjust the Gamma control.	0
R34h	Gamma control (5)	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	Adjust the Gamma control.	0
R35h	Gamma control (6)	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	Adjust the Gamma control.	0
R36h	Gamma control (7)	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	Adjust the Gamma control.	0
R37h	Gamma control (8)	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	Adjust the Gamma control.	0
R3Fh	Gamma control (9)	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VDR1	VDR0	Adjust the Gamma control.	0

Note:
1. * means 'doesn't matter'.
2. After setting TE = 1, 18 (max.) clock cycles are required for a serial transfer to be completed. During that time, do not change the bits of instructions, which are to be transferred.
3. High-speed write mode is available only for the RAM writing.

Reset Function

The HD66770 is internally initialized by RESET input. Reset the gate driver/Power supply IC as its settings are not automatically reinitialized when the HD66770 is reset. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization:

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SS = 0, CS = 0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Power control 1 (SAP2-0 = 000, BT2-0 = 000, DC2–0 = 000, AP2–0 = 000: LCD power off, SLP = 0, STB = 0: Standby mode off)
5. Power control 2 (CAD = 0, VRN4-0 = 0000, VRP4-0 = 0000
6. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode)
7. Compare register (CP15–0: 0000000000000000)
8. Display control (PT1-0 = 00, VLE2–1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL = 0: 65536 color mode, REV = 0, D1–0 = 00: Display off)
9. COM driver interface control (TE = 0, IDX2-0 = 000)
10. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, EQ1-0 = 00: no equalizer, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clock cycle in 1H period)
11. Power control 3 (VC2-0 = 000)
12. Power control 4 (VRL3-0 = 0000, PON=0 VRH3-0= 00000)
13. Power control 5 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000
14. Gate scanning starting position (SCN4-0 = 00000)
15. Vertical scroll (VL7–0 = 0000000)
16. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
17. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
18. Horizontal RAM address position (HEA7-0 = 10000011, HSA7-0 = 00000000)
19. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
20. RAM write data mask (WM15–0 = 0000H: No mask)
21. RAM address set (AD15–0 = 0000H)
22. Gamma control
    (PKP02–00 = 000, PKP12–10 = 000, PKP22–20 = 000, PKP32–30 = 000, PK42–40 = 000, PKP52–50 = 000, PRP02–00 = 000, PRP12–10 = 000)
    (PKN02–00 = 000, PKN12–10 = 000, PKN22–20 = 000, PKN32–30 = 000, PKN42–40 = 000, PKN52–50 = 000, PRN02–00 = 000, PRN12–10 = 000)
    (VDR–1 = “00”)

GRAM Data Initialization:

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = 00).

Output Pin Initialization:

1. LCD driver output pins (Source output): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal
3. Gate interface signals (GCS*, GCL, and GDA): Halt
4. Timing signals (CL1, M, FLM, DISPTMG, and DCCLK): Halt

Parallel Data Transfer

16-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/GND level allows 68-system E-clock-synchronized 16-bit parallel data transfer. Setting the IM2/1/0 to the GND/Vcc/GND level allows 80-system 16-bit parallel data transfer. When the number of buses or the mounting area is limited, use an 8-bit bus interface.

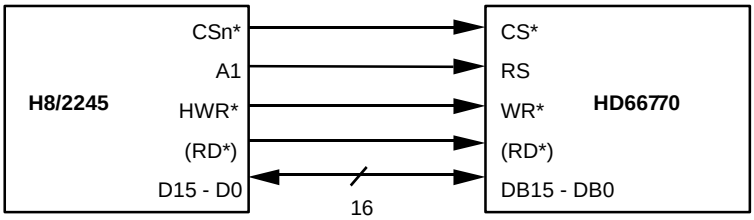


Figure 34 Interface to 16-bit Microcomputer

8-bit Bus Interface

Setting the IM2/1/0 (interface mode) to the GND/GND/Vcc level allows 68-system E-clock-synchronized 8-bit parallel data transfer using pins DB15–DB8. Setting the IM1/0 to the Vcc/Vcc level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB7–DB0 to the Vcc or GND level. Note that the upper bytes must also be written when the index register is written to.

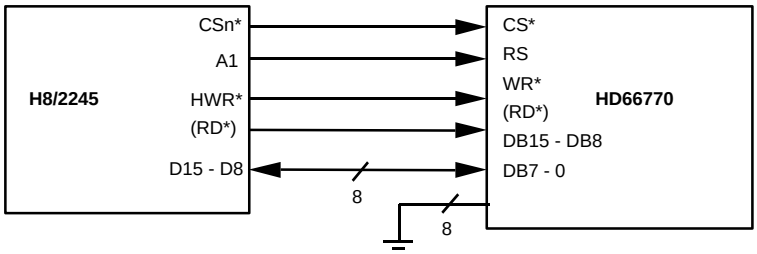


Figure 35 Interface to 8-bit Microcomputer

Note: Transfer synchronization function for an 8-bit bus interface
The HD66770 supports the transfer synchronization function which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.

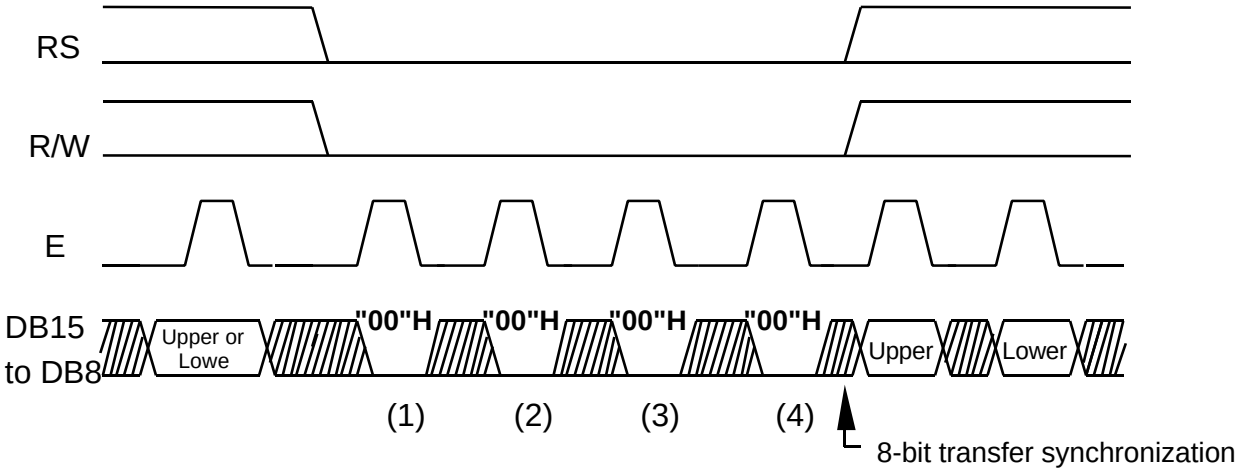


Figure 36 8-bit Transfer Synchronization

Serial Data Transfer

Setting the IM1 pin to the GND level and the IM2 pin to the Vcc level allows standard clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at Vcc or GND.

The HD66770 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66770 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66770. The HD66770, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66770 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

After receiving the start byte, the HD66770 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66770 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The HD66770 starts to read correct RAM data from the fifth byte.

Table 30 Start Byte Format

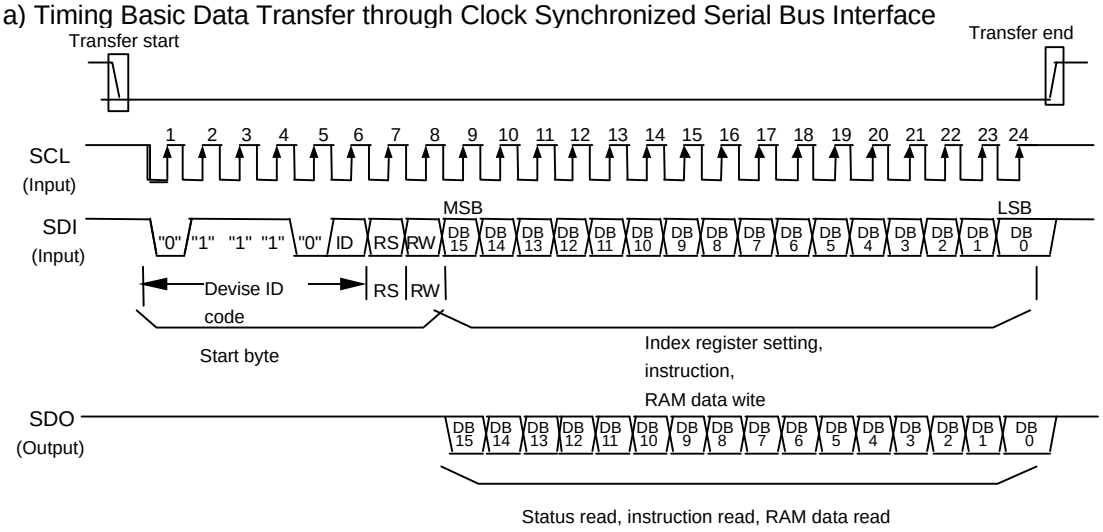
Transfer Bit	**S**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

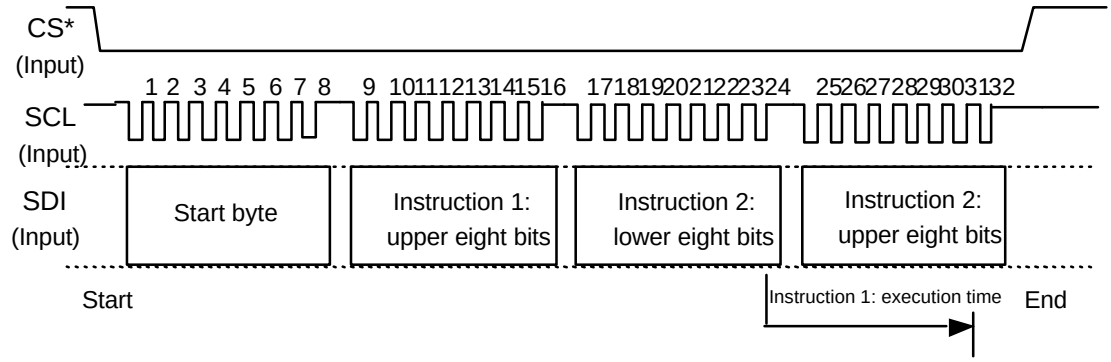
Table 31 RS and R/W Bit Function

RS	**R/W**	**Function**
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

a) Timing Basic Data Transfer through Clock Synchronized Serial Bus Interface

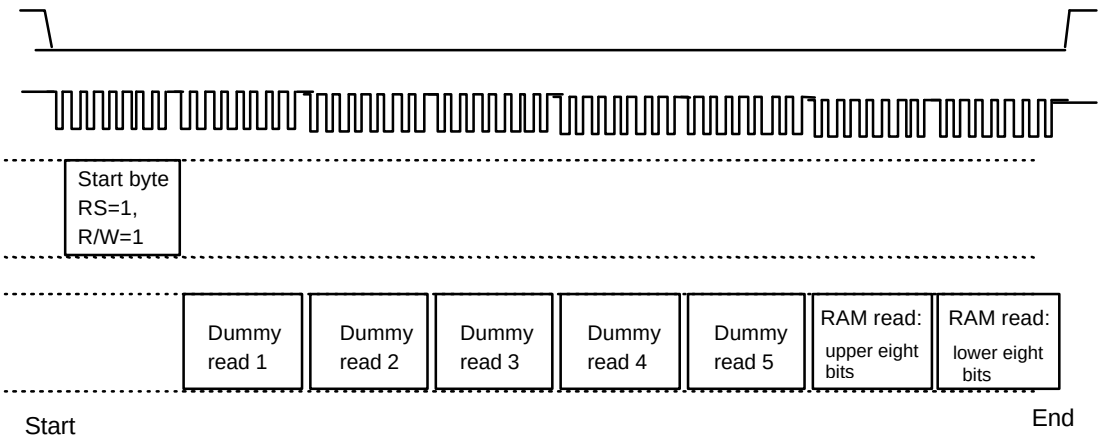


b) Timing of Consecutive Data-Transfer through Clock-synchronized serial Bus Interface



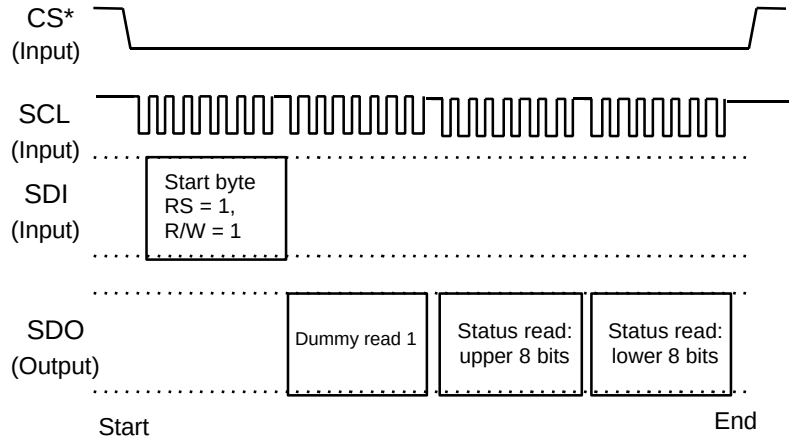
Note: The first byte after the start byte is always the upper eight bits.

c) RAM-Data Read-Transfer Timing



Note: Five bytes of the RAM read data after the start byte are invalid. The HD66770 starts to read the correct RAM data from the sixth byte.

d) Status Read / Instruction Read



Note: One byte of the read data after the start byte are invalid.
The HD66770 starts to read the correct data from the second byte.

Figure 38: Procedure for Transfer on Clock-Synchronized Serial Bus Interface (2)

High-Speed Burst RAM Write Function

The HD66770 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66770 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

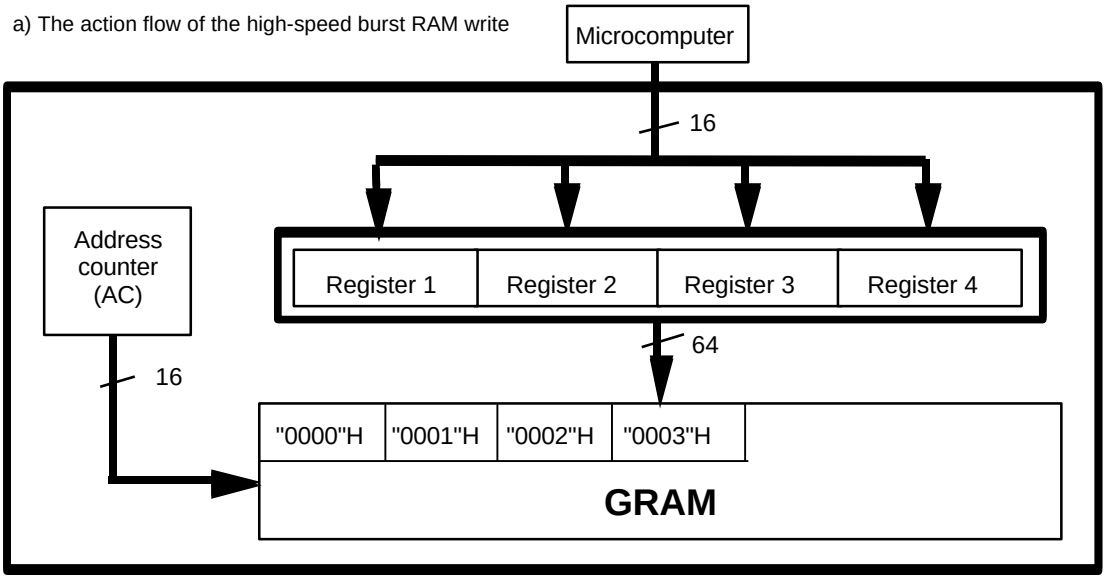
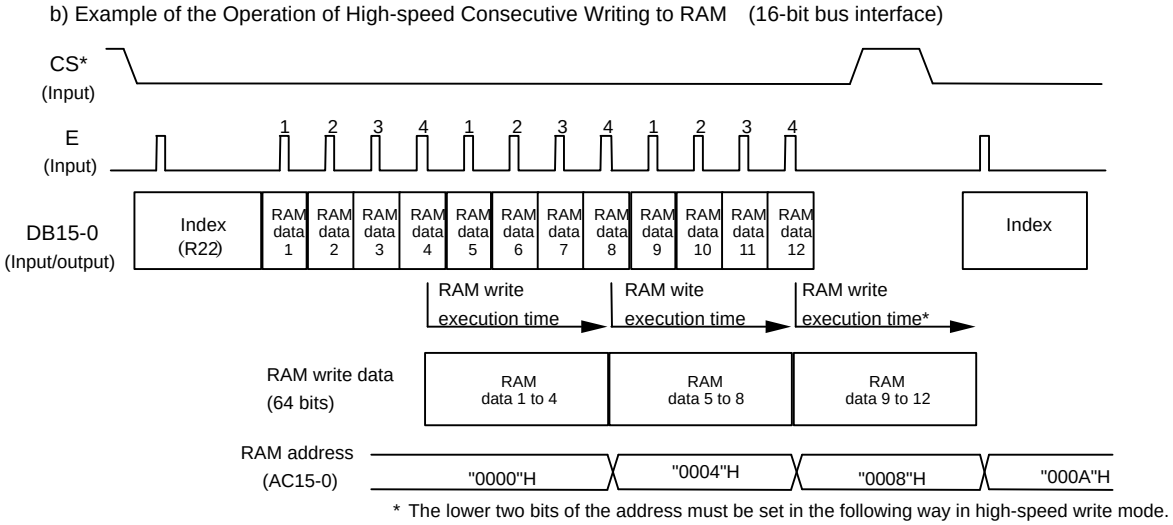


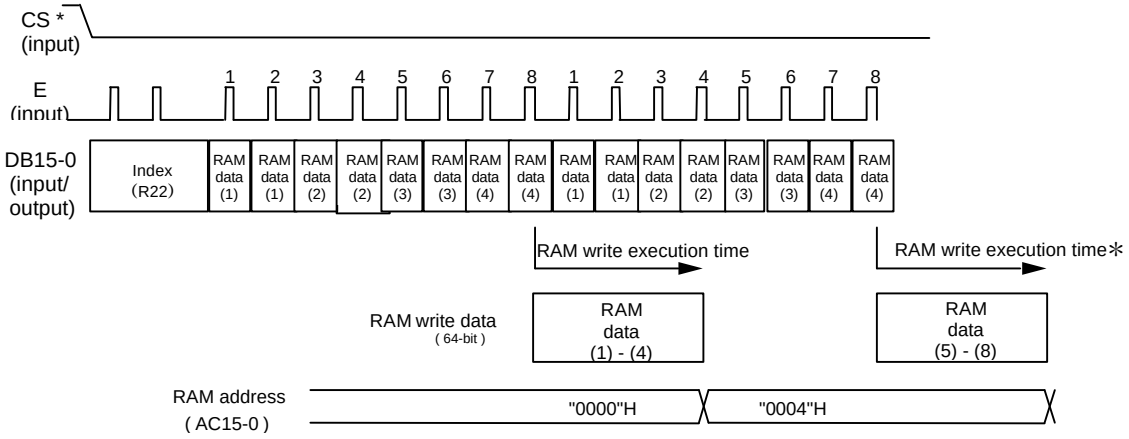
Figure 42 Flow of Operation in High-Speed Consecutive Writing to RAM



* The lower two bits of the address must be set in the following way in high-speed write mode.
When ID0 becomes 0, the lower two bits of the address must be set to 11
When ID1 becomes 1, the lower two bits of the address must be set to 00.

Note: When a high-speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.

C) Example of the Operation of High-Speed Consecutive Writing to RAM (8-bit bus interface)



* The lower two bits of the address must be set in the following way in high-speed write mode.
When ID0 becomes 0, the lower two bits of the address must be set to 11.
When ID1 becomes 0, the lower two bits of the address must be set to 00.

By using high-speed burst RAM write function, data is written to RAM each four words. Therefore when using 8-bit bus interface, data will be stored 8 times to internal register before written to RAM

When high-speed RAM write mode is used, note the following.

Notes: 1. The logical and compare operations cannot be used.

2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.

   *When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.

   *When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.

3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
4. When the index register and RAM data write (R22h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.
5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

Table 32 Comparison between Normal and High-Speed RAM Write Operations

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	Set necessary more than four word

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly by inserting dummy write operations so that RAM access counts become 4N as shown in the tables below.
Dummy write operations may have to be inserted as the first or last operations for a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Number of dummy write operations of a row must be 4N.

Table 33 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations to be Inserted at the Start of a Row
0	0	0
0	1	1
1	0	2
1	1	3

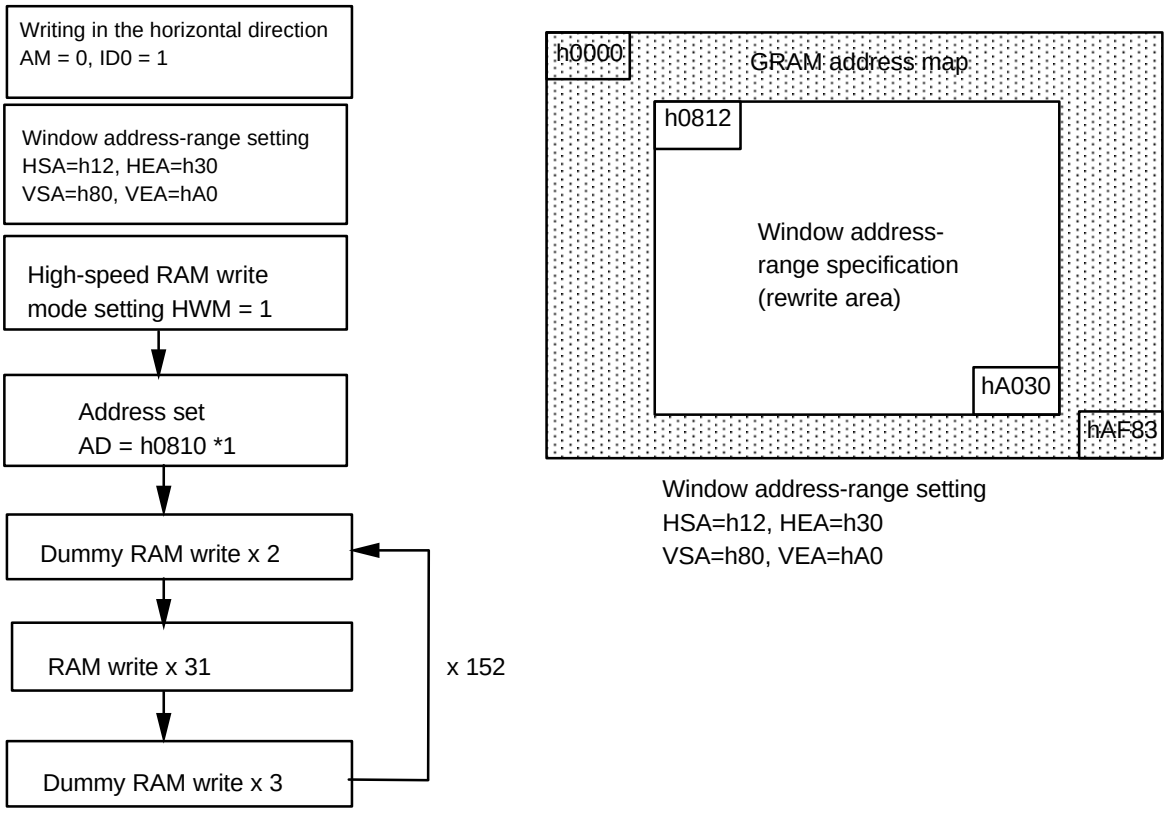
Table 34 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations to be Inserted at the End of a Row
0	0	3
0	1	2
1	0	1
1	1	0

Each row of access must consist of $4 \times N$ operations, including the dummy writes.
Horizontal access count =first dummy write count + write data count + last dummy write count = $4 \times N$

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).



Note: The address set for the high-speed RAM write must be 00 or 11 according to the value of the ID0 bit. Only RAM in the specified window address-range will be over written.

Figure 45: Example of the High-Speed RAM Write with a Window Address-Range Specification

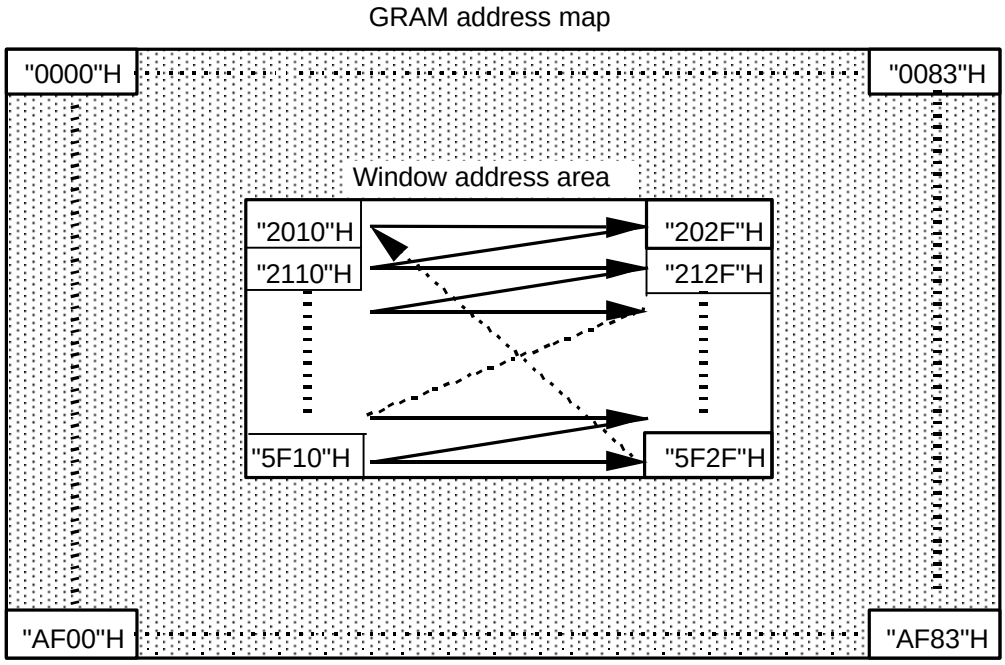
Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA7-0) or the vertical address register (start: VSA7-0, end: VEA7-0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]
(horizontal direction) 00H ≤ HSA7-0 ≤ HEA7-0 ≤ 83H
(vertical direction) 00H ≤ VSA7-0 ≤ VEA7-0 ≤ AFH
[Restriction on address settings during the window address]
(RAM address) HSA7 to 0 ≤ AD7-0 ≤ HEA7-0
VSA7-0 ≤ AD15-8 ≤ VEA7-0
Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.
ID0=0: The lower two bits of the address must be set to 11.
ID0=1: The lower two bits of the address must be set to 00.



Window address-range specification area
HSA7-0 = "10"H、HSE7-0 = "2F"H
VSA7-0 = "20"H、VEA7-0 = "5F"H

I/D = 1 (increment)
AM = 0 (horizontal writing)

Figure 46 Example of Address Operation in the Window Address Specification

Graphics Operation Function

The HD66770 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 16-bit write data.
2. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match.

Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Table 35 Graphics Operation

	Bit Setting			
Operation Mode	**I/D**	**AM**	**LG2–0**	**Operation and Usage**
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal-border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal-border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal-border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

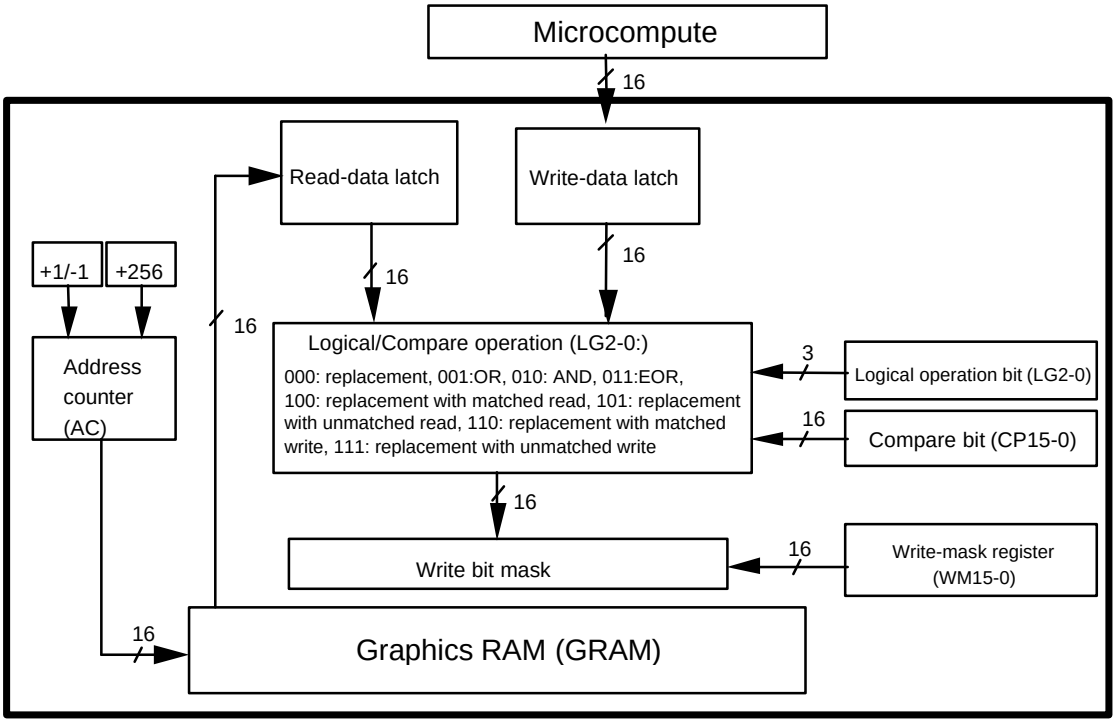


Figure 47 Data Processing Flow of the Graphic Operation

Write-data Mask Function

The HD6677- has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM15–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.

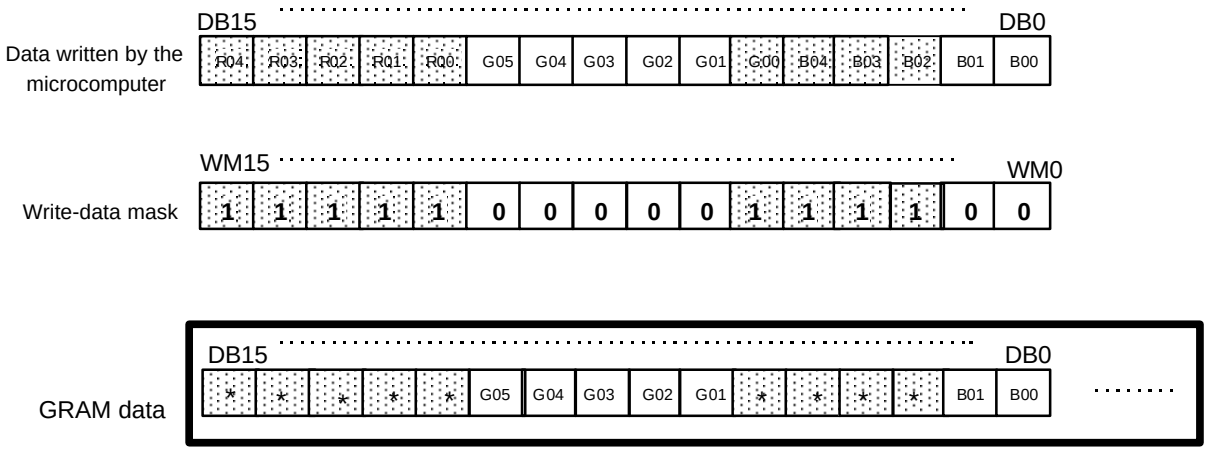


Figure 48 Example of Write-data Mask Function Operation

Graphics Operation Processing

1. Write mode 1: AM = 0, LG2–0 = 000

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

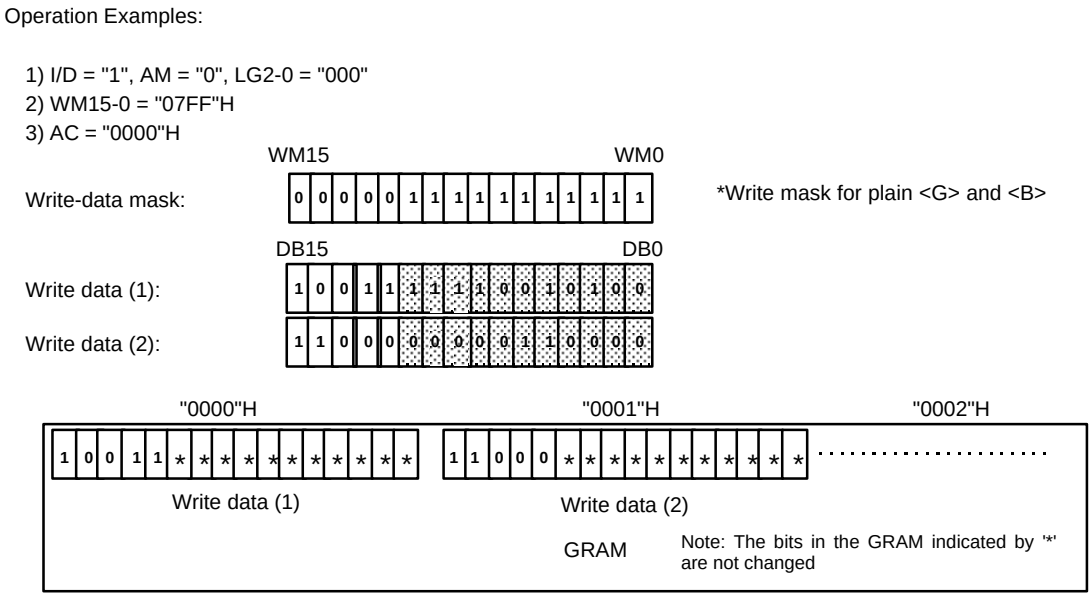


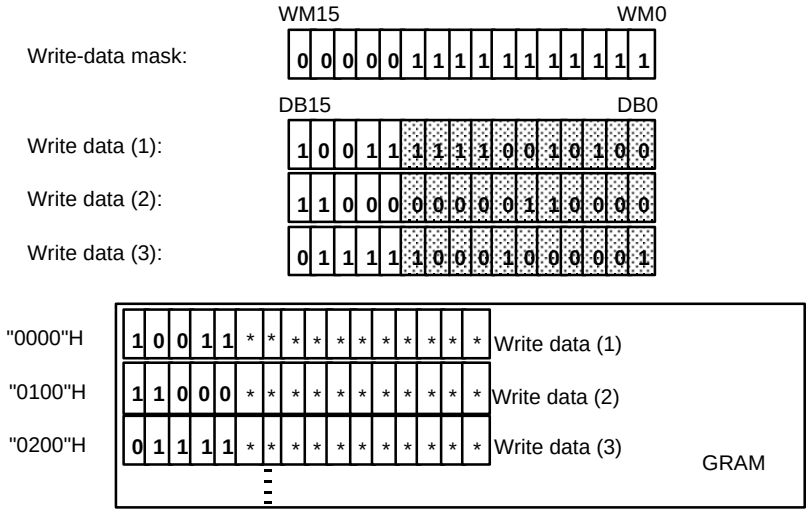
Figure 49 Writing Operation of Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D = "1", AM = "1", LG2-0 = "000"
2) WM15-0 = "07FF"H
3) AC = "0000"H



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "000"H.

Figure 50 Writing Operation of Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP15–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.

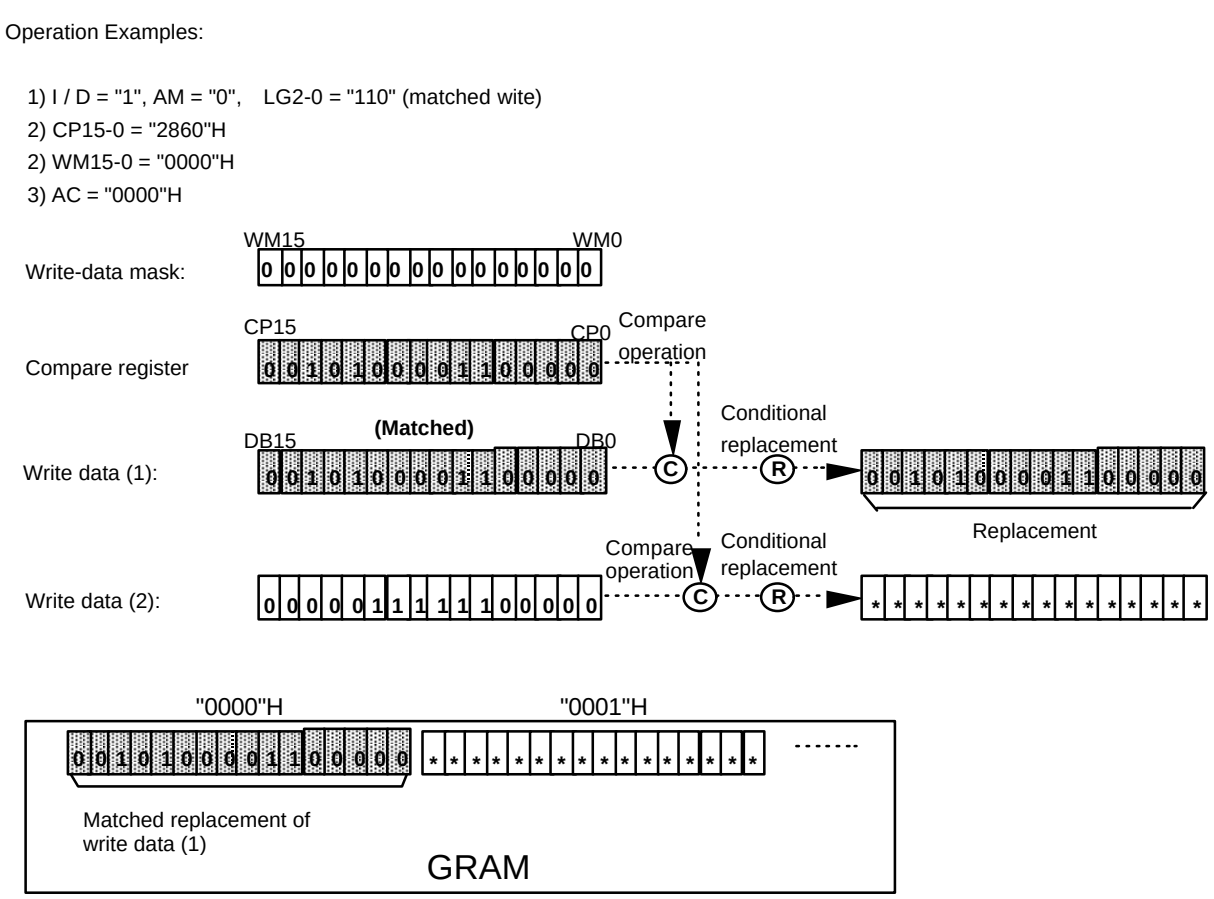


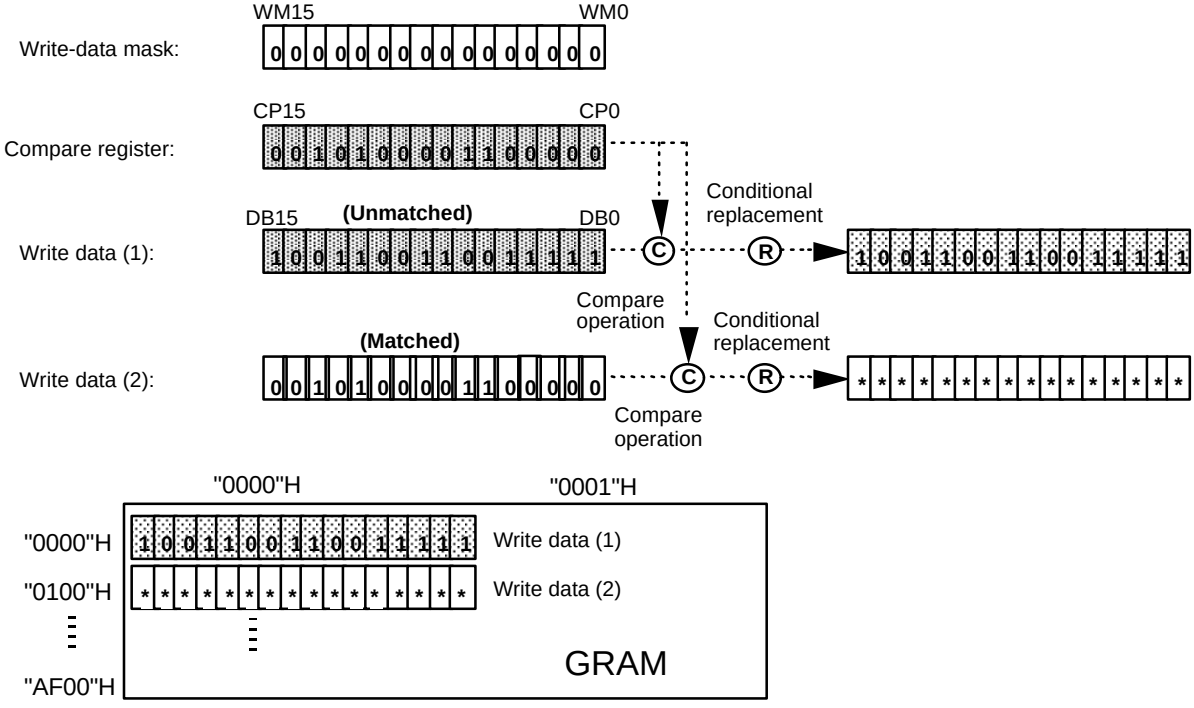
Figure 51 Writing Operation of Write

4. Write mode 4: AM = 1, LG2–0 = 110/111

This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP15–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I/D = "1", AM = "1", LG2-0 = "111" (unmatched write)
2) CP15-0 = "2860"H
2) WM15-0 = "0000"H
3) AC = "0000"H



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

Figure 52 Writing Operation of Write Mode 4

5. Read/Write mode 1: AM = 0, LG2–0 = 001/010/011

This mode is used when the data is horizontally written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

Operation Examples:

1) I/D = "1", AM = "0", LG2-0 = "001"(OR)
2) WM15-0 = "0000"H
3) AC = "0000"H

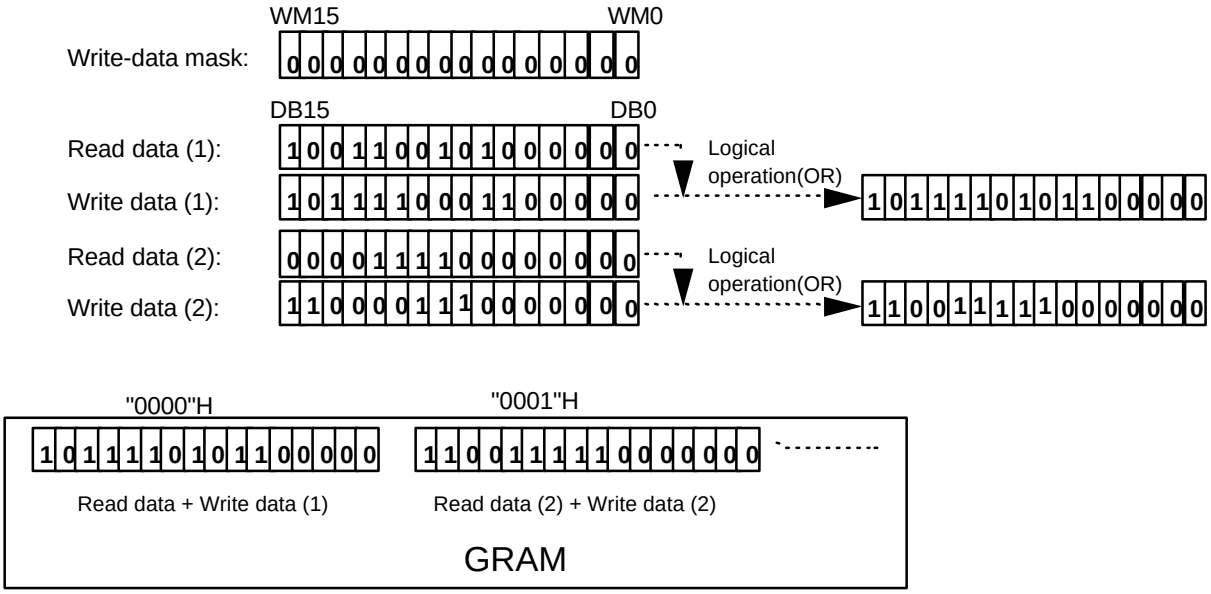
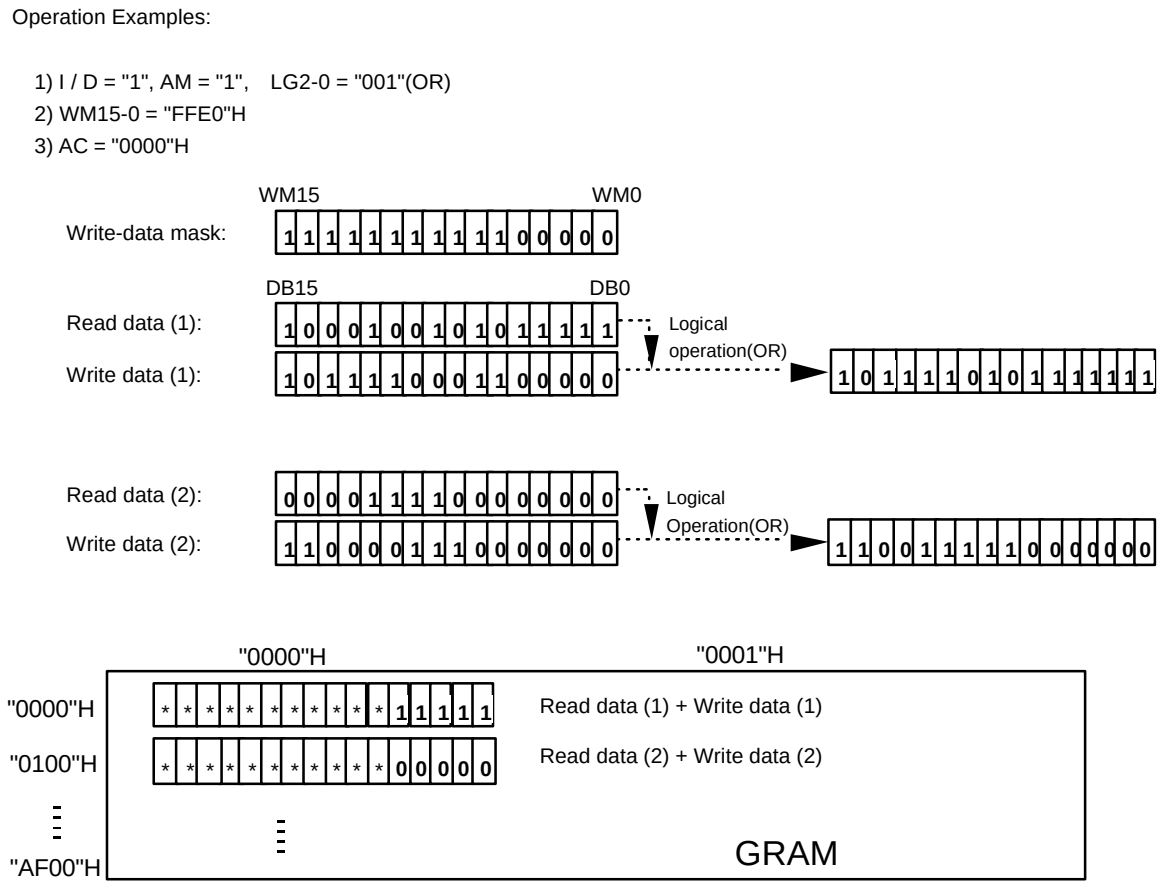


Figure 53 Writing Operation of Read/Write Mode 1

6. Read/Write mode 2: AM = 1, LG1–0 = 001/010/011

This mode is used when the data is vertically written at high speed by performing a logical operation with the original data. It reads the display data (original data), which has already been written in the GRAM, performs a logical operation with the write data sent from the microcomputer, and rewrites the data to the GRAM. This mode can read the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as for the write operation since the read operation of the original data does not latch the read data into the microcomputer and temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

Figure 54 Writing Operation of Read/Write Mode 2

7. Read/Write mode 3: AM = 0, LG2–0 = 100/101

This mode is used when the data is horizontally written by comparing the original data and the set value of compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the comparison satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edges of the GRAM.

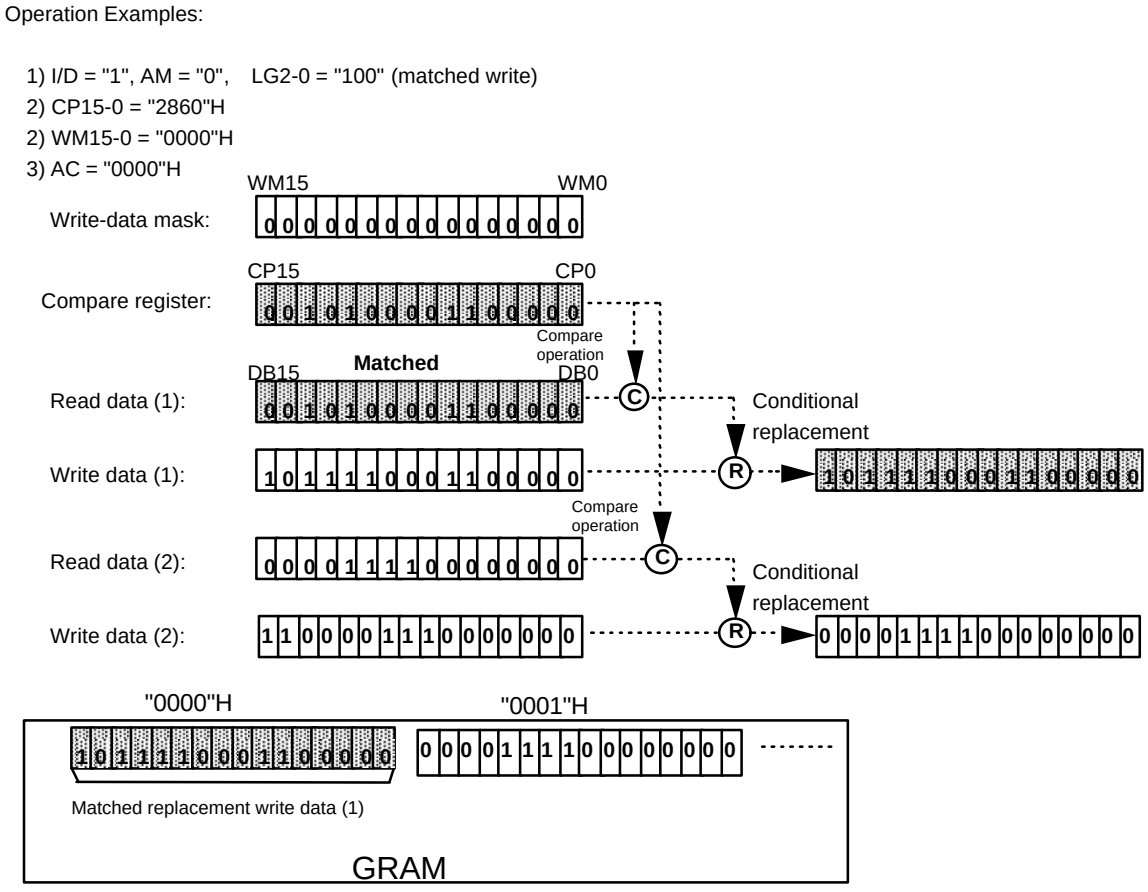


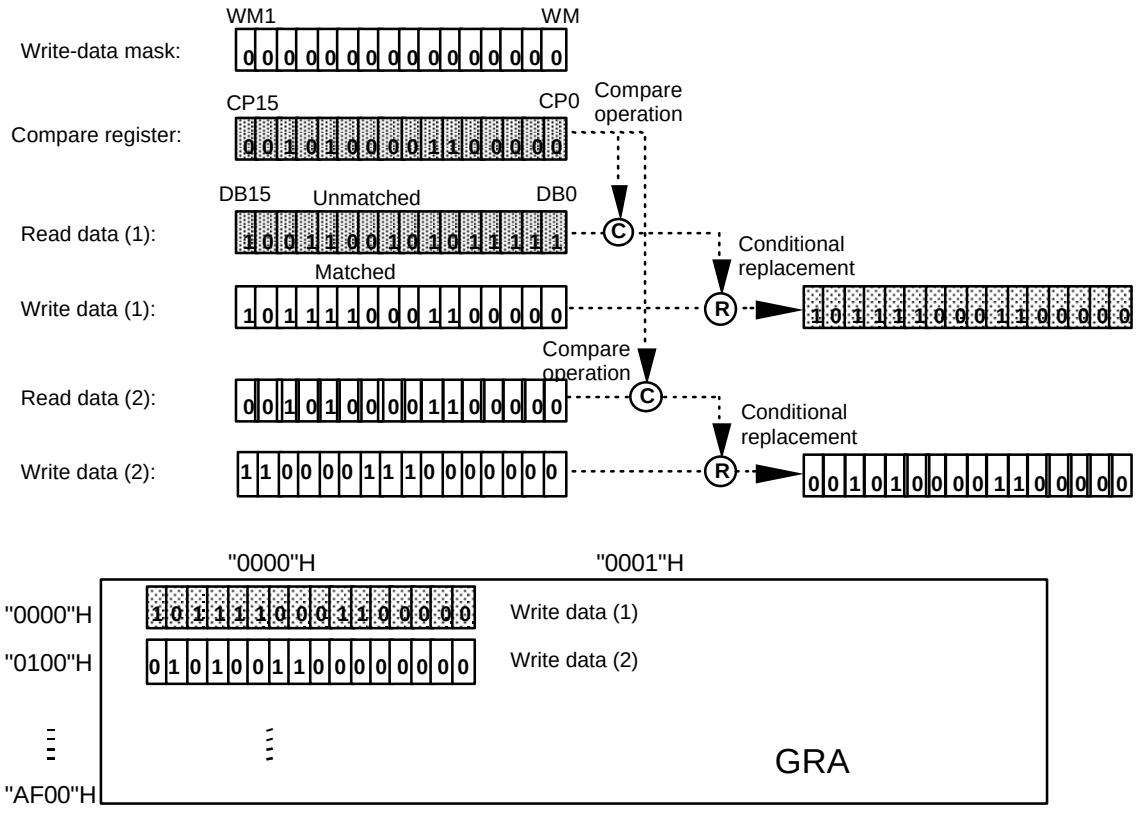
Figure 55 Writing Operation of Read/Write Mode 3

8. Read/Write mode 4: AM = 1, LG2–0 = 100/101

This mode is used when the data is vertically written by comparing the original data and the set value of the compare register (CP15–0). It reads the display data (original data), which has already been written in the GRAM, compares the original data and the set value of the compare register in byte units, and writes the data sent from the microcomputer to the GRAM only when the result of the compare operation satisfies the condition. This mode reads the data during the same access-pulse width (68-system: enabled high level, 80-system: RD* low level) as the write operation since reading the original data does not latch the read data into the microcomputer but temporarily holds it in the read-data latch. However, the bus cycle requires the same time as the read operation. The write-data mask function (WM15–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.

Operation Examples:

1) I / D = "1", AM = "1", LG2-0 = "101" (unmatched write)
2) CP15-0 = "2860"H
2) WM15-0 = "0000"H
3) AC = "0000"H



Note: 1. The bits in the GRAM indicated by '*' are not changed.
2. After writing to address "AF00"H, the AC jumps to "0001"H.

Figure 56 Writing Operation of Read/Write Mode 4

Gamma Adjustment Function

The HD66770incorporates gamma adjustment function for the 65,536-color display. Gamma adjustment is implemented by deciding the 8-grayscale level with angle adjustment and micro adjustment register. Also, angle adjustment and micro adjustment is fixed for each of the internal positive and negative polarity. Set up by the liquid crystal panel's specification.

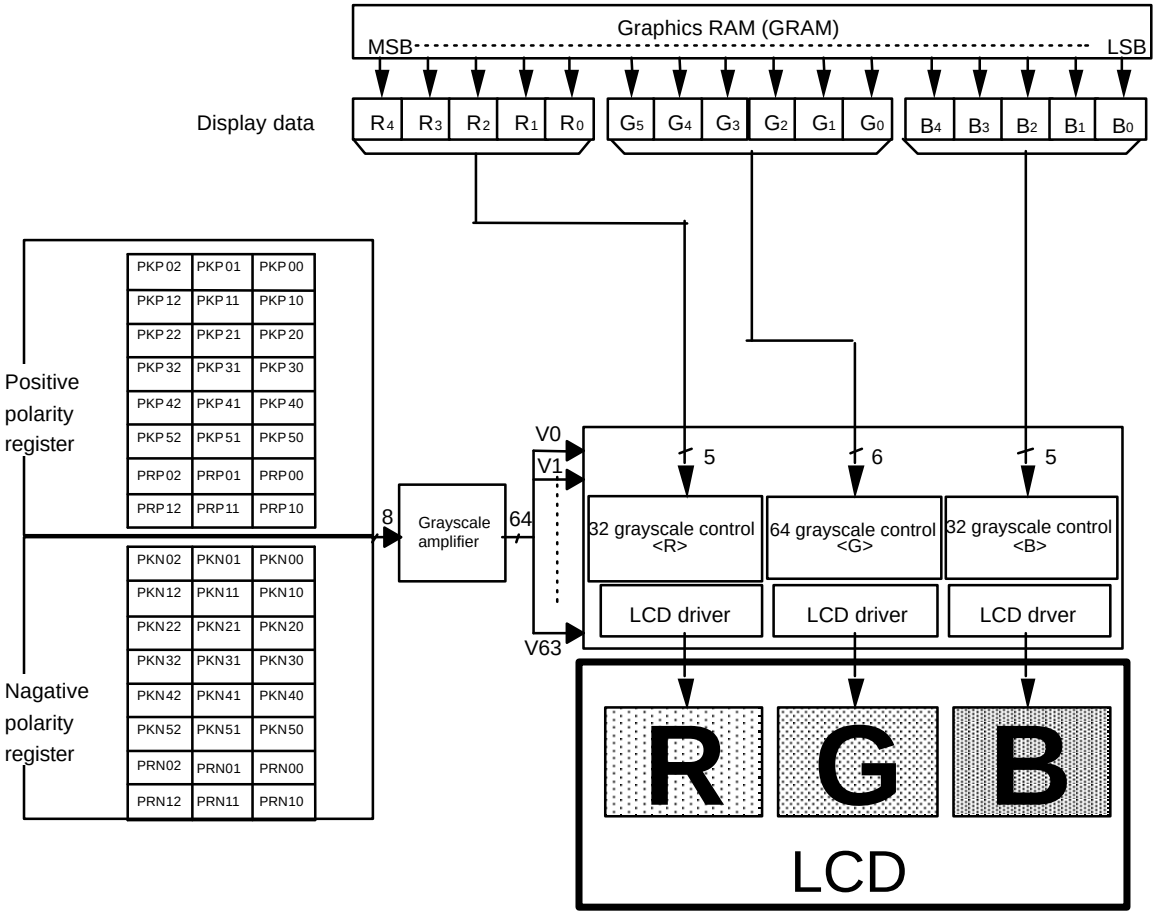


Figure 57: Gamma Adjustment Function

Structure of Grayscale Amplifier

Indicating structure of the grayscale amplifier as below. Determine 8 level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Also, dividing these levels with ladder resistors generates V0 to V64.

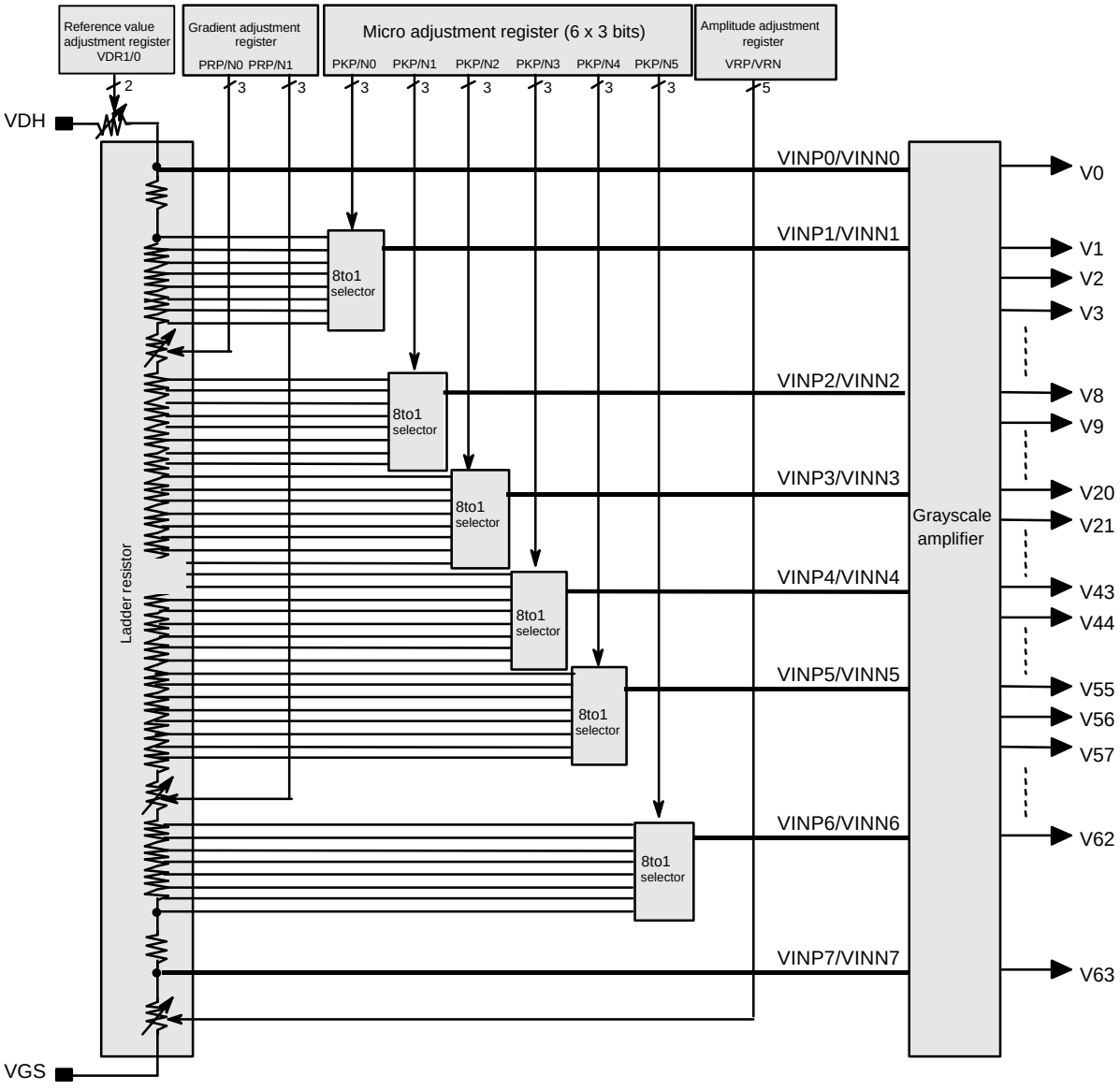


Figure 58: Structure of Grayscale Amplifier

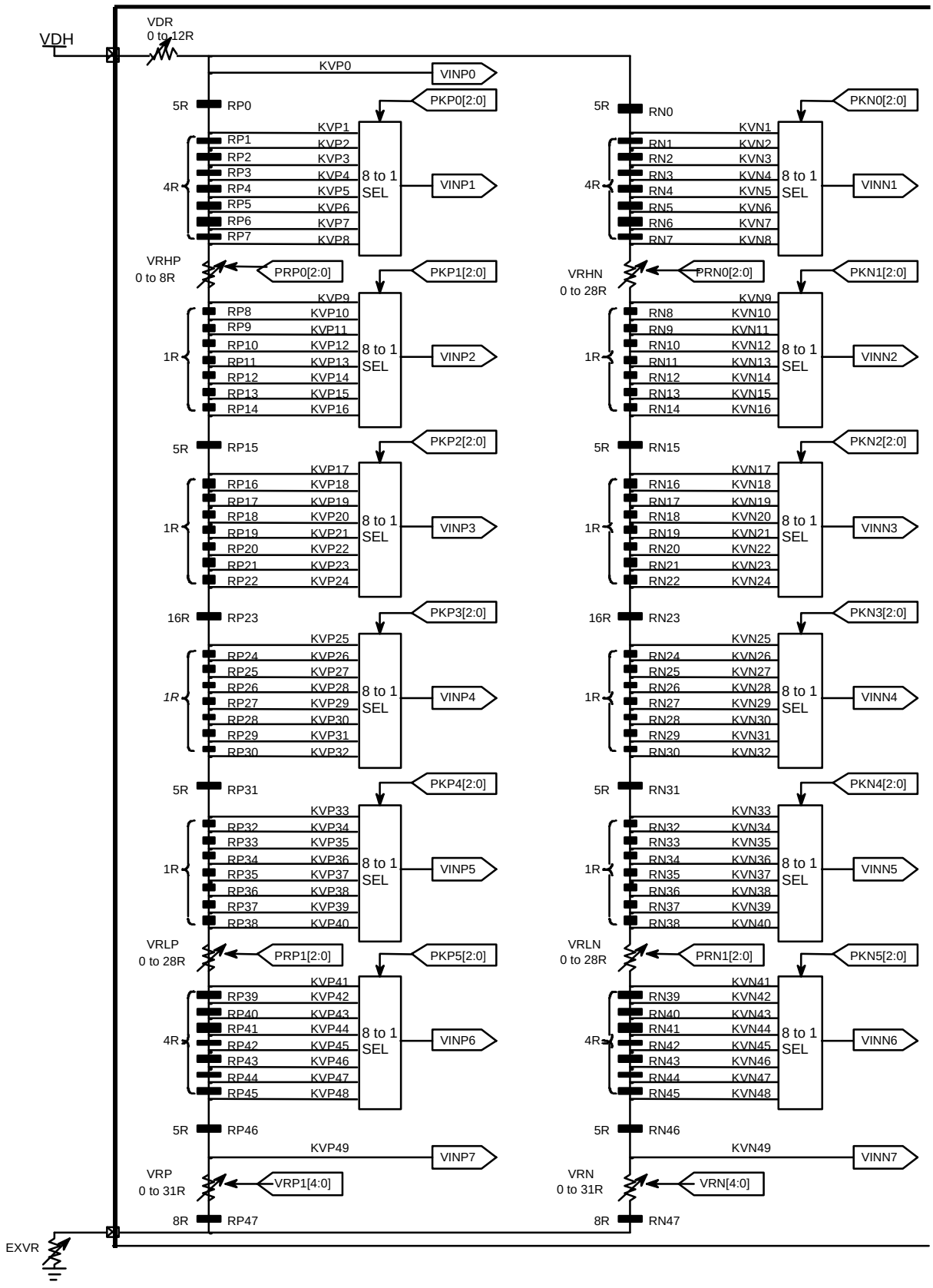


Figure 59: Structure of Ladder / 8 to 1 Selector

Gamma Adjustment Register

This block is the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. This register can independent set up to positive/negative polarities and there are four types of register groups to adjust gradient, amplitude, reference-value, and micro-adjustment on number of the grayscale, characteristics of the grayscale voltage. (Using the same setting for Reference-value and R.G.B.) Following graphics indicates the operation of each adjusting register.

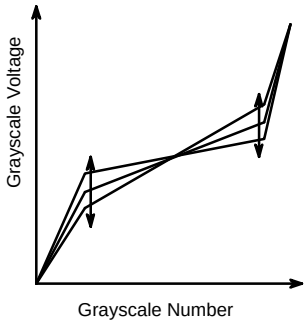


Figure 60 Gradient Adjustment

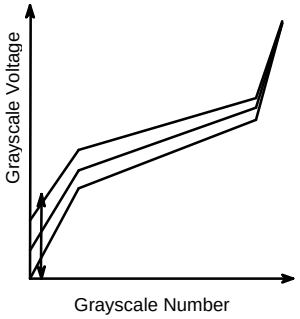


Figure 61 Amplitude Adjustment

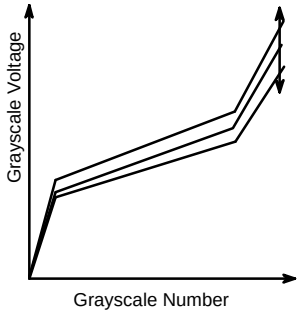


Figure 62 Reference-value Adjustment

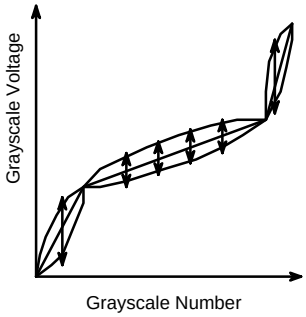


Figure 63 Micro-adjustment

1. Gradient adjusting register

The gradient-adjusting resistor is to adjust around middle gradient, specification of the grayscale number and the grayscale voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRL (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

2. Amplitude adjusting register

The amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP (N)) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor. (Adjust upper side by input VDH level.) Also, there is an independent resistor on the positive/negative polarities as well as the gradient-adjusting resistor.

3. Reference-value adjusting register

Resister of reference value is to adjust the reference value of grayscale voltage. This function is implemented by controlling the variable resistor (VDR) above the ladder resistor block for grayscale voltage generation. This resistor is common to both the positive and negative.

4. Micro-adjusting register

The micro-adjusting register is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Resistor Classification	For Positive Polarity	For Negative Polarity	Set-up Contents
Gradient Adjustment	PRP0[2:0]	PRN0[2:0]	Variable Resistor VR HP
	PRP1[2:0]	PRN1[2:0]	Variable Resistor VR LP
Amplitude Adjustment	VRP[4:0]	VRN[4:0]	Variable Resistor VRP
Reference-value Adjustment	VDR[1:0]		Variable Resistor VDR
Micro-adjustment	PKP0[2:0]	PKN0[2:0]	8 to 1 selector voltage level for the grayscale 1
	PKP1[2:0]	PKN1[2:0]	8 to 1 selector voltage level for the grayscale 8
	PKP2[2:0]	PKN2[2:0]	8 to 1 selector voltage level for the grayscale 20
	PKP3[2:0]	PKN3[2:0]	8 to 1 selector voltage level for the grayscale 43
	PKP4[2:0]	PKN4[2:0]	8 to 1 selector voltage level for the grayscale 55
	PKP5[2:0]	PKNS5[2:0]	8 to 1 selector voltage level for the grayscale 62

Table 36: Output Signal List

Ladder Resistor / 8 to 1 Selector

Block configuration

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistor. The gamma registers control the variable resistors and 8 to 1 selector resistors. Also, there are pins that connect to the external variable resistor. And it allows compensating the dispersion of length between one panel to another.

Variable Resistor

There are 3 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)), for the amplitude adjustment (VRP (N)), and for the reference-value adjustment (VDR). The ohmic value is set by the gradient adjusting resistor, the amplitude-adjusting resistor, and the reference-value adjusting resistor as below.

Table 37: Gradient Adjustment

Register Value PRP (N) [2.0]	Resistance Value VRP (N)
000	0R
001	4R
010	8R
011	12R
101	20R
110	24R
111	28R

Table 38: Amplitude Adjustment

Register Value VRP (N) [4.0]	Resistance Value VRP (N)
00000	0R
00001	1R
00010	2R
⋮	⋮
11101	29R
11110	30R
11111	31R

Table 39: Reference-value Adjustment

Register Value VDR [1.0]	Resistance Value VDR
00	0R
01	4R
10	8R
11	12R

The 8 to 1 Selector

In the 8 to 1 selector, the voltage level can be selected from the levels which are generated by ladder resistors. And output the six types of the reference voltage, the VIN1- to VIN6. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Register Value	Selected Voltage					
PKP (N) [2:0]	VINP (N) 1	VINP (N) 2	VINP (N) 3	VNIP (N) 4	VNIP (N) 5	VINP (N) 6
000	KVP (N) 1	KVP (N) 9	KVP (N) 17	KVP (N) 25	KVP (N) 33	KVP (N) 41
001	KVP (N) 2	KVP (N) 10	KVP (N) 18	KVP (N) 26	KVP (N) 34	KVP (N) 42
010	KVP (N) 3	KVP (N) 11	KVP (N) 19	KVP (N) 27	KVP (N) 35	KVP (N) 43
011	KVP (N) 4	KVP (N) 12	KVP (N) 20	KVP (N) 28	KVP (N) 36	KVP (N) 44
100	KVP (N) 5	KVP (N) 13	KVP (N) 21	KVP (N) 29	KVP (N) 37	KVP (N) 45
101	KVP (N) 6	KVP (N) 14	KVP (N) 22	KVP (N) 30	KVP (N) 38	KVP (N) 46
110	KVP (N) 7	KVP (N) 15	KVP (N) 23	KVP (N) 31	KVP (N) 39	KVP (N) 47
111	KVP (N) 8	KVP (N) 16	KVP (N) 24	KVP (N) 32	KVP (N) 40	KVP (N) 48

Table 40

Table 41 Voltage formula: Positive

Pins	Formula	MIcro-adjusting register value	Reference Voltage
KVP0	VDH*r	-	VINP0
KVP1	VDH−ΔV*5R/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VDH−ΔV*9R/SUMRP	PKP02-00 = "001"	
KVP3	VDH−ΔV*13R/SUMRP	PKP02-00 = "010"	
KVP4	VDH−ΔV*17R/SUMRP	PKP02-00 = "011"	
KVP5	VDH−ΔV*21R/SUMRP	PKP02-00 = "100"	
KVP6	VDH−ΔV*25R/SUMRP	PKP02-00 = "101"	
KVP7	VDH−ΔV*29R/SUMRP	PKP02-00 = "110"	
KVP8	VDH−ΔV*33R/SUMRP	PKP02-00 = "111"	
KVP9	VDH−ΔV*(33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VDH−ΔV*(34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VDH−ΔV*(35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VDH−ΔV*(36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VDH−ΔV*(37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VDH−ΔV*(38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VDH−ΔV*(39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VDH−ΔV*(40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VDH−ΔV*(45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VDH−ΔV*(46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VDH−ΔV*(47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VDH−ΔV*(48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VDH−ΔV*(49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VDH−ΔV*(50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VDH−ΔV*(51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VDH−ΔV*(52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VDH−ΔV*(68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VDH−ΔV*(69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VDH−ΔV*(70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VDH−ΔV*(71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VDH−ΔV*(72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VDH−ΔV*(73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VDH−ΔV*(74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VDH−ΔV*(75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VDH−ΔV*(80R+VRHP)/SUMRP	PKP42-40 = "000"	VINP5
KVP34	VDH−ΔV*(81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VDH−ΔV*(82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VDH−ΔV*(83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VDH−ΔV*(84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VDH−ΔV*(85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VDH−ΔV*(86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VDH−ΔV*(87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VDH−ΔV*(87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VDH−ΔV*(91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VDH−ΔV*(95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VDH−ΔV*(99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VDH−ΔV*(103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VDH−ΔV*(107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VDH−ΔV*(111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VDH−ΔV*(115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VDH−ΔV*(120R+VRHP+VRLP)/SUMRP	-	VINP7

r: {[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}/{VDR+[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}

SUMRP: Total of the positive polarity ladder resistance = 128 R + VRHP + VRLP + VRP

SUMRN: Total of the negative polarity ladder resistance = 128 R + VRLN + VRN

ΔV: Voltage difference between KV0 to KV49 period =VDH*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 42: Voltage Formula (Positive Polarity)

	Formula
V0	VINN0
V1	VINN1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VINP
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VINN6
V63	VINN7

Note:
Keep the relation below
DDVDH-V8>1-1V
V55-GND>1-1V

Table 43: Voltage Formula (Negative Polarity)

Pins	Formula	Micro-adjusting register value	Reference Voltage
KVN0	VDH*r	-	VINN0
KVN1	VDH－ΔV*5R/SUMRN	PKN02-00 = "000"	VINN1
KVN2	VDH－ΔV*9R/SUMRN	PKN02-00 = "001"	
KVN3	VDH－ΔV*13R/SUMRN	PKN02-00 = "010"	
KVN4	VDH－ΔV*17R/SUMRN	PKN02-00 = "011"	
KVN5	VDH－ΔV*21R/SUMRN	PKN02-00 = "100"	
KVN6	VDH－ΔV*25R/SUMRN	PKN02-00 = "101"	
KVN7	VDH－ΔV*29R/SUMRN	PKN02-00 = "110"	
KVN8	VDH－ΔV*33R/SUMRN	PKN02-00 = "111"	
KVN9	VDH－ΔV*(33R+VRHN)/SUMRN	PKN12-10 = "000"	VINN2
KVN10	VDH－ΔV*(34R+VRHN)/SUMRN	PKN12-10 = "001"	
KVN11	VDH－ΔV*(35R+VRHN)/SUMRN	PKN12-10 = "010"	
KVN12	VDH－ΔV*(36R+VRHN)/SUMRN	PKN12-10 = "011"	
KVN13	VDH－ΔV*(37R+VRHN)/SUMRN	PKN12-10 = "100"	
KVN14	VDH－ΔV*(38R+VRHN)/SUMRN	PKN12-10 = "101"	
KVN15	VDH－ΔV*(39R+VRHN)/SUMRN	PKN12-10 = "110"	
KVN16	VDH－ΔV*(40R+VRHN)/SUMRN	PKN12-10 = "111"	
KVN17	VDH－ΔV*(45R+VRHN)/SUMRN	PKN22-20 = "000"	VINN3
KVN18	VDH－ΔV*(46R+VRHN)/SUMRN	PKN22-20 = "001"	
KVN19	VDH－ΔV*(47R+VRHN)/SUMRN	PKN22-20 = "010"	
KVN20	VDH－ΔV*(48R+VRHN)/SUMRN	PKN22-20 = "011"	
KVN21	VDH－ΔV*(49R+VRHN)/SUMRN	PKN22-20 = "100"	
KVN22	VDH－ΔV*(50R+VRHN)/SUMRN	PKN22-20 = "101"	
KVN23	VDH－ΔV*(51R+VRHN)/SUMRN	PKN22-20 = "110"	
KVN24	VDH－ΔV*(52R+VRHN)/SUMRN	PKN22-20 = "111"	
KVN25	VDH－ΔV*(68R+VRHN)/SUMRN	PKN32-30 = "000"	VINN4
KVN26	VDH－ΔV*(69R+VRHN)/SUMRN	PKN32-30 = "001"	
KVN27	VDH－ΔV*(70R+VRHN)/SUMRN	PKN32-30 = "010"	
KVN28	VDH－ΔV*(71R+VRHN)/SUMRN	PKN32-30 = "011"	
KVN29	VDH－ΔV*(72R+VRHN)/SUMRN	PKN32-30 = "100"	
KVN30	VDH－ΔV*(73R+VRHN)/SUMRN	PKN32-30 = "101"	
KVN31	VDH－ΔV*(74R+VRHN)/SUMRN	PKN32-30 = "110"	
KVN32	VDH－ΔV*(75R+VRHN)/SUMRN	PKN32-30 = "111"	
KVN33	VDH－ΔV*(80R+VRHN)/SUMRN	PKN42-40 = "000"	VINN5
KVN34	VDH－ΔV*(81R+VRHN)/SUMRN	PKN42-40 = "001"	
KVN35	VDH－ΔV*(82R+VRHN)/SUMRN	PKN42-40 = "010"	
KVN36	VDH－ΔV*(83R+VRHN)/SUMRN	PKN42-40 = "011"	
KVN37	VDH－ΔV*(84R+VRHN)/SUMRN	PKN42-40 = "100"	
KVN38	VDH－ΔV*(85R+VRHN)/SUMRN	PKN42-40 = "101"	
KVN39	VDH－ΔV*(86R+VRHN)/SUMRN	PKN42-40 = "110"	
KVN40	VDH－ΔV*(87R+VRHN)/SUMRN	PKN42-40 = "111"	
KVN41	VDH－ΔV*(87R+VRHN+VRLN)/SUMRN	PKN52-50 = "000"	VINN6
KVN42	VDH－ΔV*(91R+VRHN+VRLN)/SUMRN	PKN52-50 = "001"	
KVN43	VDH－ΔV*(95R+VRHN+VRLN)/SUMRN	PKN52-50 = "010"	
KVN44	VDH－ΔV*(99R+VRHN+VRLN)/SUMRN	PKN52-50 = "011"	
KVN45	VDH－ΔV*(103R+VRHN+VRLN)/SUMRN	PKN52-50 = "100"	
KVN46	VDH－ΔV*(108R+VRHN+VRLN)/SUMRN	PKN52-50 = "101"	
KVN47	VDH－ΔV*(111R+VRHN+VRLN)/SUMRN	PKN52-50 = "110"	
KVN48	VDH－ΔV*(115R+VRHN+VRLN)/SUMRN	PKN52-50 = "111"	
KVN49	VDH－ΔV*(120R+VRHN+VRLN)/SUMRN	-	VINN7

r: {[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}/{VDR+[(SUMRP*SUMRN)/(SUMRP+SUMRN)]+EXVR}

SUMRP: Total of the positive polarity ladder resistance = 128 R + VRHP + VRLP + VRP

SUMRN: Total of the negative polarity ladder resistance = 128 R + VRLN + VRN

ΔV: Voltage difference between KV0 to KV49 period ＝VDH*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Table 44 Voltage Formula (Negative Polarity)

	Formula
V0	VINN0
V1	VINN1
V2	V3+(V1-V3)*(8/24)
V3	V8+(V1-V8)*(450/800)
V4	V8+(V3-V8)*(16/24)
V5	V8+(V3-V8)*(12/24)
V6	V8+(V3-V8)*(8/24)
V7	V8+(V3-V8)*(4/24)
V8	VINN2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINN5
V56	V60+(V55-V60)*(20/24)
V57	V60+(V55-V60)*(16/24)
V58	V60+(V55-V60)*(12/24)
V59	V60+(V55-V60)*(8/24)
V60	V62+(V55-V62)*(350/800)
V61	V62+(V60-V62)*(16/24)
V62	VINN6
V63	VINN7

Note:
Keep the relation below
DDVDH-V8>1-1V
V55-GND>1-1V

Relationship between RAM Data and Output

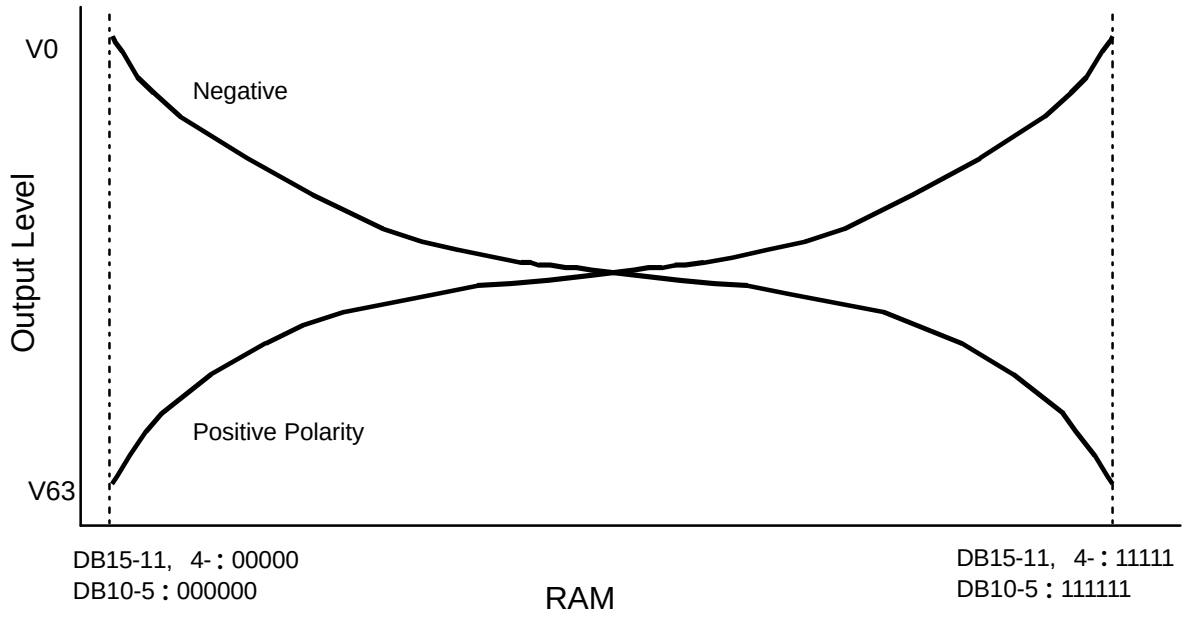


Figure 64: Relationship between RAM Data and Output

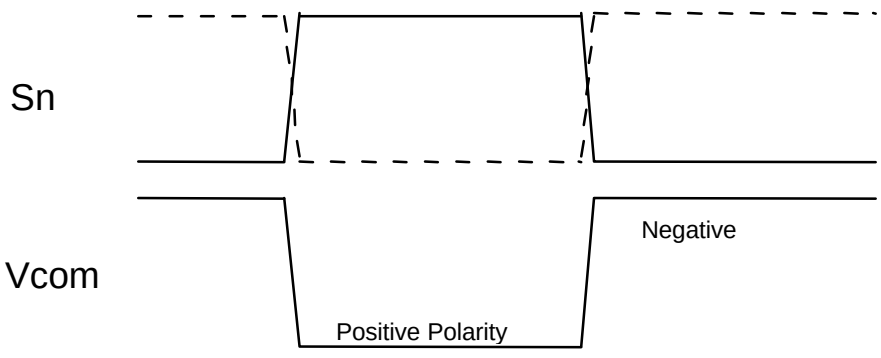


Figure 65: Relationship between Source Output and Vcom

The 8-color Display Mode

The HD66770 carries 8-color display mode. Using grayscale levels are V0 and V63 and all other level power supplies are halt. So that it attempts to lower power consumption. Also, during the 8-color mode, the Gamma micro adjustment register, PKP00-PKP52 and PKN00-PKN52 are invalid. Rewrite the data of GRAM R/B to 00000 or 11111, G to 000000 or 111111 before set the mode in order to select V0/V63. The level power supply (V1-V62) is in OFF condition during the 8-color mode.

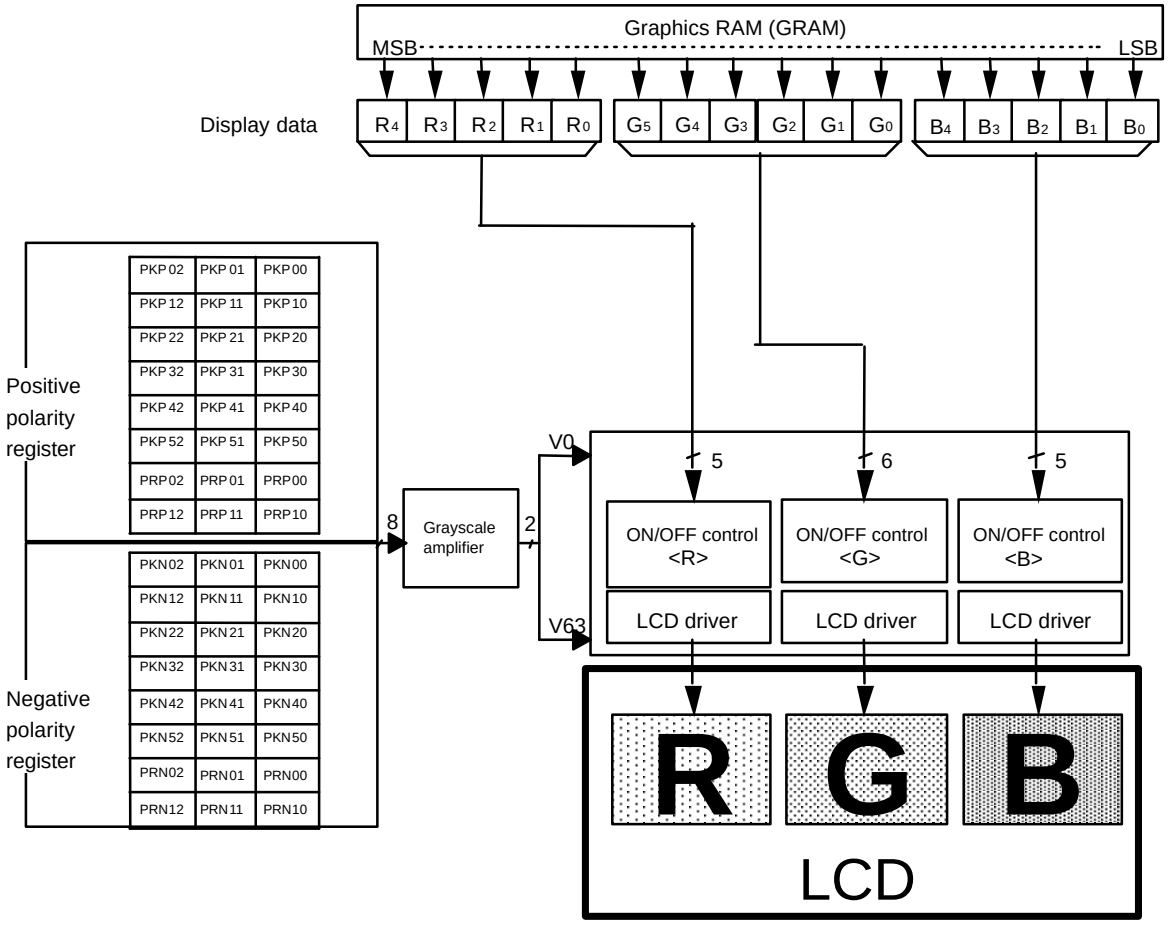


Figure 66: Grayscale Control

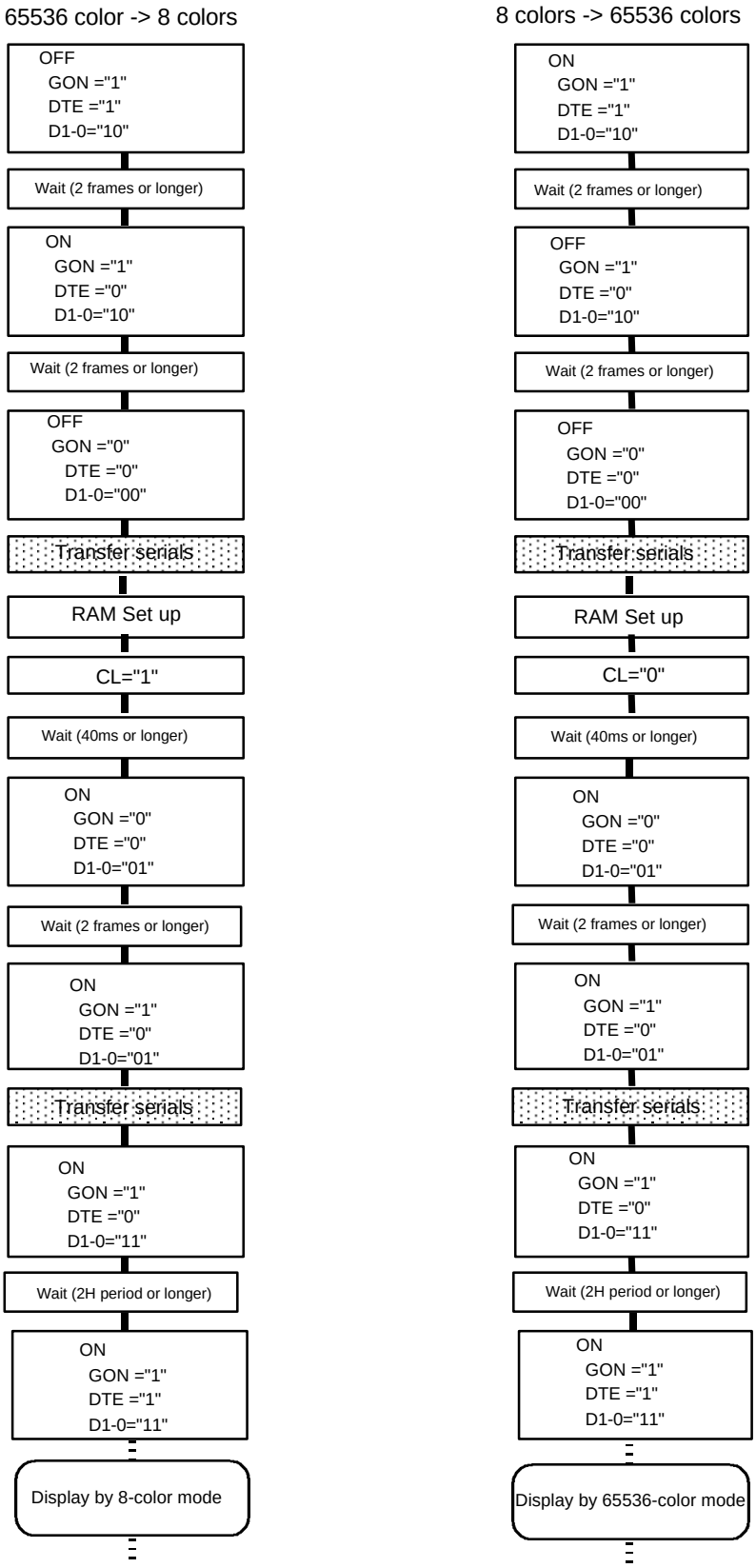

65536 color -> 8 colors
OFF
GON ="1"
DTE ="1"
D1-0="10"
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="10"
Wait (2 frames or longer)
OFF
GON ="0"
DTE ="0"
D1-0="00"
Transfer serials
RAM Set up
CL="1"
Wait (40ms or longer)
ON
GON ="0"
DTE ="0"
D1-0="01"
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="01"
Transfer serials
ON
GON ="1"
DTE ="0"
D1-0="11"
Wait (2H period or longer)
ON
GON ="1"
DTE ="1"
D1-0="11"
Display by 8-color mode
8 colors -> 65536 colors
ON
GON ="1"
DTE ="1"
D1-0="10"
Wait (2 frames or longer)
OFF
GON ="1"
DTE ="0"
D1-0="10"
Wait (2 frames or longer)
OFF
GON ="0"
DTE ="0"
D1-0="00"
Transfer serials
RAM Set up
CL="0"
Wait (40ms or longer)
ON
GON ="0"
DTE ="0"
D1-0="01"
Wait (2 frames or longer)
ON
GON ="1"
DTE ="0"
D1-0="01"
Transfer serials
ON
GON ="1"
DTE ="0"
D1-0="11"
Wait (2H period or longer)
ON
GON ="1"
DTE ="1"
D1-0="11"
Display by 65536-color mode

Figure 67

Example of System Configuration

Following diagram indicates the system structure, which composes the 132 (horizontal) x 176 (vertical) dot TFT-LCD panel. This must be used together with the gate driver; HD66771 and the Power supply IC; HD667P00.

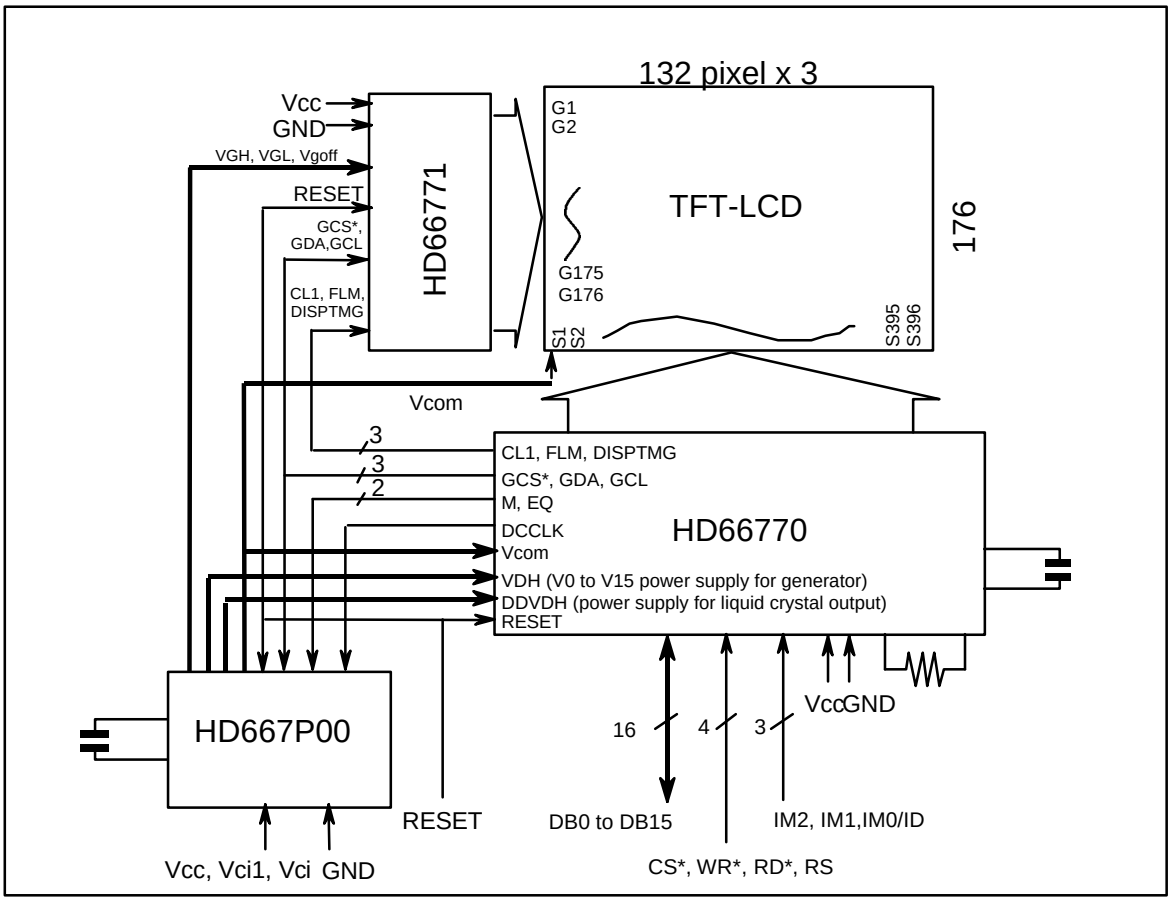
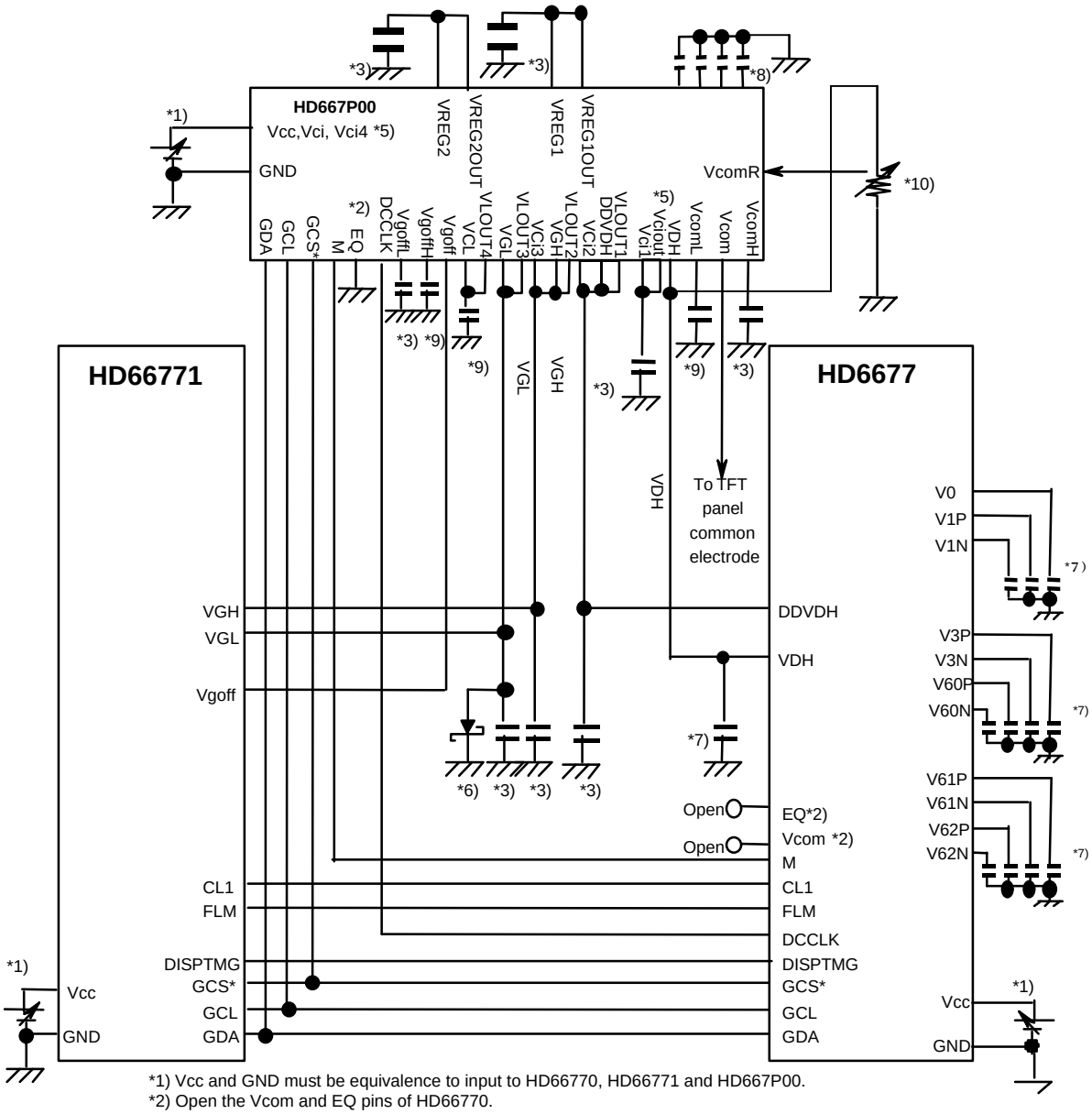


Figure 68 Example of TFT Display System

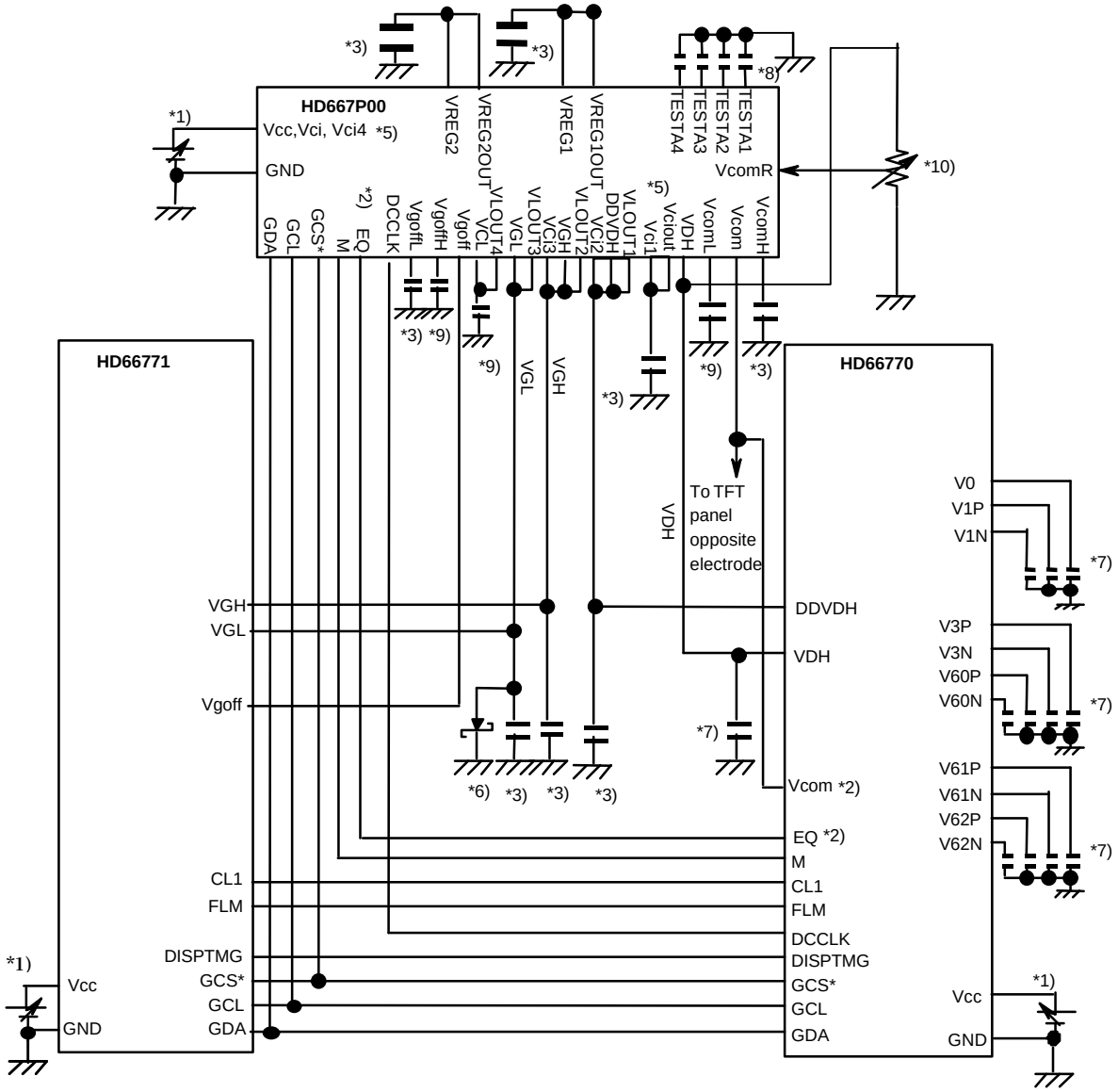
Setting of the Vcom voltage changes connecting method.
Following diagram indicates a connection example of the HD66771 and HD667P00 when VcomL < 0V, 0V <= VcomL < 5.5V.



*1) Vcc and GND must be equivalence to input to HD66770, HD66771 and HD667P00.
*2) Open the Vcom and EQ pins of HD66770.
EQ pins of HD667P0 must be GND.
*3) Use the 1uF condenser with the B property when it is connected in the stabilized capacity.
*4) Condensers connected to following terminals of HD667P00 are omitted.
C11 to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, C41+
For these connections of condensers, connections refer to function of the HD667P00 pins to
*5) Supply voltage of 2.5V to 3.3V to Vci with the external power supply. And supply voltage of 2.5V to 3.3V to Vci1 or for connecting Vciout and Vci1 with the external power supply.
*6) Connect the shot key barrier diode, which contains approx. VF = 0.3 V/1mA and VR >= 30V.
*7) Use the condenser of 0.1uF with the B property when it is connected in the stabilized capacity.
*8) Connect the 0.1µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.
*9) When step-up circuit 4, VcomL and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.
*10) Use a vaiable resistor more than 200kΩ.

Figure 69: Connection Example of HD66770 and HD66771 (when VcomL < 0V)

Following diagram indicates a connection example of the gate driver, HD66771 and Power supply IC when 0 <= VcomL < 5.5, and using equalizing function.



*1) Vcc and GND must be equivalence to input to HD66770, HD66771 and HD667P00.

*2) Connect EQ pins of HD66770 and EQ pins of HD667P00. Connect Vcom pins to Vcom pins of the HD667P00. Also, do not use when Vcom voltage is 5.5V or higher.

*3) Use the 1uFcondenser with the B property when it is connected in the stabilized capacity.

*4) Condensers connected to following terminals of HD667P00 are omitted.
C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23-, C31-, C31+, C41-, C41+
For these connections of condensers, refer to function of the HD667P00 pins to connect.

*5) Supply voltage of 2.5V to 3.3V to Vci with the external power supply. And supply voltage 2.5V to 3.3V to Vci 1 for connecting Vciout and Vci1 with the external power supply. When Vci1 is connecting to the external power supply, leave Vciout open.

*6) Connect the schotkey barrier diode, which contains approx. VF = 0.3 V/1mA and VR>= 30V.

*7) Use the condenser of 0.1uF with the B property when it is connected in the stabilized capacity.

*8) Connect the 0.1µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.

*9) When step-up circuit 4, VcomL and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.

*10) Use a variable resistor more than 200kΩ.

Figure 70: Connection Example of HD66770 and HD66771 (when 0V <= VcomL< 5.5V)

Specification of capacitor connected to HD66770 and HD667P00

The following table indicates the specification of capacitor connected to HD66770 and HD667P00.

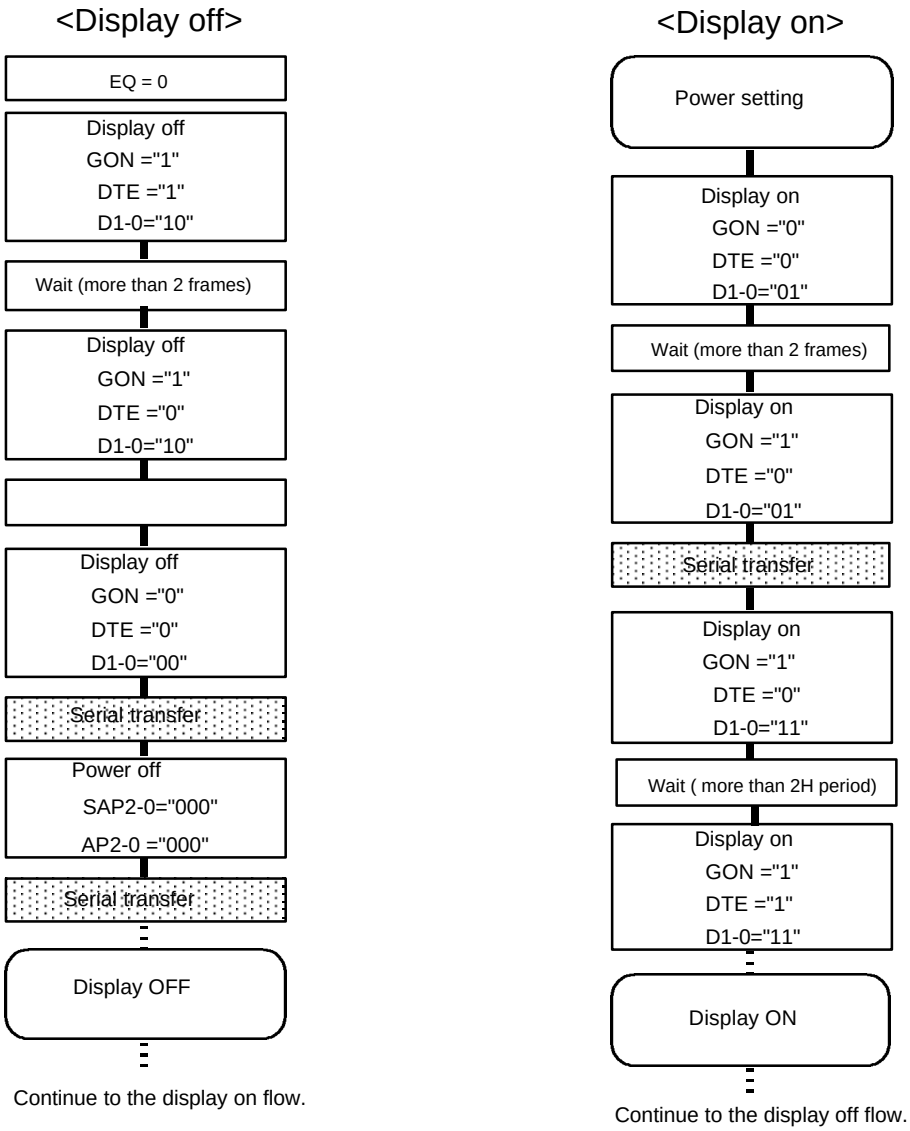
Product	Capacity of capacitor	Recommendation resist pressure for capacitor	Connect pins
HD667P00	1μF (B character)	6V	VEG1OUT, Vciout, C41-/+*1, VLOUT4*1, VcomH*1, VcomL
		10V	VLOUT1, C11-/+, C12-/+, C21-/+, C22-/+, C23-/+
		25V	VREG2OUT. VLOUT2, VLOUT3, C31-/+, VgoffH*1, VgoffL
	0.1μF (B character)	6V	VDH, (TESTA1)*2, (TESTA2)*2, REGP*2, REGN*2
		25V	(TESTA3), (TESTA4)
HD66770	0.1μF (B character)	6V	V0, V1P, V1N, V3P, V3N, V60P, V60N, V62P, V62N, V63P, V63N

*1 According to the mode set HD667P00, there is some cases in which capacitor is unnecessary.

*2 Connect a capacitor to stabilize picture. Be noticed that power consumption may rise in great amount.

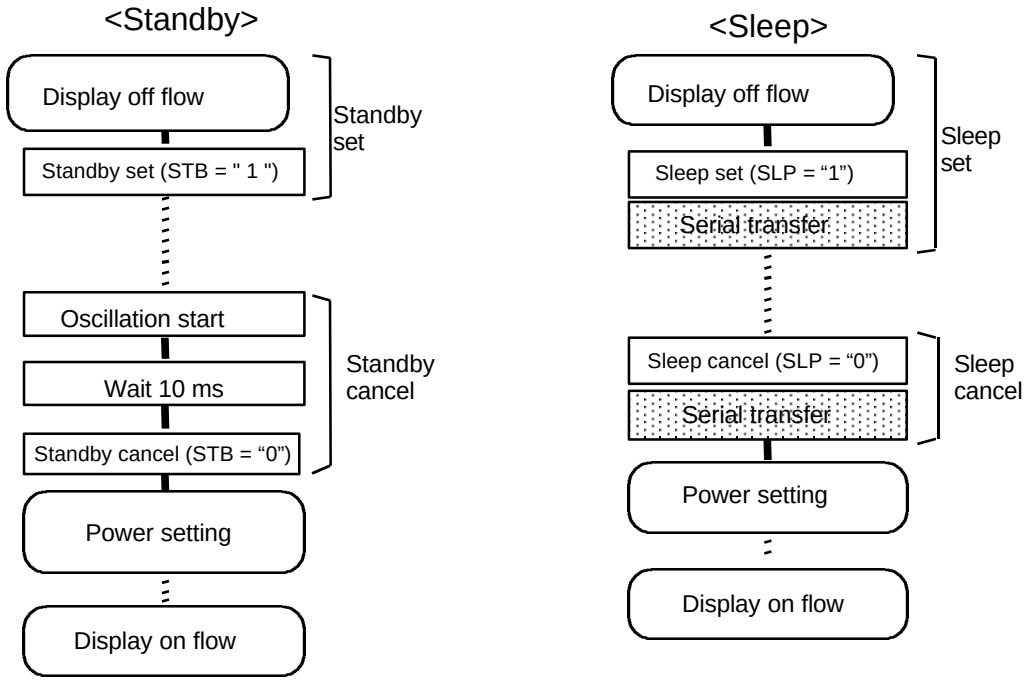
Instruction Setting Flow

When the HD66771/HD667P00 are used, follow the instruction setting flow. The instruction setting for the HD66771/HD667P00 is executed by the serial interface. When the instruction for the HD66771/HD667P00 is set, the serial transfer must be executed to the HD66771/HD667P00. The transfer to the HD66771/HD667P00 must be executed immediately after the instruction set.
Follow the below serial transfer flow about each setting and then transfer must be executed.



Note: For more information on the flow for power settings, refer to the HD667P00 data sheet.

Figure 71



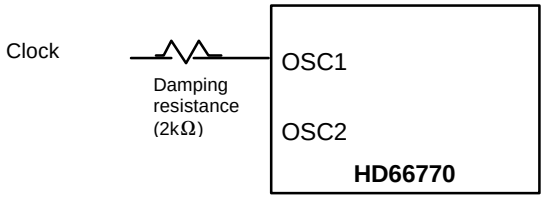
Note: For more information on the flow for power settings, refer to the HD667P00 data sheet.

Figure 72

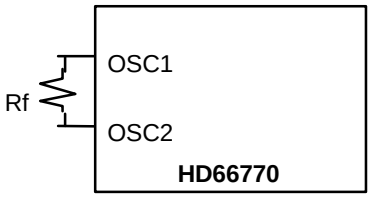
Oscillation Circuit

The HD66770 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.

1) External Clock Mode



2) External Resistance Oscillation Mode



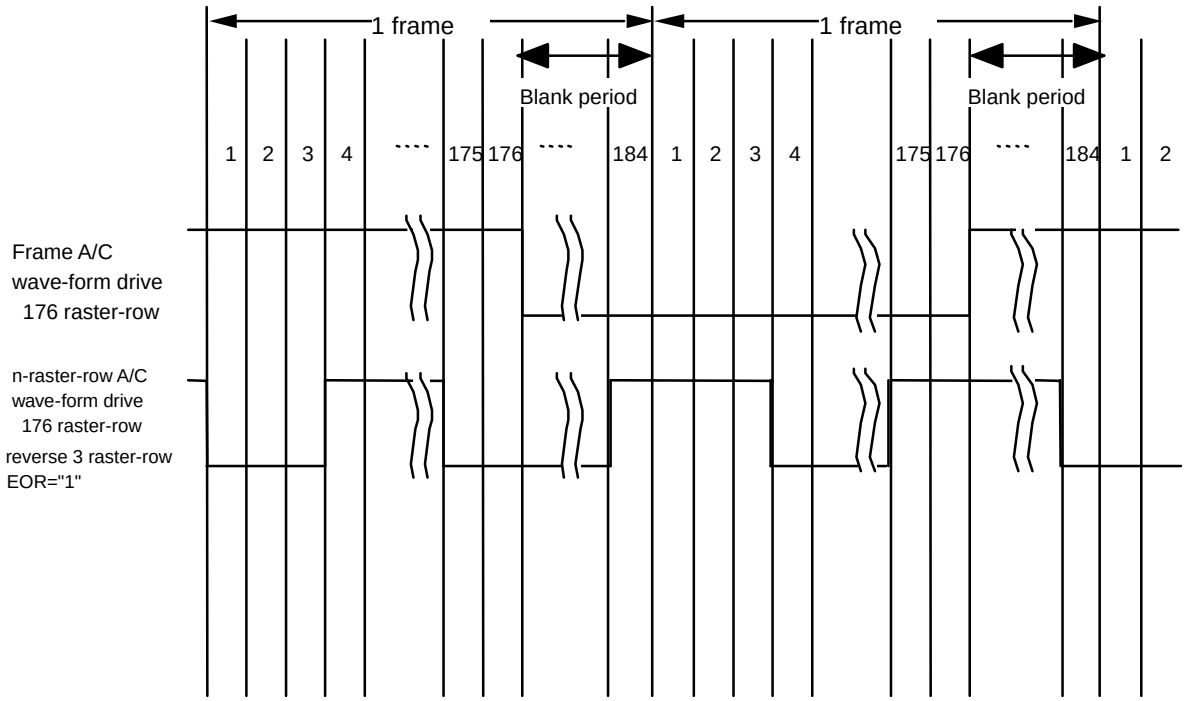
Note: The Rf resistance must be located near the OSC1/OSC2 pin on the master side.

Figure 73: Oscillation Circuits

n-raster-row Reversed AC Drive

The HD66770 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.

Determine the number of the raster-rows n (NW bit set value +1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Note: In an n-raster-row driving EOR should be “1” so that DC bias voltage is not applied.

Figure74: Example of an AC Signal under n-raster-row Reversed AC Drive

Interlace Drive

HD66770 supports the interlace drive to protect from the display flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display. Following table indicates n fields: the gate selecting position when it is 1 or 3. And the diagram below indicates the output waveform when the 3-field interlace drive is active.

Table 45

GS = "0"

FLD1-0: Setting Value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G1	○	○		
G2	○		○	
G3	○			○
G4	○	○		
G5	○		○	
G6	○			○
G7	○	○		
G8	○		○	
G9	○			○
G173	○	○		
G174	○		○	
G175	○			○
G176	○	○		

GS = "1"

FLD1-0: Setting Value	01	11		
Gate \ Field	-	(1)	(2)	(3)
G228	○	○		
G227	○		○	
G226	○			○
G225	○	○		
G224	○		○	
G223	○			○
G222	○	○		
G221	○		○	
G220	○			○
G56	○	○		
G55	○		○	
G54	○			○
G53	○	○		

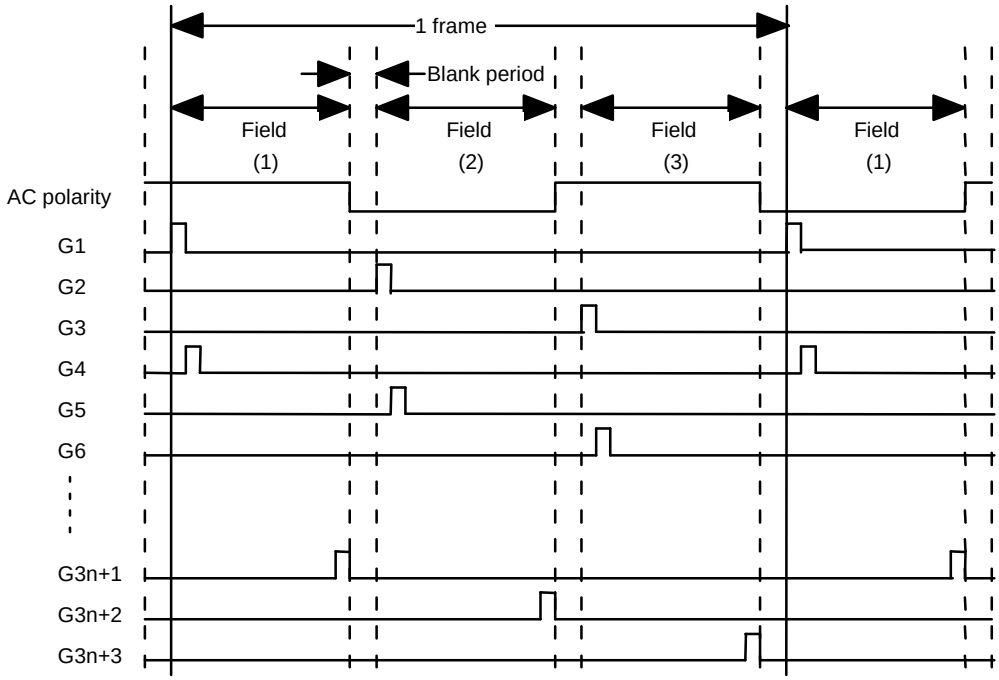


Figure 75: Gate output Timing on the 3 Field Interlace

AC Drive Timing

Following diagram indicates the timing of changing polarity on the each A/C drive method. LCD drive polarity is changed after every frame. After the A/C this timing, the blank (all outputs from the gate: Vgoff output) in 8H period is inserted. Also, LCD drive polarity is change after every field when it is on the interlace drive and a blank is inserted in every timing. The amount of blanking periods becomes 16H in a frame. When the reversed n-raster-row is driving, a blank period of the 8H period is inserted after all screens are drawn

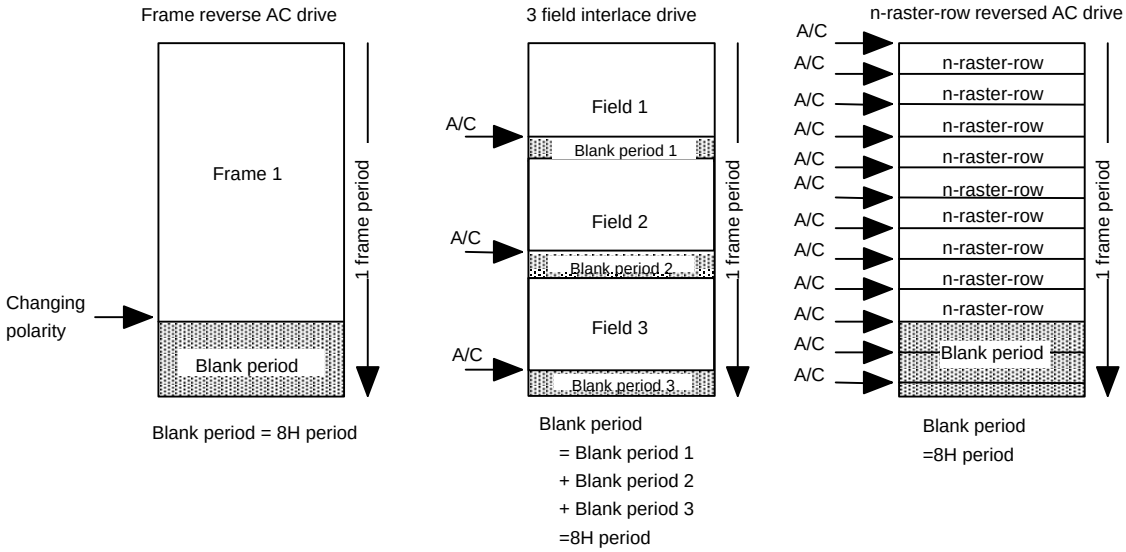


Figure 76

Frame Frequency Adjusting Function

The HD66770 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

(Formula for the frame frequency)

$$\text{Frame Frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line+8)}} \text{ [Hz]}$$

fosc: R-C oscillation frequency
Line: Numbers of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit

Example of Calculation

In case of maximum frame frequency = 60 Hz;

Driver raster-row: 176

1H period: 16 clock (RTN3 to 0 = “0000”)
Operation clock division ratio: 1 division

fosc = 60Hz x (0+16) clock x 1 division x (176+8) lines = 177 [kHz]

In this case, the CR oscillation frequency becomes 177 kHz. The external resistance value of the R-C oscillator must be adjusted to be 177 kHz.

Screen-division Driving Function

The HD66770 can select and drive two screens at any position with the screen-driving position registers (R14 and R15). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

For the 1st division screen, start lines (SS17 to 10) and end lines (SE17 to 10) are specified by the 1st screen-driving position register (R14). For the 2nd division screen, start line (SS27 to 20) and end lines (SE27 to 20) are specified by the 2nd screen-driving position register (R15). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must be the number of LCD drive raster-rows or less.

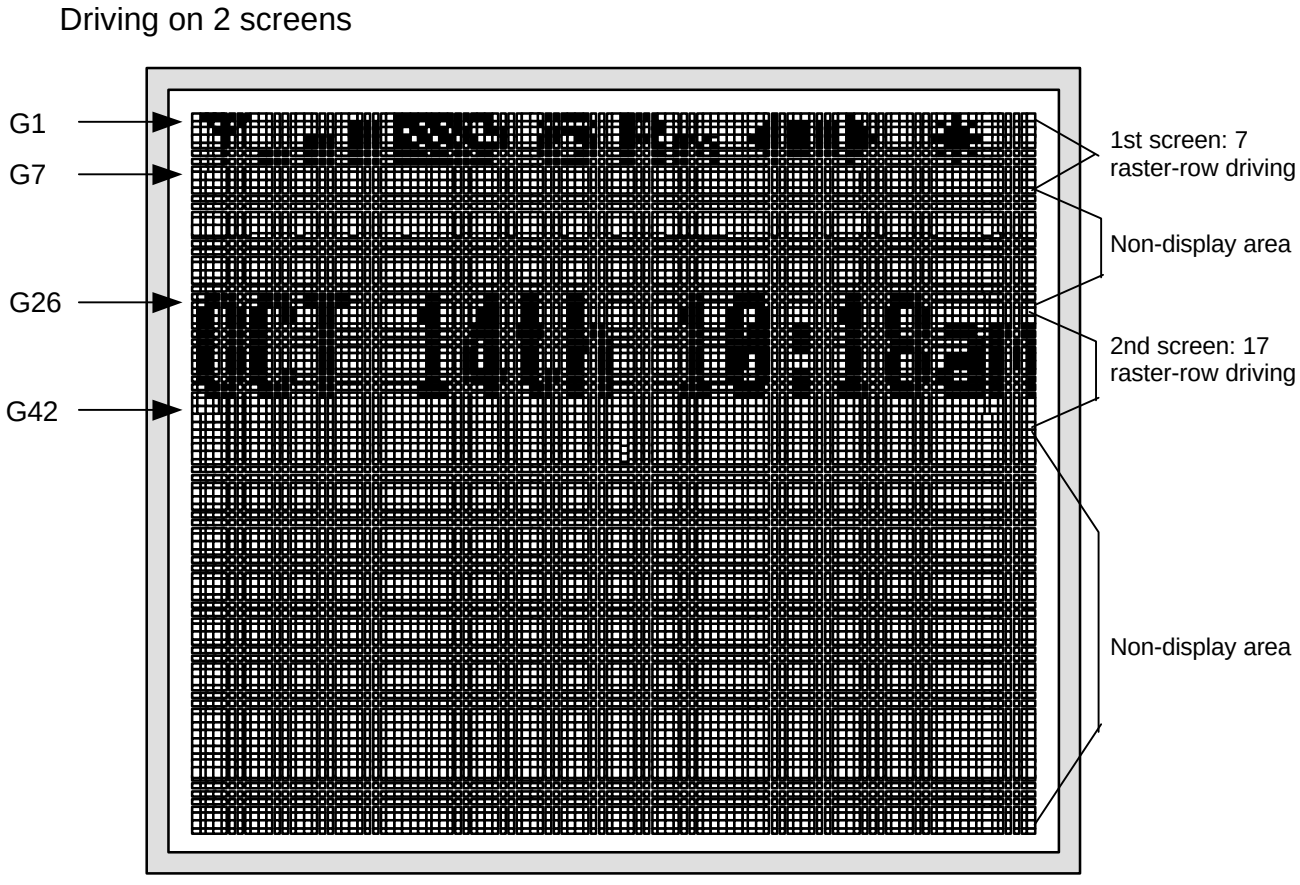


Figure 77: Display Example in 2-screen Division Driving

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line (SS17 to 10) and end line (SE17 to 10) of the 1st screen driving position register (R14) and the start line (SS27 to 20) and end line (SE27 to 20) of the 2nd screen driving position register (R15) for the HD66770. Note that incorrect display may occur if the restrictions are not satisfied.

Table 46: Restrictions on the 1st/2nd Screen Driving Position Register Settings

1st Screen Driving (SPT = 0)

Register setting	Display operation
(SE17 to 10) – (SS17 to 10) = NL	Full screen display Normally displays (SE17 to 10) to (SS17 to 10)
(SE17 to 10) – (SS17 to 10) < NL	Partial display Normally displays (SE17 to 10) to (SS17 to 10) In all other display area refers to the output level based on the PT setting. (non-display)
(SE17 to 1) – (SS17 to 10) > NL	Setting disabled

Note 1: SS17 to 10 <= SE17 to 10 <= AFH
Note 2: Setting SE27 to 20 and SS27 to 20 are invalid.

2nd Screen Driving (SPT = 1)

Register setting	Display operation
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) = NL	Full screen display Normally displays (SE17 to 10) to (SE17 to 10)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27 to 20)) < NL	Partial display Normally displays (SE27 to 20) to (SS17 to 10) In all other display area refers to the output level based on the PT setting. (non-display)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27 to 20)) > NL	Setting disabled

Table 47

Note 1: SS17 to 10 <= SE17 to 10 < SS27 to 20 <= SE27 to 20 <= AFH
Note 2: (SE27 to 20) – (SS17 to 10) <= NL

The driver output can not be set for non-display area during the partial display. Determine based on characteristic of the display panels.

PT1	PT0	Source output in non-display area		Gate output in non-display area
		Positive polarity	Negative polarity	
0	0	V63	V0	Normal operation
0	1	V63	V0	Vgoff
1	0	GND	GND	Vgoff
1	1	Hi-z	Hi-z	Vgoff

Table 48

Refer to the following flow to set up the partial display.

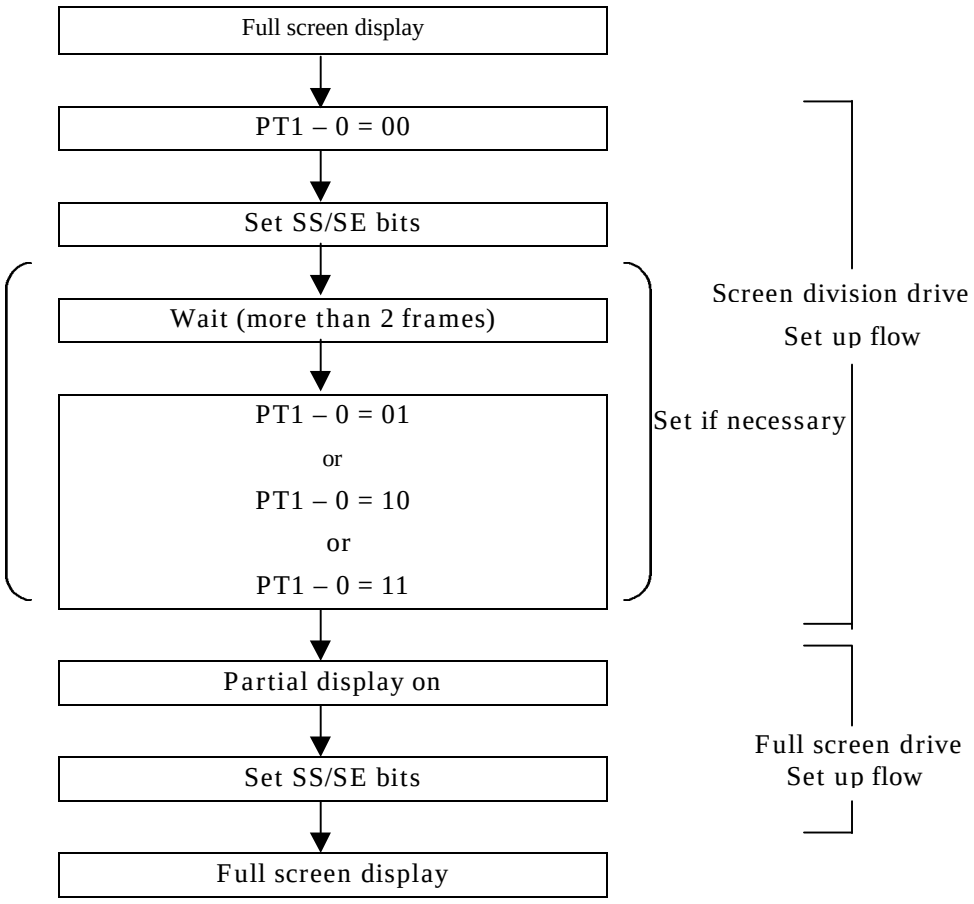


Figure 78

Absolute Maximum Ratings

Table 49

Item	Symbol	Unit	Value	Notes*
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	DDVDH-GND	V	-0.3 to + 4.6	1, 3
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 4
Storage temperature	Tstg	°C	-55 to + 110	1, 5

Notes: 1.If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. Vcc ≥ GND must be maintained

3.DDVDH≥ GND must be maintained.

4.DC characteristics and AC characteristics of shipping chips and shipping wafer are guaranteed at 85 °C.

5.This temperature specifications apply to the TCP package.

DC Characteristics (V_{CC} = 1.8 to 3.3 V, Ta = –40 to +85°C*[1])

Table 50

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	V_{CC} = 1.8 to 3.3 V	0.7 V_{CC}	—	V_{CC}	2, 3
Input low voltage	V_{IL}	V	V_{CC} = 1.8 to 3.3 V	–0.3	—	0.15V_{CC}	2, 3
Output high voltage (1) (DB0-15 pins)	V_{OH1}	V	I_{OH} = –0.1 mA	0.75V_{CC}	—	—	2
Output low voltage (1) (DB0-15 pins)	V_{OL1}	V	V_{CC} = 1.8 to 2.4 V, I_{OL} = 0.1 mA	—	—	0.2 V_{CC}	2
			VCC = 2.4 to 3.3 V, I_{OL} = 0.1 mA	—	—	0.15V_{CC}	2
I/O leakage current	I_{Li}	µA	Vin = 0 to V_{CC}	–1	—	1	4
Current consumption during normal operation (V_{CC} – GND)	I_{OP}	µA	R-C oscillation V_{CC} = 3.0 V, Ta = 25°C f_{OSC} = 177 Khz (176 duty), RAM data : 0000h	—	140	210	5,6
Current consumption during standby mode (V_{CC} – GND)	I_{ST}	µA	V_{CC} = 3 V, Ta = 25°C	—	0.1	5	
LCD drive power supply current (DDVDH – GND)	I_{LCD}	µA	V_{CC} = 3.0 V, V_{LCD} = 5.5V VDH=5.0V CR oscillation; f_{OSC} = 177 kHz (176 duty), Ta = 25°C, RAM data : 0000h, REV ="0", SAP = "001", VRN4-0 = "0", VRP4-0 = "0", PKP52-00 = "0", PRP12-00 = "0", VRN4-0 = VRP4-0 = "0", PKP52-00 = "0", PRP12-00 = "0"	—	295	400	5,6
LCD drive voltage (DDVDH – GND)	V_{LCD}	V		4.5	—	5.5	
Output voltage deviation	Vo	$_{m}$V		—	5	—	7
Dispersion of the average output voltage	V	$_{m}$V		—	—		8

AC Characteristics (V_{CC} = 1.8 to 3.3 V, Ta = –40 to +85°C*[1])

Clock Characteristics (V_{CC} = 1.8 to 3.3 V)

Table 51

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
External clock frequency	Fcp	kHz	V_{CC} = 1.8 to 3.3 V	100	200	600	9
External clock duty ratio	Duty	%	V_{CC} = 1.8 to 3.3 V	45	50	55	9
External clock rise time	Trcp	µs	V_{CC} = 1.8 to 3.3 V	—	—	0.2	9
External clock fall time	Tfcp	µs	V_{CC} = 1.8 to 3.3 V	—	—	0.2	9
R-C oscillation clock	f_{OSC}	kHz	Rf = 240kΩ, V_{CC} = 3 V	152	190	228	10

68-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0)

(Vcc = 1.8 to 2.4 V)

Table 52

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	600	—	—
	Read	t_{CYCE}	ns	Figure 1	800	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	90	—	—
	Read	PW_{EH}	ns	Figure 1	350	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	300	—	—
	Read	PW_{EL}	ns	Figure 1	400	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

High-speed Write Mode (HWM=1)

(Vcc = 1.8 to 2.4 V)

Table 53

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	200	—	—
	Read	t_{CYCE}	ns	Figure 1	800	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	90	—	—
	Read	PW_{EH}	ns	Figure 1	350	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	90	—	—
	Read	PW_{EL}	ns	Figure 1	400	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

Normal Write Mode (HWM=0)

(Vcc = 2.4 to 3.3 V)

Table 54

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	250	—	—
	Read	t_{CYCE}	ns	Figure 1	500	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—
	Read	PW_{EH}	ns	Figure 1	250	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	70	—	—
	Read	PW_{EL}	ns	Figure 1	200	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

High-Speed Write Mode (HWM=1)

(Vcc = 2.4 V to 3.3 V)

Table 55

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Enable cycle time	Write	t_{CYCE}	ns	Figure 1	100	—	—
	Read	t_{CYCE}	ns	Figure 1	500	—	—
Enable high-level pulse width	Write	PW_{EH}	ns	Figure 1	40	—	—
	Read	PW_{EH}	ns	Figure 1	250	—	—
Enable low-level pulse width	Write	PW_{EL}	ns	Figure 1	40	—	—
	Read	PW_{EL}	ns	Figure 1	200	—	—
Enable rise/fall time		t_{Er}, t_{Ef}	ns	Figure 1	—	—	25
Set up time (RS, R/W to E, CS*)		t_{ASE}	ns	Figure 1	10	—	—
Address hold time		t_{AHE}	ns	Figure 1	5	—	—
Write data set up time		t_{DSWE}	ns	Figure 1	60	—	—
Write data hold time		t_{HE}	ns	Figure 1	15	—	—
Read data delay time		t_{DDRE}	ns	Figure 1	—	—	200
Read data hold time		t_{DHRE}	ns	Figure 1	5	—	—

80-system Bus Interface Timing Characteristics

Normal Write Mode (HWM=0)

(Vcc = 1.8 to 2.4 V)

Table 56

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	600	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	300	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Setup time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{H}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1)

(Vcc = 1.8 to 2.4 V)

Table 57

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	200	—	—
	Read	t_{CYCR}	ns	Figure 2	800	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	90	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	350	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	90	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	400	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{H}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

Normal Write Mode (HWM=0)

(Vcc = 2.4 to 3.3 V)

Table 58

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	250	—	—
	Read	t_{CYCR}	ns	Figure 2	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 2	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 2	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 2	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data setup time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{H}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

High-Speed Write Mode (HWM=1)

(Vcc = 2.4 to 3.3 V)

Table 59

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 2	100	—	—
	Read	t_{CYCR}	ns	Figure 2	500	—	—
Write low-level pulse width		PW_{Lw}	ns	Figure 2	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 2	250	—	—
Write high -level pulse width		PW_{HW}	ns	Figure 2	40	—	—
Read high -level pulse width		PW_{HR}	ns	Figure 2	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 2	—	—	25
Set up time (RS to CS*, WR*, RD*)		t_{AS}	ns	Figure 2	10	—	—
Address hold time		t_{AH}	ns	Figure 2	5	—	—
Write data set up time		t_{DSW}	ns	Figure 2	60	—	—
Write data hold time		t_{H}	ns	Figure 2	15	—	—
Read data delay time		t_{DDR}	ns	Figure 2	—	—	200
Read data hold time		t_{DHR}	ns	Figure 2	5	—	—

Clock Synchronized Serial Interface Timing Characteristics

(Vcc = 1.8 to 2.4 V)

Table 60

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 3	0.1	—	20
	Read (transmitted)	t_{SCYC}	us	Figure 3	0.25	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 3	120	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 3	120	—	—
Serial clock rise/fall time		$t_{scr, scf}$	ns	Figure 3	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t_{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 3	30	—	—
Serial input data delay time		t_{SOD}	ns	Figure 3	—	—	200
Serial input data hold time		t_{SOH}	ns	Figure 3	5	—	—

(Vcc = 2.4 to 3.3 V)

Table 61

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 3	0.1	—	20
	Read (transmitted)	t_{SCYC}	us	Figure 3	0.15	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 3	70	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 3	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 3	70	—	—
Serial clock rise/fall time		$t_{scr, scf}$	ns	Figure 3	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 3	20	—	—
Chip select hold time		t_{CH}	ns	Figure 3	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 3	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 3	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure 3	—	—	130
Serial output data hold time		t_{SOH}	ns	Figure 3	5	—	—

Reset Timing Characteristics (V_{CC} = 1.8 to 3.3 V)

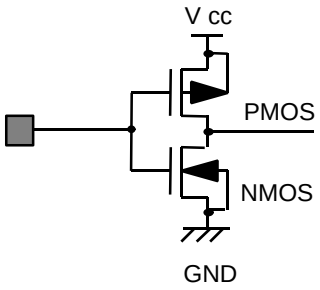
Table 62

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 4	1	—	—
Reset rise time	t_{rRES}	us	Figure 4	—	—	10

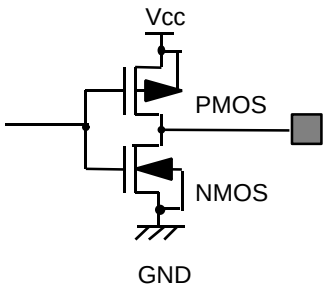
Electrical Characteristics Notes

1. For bare die and wafer products, specified up to 85°C.
2. The following three circuits are I pin, I/O pin, O pin configurations.

Pins: RESET*, CS*, E/WR*/SCL RW/RD RS, RW/RD, RS,
OSC1, IM2-1, IM0/ID, TEST1, TEST



Pins: OSC1, CL1, FLM, M, DISPTMG
GCL, GDA, GCS*, EQ, DCCLK



Pins: DB15 -DB2,
DB1／SD0, DB0/SDI

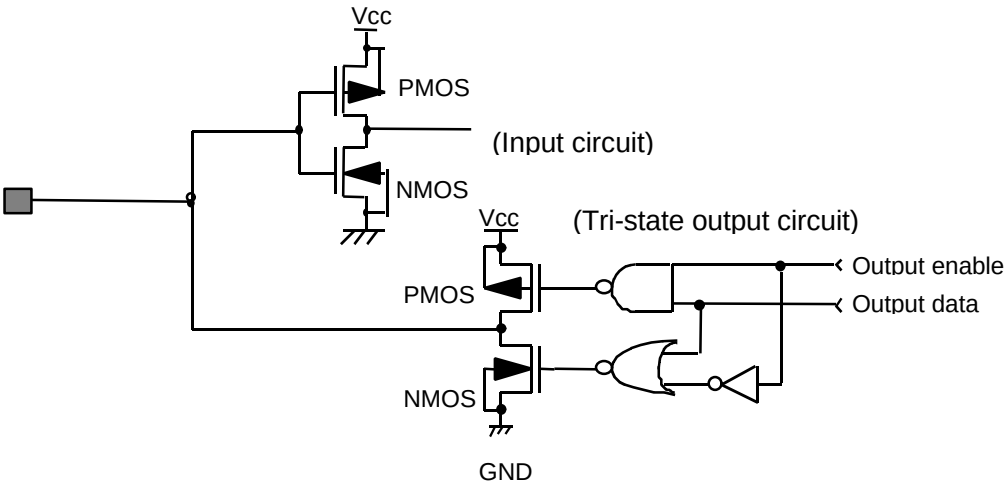


Figure 79 I/O Pin Configuration

3.The TEST pin must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.

4.This exclude the current flowing through output drive MOSs.

5.This exclude the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin is low or high when an access with the interface pin is not performed, current consumption does not change.

6.The following show the relationship between the operation frequency (fosc) and current consumption (Icc) (figure).

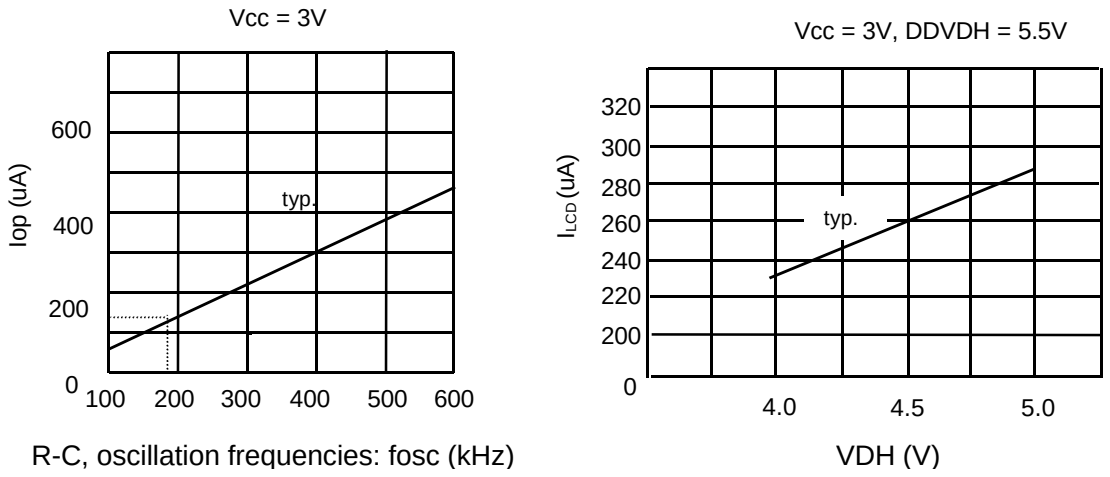


Figure 80 Relationship between the Operation Frequency and Current Consumption

7.Output-voltage deviation is the difference of output voltage between the pins next to each other. The pins output same data, and output voltage deviation is only for reference.

8.Dispersion of the average output voltage is the difference of the average of output voltage between chips next to each other.

9.Applies to the external clock input (figure).

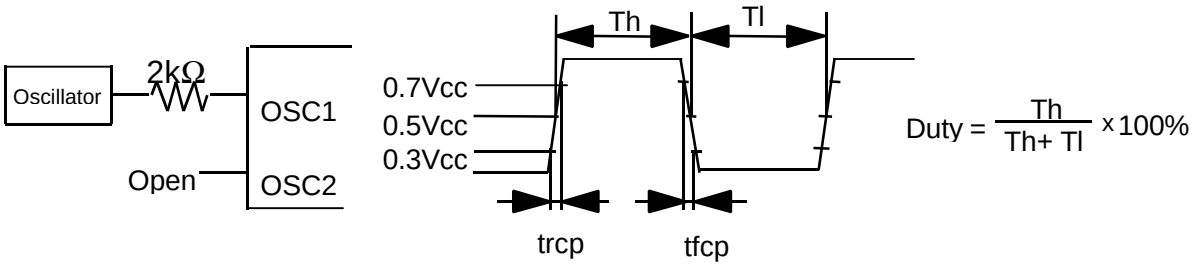
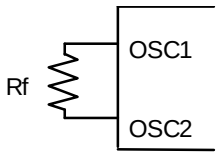


Figure 81 External Clock Supply

10.Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table).



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.

Figure 82 Internal Oscillation

(Referential Data)

Table 63

R-C Oscillation Frequency: fosc (kHz)

Oscillation Resistance (kW)	**Vcc = 1.8 V**	**Vcc = 2 V**	**Vcc = 2.4 V**	**Vcc = 3V**	**Vcc = 3.3V**
110kΩ	299	333	372	401	411
150kΩ	234	258	284	305	311
180kΩ	202	222	243	258	263
200 kΩ	186	203	222	235	240
240 kΩ	160	173	188	198	202
270 kΩ	145	157	169	177	181
300 kΩ	132	143	153	161	163
390 kΩ	106	113	121	126	128
430 kΩ	97	104	110	115	116

AC Characteristics Test Load Circuits

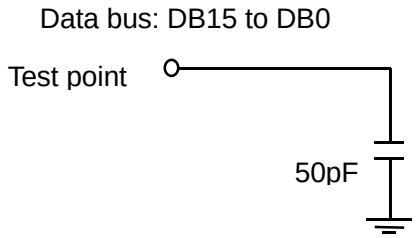


Figure 83 Load Circuit

Timing Characteristics

68-system Bus Operation

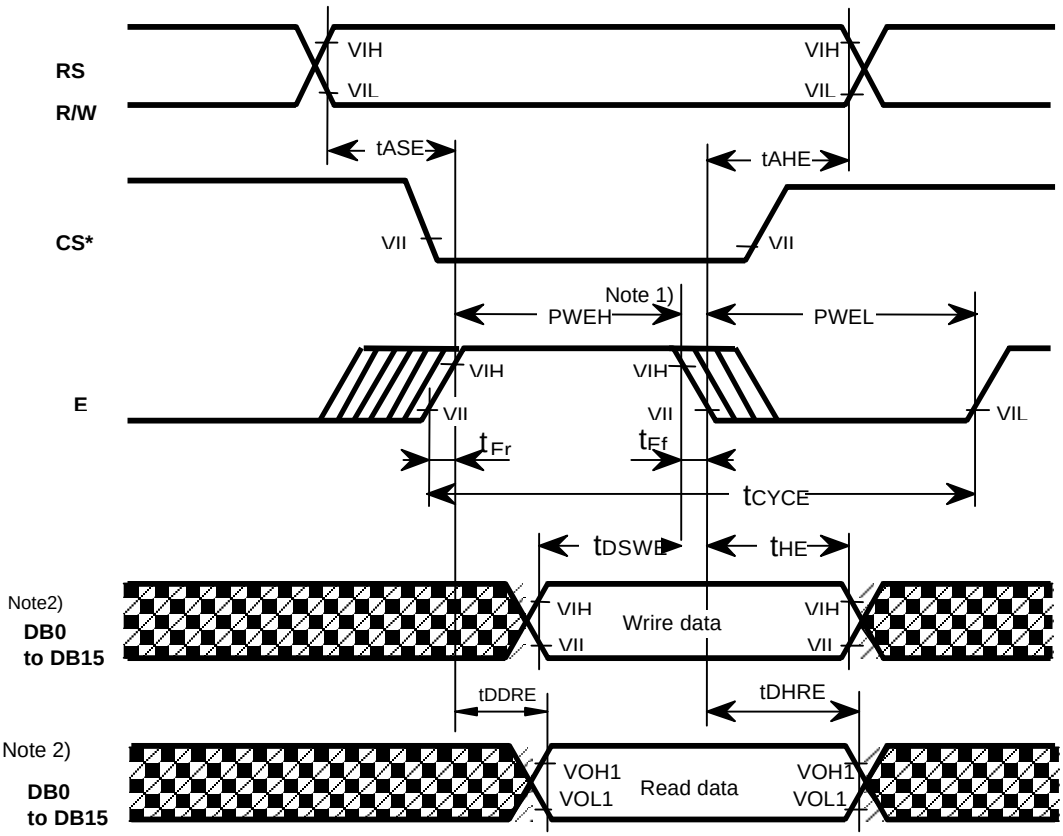


Figure 84 68-system Bus Timing

Notes: 1) PWEH is specified in the overlapped period when CS* is low and E is high.

2) Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used. Fix the DB7-0 pins to Vcc or GND.

80-system Bus Operation

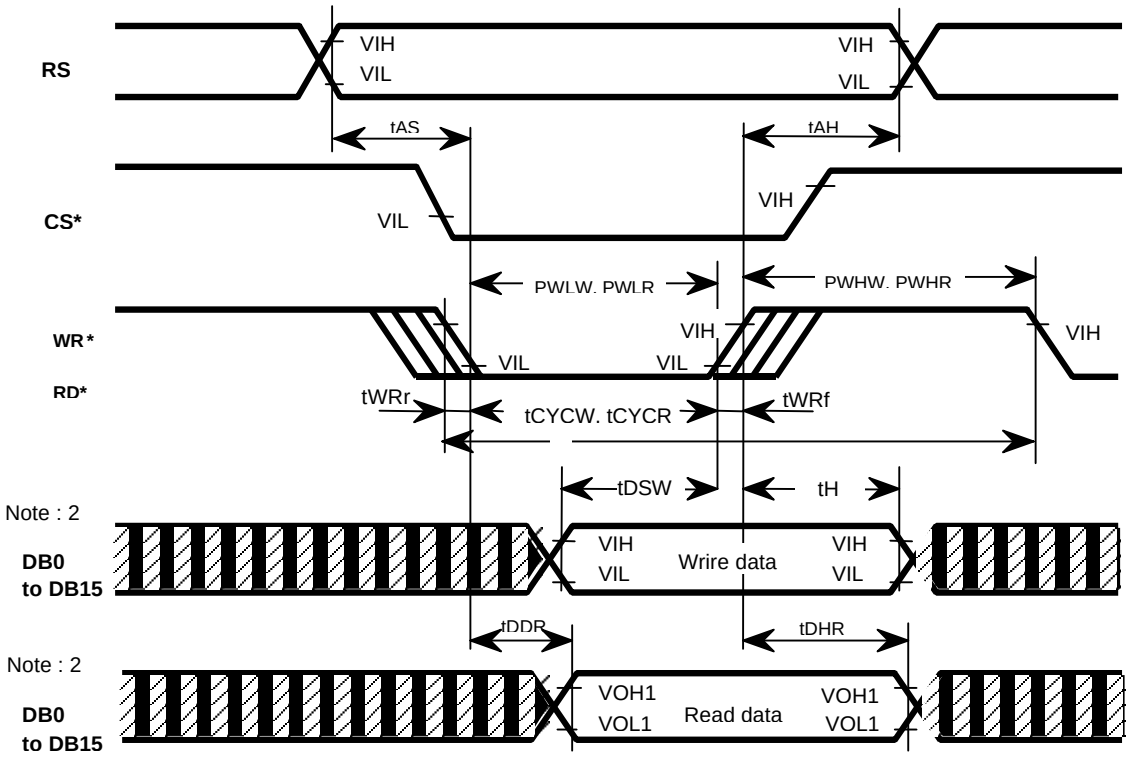


Figure 85 80-system Bus Timing

Notes: 1) PWLW and PWLR is specified in the overlapped period when CS* is low and WR* or RD* is low.

2) Parallel data transfer is enabled on the DB15-8 pins when the 8-bit bus interface is used. Fix the DB7-0 pins to Vcc or GND.

Clock Synchronized Serial Interface Operation

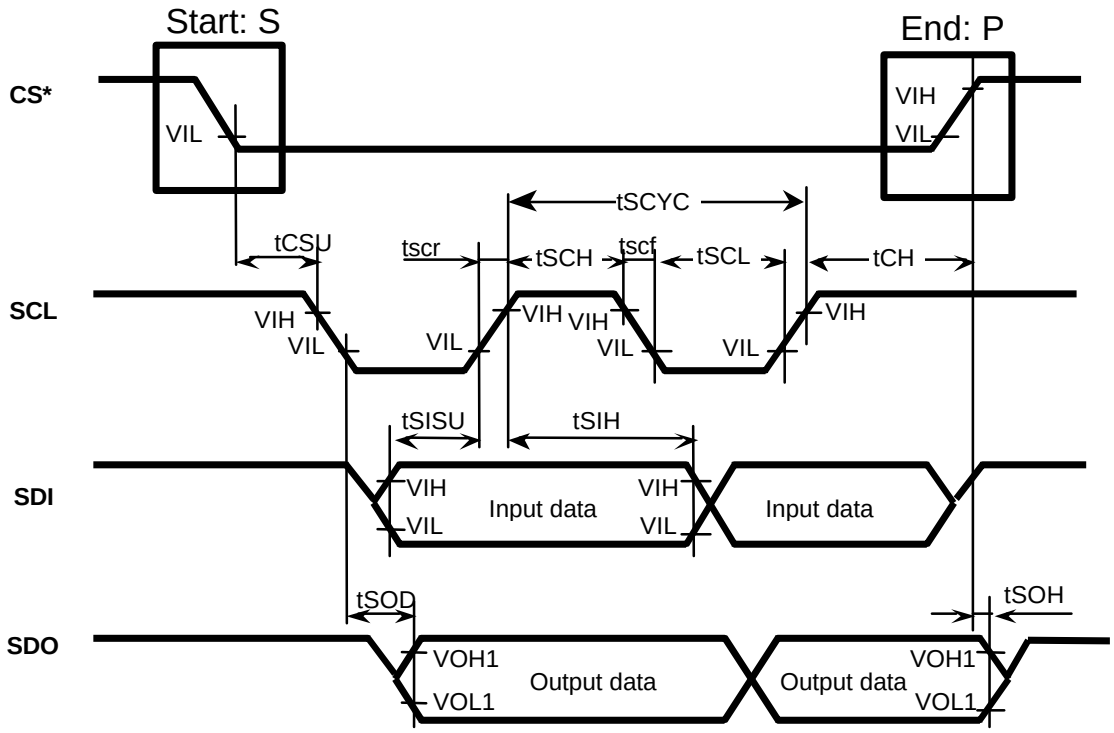


Figure 86 Clock Synchronized Serial Interface Timing

Reset Operation

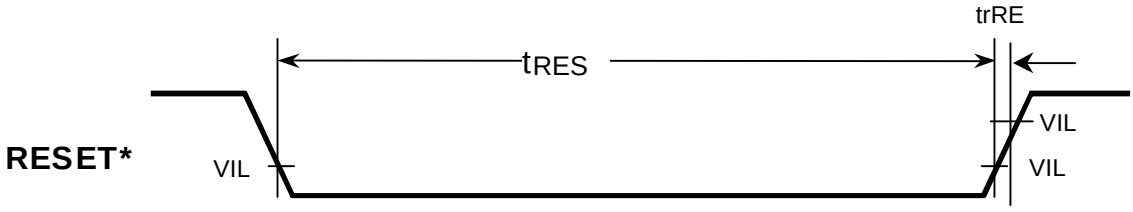


Figure 87 Reset Timing

Maintenance history report

P = page, L = line, - = blank

Rev	Date	Page	Maintenance history
0.6	2001.5.27	6,9	Chip thickness (from 400 um to 550 um)
		19,35 ,37	VRH4 bit deleted and PON bit added
		23	The explanation of REV bit changed
		32	Miswriting in the relation between GRAM data and Grayscale level
		47	Miswriting in B02
		62	Miswriting in the formula for V60
		67,71	Setting flow changed (put " wait 2H period or longer" before ON)
		69-70	The connection example changed (condenser between Vcom-Vgoff deleted) (from V61P, V61N to V63P, V63N)
		81-92	AC characteristic added
			Other miswriting
0.7	2001.6.11	43	The example of the operation of high-speed consecutive writing to RAM (8-bit bus interface) added
		62,64	Miswriting in Voltage formula for V8 and V55
1.0	2001.6.22	67	Waiting time for color transition (from 200ms to 400ms)
		82,83	specification added (current consumption, LCD drive power supply, deviation of output voltage, dispersion average of output voltage, RC oscillation clock)
		84,86	specification changed (68 system bus interface/Enable low-level pulse width PWEL/ from 100ns to 70ns) (80 system bus interface/ write high-level pulse width PWHW/ from 100ns to 70ns)
		89	graph for note 6 added
		90	table for note 10 added
1.0-1	2001.10.2	5	EQ (From "output the timing for equalizing Low: Normal display High: Equalizing " to "Indicate setting of the Vcom output to its high-impedance state during transitions of Vcom when Vcom is being AC-cycled. Low: VcomH or VcomL is being output on the Vcom pin. High: Vcom pin is in high-impedance state"
			DISPTMG (From "Non-display" to "Output Voff signal")
			GCS (From "transfer" to "transfer data")
		21	BT2-0 (Add the sentence below. "Lower amplification of the step-up circuit consumes less current.")
			SLP (from "Only the following instructions can be executed during the sleep mode." to "Only serial transfer to a gate driver / power-supply IC and the following instructions can be executed during the sleep mode)"
		22	VC2-0 (from "VREG1" to "VREG1OUT")
			VRL3-0 (from "from 2 to 8.5 times" to "from –2 to –8.5 times")
		23	VDV4-0 (from "When Vcom is driven in A/C amplitude." to "Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed.")
		26	Table14 (from "VGH" to "Vgon")

1.0-1	2001.10.2	27	TE (from “driver/IC chip of the power driver” to “driver/Power supply IC”)
			* (from “gate driver son after” to “gate driver / power supply IC soon after”)
		28	Table18 (from “the gate driver instruction” to “Power supply IC (HD667P00) instructions”)
			from “IC chip of the power supply” to “Power supply IC (HD667P00)”
		31	Note (from “common driver” to “gate driver”)
		32	SS17-0 (from “common driver” to “gate driver”)
			SE17-0 (from “black display driving ” to “bib-selection driving”)
			SE27-0 (from “4FH” to “AFH”)
		40	3. (from “B-pattern LC AC drive control” to “LCD driving AC control)”
		51	Restriction on window address-range settings (from “3FH” to “83H”) Restriction on address settings during the window address (from “HSA5” to “HSA7”)
		63	from “subtle adjustment” to “micro adjustment”
		66	Title for Y axis of Figure 60,61,and 62 (from vertical writing to horizontal writing)
			Add the number 1 and 2 to “Gradient adjusting register ” and “Amplitude adjusting register”.
		67	Add the number 3 to “Micro-adjusting register”.
		68	Add the sub-title “Block configuration” for the title “Ladder Registor/8 to 1 Selector”
		75	Corrected the Waiting time (from 400ms to 40ms)
		76	Corrected the title. (from “System Structure Example ” to “Example of System Configuration”)
		77	Corrected Note 4 (from “Following connection capacity if GD667P00 is not stated.” To “Condensers connected to following terminals of HD667P00 are omitted.”)
		78	Corrected Note 1 (from HD667P0 to HD667P00)
		79	Add the sentence at the end of the sentence. (Follow the below serial transfer flow about each setting and then transfer must be executed.)

P = page, L = line, - = blank

Rev	Date	Page	Maintenance history
1.0-1	2001.10.2	81	Delete unnecessary note from Figure 72 (200KHz)
			Correct Note (from “The Rf resistance must be located near the OSC1/OSC2 pin on the chip.” to “ The Rf resistance must be located near the OSC1/OSC2 pin on the master side.”)
		82	Correct Note (from “Specify the number of AC drive raster-rows and the necessity of EOR so that DC bias is not generated the liquid crystal.” to “In an n-raster-row driving EOR should be “1” so that DC bias voltage is not applied.)”
		83	Correct the sentence (L5, “field interlace,,, “ to “3-field interlace,,,”)
		84	Correct the title (from “Timing of Changing Polarity” to “AC Driving Timing”)
			Add a sentence (in L5 “The amount of blanking periods becomes 16H in a frame.”)
		86	Correct a sentence (in L7-8 “,,,the 1st and 2nd screens must correspond to the LCD-driving duty set value.” to “,,,the 1st and 2nd screens must be the number of LCD drive raster-rows or less.”)
1.1	2002.4.5	7	Change product model name. “From HD66770 to HD667A70”
		10	Change product model name. “From HD66770 to HD667B70”
		33	Add Note 3
		37	Add Grayscale reference-value adjusting resistor. (R3F)
			Add an explanation sentence for VDR1-0.
		39	Add Grayscale reference-value adjusting resistor. (R3Fh)
		64-68	Add Grayscale reference-value adjusting resistor.
		69,71	Change a formula (r) for adding grayscale reference-value adjusting resistor.
		77,78	Change example chart of connection. (Figure 69, and 70)
		79	Add New page, “Specification of capacitor”.
		80	Change a flow of “Display OFF” (Add “EQ=1”)