HD66774

240-Channel Gate Driver for Color-TFT Liquid Crystal Displays

HITACHI

Rev.1.0
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Description

HD66774 is a gate-driver IC for systems with color-TFT-liquid-crystal dot-matrix graphic displays. It incorporates a circuit for driving 240 channels of TFT gate-line driving and all the power-supply circuits that are required for liquid crystal displays, and realizes the liquid crystal display by adding only an external capacitor.

When used with the HD66770 396-channel source driver with on-chip RAM, and used with the HD66772 528-channel source driver with on-chip RAM, this LSI is suitable for color TFT displays of cellular phones having 132-by-176 and 176-by-240 dots, respectively.

Features

- TFT gate-line driving circuits
  - 240 outputs
- Gate-line scanning
  - Centering-screen function (vertically separated, comb type)
- Internal power-supply circuit
  - Step-up circuit: five to nine times, positive-polarity inversion
  - Structure of TFT-display retention capacitor: Cst or Cadd
- Alternating functions for TFT-display counter-electrode power supply
  - N-line alternating drive of Vcom (Vgoff is also available for N-line alternating drive for Cadd)
  - Adjustment of Vcom (Vgoff) amplitude: internal 22-level digital potentiometer
- Output power-supply voltage
  - For the source driver: DDVDH - GND = 4.5 to 5.5 V (power supply for HD66770/772 liquid crystal output circuits), VDH - GND = 3.0 to DDVDH-0.5V (reference power supply for HD66770/772 grayscale voltages)

— For the TFT-display counter electrode: Vcom amplitude = 6 V (max), VcomH - GND = 3.0V to VDH , VcomL - GND = 1.0 V to VCL + 0.5 V.

- Mode setting
  — Serial transfer from the HD66770/772 source driver
- Low-power consumption
  — Equalizing function and the switching performance of step-up circuits and operational amplifiers
- Input power-supply voltage
  — Vcc - GND = 1.7 to 3.6 V
  — Vci - GND = 2.5 to 3.6 V (internal reference power-supply voltage)
- Pad arrangement
  — Wiring-through area for high-level mounting

Type Number

Type Number	External Appearance
HCD66774BP	Die with Au bump

Pin Functions

Table 1 Pin Functions

Signal Name	Quantity*	Input/ Output	Connected to	Function
Vcc1, Vcc2	2	Input	Power supply	VCC-GND: A logic-circuit power supply. Supply the same voltage as that for HD66770/772. Vcc1 and Vcc2 are equivalent. Supply the voltage to either or both.
GND	1	Input	Power supply	
VDH	1	Output	Capacitor for stabilization, HD66770/772	A reference power supply for the HD66770/772 source-driver grayscale voltage. Adjust the VDH level with VREG1OUT because the VREG1OUT input voltage is output as the output level. Connect a capacitor for stabilization.
VGH	1	Input	VLOUT2 or power supply	A power supply for the gate-line driving circuit, and a positive-side power supply for TFT-gate on level, internal step-up circuits, bias circuits, and operational amplifiers. Connect VLOUT2. When VLOUT2 is not used, connect an external-voltage power supply lower than 16.5 V.
VGL	1	Input	VLOUT3 or power supply	A power supply for the gate-line driving circuit, and a negative-side power supply for the power supply for the gate-line driving circuit, internal step-up circuits, bias circuits, and operational amplifiers. Connect VLOUT3. When VLOUT3 is not used, connect an external-voltage power supply higher than -16.5 V.
Vci	1	Input	Vcc or power supply	A power supply for the analog circuit. Connect a 2.5- to 3.6-V external-voltage power supply.
Vciout	1	Output	Vci1 and capacitor for stabilization or open	Outputs the internal reference voltage generated between Vci and GND. The internal reference voltage can be set by a register.
Vci1	1	Input	VciOUT or power supply	A step-up voltage for step-up circuit 1. Connect Vciout or an external power supply lower than 2.75 V.
VLOUT1	1	Output	DDVDH and capacitor for stabilization or open	Outputs a voltage that doubles or triples the voltage from step-up voltage Vci1. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. When this pin is not used, leave it open.

Table 1 Pin Functions (cont)

Signal Name	Quantity*	Input/ Output	Connected to	Function
DDVDH	1	Input	VLOUT1 or power supply and HD66770/772	A power supply for outputting the HD66770/772 source driver liquid crystal. Connect this pin to VLOUT1. When VLOUT1 is not used, connect an external power supply lower than 5.5 V.
Vci2	1	Input	VLOUT1 or power supply	A reference voltage in step-up circuit 2. Connect this pin to VLOUT1. When VLOUT1 is not used, connect an external power supply lower than 5.5 V.
VLOUT2	1	Output	VGH, capacitor for stabilization or open	A voltage that doubles, triples, or quadruples, and outputs a voltage between DDVDH and GND in step-up circuit 2. The step-up factor can be set in an internal register. Connect a capacitor for stabilization. When this pin is not used, leave it open.
Vci3	1	Input	VLOUT2 or power supply	A reference voltage in step-up circuit 3. Connect this pin to VLOUT2. When VLOUT2 is not used, connect an external power supply lower than 16.5 V.
VLOUT3	1	Output	VGL, capacitor for stabilization or open	A voltage that outputs a voltage between VLOUT2 and GND as an equivalent negative voltage in step-up circuit 3. Connect a capacitor for stabilization. When this pin is not used, leave it open.
Vci4	1	Input	Vcc or Vci or power supply	A reference voltage in step-up circuit 4. Connect Vci or an external power supply lower than 2.5 V to 3.6 V.
VLOUT4	1	Output	VCL and capacitor for stabilization or open	A voltage that outputs a voltage between Vci4 and GND as an equivalent negative voltage in step-up circuit 4. Connect a capacitor for stabilization and the VCL pin. When this pin is not used, leave it open.
VCL	1	Input	VLOUT4 or power supply	A power supply for generating VcomL. When VcomL is a negative voltage, connect VLOUT4 or an external power supply of –3.6 to –2.5V.

Table 1 Pin Functions (cont)

Signal Name	Quantity*	Input/ Output	Connected to	Function
VREG1OUT	1	Output	Capacitor for stabilization and VREG1 or open	This pin generates and outputs a reference voltage for VREG1 between DDVDH and GND from the reference voltage between Vci and GND that is internally generated. The amplification can be set in an internal register. Connect this pin to VREG1 and a capacitor for stabilization. When this pin is not used, leave it open.
VREG1	1	Input	VREG1OUT or power supply	A reference voltage for generating Vcom. Connect VREG1OUT. When VREG1OUT is not used, connect an external power supply lower than DDVDH.
VREG2OUT	1	Output	Capacitor for stabilization and VREG2 or open	This pin generates and outputs a reference voltage for VREG2 between GND and VGL from the reference voltage between Vci and GND that is internally generated. The amplification can be set in an internal register. Connect this pin to VREG2 and a capacitor for stabilization. When this pin is not used, leave it open.
VREG2	1	Input	VREG2OUT or power supply	A reference voltage for generating Vgoff. Connect VREG2OUT. When VREG2OUT is not used, connect an external power supply lower than VGL.
C11+, C11- to C23+, C23-	10	-	Step-up capacitor	Connect the step-up capacitor according to the step-up factor. When the internal step-up circuit is not used, leave this pin open.
C31+, C31-	2	-	Step-up capacitor	Connect a step-up capacitor for generating the VGL level from the VGH and GND levels. When the internal step-up circuit is not used, leave these pins open.
C41+, C41-	2	-	Step-up capacitor	Connect a step-up capacitor for generating the –Vci4 level from the Vci4 and GND levels. When the internal step-up circuit is not used, leave these pins open.
Vcom1 Vcom2 Vcom3	3	Output	TFT-display common electrode	A power supply for the TFT-display common electrode. When the reversing Vcom alternation is not driven, the amplitude between VcomH and VcomL is output. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display common electrode.

Table 1 Pin Functions (cont)

Signal Name	Quantity*	Input/ Output	Connected to	Function
VcomR	1	Input	Variable resistor or open	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between VDH and GND. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	1	Output	Capacitor for stabilization	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	1	Output	Capacitor for stabilization or open	This pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VgoffOUT	1	Output	Vgoff or open	An output power supply for driving the gate line. Alternation can be driven by synchronizing Vcom with the setting of the internal register. Set the internal register according to the structure of the TFT-display retention capacitor. For the amplitude at the alternation driving, this pin outputs a voltage between VcomH and VcomL with the VgoffL reference voltage.
Vgoff	1	Input	Capacitor for stabilization, and VgoffOUT or power supply	This pin is a negative voltage at the TFT-gate off level. Connect this pin to VgoffOUT. When VgoffOUT is not used, connect an external-voltage power supply higher than the VGL voltage.
VgoffH	1	Output	Capacitor for stabilization or open	When the Vgoff alternation is driven, this pin indicates a high level of VgoffOUT. Connect this pin to a capacitor for stabilization. When the CAD bit is low, the VgoffH output stops and a capacitor for stabilization is not needed.
VgoffL	1	Output	Capacitor for stabilization	The VgoffOUT voltage when the Vgoff alternation is not driven. When the Vgoff alternation is driven, this pin indicates a low level of VgoffOUT. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization.
REGN, REGP	2	Input/ output	Open or capacitor for stabilization	Test pins for VREG1OUT, Vciout, and VREG2OUT. Leave these pins open.

Table 1 Pin Functions (cont)

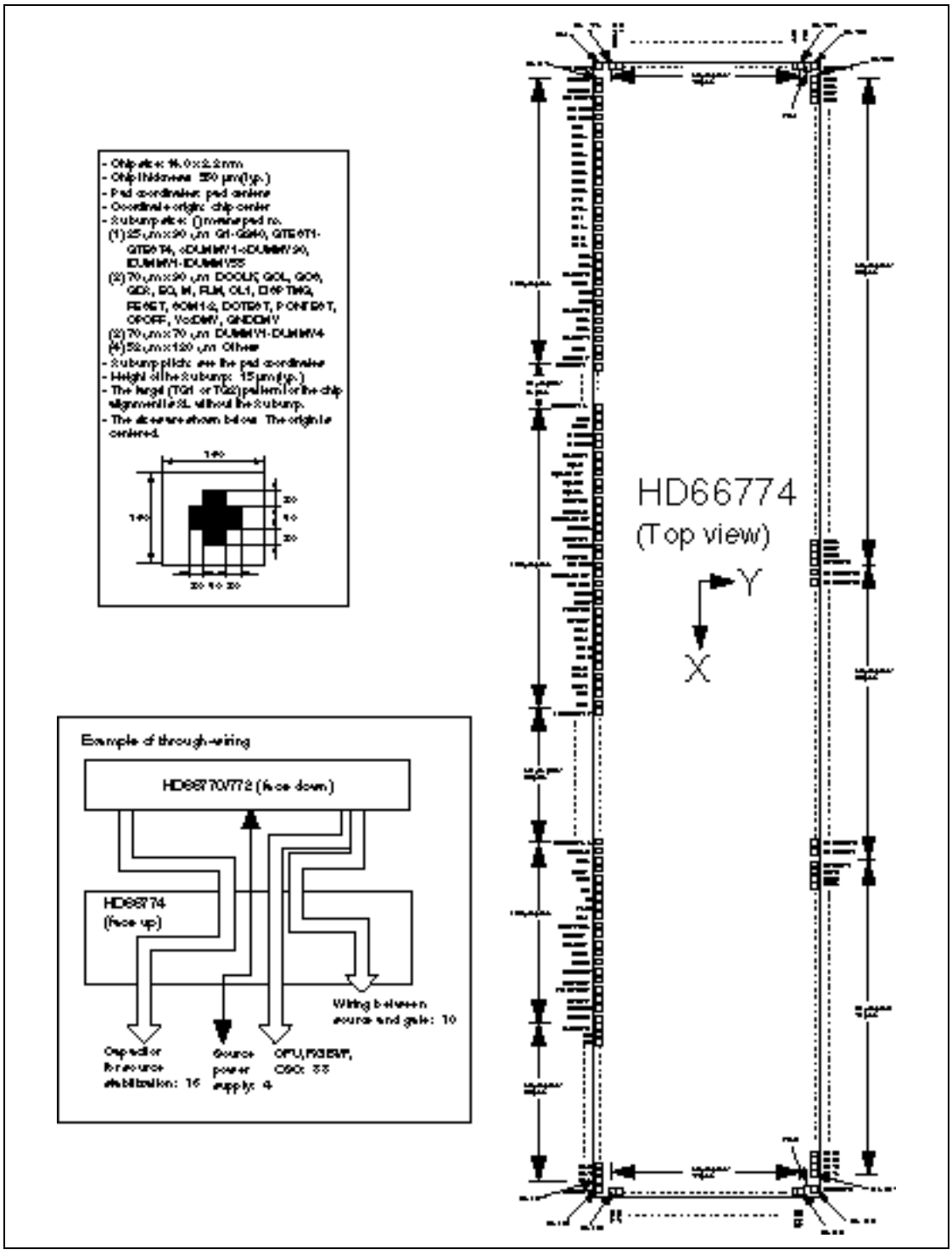
Signal Name	Quantity*	Input/ Output	Connected to	Function
M	1	Input	M of HD66770/772	Inputs alternating signal of Vcom and Vgoff. The following levels are output according to the status of M: Low: VcomL or VgoffL, high: VcomH or VgoffH When the VCOMG bit is low, the VcomL output stops and the low level of Vcom is output as GND. When the CAD bit is low, the VgoffH output stops.
EQ	1	Input	GND or EQ of HD66770/772	When the Vcom alternation is driven, the output of Vcom or VgoffOUT is Hi-Z at the transition timing of Vcom or VgoffOUT. The following levels are output according to the status of EQ: <table><tr><th>EQ</th><th>Vcom</th><th>Vgoff</th></tr><tr><td>Low</td><td>Vcom H/VcomL</td><td>VgoffH/VgoffL</td></tr><tr><td>High</td><td>Hi-Z</td><td>Hi-Z(Cadd structure) VgoffL(Cst structure)</td></tr></table> Note: When EQ = high, the output status of VgoffOUT depends on the mode setting of the structure of the TFT-display retention capacitor. For the mode setting, refer to the Instructions section. When EQ is not used, connect this pin to GND.
DCCLK	1	Input	DCCLK of HD66770/772	A clock for the step-up circuits supplied from HD66770/772.
CL1	1	Input	CL1 of HD66770/772	Clock input pin supplied from HD66770/772. Gate line output changes at the falling edge of this signal. This signal is supplied from HD66770/772.
FLM	1	Input	FLM of HD66770/772	Performs frame synchronization with the source driver. This signal is supplied from HD66770/772.
DISPTMG	1	Input	DISPTMG of HD66770/772	Display-off signal. This signal becomes valid asynchronously with the FLM and CL1. High: Normal output; Low: All output Vgoff.
GCL	1	Input	GCL of HD66770/772	Operates as a clock for the transfer of register settings. Latches data on the rising edge of the clock.
GDA	1	Input	GDA of HD66770/772	Operates as the data for the transfer of register settings.
GCS*	1	Input	GCS* of HD66770/772	A chip-select signal. Low: selected (data-transfer enabled), high: not selected (data-transfer disabled)
RESET*	1	Input	External reset circuit	The reset pin. When a low level is input here, the LSI is reinitialized. Be sure to apply a signal to this pin during the system's power-on reset.

Table 1 Pin Functions (cont)

Signal Name	Quantity*	Input/ Output	Connected to	Function
SCM1, 2	2	Input	Vcc or GND	Input for selecting the scan mode. Must be fixed to Vcc or GND depending on the selected scan mode.
OPOFF	1	Input	Vcc or GND	When OPOFF = Vcc, the operation of the operational amplifier stops. (At this time, the function is AP2-0 = (0,0,0) or equivalent.) When the voltage for driving the gate circuit is supplied from the external power supply voltage, OPOFF = Vcc should be satisfied. When it is supplied from the internal power supply voltage, OPOFF = GND must be satisfied.
G1-240	240	Output	Liquid crystal output	An output signal to the gate line. Outputs VGH as the gate-line selection level, or Vgoff as the gate-line non-selection level.
GTEST1-4	4	Output	Liquid crystal output or open	Dummy gate outputs. When CAD bit is high, output VGH and Vgoff level. When CAD is low, output Vgoff level. When this pin is not used, leave it open.
TESTA1	1	Input/ output	Test pin	A test pin for the VcomH output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA2	1	Input/ output	Test pin	A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA3	1	Input/ output	Test pin	A test pin for the VgoffH output. Leave it open or connect a capacitor for stabilization according to the display quality.
TESTA4	1	Input/ output	Test pin	A test pin for the VcomL output. Leave it open or connect a capacitor for stabilization according to the display quality.
PONTEST DCTEST2	2	Input	GND	Test pins. Connect GND.
VTEST	1	Input/ output	Test pin	A test pin. Must be left open.

Note: The quantity does not match the number of pads.

HCD66774BP Pad Arrangement



HCD66774BP Pad Coordinates

The pad coordinates are shown below. The pad numbers in the pad arrangement correspond to the numbers in the following table that lists the pad center coordinates with the chip-centered origin.

No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)
1	DUMMY1	-6870	-1470	61	VcomL	-1260	-1437	121	GCL	3280	-1460
2	Vcom1	-6680	-1437	62	TESTA4	-1160	-1437	122	GCS*	3380	-1460
3	Vcom1	-6580	-1437	63	VcomH	-1060	-1437	123	GDA	3480	-1460
4	DUMMY5	-6480	-1437	64	TESTA1	-960	-1437	124	EQ	3580	-1460
5	Vcom2	-6380	-1437	65	VcomR	-860	-1437	125	M	3680	-1460
6	Vcom2	-6280	-1437	66	VREG1OUT	-760	-1437	126	FLM	3780	-1460
7	C31-	-6180	-1437	67	VREG1	-660	-1437	127	CL1	3880	-1460
8	C31+	-6080	-1437	68	REGN	-560	-1437	128	DISPTMG	3980	-1460
9	C21-	-5980	-1437	69	REGP	-460	-1437	129	RESET*	4080	-1460
10	C21+	-5880	-1437	70	TESTA2	-360	-1437	130	VccDMY	4180	-1460
11	C22-	-5780	-1437	71	VTEST	-260	-1437	131	SCM1	4280	-1460
12	C22+	-5680	-1437	72	Vcc1	-160	-1437	132	SCM2	4380	-1460
13	C23-	-5580	-1437	73	Vcc1	-60	-1437	133	GndDMY	4480	-1460
14	C23+	-5480	-1437	74	Gnd	40	-1437	134	DCTEST	4580	-1460
15	C41-	-5380	-1437	75	Gnd	140	-1437	135	PONTEST	4680	-1460
16	C41+	-5280	-1437	76	Vcc2	240	-1437	136	OPOFF	4780	-1460
17	C11-	-5180	-1437	77	Vcc2	340	-1437	137	Vcom3	4880	-1437
18	C11+	-5080	-1437	78	Vci4	440	-1437	138	Vcom3	4980	-1437
19	C12-	-4980	-1437	79	Vci	540	-1437	139	GTEST2	5075	-1460
20	C12+	-4880	-1437	80	Vci	640	-1437	140	G2	5135	-1460
21	VGL	-4780	-1437	81	iDUMMY17	740	-1460	141	G4	5195	-1460
22	VGL	-4680	-1437	82	iDUMMY18	800	-1460	142	G6	5255	-1460
23	VLOUT3	-4580	-1437	83	iDUMMY19	860	-1460	143	G8	5315	-1460
24	Vci3	-4480	-1437	84	iDUMMY20	920	-1460	144	G10	5375	-1460
25	VGH	-4380	-1437	85	iDUMMY21	980	-1460	145	G12	5435	-1460
26	VGH	-4280	-1437	86	iDUMMY22	1040	-1460	146	G14	5495	-1460
27	VLout2	-4180	-1437	87	iDUMMY23	1100	-1460	147	G16	5555	-1460
28	VCL	-4080	-1437	88	iDUMMY24	1160	-1460	148	G18	5615	-1460
29	VCL	-3980	-1437	89	iDUMMY25	1220	-1460	149	G20	5675	-1460
30	VLout4	-3880	-1437	90	iDUMMY26	1280	-1460	150	G22	5735	-1460
31	Vci1	-3780	-1437	91	iDUMMY27	1340	-1460	151	G24	5795	-1460
32	Vciout	-3680	-1437	92	iDUMMY28	1400	-1460	152	G26	5855	-1460
33	iDUMMY1	-3520	-1460	93	iDUMMY29	1460	-1460	153	G28	5915	-1460
34	iDUMMY2	-3460	-1460	94	iDUMMY30	1520	-1460	154	G30	5975	-1460
35	iDUMMY3	-3400	-1460	95	iDUMMY31	1580	-1460	155	G32	6035	-1460
36	iDUMMY4	-3340	-1460	96	iDUMMY32	1640	-1460	156	G34	6095	-1460
37	iDUMMY5	-3280	-1460	97	iDUMMY33	1700	-1460	157	G36	6155	-1460
38	iDUMMY6	-3220	-1460	98	iDUMMY34	1760	-1460	158	G38	6215	-1460
39	iDUMMY7	-3160	-1460	99	iDUMMY35	1820	-1460	159	G40	6275	-1460
40	iDUMMY8	-3100	-1460	100	iDUMMY36	1880	-1460	160	G42	6335	-1460
41	iDUMMY9	-3040	-1460	101	iDUMMY37	1940	-1460	161	G44	6395	-1460
42	iDUMMY10	-2980	-1460	102	iDUMMY38	2000	-1460	162	G46	6455	-1460
43	iDUMMY11	-2920	-1460	103	iDUMMY39	2060	-1460	163	G48	6515	-1460
44	iDUMMY12	-2860	-1460	104	iDUMMY40	2120	-1460	164	G50	6575	-1460
45	iDUMMY13	-2800	-1460	105	iDUMMY41	2180	-1460	165	G52	6635	-1460
46	iDUMMY14	-2740	-1460	106	iDUMMY42	2240	-1460	166	G54	6695	-1460
47	iDUMMY15	-2680	-1460	107	iDUMMY43	2300	-1460	167	G56	6755	-1460
48	iDUMMY16	-2620	-1460	108	iDUMMY44	2360	-1460	168	DUMMY2	6870	-1470
49	VDH	-2460	-1437	109	iDUMMY45	2420	-1460	169	G58	6860	-1280
50	Vci2	-2360	-1437	110	iDUMMY46	2480	-1460	170	G60	6860	-1220
51	DDVDH	-2260	-1437	111	iDUMMY47	2540	-1460	171	G62	6860	-1160
52	DDVDH	-2160	-1437	112	iDUMMY48	2600	-1460	172	G64	6860	-1100
53	VLOUT1	-2060	-1437	113	iDUMMY49	2660	-1460	173	G66	6860	-1040
54	Vgoff	-1960	-1437	114	iDUMMY50	2720	-1460	174	G68	6860	-980
55	VgoffOUT	-1860	-1437	115	iDUMMY51	2780	-1460	175	G70	6860	-920
56	VgoffH	-1760	-1437	116	iDUMMY52	2840	-1460	176	G72	6860	-860
57	VgoffL	-1660	-1437	117	iDUMMY53	2900	-1460	177	G74	6860	-800
58	TESTA3	-1560	-1437	118	iDUMMY54	2960	-1460	178	G76	6860	-740
59	VREG2	-1460	-1437	119	iDUMMY55	3020	-1460	179	G78	6860	-680
60	VREG2OUT	-1360	-1437	120	DCCLK	3180	-1460	180	G80	6860	-620

No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)
181	G82	6860	-560	241	G200	5000	1460	301	oDUMMY39	1340	1460
182	G84	6860	-500	242	G202	4940	1460	302	oDUMMY40	1280	1460
183	G86	6860	-440	243	G204	4880	1460	303	oDUMMY41	1220	1460
184	G88	6860	-380	244	G206	4820	1460	304	oDUMMY42	1160	1460
185	G90	6860	-320	245	G208	4760	1460	305	oDUMMY43	1100	1460
186	G92	6860	-260	246	G210	4700	1460	306	oDUMMY44	1040	1460
187	G94	6860	-200	247	G212	4640	1460	307	oDUMMY45	980	1460
188	G96	6860	-140	248	G214	4580	1460	308	oDUMMY46	920	1460
189	G98	6860	-80	249	G216	4520	1460	309	oDUMMY47	860	1460
190	G100	6860	-20	250	G218	4460	1460	310	oDUMMY48	800	1460
191	G102	6860	40	251	G220	4400	1460	311	oDUMMY49	740	1460
192	G104	6860	100	252	G222	4340	1460	312	oDUMMY50	680	1460
193	G106	6860	160	253	G224	4280	1460	313	oDUMMY51	620	1460
194	G108	6860	220	254	G226	4220	1460	314	oDUMMY52	560	1460
195	G110	6860	280	255	G228	4160	1460	315	oDUMMY53	500	1460
196	G112	6860	340	256	G230	4100	1460	316	oDUMMY54	440	1460
197	G114	6860	400	257	G232	4040	1460	317	oDUMMY55	380	1460
198	G116	6860	460	258	G234	3980	1460	318	oDUMMY56	320	1460
199	G118	6860	520	259	G236	3920	1460	319	oDUMMY57	260	1460
200	G120	6860	580	260	G238	3860	1460	320	oDUMMY58	200	1460
201	G122	6860	640	261	G240	3800	1460	321	oDUMMY59	140	1460
202	G124	6860	700	262	GTEST4	3740	1460	322	oDUMMY60	80	1460
203	G126	6860	760	263	oDUMMY1	3620	1460	323	oDUMMY61	20	1460
204	G128	6860	820	264	oDUMMY2	3560	1460	324	oDUMMY62	-40	1460
205	G130	6860	880	265	oDUMMY3	3500	1460	325	oDUMMY63	-100	1460
206	G132	6860	940	266	oDUMMY4	3440	1460	326	oDUMMY64	-160	1460
207	G134	6860	1000	267	oDUMMY5	3380	1460	327	oDUMMY65	-220	1460
208	G136	6860	1060	268	oDUMMY6	3320	1460	328	oDUMMY66	-280	1460
209	G138	6860	1120	269	oDUMMY7	3260	1460	329	oDUMMY67	-340	1460
210	G140	6860	1180	270	oDUMMY8	3200	1460	330	oDUMMY68	-400	1460
211	G142	6860	1240	271	oDUMMY9	3140	1460	331	oDUMMY69	-460	1460
212	G144	6860	1300	272	oDUMMY10	3080	1460	332	oDUMMY70	-520	1460
213	DUMMY3	6870	1470	273	oDUMMY11	3020	1460	333	oDUMMY71	-580	1460
214	G146	6620	1460	274	oDUMMY12	2960	1460	334	oDUMMY72	-640	1460
215	G148	6560	1460	275	oDUMMY13	2900	1460	335	oDUMMY73	-700	1460
216	G150	6500	1460	276	oDUMMY14	2840	1460	336	oDUMMY74	-760	1460
217	G152	6440	1460	277	oDUMMY15	2780	1460	337	oDUMMY75	-820	1460
218	G154	6380	1460	278	oDUMMY16	2720	1460	338	oDUMMY76	-880	1460
219	G156	6320	1460	279	oDUMMY17	2660	1460	339	oDUMMY77	-940	1460
220	G158	6260	1460	280	oDUMMY18	2600	1460	340	oDUMMY78	-1000	1460
221	G160	6200	1460	281	oDUMMY19	2540	1460	341	oDUMMY79	-1060	1460
222	G162	6140	1460	282	oDUMMY20	2480	1460	342	oDUMMY80	-1120	1460
223	G164	6080	1460	283	oDUMMY21	2420	1460	343	oDUMMY81	-1180	1460
224	G166	6020	1460	284	oDUMMY22	2360	1460	344	oDUMMY82	-1240	1460
225	G168	5960	1460	285	oDUMMY23	2300	1460	345	oDUMMY83	-1300	1460
226	G170	5900	1460	286	oDUMMY24	2240	1460	346	oDUMMY84	-1360	1460
227	G172	5840	1460	287	oDUMMY25	2180	1460	347	oDUMMY85	-1420	1460
228	G174	5780	1460	288	oDUMMY26	2120	1460	348	oDUMMY86	-1480	1460
229	G176	5720	1460	289	oDUMMY27	2060	1460	349	oDUMMY87	-1540	1460
230	G178	5660	1460	290	oDUMMY28	2000	1460	350	oDUMMY88	-1600	1460
231	G180	5600	1460	291	oDUMMY29	1940	1460	351	oDUMMY89	-1660	1460
232	G182	5540	1460	292	oDUMMY30	1880	1460	352	oDUMMY90	-1720	1460
233	G184	5480	1460	293	oDUMMY31	1820	1460	353	GTEST3	-1860	1460
234	G186	5420	1460	294	oDUMMY32	1760	1460	354	G239	-1920	1460
235	G188	5360	1460	295	oDUMMY33	1700	1460	355	G237	-1980	1460
236	G190	5300	1460	296	oDUMMY34	1640	1460	356	G235	-2040	1460
237	G192	5240	1460	297	oDUMMY35	1580	1460	357	G233	-2100	1460
238	G194	5180	1460	298	oDUMMY36	1520	1460	358	G231	-2160	1460
239	G196	5120	1460	299	oDUMMY37	1460	1460	359	G229	-2220	1460
240	G198	5060	1460	300	oDUMMY38	1400	1460	360	G227	-2280	1460

No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)
361	G225	-2340	1460	421	G105	-5940	1460
362	G223	-2400	1460	422	G103	-6000	1460
363	G221	-2460	1460	423	G101	-6060	1460
364	G219	-2520	1460	424	G99	-6120	1460
365	G217	-2580	1460	425	G97	-6180	1460
366	G215	-2640	1460	426	G95	-6240	1460
367	G213	-2700	1460	427	G93	-6300	1460
368	G211	-2760	1460	428	G91	-6360	1460
369	G209	-2820	1460	429	G89	-6420	1460
370	G207	-2880	1460	430	G87	-6480	1460
371	G205	-2940	1460	431	G85	-6540	1460
372	G203	-3000	1460	432	G83	-6600	1460
373	G201	-3060	1460	433	DUMMY4	-6870	1470
374	G199	-3120	1460	434	G81	-6860	1300
375	G197	-3180	1460	435	G79	-6860	1240
376	G195	-3240	1460	436	G77	-6860	1180
377	G193	-3300	1460	437	G75	-6860	1120
378	G191	-3360	1460	438	G73	-6860	1060
379	G189	-3420	1460	439	G71	-6860	1000
380	G187	-3480	1460	440	G69	-6860	940
381	G185	-3540	1460	441	G67	-6860	880
382	G183	-3600	1460	442	G65	-6860	820
383	G181	-3660	1460	443	G63	-6860	760
384	G179	-3720	1460	444	G61	-6860	700
385	G177	-3780	1460	445	G59	-6860	640
386	G175	-3840	1460	446	G57	-6860	580
387	G173	-3900	1460	447	G55	-6860	520
388	G171	-3960	1460	448	G53	-6860	460
389	G169	-4020	1460	449	G51	-6860	400
390	G167	-4080	1460	450	G49	-6860	340
391	G165	-4140	1460	451	G47	-6860	280
392	G163	-4200	1460	452	G45	-6860	220
393	G161	-4260	1460	453	G43	-6860	160
394	G159	-4320	1460	454	G41	-6860	100
395	G157	-4380	1460	455	G39	-6860	40
396	G155	-4440	1460	456	G37	-6860	-20
397	G153	-4500	1460	457	G35	-6860	-80
398	G151	-4560	1460	458	G33	-6860	-140
399	G149	-4620	1460	459	G31	-6860	-200
400	G147	-4680	1460	460	G29	-6860	-260
401	G145	-4740	1460	461	G27	-6860	-320
402	G143	-4800	1460	462	G25	-6860	-380
403	G141	-4860	1460	463	G23	-6860	-440
404	G139	-4920	1460	464	G21	-6860	-500
405	G137	-4980	1460	465	G19	-6860	-560
406	G135	-5040	1460	466	G17	-6860	-620
407	G133	-5100	1460	467	G15	-6860	-680
408	G131	-5160	1460	468	G13	-6860	-740
409	G129	-5220	1460	469	G11	-6860	-800
410	G127	-5280	1460	470	G9	-6860	-860
411	G125	-5340	1460	471	G7	-6860	-920
412	G123	-5400	1460	472	G5	-6860	-980
413	G121	-5460	1460	473	G3	-6860	-1040
414	G119	-5520	1460	474	G1	-6860	-1100
415	G117	-5580	1460	475	GTEST1	-6860	-1160
416	G115	-5640	1460				
417	G113	-5700	1460				
418	G111	-5760	1460				
419	G109	-5820	1460				
420	G107	-5880	1460				

No.	Pin Name	X (um)	Y (um)
-	TG1	-6740	1430
-	TG2	6740	1430

Internal Block Diagram

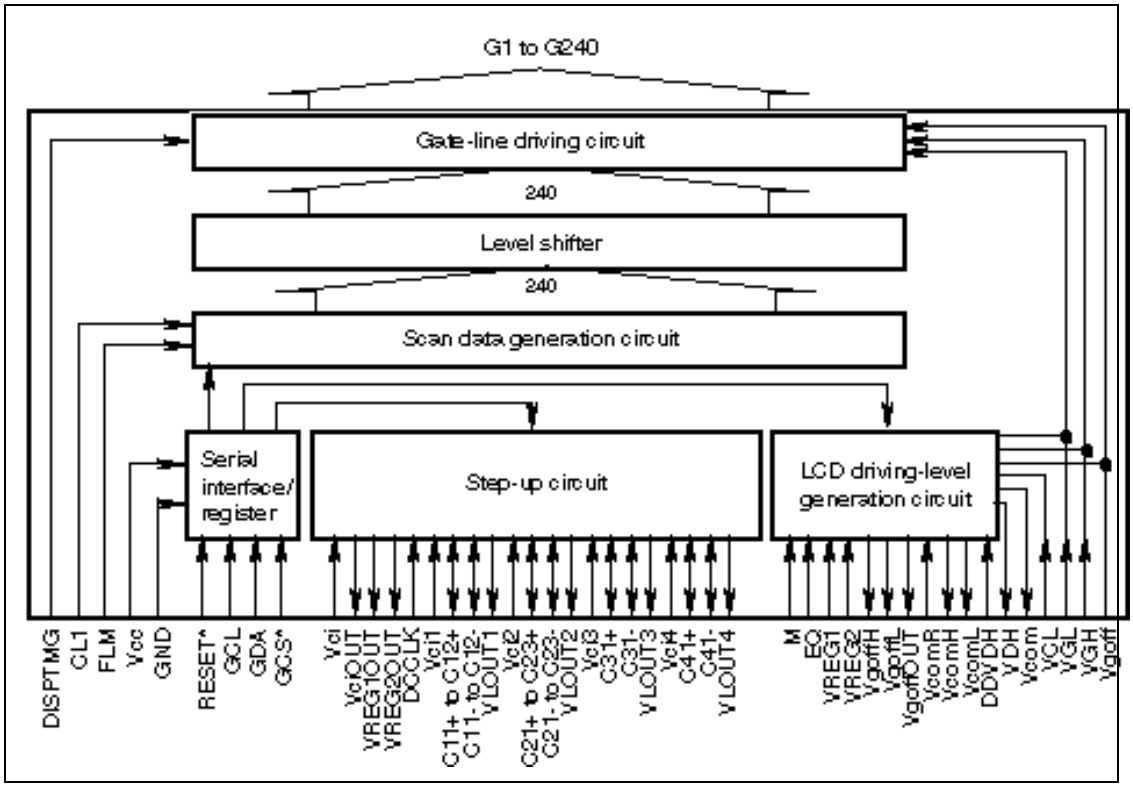


Figure 1 Block Diagram

Block Functions

1. Step-up circuit

Boosts the Vci1 voltage five to nine times. The required voltage is generated by combining double or triple step-up circuit 1 and double, triple, or quadruple step-up circuit 2. The factor is controlled by the register settings. A negative-polarity voltage is also generated according to the boosted voltage. For details on the register settings for the factor, refer to the Instructions section. The voltage generated from this circuit is used as the power-supply voltage that is supplied to VGH, VGL, and DDVDH. DDVDH level is supplied to HD66770/772.

2. Liquid-crystal driving-level generation circuit

Generates the VgoffOUT, VDH, and Vcom levels that are required to drive the TFT liquid crystal display, in addition to the voltage generated by the step-up circuit. VDH level is supplied to HD66770/772.

3. Interface/register circuit

Transfers data to the internal control register.

4. Scan data generation circuit

Selects the output of the gate line one by one according to the FLM signal, CL1 signal, and the setting of the internal control registers.

5. Level shifter

Converts the level of the operating power supply voltage Vcc - GND of the logic circuit to the level of the operating power supply voltage VGH - VGL of the gate-line driving circuit.

6. Gate-line driving circuit

Selects and outputs either the VGH or the Vgoff level according to the selection signal generated at the scan data generation circuit and the level shifter.

Instructions

Outline

HD66774 has five internal registers. The data is written on to these registers by using a gate serial data interface. This interface can be directly connected to the HD66770 or HD66772 source driver for an automatic transfer of instructions. When an instruction is written on to HD66770/772 via the bus from the CPU, it is output from the serial interface of HD66770/772, and HD66774 receives the instruction to adjust the settings of one of its internal registers.

In the bit configuration for the transfer of instructions, the upper three bits are index numbers that indicate the target register of the transfer, and the lower 13 bits are the data.

Detailed Description

Power Control 1 (R00h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	GON	VCOMG	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP
Index code															

Figure 2 Power Control 1 Instructions

BT2-0: Control the step-up factor of the step-up circuit. Adjust the step-up factor according to the power-supply voltage to be used. Set the output of VLOUT1 to 5.5 V or lower.

DC2-0: Set the step-up cycle of the step-up circuit. When the cycle is accelerated, the driving ability of the step-up circuit increases, but its current consumption increases too. Adjust the cycle taking into account the display quality and power consumption.

AP2-0: Adjust the amount of fixed current from the fixed-current source in the internal operational amplifier circuit. When the amount of fixed current becomes large, the driving ability of the operational-amplifier circuit increases. Adjust the fixed current taking into account the power-supply ability for each driver and the power consumption. During times when there is no display, such as when the system is in a sleep or a standby mode, AP2-0 can be set to (0, 0, 0) and the power consumption can be reduced by shutting down the operational amplifier.

SLP: Sets the sleep mode. When SLP = 1, G1 to G240 and GTEST1 to GTEST4 are output as GND, and bits AP2-0 are all fixed to 0. This stops the operation of the power-supply circuit. The state of the SLP bit does not change the values of these bits.

GON: When GON = 0 and DISPTMG = 0, G1 to G240 and GTEST1 to GTEST4 are output as GND. The Vcom output is also fixed to GND. When GON = 1, G1 to G240 are normally output and GTEST1 to GTEST4 output VGH/Vgoff level according to the state of CAD bit.

VCOMG: When VCOMG = 0, the low-level voltage of Vcom becomes GND, and the amplifier for the negative voltage and step-up circuit 4 stop. This enables low-power consumption. When VCOMG = 1, a positive or a negative voltage (1.0 V to –Vci + 0.5 V) of VcomL can be output. At this time, use the flow of power-supply setting. When VCOMG = 0, if the Vcom alternation is driven, the settings of VDV4-0 become invalid. Adjust the alternating amplitudes of Vcom and Vgoff with VCM4-0 in the VcomH settings.

Table 2 BT Bits and VLOUT1 and VLOUT2 Outputs

BT2	BT1	BT0	VLOUT1 Output	VLOUT2 Output	Notes*	Capacitor connection terminal
0	0	0	2 x Vci1	3 x Vci2	VLOUT2 = Vci1 x six times	VLOUT1 to VLOUT4,C11±, C21±,C22±,C31±,C41±
0	0	1	2 x Vci1	4 x Vci2	VLOUT2 = Vci1 x eight times	VLOUT1 to VLOUT4,C11±, C21±,C22±,C23±,C31±,C41±
0	1	0	3 x Vci1	3 x Vci2	VLOUT2 = Vci1 x nine times	VLOUT1 to VLOUT4,C11±, C12±,C21±,C22±,C31±,C41±
0	1	1	3 x Vci1	2 x Vci2	VLOUT2 = Vci1 x six times	VLOUT1 to VLOUT4,C11±, C12±,C21±,C22±,C31±,C41±
1	0	0	2 x Vci1	Vci1 + 2 x Vci2	VLOUT2 = Vci1 x five times	VLOUT1 to VLOUT4,C11±, C21±,C22±,C31±,C41±
1	0	1	2 x Vci1	Vci1 + 3 x Vci2	VLOUT2 = Vci1 x seven times	VLOUT1 to VLOUT4,C11±, C21±,C22±,C23±,C31±,C41±
1	1	0	Step-up stopped	3 x Vci2	VLOUT2 = Vci2 x three times	VLOUT1 to VLOUT4,C21±, C22±,C31±,C41±
1	1	1	Setting inhibited	Setting inhibited	Setting inhibited	—

Note: The step-up factors of VLOUT2 are derived from Vci1 when VLOUT1 and Vci2 are shorted. The conditions of VLOUT1 ≤ 5.5 V and VLOUT2 ≤ 16.5 V must be satisfied.

Table 3 DC Bits and Step-up Cycle

DC2	DC1	DC0	Step-up Cycle in Step-up Circuit 1	Step-up Cycle in Step-up Circuits 2/3/4
0	0	0	DCCLK divided by four	DCCLK divided by 16
0	0	1	DCCLK divided by two	DCCLK divided by 16
0	1	0	DCCLK	DCCLK divided by 16
0	1	1	DCCLK divided by two	DCCLK divided by four
1	0	0	DCCLK divided by four	DCCLK divided by eight
1	0	1	DCCLK divided by two	DCCLK divided by eight
1	1	0	DCCLK	DCCLK divided by eight
1	1	1	DCCLK	DCCLK divided by four

Table 4 AP Bits and Amount of Current in Operational Amplifier

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier and step-up circuit stops.
0	0	1	Small
0	1	0	Small medium
0	1	1	Medium
1	0	0	Medium large
1	0	1	Large
1	1	0	Setting inhibited
1	1	1	Setting inhibited

Voltage Setting 1 (R01h)

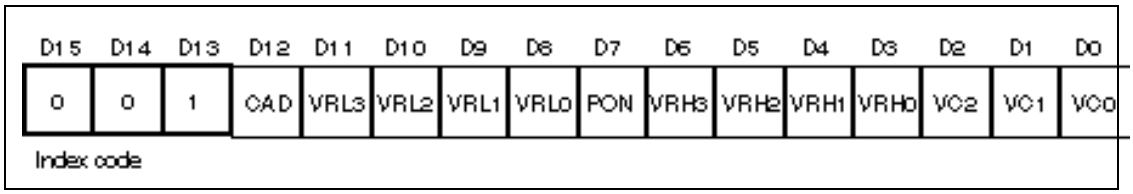


Figure 3 Voltage Setting 1 Instructions

VC2-0: Adjust the VREG1OUT, VREG2OUT, and Vciout voltages to a fraction of Vci.

PON: Starts operation of step-up circuit 3. The operation stops when PON = 0 and starts when PON = 1. For the timing when PON = 1, refer to the Flow of Power-Supply Setting section.

VRH3-0: Set the amplified factor of the VREG1OUT voltage (the voltage for the VREG1 reference voltage when the VDH and Vcom amplification is generated). These bits amplify the voltage 1.45 to 2.85 times the voltage set by VC2-0.

VRL3-0: Set the amplified factor of the VREG2OUT voltage (the voltage for the VREG2 reference voltage when Vgoff is generated). These bits amplify the voltage -3 to -9.5 times the voltage set by VC2-0. Note that the reference voltage of VREG2OUT is Vci.

CAD: Set this bit according to the structure for the TFT-display retention capacitor.
CAD = 0: Set this bit when the Cst retention capacitor is structured. The VgoffOUT outputs the VgoffL level regardless of the Vcom alternating drive.
CAD = 1: Set this bit when the Cadd retention capacitor is structured. At the Vcom alternating drive, the VgoffOUT voltage is output in the VgoffL voltage reference by the amount of Vcom alternating amplitude. GTEST1 to GTEST4 output VGH/Vgoff levels in the timing which is shown in figure 4.

Table 5 VC Settings and Internal Reference Voltage

VC2	VC1	VC0	REGP and VciOUT Output Voltage	REGN Output Voltage
0	0	0	0.92 x Vci	0.08 x Vci
0	0	1	0.83 x Vci	0.17 x Vci
0	1	0	0.73 x Vci	0.27 x Vci
0	1	1	0.68 x Vci	0.32 x Vci
1	0	0	Vci *2	GND
1	0	1	Setting inhibited	Setting inhibited
1	1	0	Setting inhibited	Setting inhibited
1	1	1	Setting inhibited	Setting inhibited

Note: 1. Leave REGP and REGN pins open because the voltage set above is output for REGP and REGN.

2. When VC2-0=100, VciOUT output is Hi-Z.

Table 6 VRH Bits and VREG1OUT Voltage

VRH3	VRH2	VRH1	VRH0	VREG1OUT Voltage
0	0	0	0	REGP x 1.45 times
0	0	0	1	REGP x 1.55 times
0	0	1	0	REGP x 1.65 times
0	0	1	1	REGP x 1.75 times
0	1	0	0	REGP x 1.80 times
0	1	0	1	REGP x 1.85 times
0	1	1	0	REGP x 1.90 times
0	1	1	1	Stopped
1	0	0	0	REGP x 2.175 times
1	0	0	1	REGP x 2.325 times
1	0	1	0	REGP x 2.475 times
1	0	1	1	REGP x 2.625 times
1	1	0	0	REGP x 2.700 times
1	1	0	1	REGP x 2.775 times
1	1	1	0	REGP x 2.850 times
1	1	1	1	Stopped

Note: Adjust the settings between the voltage set by VC2-0 and VRH0 to VRH3 so that the VREG1OUT voltage is lower than 5.0 V.

Table 7 VRL Bits and VREG2OUT Voltage

VRL3	VRL2	VRL1	VRL0	VREG2OUT Voltage
0	0	0	0	Vci -(Vci – REGN) x 3.0 times
0	0	0	1	Vci -(Vci – REGN) x 3.5 times
0	0	1	0	Vci -(Vci – REGN) x 4.0 times
0	0	1	1	Vci -(Vci – REGN) x 4.5 times
0	1	0	0	Vci -(Vci – REGN) x 5.0 times
0	1	0	1	Vci -(Vci – REGN) x 5.5 times
0	1	1	0	Vci -(Vci – REGN) x 6.0 times
0	1	1	1	Stopped
1	0	0	0	Vci -(Vci – REGN) x 6.5 times
1	0	0	1	Vci -(Vci – REGN) x 7.0 times
1	0	1	0	Vci -(Vci – REGN) x 7.5 times
1	0	1	1	Vci -(Vci – REGN) x 8.0 times
1	1	0	0	Vci -(Vci – REGN) x 8.5 times
1	1	0	1	Vci -(Vci – REGN) x 9.0 times
1	1	1	0	Vci -(Vci – REGN) x 9.5 times
1	1	1	1	Stopped

Notes: 1. Adjust the settings between the voltage set by Vci – (VC2-0) voltage and VRL0 to VRL3 so that the VREG2OUT voltage is higher than –16.0 V.

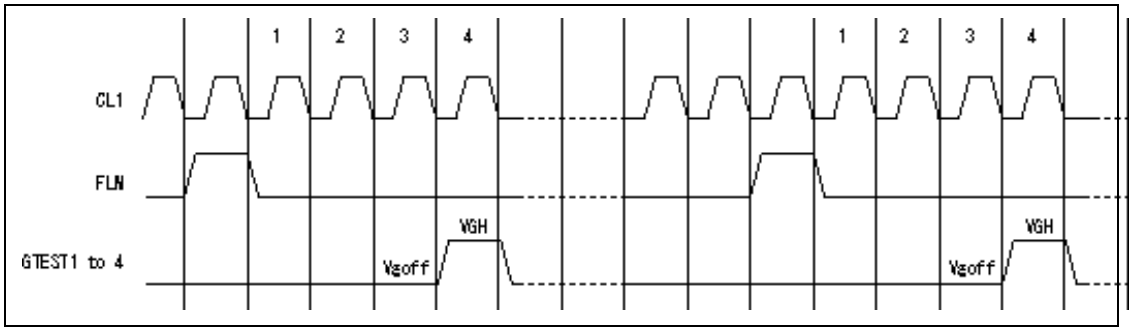


Figure 4 Output Timing for GTEST1 to GTEST4

Voltage Setting 2 (R02h)

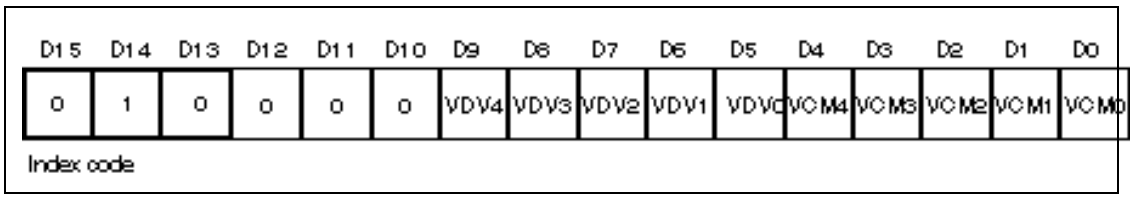


Figure 5 Voltage Setting 2 Instructions

VCM4-0: Set the VcomH voltage (a high-level voltage at the Vcom alternating drive).
These bits amplify the VcomH voltage 0.4 to 0.98 times the VREG1 voltage. When VCOM4-0 = 1,

the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

VDV4-0: Set the alternating amplitudes of Vcom and Vgoff at the Vcom alternating drive. These bits amplify Vcom and Vgoff 0.6 to 1.23 times the VREG1 voltage. When the Vcom alternation is not driven, the settings become invalid.

Table 8 VCM4-0 Bits and VcomH Voltage

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH Voltage
0	0	0	0	0	VREG1 x 0.40 times
0	0	0	0	1	VREG1 x 0.42 times
0	0	0	1	0	VREG1 x 0.44 times
:	:	:	:	:	:
0	1	1	0	0	VREG1 x 0.64 times
0	1	1	0	1	VREG1 x 0.66 times
0	1	1	1	0	VREG1 x 0.68 times
0	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.
1	0	0	0	0	VREG1 x 0.70 times
1	0	0	0	1	VREG1 x 0.72 times
1	0	0	1	0	VREG1 x 0.74 times
:	:	:	:	:	:
1	1	1	0	0	VREG1 x 0.94 times
1	1	1	0	1	VREG1 x 0.96 times
1	1	1	1	0	VREG1 x 0.98 times
1	1	1	1	1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.

Note: Adjust the settings between VREG1 and VCM0 to VCM4 so that the VcomH voltage is lower than VDH.

Table 9 VDV4-0 Bits and Vcom Amplitude

VDV4	VDV3	VDV2	VDV1	VDV0	Vcom Amplitude
0	0	0	0	0	VREG1 x 0.60 times
0	0	0	0	1	VREG1 x 0.63 times
0	0	0	1	0	VREG1 x 0.66 times
:	:	:	:	:	:
0	1	1	0	0	VREG1 x 0.96 times
0	1	1	0	1	VREG1 x 0.99 times
0	1	1	1	0	VREG1 x 1.02 times
0	1	1	1	1	Setting inhibited
1	0	0	0	0	VREG1 x 1.05 times
1	0	0	0	1	VREG1 x 1.08 times
1	0	0	1	0	VREG1 x 1.11 times
1	0	0	1	1	VREG1 x 1.14 times
1	0	1	0	0	VREG1 x 1.17 times
1	0	1	0	1	VREG1 x 1.20 times
1	0	1	1	0	VREG1 x 1.23 times
1	0	1	1	1	Setting inhibited
1	1	*	*	*	Setting inhibited

Note: Adjust the settings between VREG1 and VDV0 to VDV4 so that the Vcom and VgoffOUT amplitudes are lower than 6.0 V.

Output Start-Position Control and Number of Valid Lines Control (R06h)

Output Scan-Direction Control and Output Scan-Method Control (R07h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	GS	NL4	NL3	NL2	NL1	NL0	SCN4	SCN3	SCN2	SCN1	SCN0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	FLD1	FLD0

Index code

Figure 6 R06h and R07h Instructions

GS: Selects the output scan direction of the gate driver. For description on the GS value and the scan direction, refer to the section of scan mode setting.

SCN4-0: Set the output start position. According to the correspondence between the setting values and the output start position in table 11, start driving the gate line by the gate-line selection circuit.

NL4-0: Set the number of valid lines from the output start position. According to the correspondence between the setting values and the valid lines in table 12, drive the gate line for the number of valid lines using the gate-line selection circuit.

Set the NL4-0 and SCN4-0 so that (output start position + number of valid lines) - 1 ≤ 240 lines.

Table 10 Correspondence between SCN4-0 and Output Start Position

					Output Start Position					
SCN4	SCN3	SCN2	SCN1	SCN0	SCM1=GND SCM2=GND GS=0	SCM1=GND SCM2=GND GS=1	SCM1=Vcc SCM2=GND GS=0	SCM1=Vcc SCM2=GND GS=1	SCM1=Vcc SCM2=Vcc GS=0	SCM1=Vcc SCM2=Vcc GS=1
0	0	0	0	0	G1	G2	G1	G240	G1	G240
0	0	0	0	1	G17	G18	G17	G224	G9	G232
0	0	0	1	0	G33	G34	G33	G208	G17	G224
0	0	0	1	1	G49	G50	G49	G192	G25	G216
0	0	1	0	0	G65	G66	G65	G176	G33	G208
0	0	1	0	1	G81	G82	G81	G160	G41	G200
0	0	1	1	0	G97	G98	G97	G144	G49	G192
0	1	1	1	1	G113	G114	G113	G128	G57	G184
0	1	0	0	0	G129	G130	G129	G112	G65	G176
0	1	0	0	1	G145	G146	G145	G96	G73	G168
0	1	0	1	0	G161	G162	G161	G80	G81	G160
0	1	0	1	1	G177	G178	G177	G64	G89	G152
0	1	1	0	0	G193	G194	G193	G48	G97	G144
0	1	1	0	1	G209	G210	G209	G32	G105	G136
0	1	1	1	0	G225	G226	G225	G16	G113	G128
0	1	1	1	1	G240	G239	G2	G239	G121	G120
1	0	0	0	0	G224	G223	G18	G223	G129	G112
1	0	0	0	1	G208	G207	G34	G207	G137	G104
1	0	0	1	0	G192	G191	G50	G191	G145	G96
1	0	0	1	1	G176	G175	G66	G175	G153	G88
1	0	1	0	0	G160	G159	G82	G159	G161	G80
1	0	1	0	1	G144	G143	G98	G143	G169	G72
1	0	1	1	0	G128	G127	G114	G127	G177	G64
1	0	1	1	1	G112	G111	G130	G111	G185	G56
1	1	0	0	0	G96	G95	G146	G95	G193	G48
1	1	0	0	1	G80	G79	G162	G79	G201	G40
1	1	0	1	0	G64	G63	G178	G63	G209	G32
1	1	0	1	1	G48	G47	G194	G47	G217	G24
1	1	1	0	0	G32	G31	G210	G31	G225	G16

Table 11 Correspondence between NL4-0 and the Number of Valid Lines

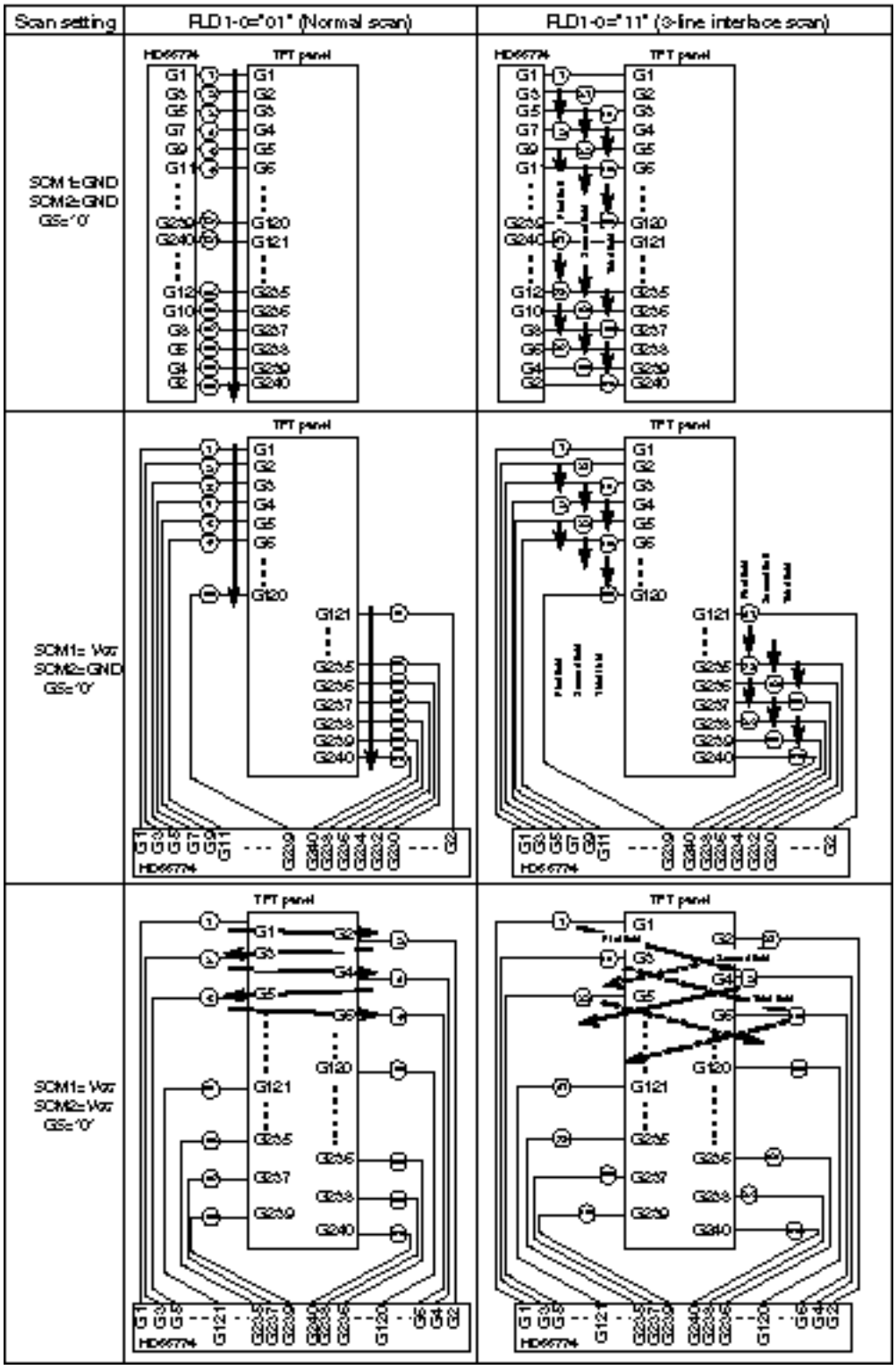
NL4	NL3	NL2	NL1	NL0	Number of Valid Lines
0	0	0	0	0	Setting inhibited
0	0	0	0	1	16
0	0	0	1	0	24
0	0	0	1	1	32
0	0	1	0	0	40
0	0	1	0	1	48
0	0	1	1	0	56
0	0	1	1	1	64
0	1	0	0	0	72
0	1	0	0	1	80
0	1	0	1	0	88
0	1	0	1	1	96
0	1	1	0	0	104
0	1	1	0	1	112
0	1	1	1	0	120
0	1	1	1	1	128
1	0	0	0	0	136
1	0	0	0	1	144
1	0	0	1	0	152
1	0	0	1	1	160
1	0	1	0	0	168
1	0	1	0	1	176
1	0	1	1	0	184
1	0	1	1	1	192
1	1	0	0	0	200
1	1	0	0	1	208
1	1	0	1	0	216
1	1	0	1	1	224
1	1	1	0	0	232
1	1	1	0	1	240

FLD1-0: Set the number of valid lines to drive n-line interlacing. Table 13 shows the correspondence between the setting value and the number of fields. Table 14 shows the scan method. The numbers in circles indicate the scanning order.

Table 12 Correspondence between FLD1-0 and N-Line Interlacing Scan

FLD1	FLD0	Scan Method
0	0	Setting inhibited
0	1	One field
1	0	Setting inhibited
1	1	Three fields

Table 13 N-Line Interlacing Scan Method

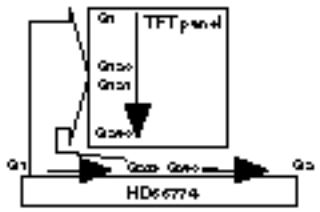
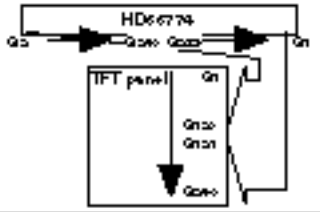
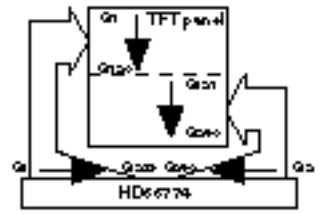
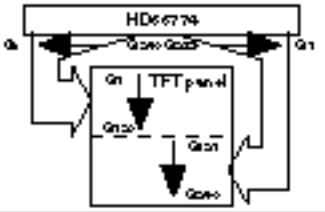
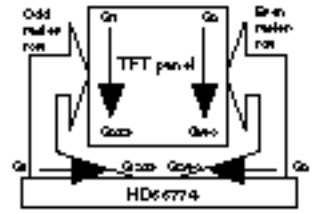
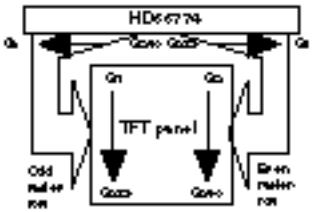


Note: The numbers in circles indicate the scanning order.

Scan Mode Setting

Shift direction of the gate signal can be changed by setting the input levels of the SMC1 and 2 pins and the GS bit setting, which enables various types of connections between the liquid crystal display panel and the HD66774.

Table 14 Scan Mode Setting

SCM1	SCM2	GS	Mounting example and scan direction	
GND	GND	0		G1→G3→ · · · → G237→G239→ G240→G238 → · · · →G4→G2
GND	GND	1		G2→G4→ · · · → G238→G240→ G239→G237 → · · · →G3→G1
VCC	GND	0		G1→G3→ · · · → G237→G239→ G2→G4→ · · · → G238→G240
VCC	GND	1		G240→G238 → · · · → G4→G2→ G239→G237 → · · · → G3→G1
VCC	VCC	0		G1→G2→G3→ G4→ · · · →G237→ G238→G239→G240
VCC	VCC	1		G240→G239→G238 →G237→ · · · →G4 →G3→G2→G1

Note: The SCM1 and 2 are set by pins and the GS is set by instructions.

Gate Serial Transfer

The register settings are transferred from HD66770 or HD66772 source driver. The interface consists of a chip select (GCS*), a transfer clock (GCL), and data input (GDA) lines.

The data transfer starts when the falling edge of the GCS* line indicates that the data is to be transferred. The transfer ends when the rising edge of the GCS* line indicates that the transfer is over. The bits are transferred in 16-bit units, and the data is transferred in the order from MSB to LSB.

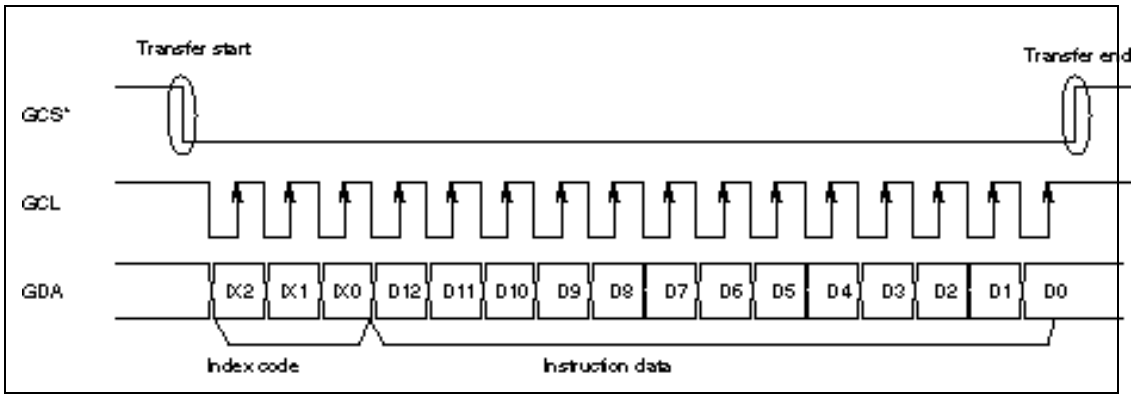


Figure 7 Format for Data Transfer

Reset Functions

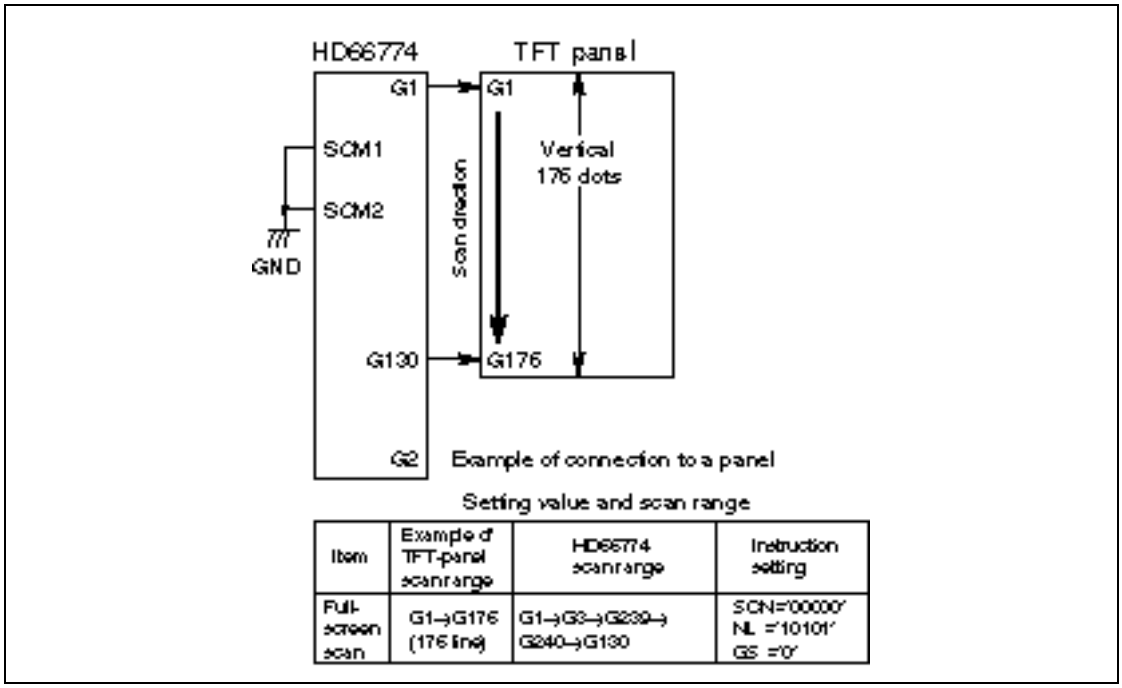
HD66774 sets the internal initialization with the RESET pin. Input a power-on reset signal when the power is applied as in the case with HD66770 or HD66772. Table 15 shows the initial setting values.

Table 15 Initial Setting Values for Registers at Reset

Index Code	Control Bit	Initial Value	Status
R00h	SLP	0	Cancels sleep mode.
	AP2-0	000	Stops operational amplifier and step-up circuit operations.
	DC2-0	000	Step-up cycle: Equal to DCCLK
	GON	0	Vcom and Vgoff output control for display off: GND
	BT2-0	000	Step-up factor VLOUT2 = Vci x five times
	VCOMG	0	Vcom output control for display on: GND
R01h	VC2-0	000	Internal reference voltage of VREG1OUT/Vciout: 0.92 Vcc Internal reference voltage of VREG2OUT: 0.08 Vcc
	PON	0	Stops operations in the step-up circuit 3.
	VRH3-0	0000	VREG1OUT output voltage: REGP x 1.45 times
	VRL3-0	0000	VREG2OUT output voltage: -(Vci - REGN) x 3.0 times
	CAD	0	Structure for TFT-display retention volume: Cst
R02h	VCM4-0	00000	VcomH output voltage: VREG1 x 0.4 times
	VDV4-0	00000	Vcom amplitude: VREG1 x 0.6 times
R06h	SCN4-0	00000	Output start position: G1
	NL4-0	11101	Number of valid lines: 240
	GS	0	Scan direction control: G1-G240
R07h	FLD1-0	01	N-line interlacing control: normal scan

Interface between the Liquid Crystal Display Panel

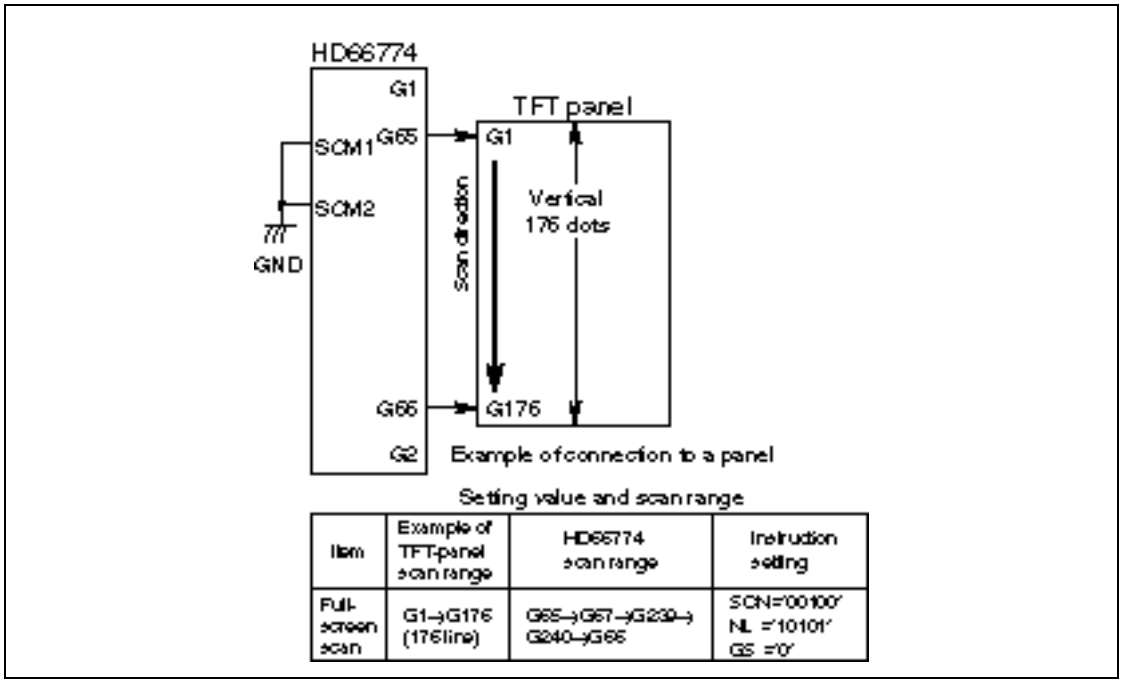
Figures 8 to 13 show the connection example for the configuration of the 176-dot-row TFT-LCD panel using the HD66774, and SCN, NL, and GS bit settings and the scanning range of gate lines.



Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G1→G2→G239→ G240→G130	SCN="00000" NL ="10101" GS ="0"

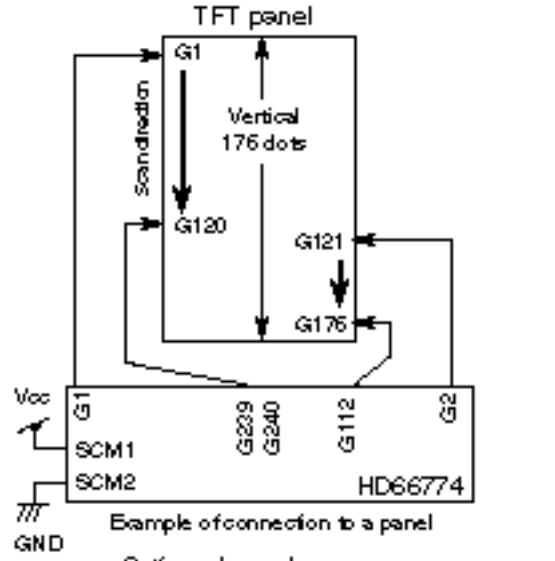
Figure 8 Connection Example (1)



Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G65→G67→G239→ G240→G65	SCN="00100" NL ="10101" GS ="0"

Figure 9 Connection Example (2)

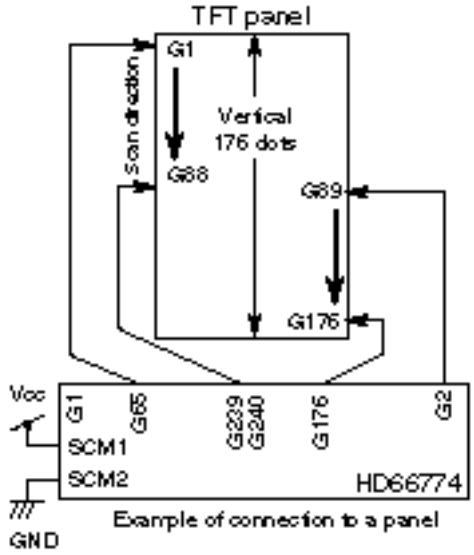


Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G1→G3→G239→ G2→G112	SCN='00000' NL = '10101' GS = '0'

Figure 10 Connection Example (3)

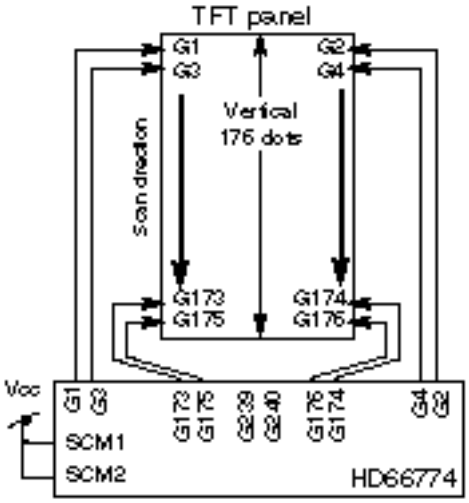


Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G65→G239 G2→G176	SCN='01000' NL ='10101' GS ='0'

Figure 11 Connection Example (4)

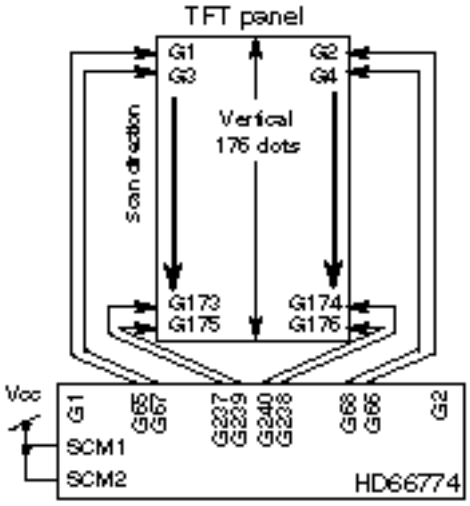


Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G1→G2→G3→G4 →・・・→G173 G174→G175→G176	SCN='00000' NL ='10101' GS ='0'

Figure 12 Connection Example (5)



Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66774 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G65→G66→G67→G68 → · · · →G237→ G238→G239→G240	SCN='01000' NL ='10101' GS ='0'

Figure 13 Connection Example (6)

Flow of Power-Supply Setting

Apply the power in a sequence as shown in figure 14.

The stable times of the oscillation circuit, step-up circuit, and operational amplifier depend on the external resistor or capacitance.

After the serial signal transfer has started by TE and IDX2-0 in HD66770 or HD66772, the mode settings of HD66774 become valid with a delay of CL1 = 1 cyc. Take this fact into account when setting the modes.

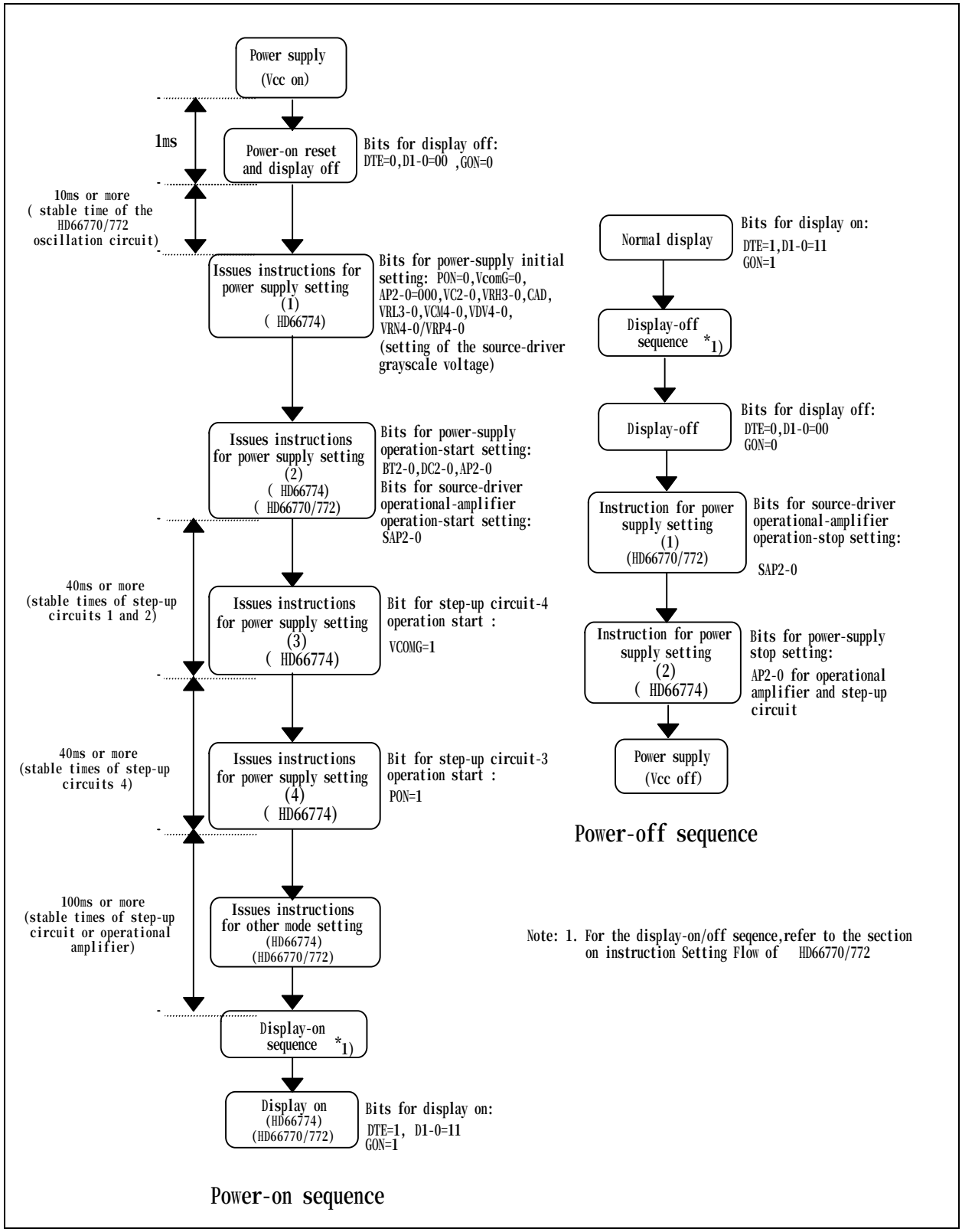


Figure 14 Flow of Power-Supply Setting

Configuration of Internal Power-Supply Generation Circuit

Figure 15 shows a configuration of the voltage generation circuit of HD66774. The step-up circuits consist of step-up circuits 1 to 4. Step-up circuit 1 doubles or triples the voltage supplied to Vci1, and that voltage is doubled, tripled, or quadrupled in step-up circuit 2. Step-up circuit 3 reverses the VGH level with reference to GND and generates the VGL level. Step-up circuit 4 reverses the Vci level with reference to GND and generates the VCL level. These step-up circuits generate power supplies required for TFT-LCD driving. Reference voltages VDH, Vcom, and Vgoff for the HD66770 or HD66772 grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit, REGP or REGN voltage, and generate each level depending on that voltage. The Vcom and Vgoff voltages can be alternated with any voltages. Connect DDVDH and VDH to HD66770 or HD66772, and Vcom to the panel and HD66770 or HD66772.

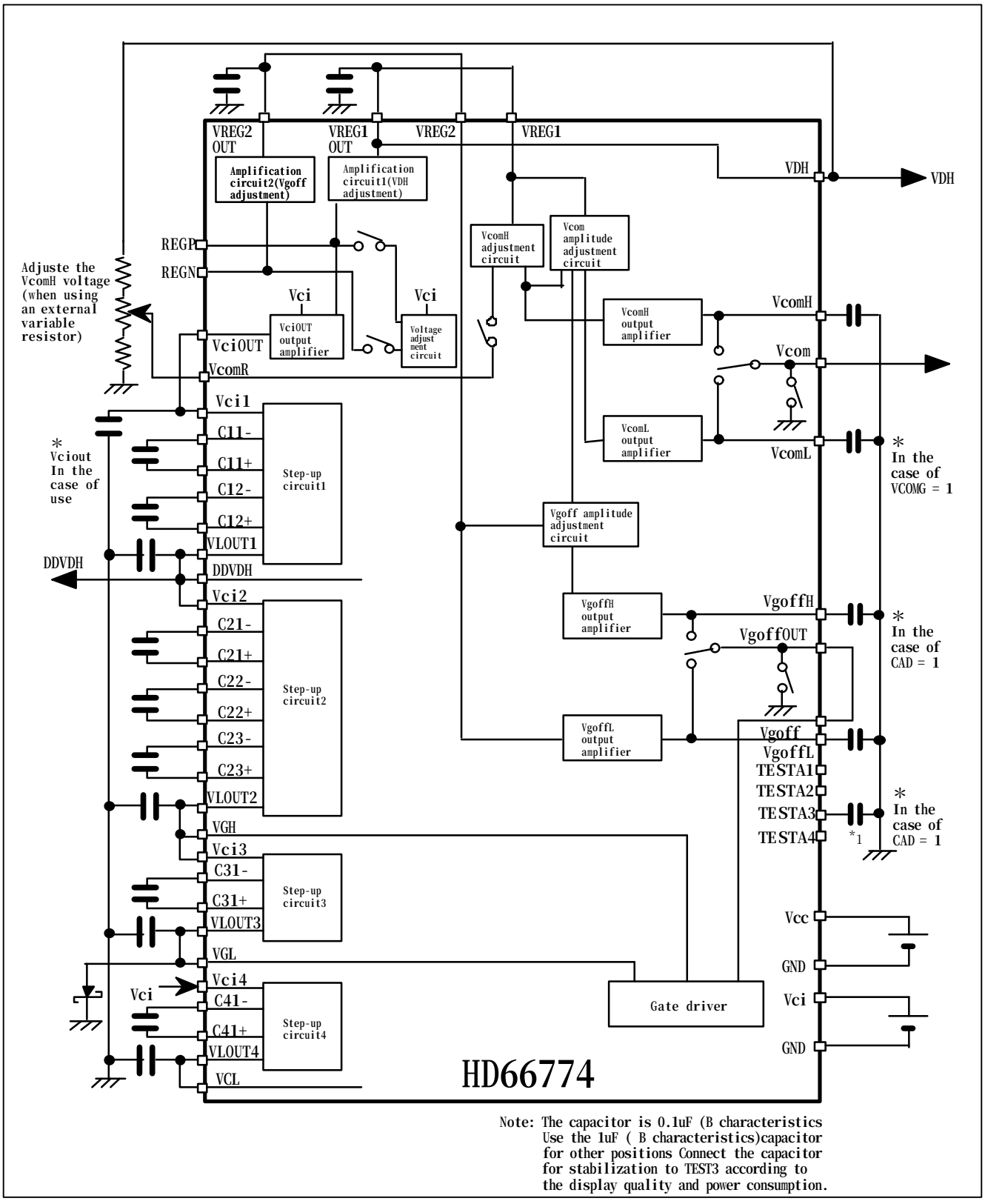


Figure 15 Configuration of the Internal Power-Supply Circuit

Pattern Diagrams for Voltage Setting

Figure 16 shows a pattern diagram for the HD66774 voltage setting and an example of waveforms when HD66774 is combined with HD66770 or HD66772.

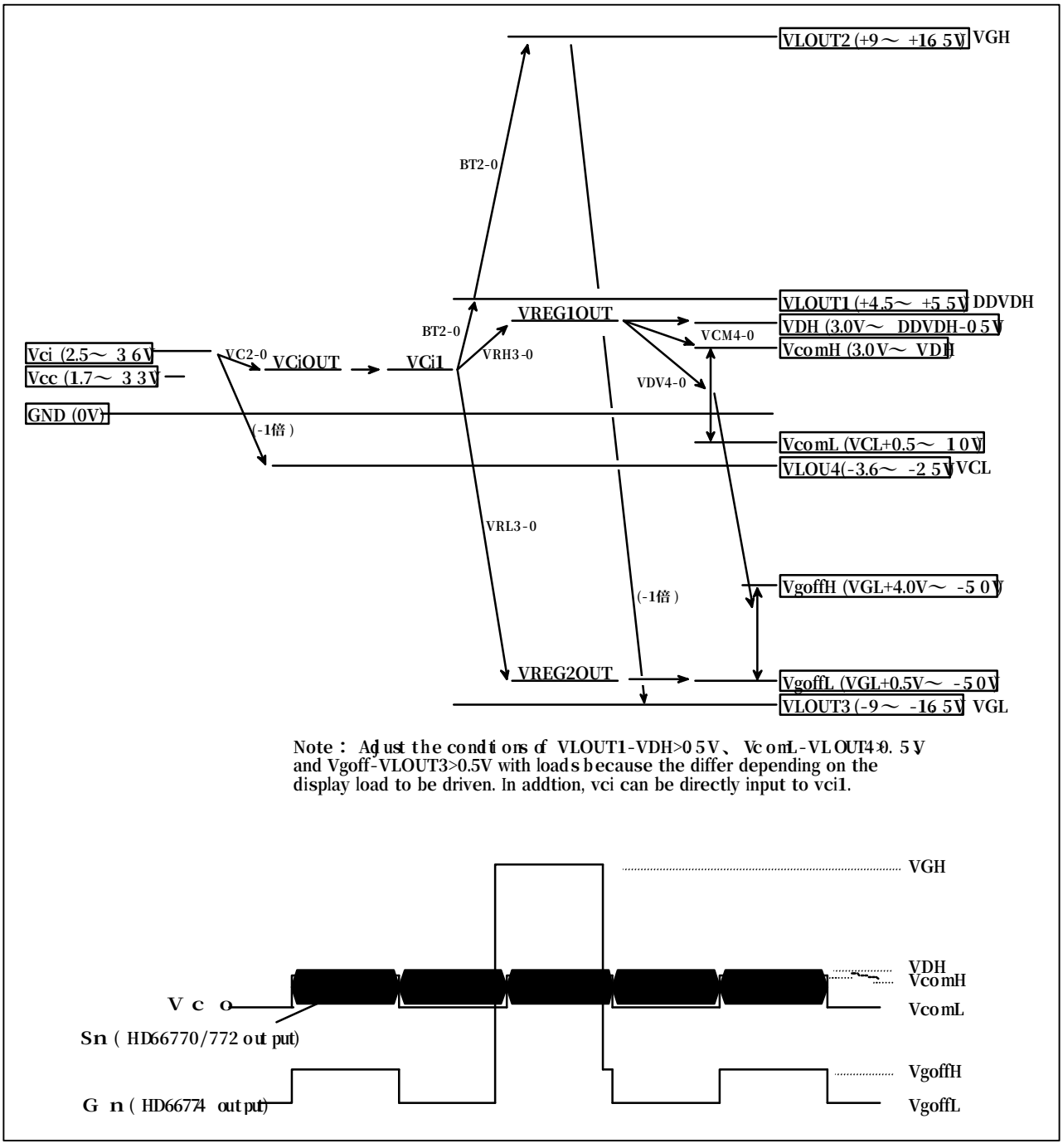


Figure 16 Pattern Diagram and an Example of Waveforms

Example of System Configuration

Figure 17 shows a TFT-LCD panel with 132 (horizontal)-by-176 (vertical) dots, configured by using the HD66770 source driver.

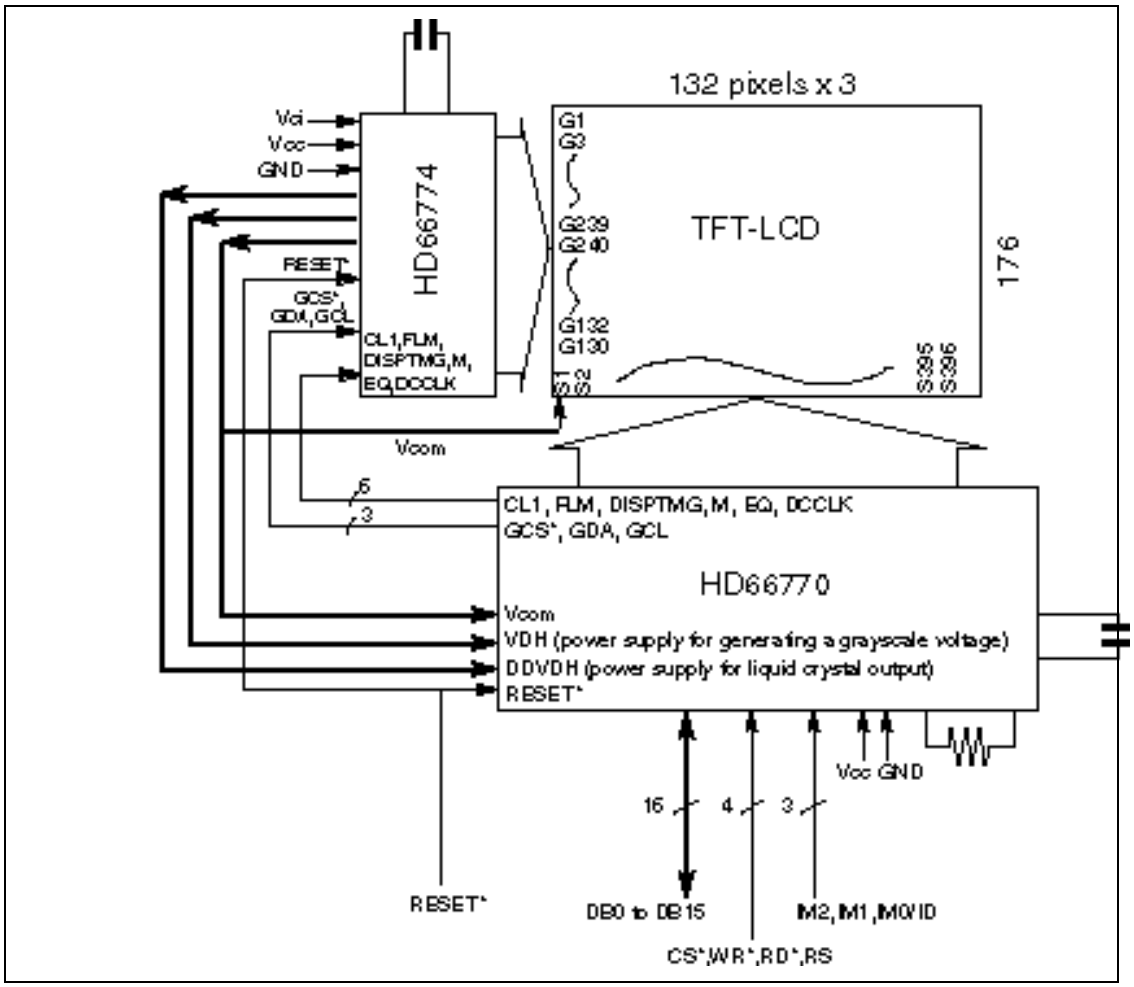
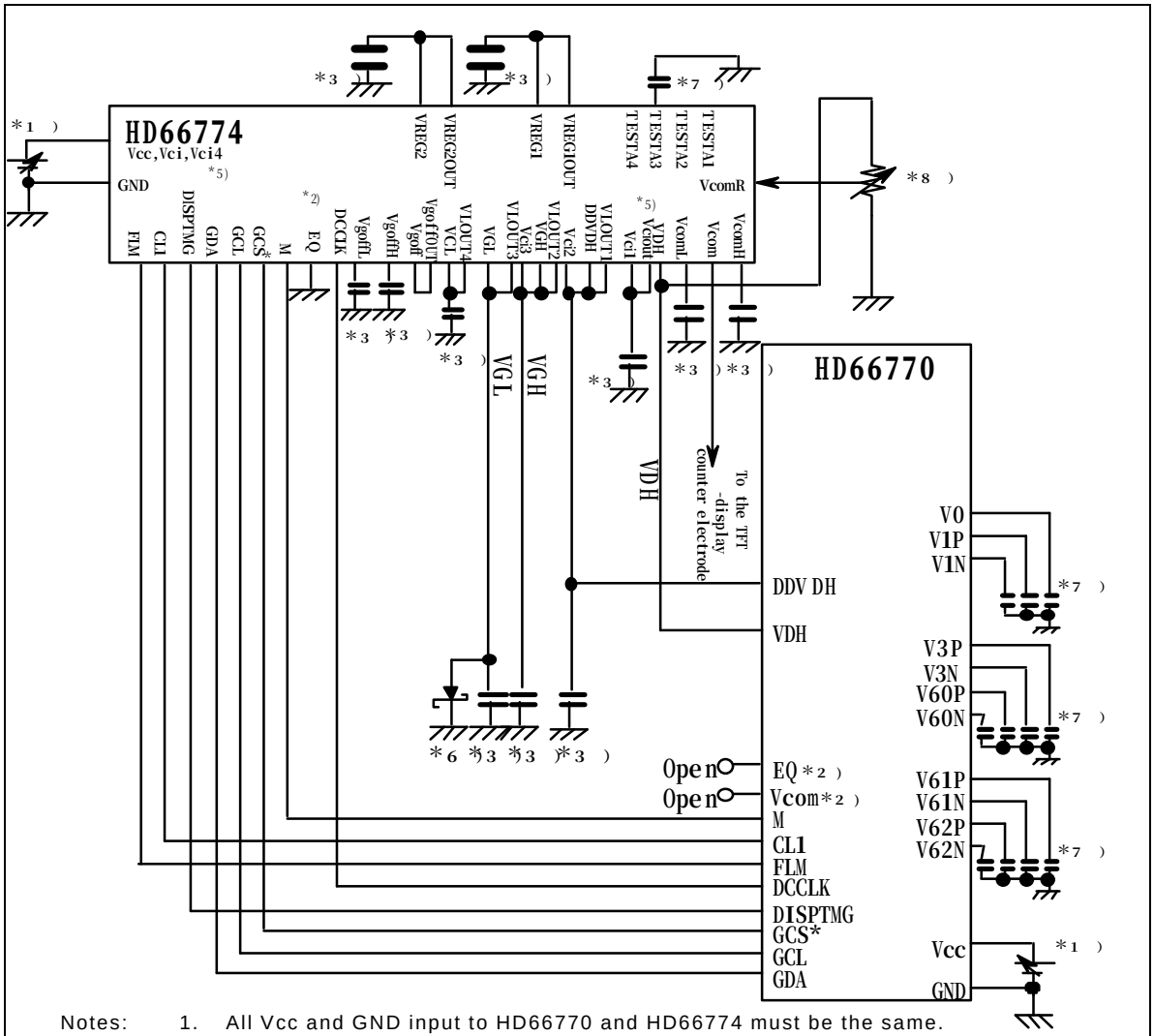


Figure 17 System Configuration

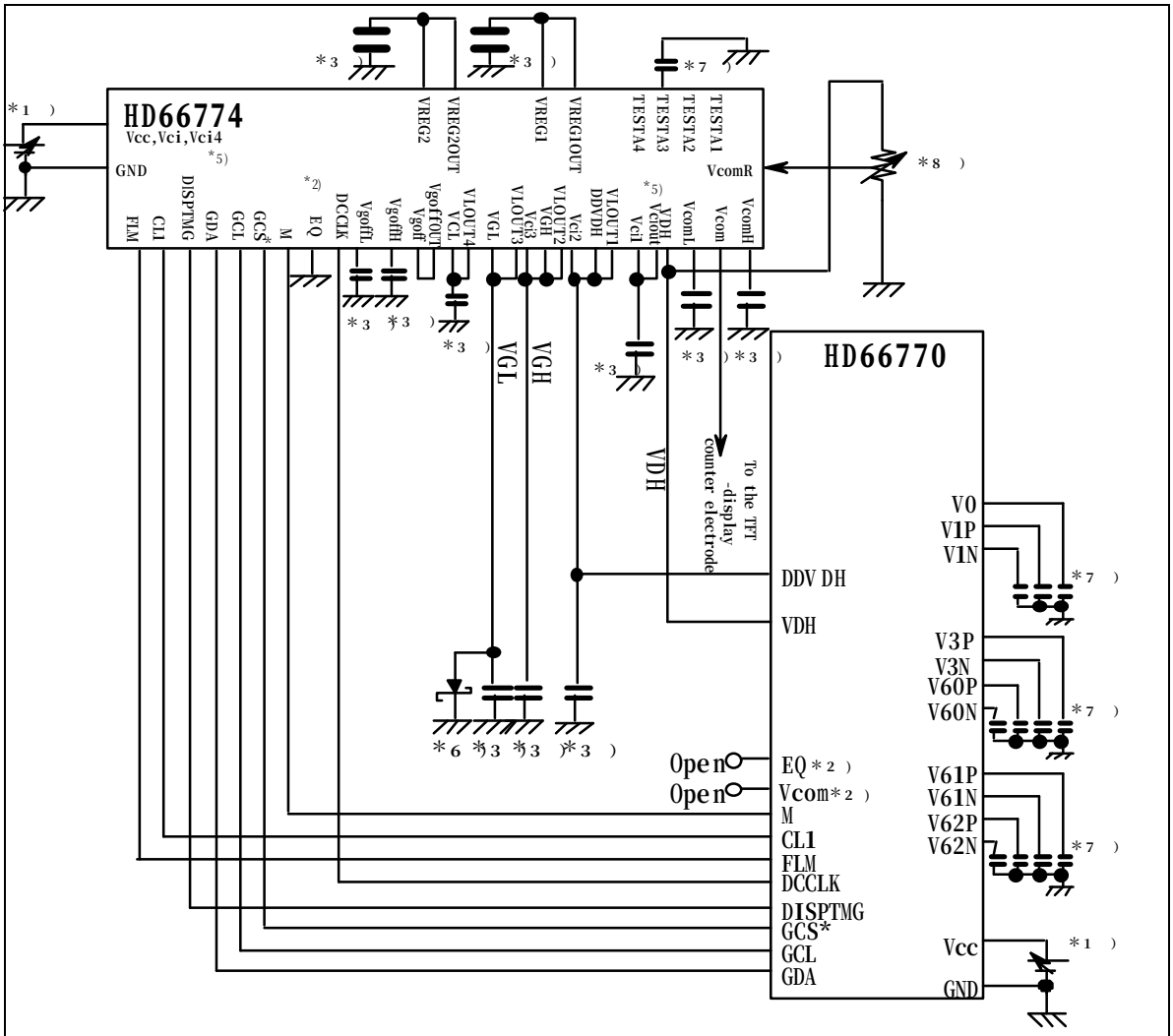
Example of Connection to HD66770

Connection differs according to the voltage setting of Vcom. Figure 18 shows an example of connection to HD66770 when VcomL < 0 V and 0 V ≤ VcomL < 5.5 V.



Notes:
1. All Vcc and GND input to HD66770 and HD66774 must be the same.
2. Leave the EQ and Vcom pins of HD66770 open. Set the EQ pin of HD66774 to GND.
3. Use the 1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD66774. Connect these capacitors according to the HD66774 pin functions.
5. Apply 2.5 to 3.6 V to Vci by using an external power supply, and connect VciOUT to Vci1 or apply 2.75 V or lower to Vci1 by using an external power supply. Apply 2.5 to 3.6 V or lower to Vci4 by using an external power supply.
6. Conncet the Shottky barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Use 200-kΩ or higher variable resistor.

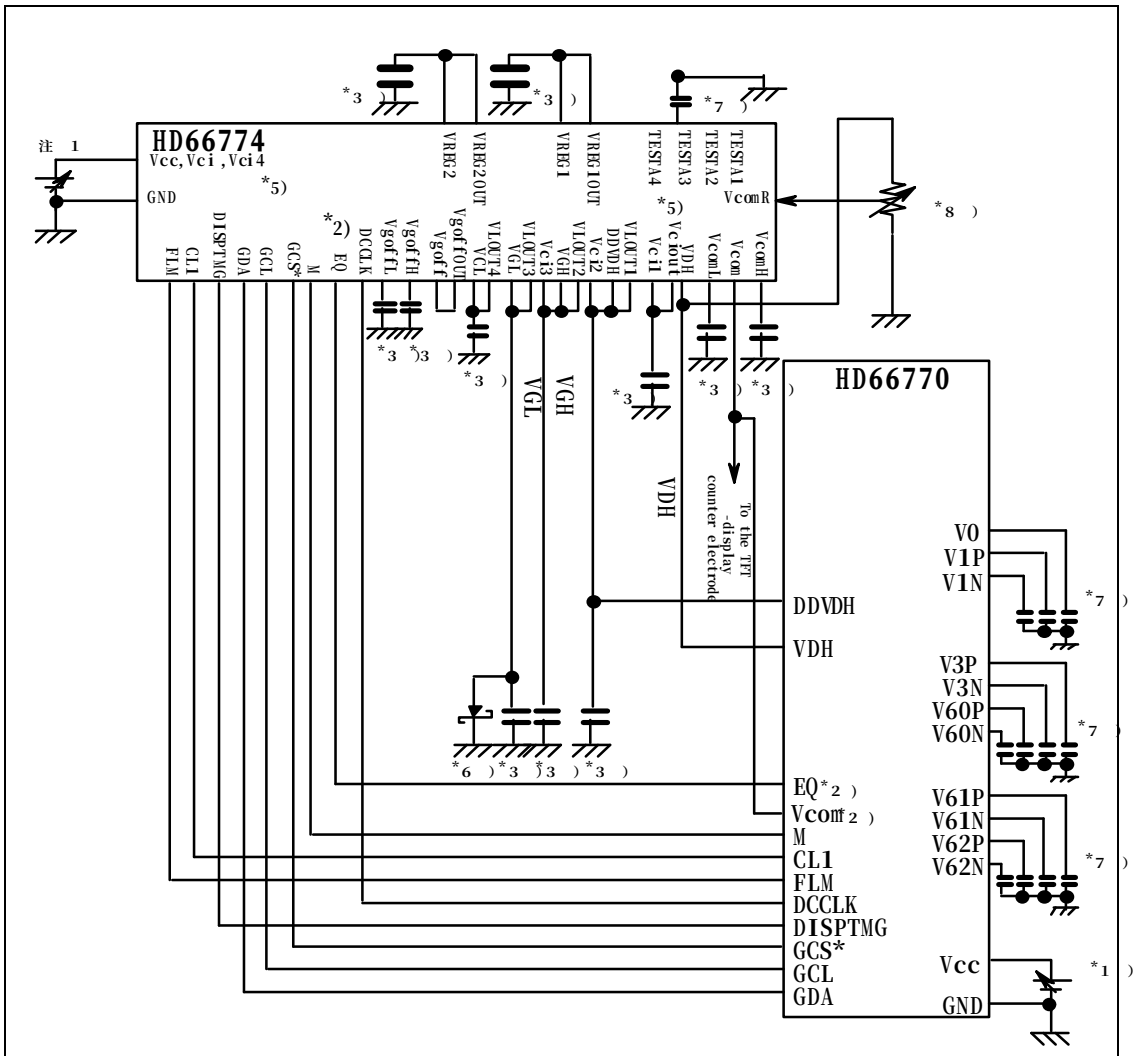
Figure 18 Example of Connection to HD66770 when VcomL < 0 V



Notes:
1. All Vcc and GND input to HD66770 and HD66774 must be the same.
2. Leave the EQ and Vcom pins of HD66770 open. Set the EQ pin of HD66774 to GND.
3. Use the 1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD66774. Connect these capacitors according to the HD66774 pin functions.
5. Apply 2.5 to 3.6 V to Vci by using an external power supply, and connect VciOUT to Vci1 or apply 2.75 V or lower to Vci1 by using an external power supply. Apply 2.5 to 3.6 V or lower to Vci4 by using an external power supply.
6. Conncet the Shottky barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Use 200-kΩ or higher variable resistor.

Figure 18 Example of Connection to HD66770 when VcomL < 0 V

Figure 19 shows an example of connection to HD66770 source driver when 0 ≤ VcomL < 5.5 V.



Notes:

1. All Vcc and GND input to HD66770 and HD66774 must be the same.
2. Connect the EQ pins of HD66770 and HD66774. The Vcom pin must be connected to the Vcom pin of HD66774. Do not set the Vcom voltage higher than 5.5 V.
3. Use the 1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD66774. Connect these capacitors according to the HD66774 pin functions.
5. Apply 2.5 to 3.6 V to Vci by using an external power supply, and connect VciOUT to Vci1 or apply 2.75 V or lower to Vci1 by using an external power supply. Apply 2.5 to 3.6 V to Vci4 by using an external power supply.
6. Conncet the Shottky barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-μF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Use 200-kΩ or higher variable resistor.

Figure 19 Example of Connection to HD66770 when 0 V £ VcomL < 5.5 V

Specifications for the Capacitor Connected to HD66774

Table 16 shows the specifications for the capacitor connected to HD66774.

Table 16 Specifications for the Capacitor Connected to HD66774

Product	Capacitor	Recommended Breakdown Voltage	Connected Pin (19 in Total)
HD66774	1 μF (B characteristics)	6 V	VREG1OUT, Vciout*4, C41-/+, VLOUT4, VcomH, VcomL*3
		10 V	VLOUT1, C11-/+, C12-/+, C21-/+, C22-/+, C23-/+
		25 V	VREG2OUT, VLOUT2, VLOUT3, C31-/+, VgoffH*2, VgoffL
	0.1 μF (B characteristics)	25 V	TESTA3*2

Notes: 1. The step-up circuit capacitor C is required at different part according to the setting of step-up circuit magnification.
Refer to the instruction BT2-0.
2. Required when instruction CAD=1 (Cadd mode).
3. Required when instruction VCOMG=1.
4. Required when instruction VC2-0= “0**” (Vciout used for output).

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	Vcc	-0.3 to +7.0	V	1
	LCD drive circuit	Vci - GND	-0.3 to +7.0	V	1
		DDVDH - GND	-0.3 to +7.0	V	1
		GND - VCL	-0.3 to +4.6	V	1
		DDVDH - VCL	-0.3 to +10.0	V	
		VGH - GND	-0.3 to +18.5	V	1
		GND - VGL	-0.3 to +18.5	V	1
Input voltage		VT1	-0.3 to Vcc + 0.3	V	1, 2
Operating temperature		topr	-40 to +85	°C	
Storage temperature		Tstg	-55 to +110	°C	

Notes: 1. Voltage from GND.
2. Applies to the EQ, DCCLK, GCS*, GDA, GCL, M, DISPTMG, CL1, FLM, RESET*, SCM1, SCM2, OPOFF, DCTEST, and PONTEST pins.

Note: If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Electrical Characteristics

DC Characteristics (VCC = 1.7 to 3.6 V, GND = 0 V, VGH - VGL = 18 to 33 V, Ta = -40 to +85ºC)[*1]

Item	Symbol	Test Condition	min.	typ.	max.	Unit	Notes
Input high voltage	VIH		0.7 x Vcc	-	Vcc	V	2
Input low voltage	VIL		0	-	0.3 x Vcc	V	2
Driver on resistance	RONH	VGH – VGL = 33 V, Iload = ±100 μA	-	-	10	kΩ	3
Driver on resistance	RONL	VGH – VGL = 33 V, Iload = ±100 μA	-	-	10	kΩ	3
Input leakage current	IIL	Vin = 0 to VCC	-2.5	-	2.5	μA	2
Operating frequency	fopr		10	-	100	kHz	4
Current consumption 1	Icc	Vcc - GND = 3 V, fM = 12.3 kHz, fCL1 = 24.6 kHz			20	μA	5
Current consumption 2	Ici	Vcc - GND = 3 V, Vci - GND = 3 V, fM = 12.3 kHz, fCL1 = 24.6 kHz, fDCCLK = 24.6 kHz, VGH - VGL = 33 V			850	μA	5

Notes: 1. For electrical characteristics, guaranteed at 85ºC.

2. Applies to the EQ, DCCLK, GCS*, GDA, GCL, M, DISPTMG, CL1, FLM, RESET*, SCM1, SCM2, OPOFF, DCTEST, and PONTEST pins.

3. Resistance values between the G and V pins (VGH or Vgoff) when the load current flows one of G1 to G240 pins.
The following condition is specified. G1 to G240 pins that are not measured are left open.
VGH = +16.5 V, Vgoff = -16.5 V, Iload = ±100 μA

4. Applies to the CL1 pin.

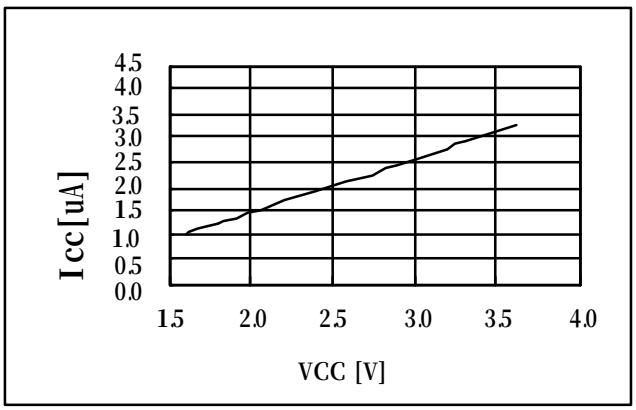
5. Values when no load current flows on the VDH, VGH, VGL, Vgoff, and Vcom pins, and when instruction settings are VC2-0 = 000 (Vci x 0.92), AP2-0 = 011 (amount of operational amplifier current), BT2-0 = 000 (step-up circuit 1: double, step-up circuit 2: triple), DC2-0 = 100 (step-up synchronization with step-up circuit 1: DCCLK, step-up synchronization with step-up circuits 2, 3, and 4: 8-divided DCCLK), VCOMG = 1, and CAD = 1.

AC Characteristics (VCC = 1.8 to 3.3 V, VGH - VGL = 18 to 33 V)

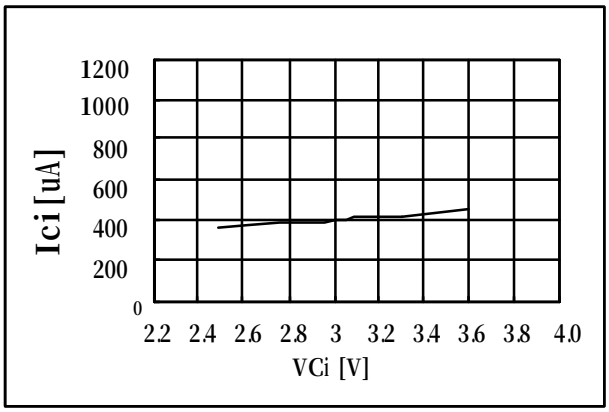
Item	Symbol	Pin	min.	typ.	max.	Unit	Notes
CL1 high-level width	tCWH	CL1	1.0	-	-	µs	
CL1 low-level width	tCWL	CL1	1.0	-	-	µs	
CL1 cycle time	tCYC	CL1	10	-	-	µs	
CL1/GCL rising time	tr	CL1	-	-	100	ns	
CL1/GCL falling time	tf	CL1	-	-	100	ns	
FLM setup time	tFS	FLM, CL1	1.0	-	-	µs	
FLM hold time	tFH	FLM, CL1	1.0	-	-	µs	
GCL cycle time	tcycG	GCL	2.5	-	-	µs	
GCL high-level width	tCWHG	GCL	1.0	-	-	µs	
GCL low-level width	tCWLG	GCL	1.0	-	-	µs	
GDA setup time	tGDS	GCL, GDA	1.0	-	-	µs	
GDA hold time	tGDH	GCL, GDA	1.0	-	-	µs	
GCS low setup time	tGSL	GCL, GCS*	1.0	-	-	µs	
GCS high hold time	tGHH	GCL, GCS*	1.0	-	-	µs	
Output delay time	tDD	CL1, G	-	-	1.0	µs	

Electrical Characteristics Notes

(ann.1) The connection of Operating voltage & Energy consumption will be written down below.



Condition of measurement :
VGH=16.5V,VGL=-16.5V
Vgoff=-16.5V,fM=100Hz
fDCCLK=25.6kHz,Cadd,
GON=1,Ta=25°C

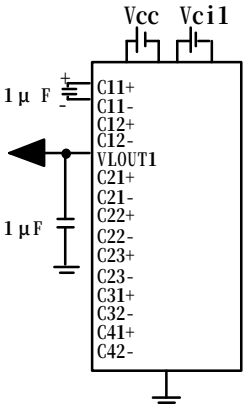


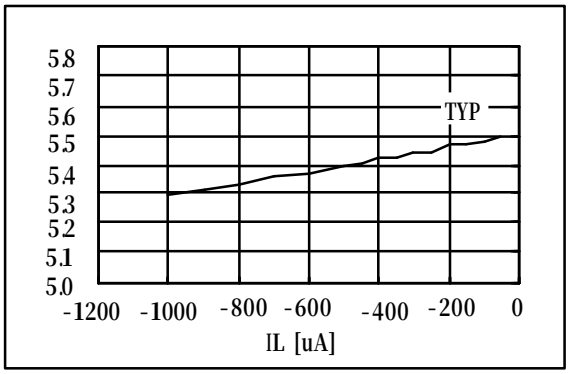
Condition of measurement :
VGH=16.5V,VGL=-16.5V
Vgoff=-16.5V,fM=100Hz
fDCCLK=25.6kHz,Cadd,
Booster scale(× 2, ×6
Booster (1devide,8devide)
Op-Amp DC current(mid),
GON=1,Ta=25°C

(ann.2) The connection of Voltage booster & Load current will be written down below.

Voltage booster circuit 1

circuit of measurement

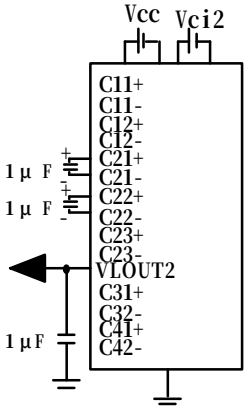


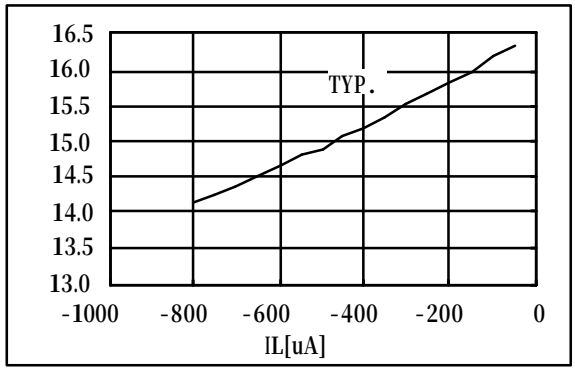


Condition of measurement ; DCDC1× double ,
DCCLK : 1devide, Vci1=2.75(V), Ta=25

Voltage booster circuit 2

Circuit of measurement

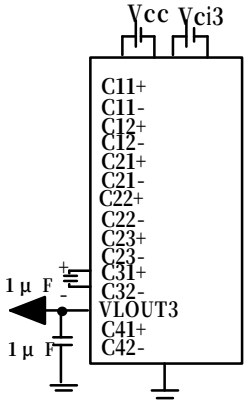


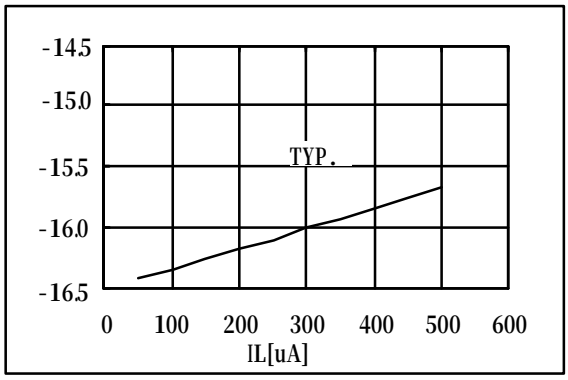


Condition of measurement; DCDC2× 3times,
DCCLK：8devide, Vci2=5.5(V), Ta=25

Voltage booster circuit 3

Circuit of mesurement

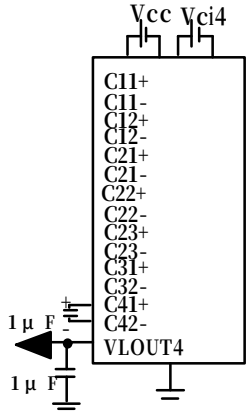


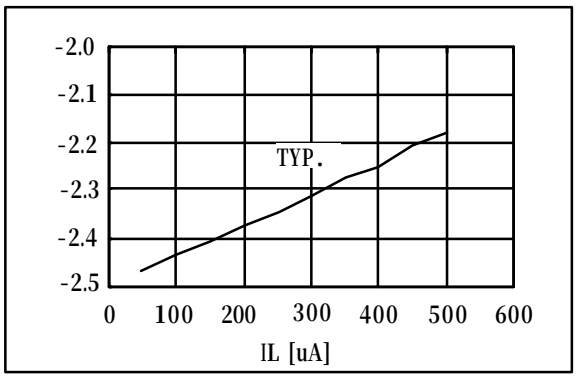


Condition of measurement； DCDC3 ×-1time
DCCLK：8devide, Vci3=5.5(V), Ta=25

Voltage booster circuit 4

Circuit of measurement

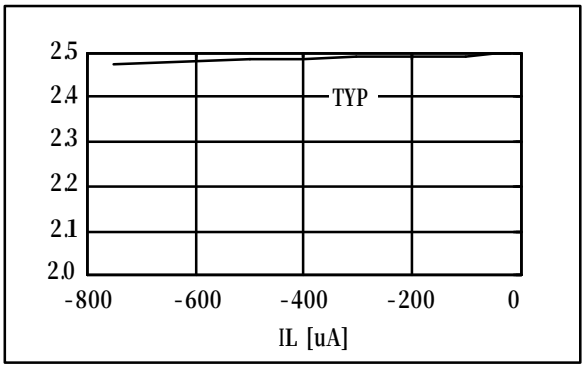




Condition of measurement ； DCDC4 ×-1time
DCCLK：8, Vci4=2.5(V), Ta=25

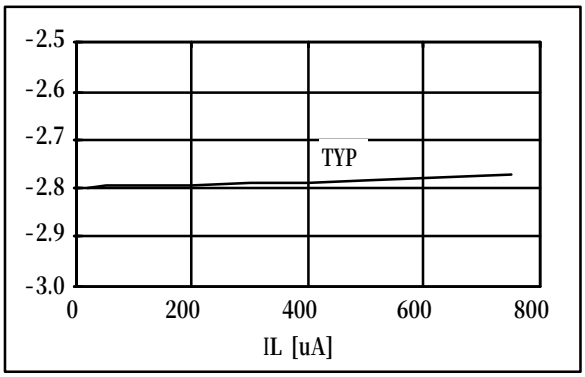
(ann. 3) The connection of Vcom & Load current will be written down below.

VCOMH(desired value = 2.5V)



Condition of measurement ; DDVDH=5.5V,
VCOMR=2.5V, Ta=25 °C

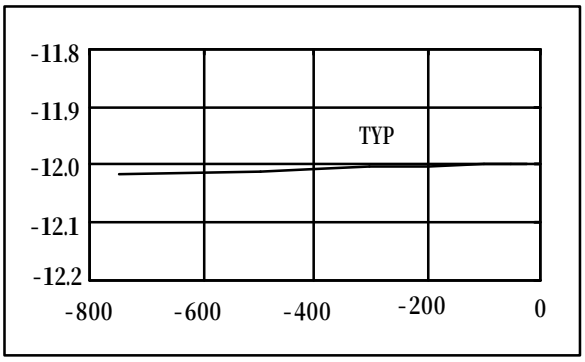
VCOML(desired va lue = -2.8V)



Condition of measurement ; DDVDH=5.5V
VCL=-3.3V, Ta=25 °C

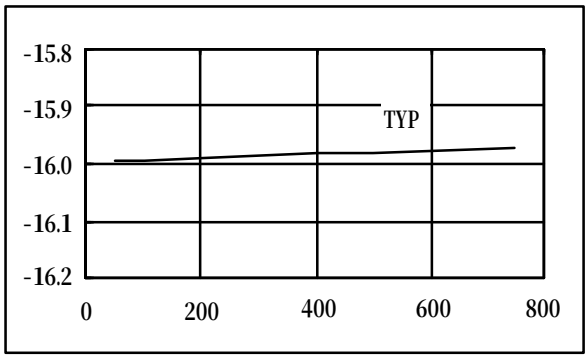
(ann.4) The connectoin of Vgoff & Load current will be written down below.

VGOFFH(desired value = -12.0V)



Condition of measurement;VGL=-16.5V,Ta=25°C

VGOFFL(desired value = -16.0V)



Condition of measurement ; VREG2=-16.0V
VGL=-16.5V,Ta=25°C

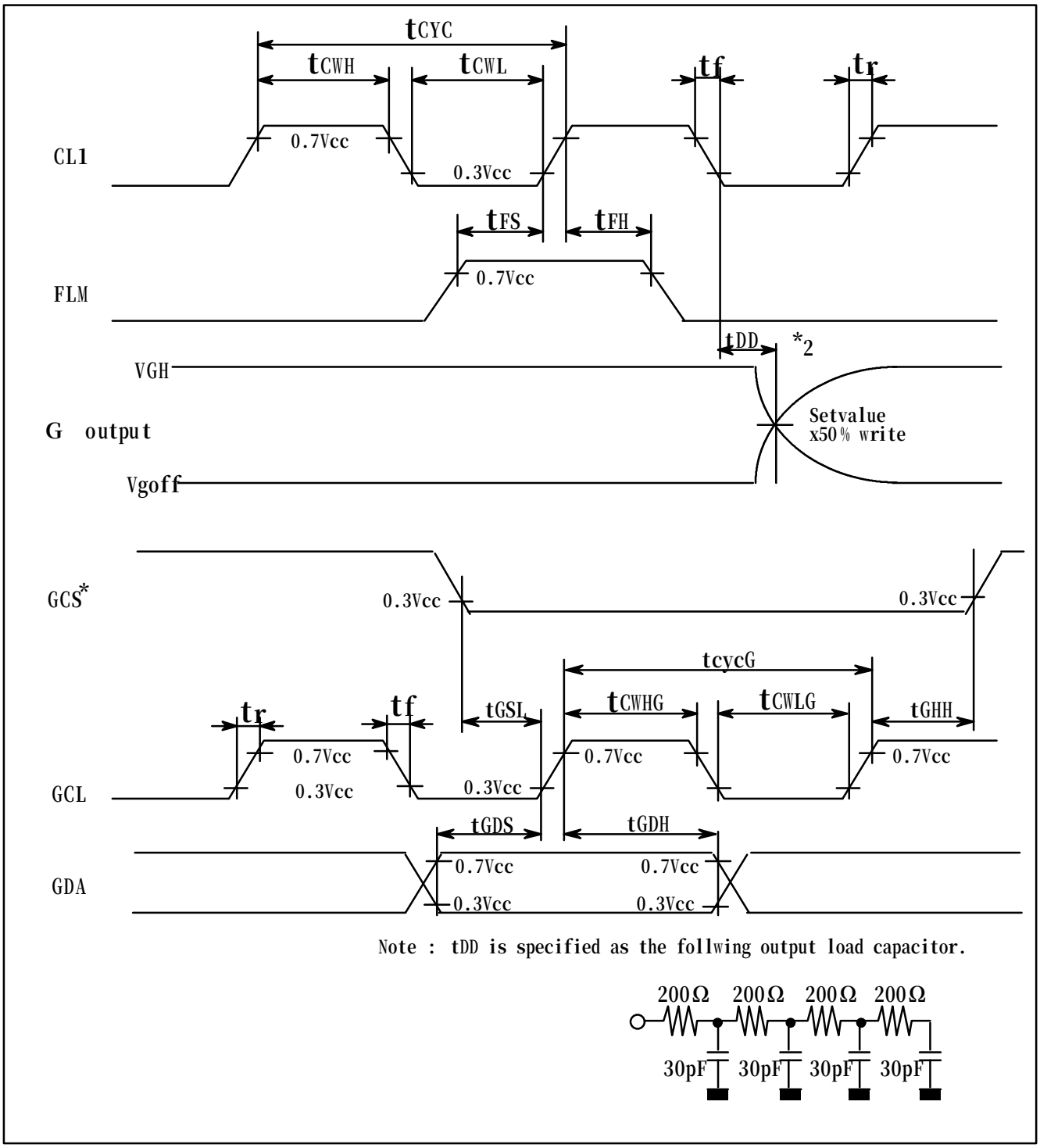


Figure 20 AC Timing

Modification history

Revision 1.0 (Jun. 27 .2002)

- First release