—PRELIMINARY—

HD66775

120-Channel Gate Driver for Color-TFT Liquid Crystal Displays

HITACHI

Rev.0.3
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Description

HD66775 is a gate-driver IC for systems with color-TFT-liquid-crystal dot-matrix graphic displays. It incorporates a circuit for driving 120 channels of TFT gate lines, and realizes the liquid crystal display.

When two HD66775s are used with the HD66770 396-channel source driver with on-chip RAM and the HD667P00 power-supply IC chip, and used with the HD66772 528-channel source driver with on-chip RAM and the HD667P00 power-supply IC chip, this LSI is suitable for color TFT displays of cellular phones having 132-by-176 and 176-by-240 dots, respectively.

Features

- TFT gate-line driving circuits
  - 120 outputs: can be expanded to 240 channels with the master/slave function (two HD66775s are used)
- Gate-line scanning
  - Centering-screen function (vertically separated, comb type)
- Mode setting
  - Serial transfer from the HD66770/772 source driver
- Power-supply voltage
  - Logic power supply: Vcc - GND = 1.8 to 3.3 V
  - Power supply for a gate-line driving circuit: VGH – VGL = 18 to 33 V (GND reference voltage: ±9 to ±16.5 V)
  - Power supply for driving a gate line: VGH – GND = 9 to 16.5 V, and Vgoff – GND = -5 to –16.5 V
- Power-supply circuit
  - Each power-supply voltage is supplied from the HD667P00 power-supply IC chip.

Hitachi semiconductor

Type Number

Type Number	External Appearance
HCD66775BP	Die with Au bump

Pin Functions

Table 1 Pin Functions

Signal Name[*1]	Quantity[*2]	Input/ Output	Connected to	Function
Vcc1/Vcc2	2	-	Power supply	VCC-GND: A logic-circuit power supply. Supply the same voltage as that for HD66770/772 and HD667P00.
GND1/GND2	2	-	Power supply	
VGH1/VGH2	2	-	HD667P00	A power supply for the gate-line driving circuit and a positive-side power supply for TFT-gate on level.
VGL1/VGL2	2	-	HD667P00	A power supply for the gate-line driving circuit and a negative-side power supply.
Vgoff1/Vgoff2	2	-	HD667P00	A power supply for driving the gate line at the TFT-gate off level.
RESET1*/ RESET2*	2	Input	External reset circuit	The reset pin. When a low level is input here, the LSI is initialized. Be sure to apply a signal to this pin during the system's power-on reset. RESET1* and RESET2* are equivalent inputs. Supply the reset signal to either, and leave the other open.
CL11/CL12	2	Input	CL1 of HD66770/772	Clock input pin supplied from HD66770/772. Gate line output changes at the falling edge of this signal.
FLM1/FLM2	2	Input	FLM of HD66770/772	Performs frame synchronization with the source driver.
GCL1/GCL2	2	Input	GCL of HD66770/772	Operates as a clock for the transfer of register settings. Latches data on the rising edge of the clock.
GDA1/GDA2	2	Input	GDA of HD66770/772	Operates as the data for the transfer of register settings.
GCS1*/GCS2*	2	Input	GCS* of HD66770/772	A chip-select signal. Low: selected (data-transfer enabled), high: not selected (data-transfer disabled)
DISPTMG1/ DISPTMG2	2	Input	DISPTMG of HD66770/772	Display-off signal. This signal becomes valid asynchronously with the FLM and CL1. High: Normal output; Low: All output Vgoff.
MS	1	Input	Vcc or GND	Input for selecting the master or slave. Must be fixed to Vcc for the input of the LSI that scans the first line.
SCM	1	Input	Vcc or GND	Input for selecting the scan mode. Must be fixed to Vcc or GND depending on the selected scan mode.
G1-G120	120	Output	Liquid crystal output	An output signal to the gate line. Outputs VGH as the gate-line selection level, or Vgoff as the gate-line non-selection level.

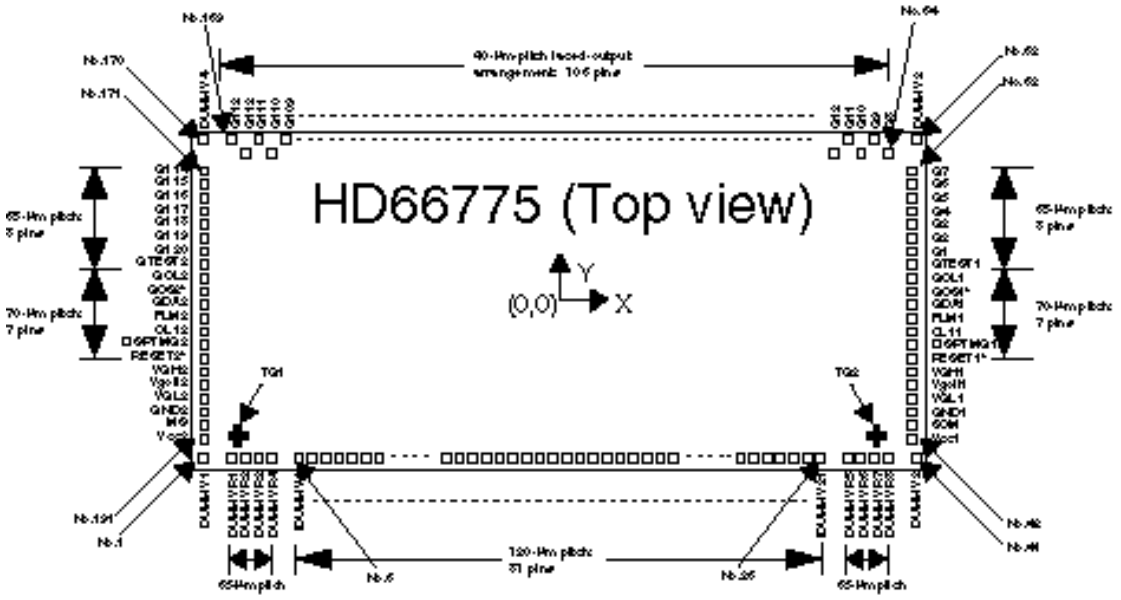
Table 1 Pin Functions (cont)

Signal Name[*1]	Quantity[*2]	Input/ Output	Connected to	Function
GTEST1, GTEST2	2	Output	Liquid crystal output or open	Dummy gate output. When CAD bit is high, output VGH and Vgoff level. When CAD bit is low, output Vgoff level. When these pins are not used, leave them open.

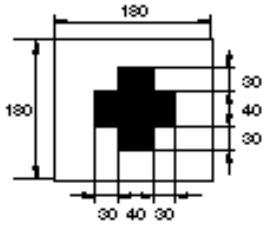
Notes: 1. Signal names 1/2 are equivalent inputs. Supply the reset signal to either, and leave the other open.

2. The quantity does not match the number of pads.

HCD66775BP Pad Arrangement



- Chip size: 4.70 x 3.00 mm
- Chip thickness: 550 µm (typ.)
- Pad coordinates: pad centers
- Coordinate origin: chip center
- Au bump size:
  (1) 35 µm x 90 µm : RESET1*, RESET2*, DISPTMG1, DISPTMG2, CL11, CL12, FLM1, FLM2, GDA1, GDA2, GCS1*, GCS2*, GCL1, GCL2, MS, SCM
  (2) 30 µm x 100 µm : iDUMMY1-iDUMMY31
  (3) 30 µm x 95 µm : GTEST1, GTEST2, G1-G120, DUMMYR1-DUMMYR8
  (4) 65 µm x 95 µm : Vcc1, Vcc2, GND1, GND2, VGL1, VGL2, Vgoff1, Vgoff2, VGH1, VGH2
  (5) 70 µm x 70 µm : DUMMY1-DUMMY4
- Au bump pitch: see the pad coordinates
- Height of the Au bump: 15 µm (typ.)
- The target (TG1 or TG2) pattern for the chip alignment is AL without the Au bump.
- The sizes are shown below. The origin is centered.



- DUMMYR1, DUMMYR3, and DUMMYR4 are connected within the chip.
- DUMMYR5, DUMMYR7, and DUMMYR8 are connected within the chip.

HCD66775BP Pad Coordinates

The pad coordinates are shown below. The pad numbers in the pad arrangement correspond to the numbers in the following table that lists the pad center coordinates with the chip-centered origin.

No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)	No.	Pin Name	X (um)	Y (um)
1	DUMMY1	-2215	-1370	61	G6	2202.5	951	121	G65	-180	1357.5
2	DUMMYR1	-2080	-1357.5	62	G7	2202.5	1016	122	G66	-220	1227.5
3	DUMMYR2	-2015	-1357.5	63	DUMMY3	2215	1370	123	G67	-260	1357.5
4	DUMMYR3	-1950	-1357.5	64	G8	2100	1227.5	124	G68	-300	1227.5
5	DUMMYR4	-1885	-1357.5	65	G9	2060	1357.5	125	G69	-340	1357.5
6	iDUMMY1	-1800	-1355	66	G10	2020	1227.5	126	G70	-380	1227.5
7	iDUMMY2	-1680	-1355	67	G11	1980	1357.5	127	G71	-420	1357.5
8	iDUMMY3	-1560	-1355	68	G12	1940	1227.5	128	G72	-460	1227.5
9	iDUMMY4	-1440	-1355	69	G13	1900	1357.5	129	G73	-500	1357.5
10	iDUMMY5	-1320	-1355	70	G14	1860	1227.5	130	G74	-540	1227.5
11	iDUMMY6	-1200	-1355	71	G15	1820	1357.5	131	G75	-580	1357.5
12	iDUMMY7	-1080	-1355	72	G16	1780	1227.5	132	G76	-620	1227.5
13	iDUMMY8	-960	-1355	73	G17	1740	1357.5	133	G77	-660	1357.5
14	iDUMMY9	-840	-1355	74	G18	1700	1227.5	134	G78	-700	1227.5
15	iDUMMY10	-720	-1355	75	G19	1660	1357.5	135	G79	-740	1357.5
16	iDUMMY11	-600	-1355	76	G20	1620	1227.5	136	G80	-780	1227.5
17	iDUMMY12	-480	-1355	77	G21	1580	1357.5	137	G81	-820	1357.5
18	iDUMMY13	-360	-1355	78	G22	1540	1227.5	138	G82	-860	1227.5
19	iDUMMY14	-240	-1355	79	G23	1500	1357.5	139	G83	-900	1357.5
20	iDUMMY15	-120	-1355	80	G24	1460	1227.5	140	G84	-940	1227.5
21	iDUMMY16	0	-1355	81	G25	1420	1357.5	141	G85	-980	1357.5
22	iDUMMY17	120	-1355	82	G26	1380	1227.5	142	G86	-1020	1227.5
23	iDUMMY18	240	-1355	83	G27	1340	1357.5	143	G87	-1060	1357.5
24	iDUMMY19	360	-1355	84	G28	1300	1227.5	144	G88	-1100	1227.5
25	iDUMMY20	480	-1355	85	G29	1260	1357.5	145	G89	-1140	1357.5
26	iDUMMY21	600	-1355	86	G30	1220	1227.5	146	G90	-1180	1227.5
27	iDUMMY22	720	-1355	87	G31	1180	1357.5	147	G91	-1220	1357.5
28	iDUMMY23	840	-1355	88	G32	1140	1227.5	148	G92	-1260	1227.5
29	iDUMMY24	960	-1355	89	G33	1100	1357.5	149	G93	-1300	1357.5
30	iDUMMY25	1080	-1355	90	G34	1060	1227.5	150	G94	-1340	1227.5
31	iDUMMY26	1200	-1355	91	G35	1020	1357.5	151	G95	-1380	1357.5
32	iDUMMY27	1320	-1355	92	G36	980	1227.5	152	G96	-1420	1227.5
33	iDUMMY28	1440	-1355	93	G37	940	1357.5	153	G97	-1460	1357.5
34	iDUMMY29	1560	-1355	94	G38	900	1227.5	154	G98	-1500	1227.5
35	iDUMMY30	1680	-1355	95	G39	860	1357.5	155	G99	-1540	1357.5
36	iDUMMY31	1800	-1355	96	G40	820	1227.5	156	G100	-1580	1227.5
37	DUMMYR5	1885	-1357.5	97	G41	780	1357.5	157	G101	-1620	1357.5
38	DUMMYR6	1950	-1357.5	98	G42	740	1227.5	158	G102	-1660	1227.5
39	DUMMYR7	2015	-1357.5	99	G43	700	1357.5	159	G103	-1700	1357.5
40	DUMMYR8	2080	-1357.5	100	G44	660	1227.5	160	G104	-1740	1227.5
41	DUMMY2	2215	-1370	101	G45	620	1357.5	161	G105	-1780	1357.5
42	Vcc1	2202.5	-1267.5	102	G46	580	1227.5	162	G106	-1820	1227.5
43	SCM	2202.5	-1184.5	103	G47	540	1357.5	163	G107	-1860	1357.5
44	GND1	2202.5	-1101.5	104	G48	500	1227.5	164	G108	-1900	1227.5
45	VGL1	2202.5	-871.5	105	G49	460	1357.5	165	G109	-1940	1357.5
46	Vgoff1	2202.5	-691.5	106	G50	420	1227.5	166	G110	-1980	1227.5
47	VGH1	2202.5	-301.5	107	G51	380	1357.5	167	G111	-2020	1357.5
48	RESET1*	2202.5	-86.5	108	G52	340	1227.5	168	G112	-2060	1227.5
49	DISPTMG1	2202.5	-16.5	109	G53	300	1357.5	169	G113	-2100	1357.5
50	CL11	2202.5	53.5	110	G54	260	1227.5	170	DUMMY4	-2215	1370
51	FLM1	2202.5	123.5	111	G55	220	1357.5	171	G114	-2202.5	1016
52	GDA1	2202.5	193.5	112	G56	180	1227.5	172	G115	-2202.5	951
53	GCS1*	2202.5	263.5	113	G57	140	1357.5	173	G116	-2202.5	886
54	GCL1	2202.5	333.5	114	G58	100	1227.5	174	G117	-2202.5	821
55	GTEST1	2202.5	561	115	G59	60	1357.5	175	G118	-2202.5	756
56	G1	2202.5	626	116	G60	20	1227.5	176	G119	-2202.5	691
57	G2	2202.5	691	117	G61	-20	1357.5	177	G120	-2202.5	626
58	G3	2202.5	756	118	G62	-60	1227.5	178	GTEST2	-2202.5	561
59	G4	2202.5	821	119	G63	-100	1357.5	179	GCL2	-2202.5	333.5
60	G5	2202.5	886	120	G64	-140	1227.5	180	GCS2*	-2202.5	263.5

No.	Pin Name	X (um)	Y (um)
181	GDA2	-2202.5	193.5
182	FLM2	-2202.5	123.5
183	CL12	-2202.5	53.5
184	DISPTMG2	-2202.5	-16.5
185	RESET2*	-2202.5	-86.5
186	VGH2	-2202.5	-301.5
187	Vgoff2	-2202.5	-691.5
188	VGL2	-2202.5	-871.5
189	GND2	-2202.5	-1101.5
190	MS	-2202.5	-1184.5
191	Vcc2	-2202.5	-1267.5

No.	Pin Name	X (um)	Y (um)
-	TG1	-1970	-1185
-	TG2	1970	-1185

Internal Block Diagram

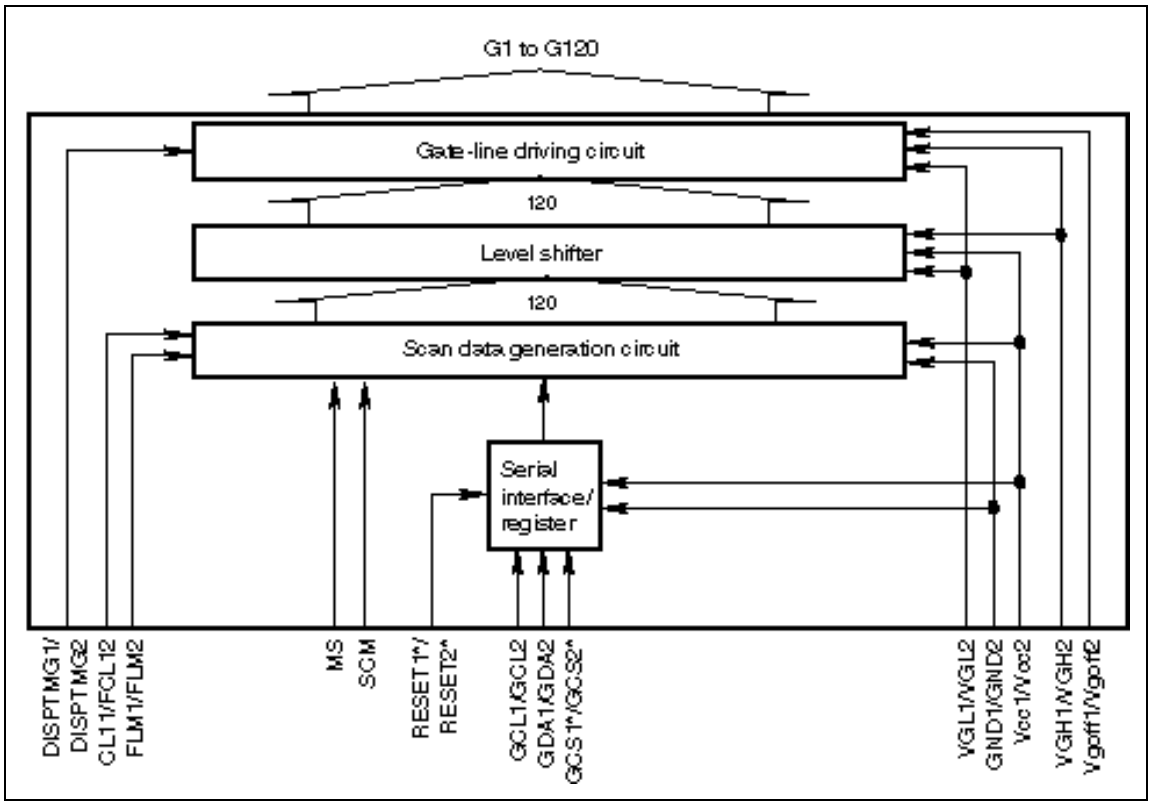


Figure 1 Block Diagram

Block Functions

1. Interface circuit

   Transfers data to the internal control register.

2. Scan data generation circuit

   Selects the output of the gate line one by one according to the FLM signal and the setting of the internal control registers.

3. Level shifter

   Converts the level of the operating power supply voltage Vcc - GND of the logic circuit to the level of the operating power supply voltage VGH - VGL of the gate-line driving circuit.

4. Gate-line driving circuit

   Selects and outputs either the VGH or the Vgoff level according to the selection signal generated at the scan data generation circuit and the level shifter.

Instructions

Outline

HD66775 has three internal registers. The data is written on to these registers by using a gate serial data interface. This interface can be directly connected to the HD66770 or HD66772 source driver for an automatic transfer of instructions. When an instruction is written on to HD66770/772 via the bus from the CPU, it is output from the serial interface of HD66770/772, and HD66775 receives the instruction to adjust the settings of one of its internal registers.

When the display system uses two HD66775s, the same instructions are transferred to both. Both HD66775s use the master/slave function to scan the gate line as well the LSI in this case is scanned.

In the bit configuration for the transfer of instructions, the upper three bits are index numbers that indicate the target register of the transfer, and the lower 13 bits are the data. This interface is common for HD66775 and HD667P00. Index numbers R00h to R02h are instructions for HD667P00, SLP and GON of R00h, and numbers R06h to R07h are instructions for HD66775.

Detailed Description

Display-Off Control (R00h)

Output Start-Position Control and Number of Valid Lines Control (R06h)

Output Scan-Direction Control and Output Scan-Method Control (R07h)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	*	GON	*	*	*	*	*	*	*	*	*	*	SLP
0	0	1	GAD	*	*	*	*	*	*	*	*	*	*	*	*
1	1	0	0	0	GS	NL4	NL3	NL2	NL1	NL0	SCN4	SCN3	SCN2	SCN1	SCN0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	FLD1	FLD0

Index code

Figure 2 R06h and R07h Instructions

SLP: When SLP = 1, the HD66775 is in the sleep mode. G1 to G120 and GTEST1 and GTEST2 are output as GND. However, the register settings are kept. For details, refer to the target specifications of the HD66770/772.

GON: When GON = 0 and DISPTMG = 0, G1 to G120 and GTEST1 and GTEST2 are output as GND. When GON = 1, G1 to G120 are normally output. For the display on/off flow, refer to the section of the instruction setting flow of the HD66770/772.

CAD: When CAD is low, GTEST1 and GTEST2 output Vgoff level. When CAD is high, GTEST1 and GTEST2 output VGH/Vgoff levels in the timing which is shown in figure 3.

GS: Selects the output scan direction of the gate driver. For description on the GS value and the scan direction, refer to the section of master/slave function and scan mode setting.

SCN4-0: Set the output start position. According to the correspondence between the setting values and the output start position in table 2, start driving the gate line by the gate line selection circuit.

NL4-0: Set the number of valid lines from the output start position. According to the correspondence between the setting values and the valid lines in table 3, drive the gate line for the number of valid lines using the gate-line selection circuit.

Set the NL4-0 and SCN4-0 so that (output start position + number of valid lines) - 1 ≤ 240 lines.

FLD1-0: Set the number of valid lines to drive n-line interlacing. Table 4 shows the correspondence between the setting value and the number of fields. Table 5 shows the scan method. The numbers in circles indicate the scanning order.

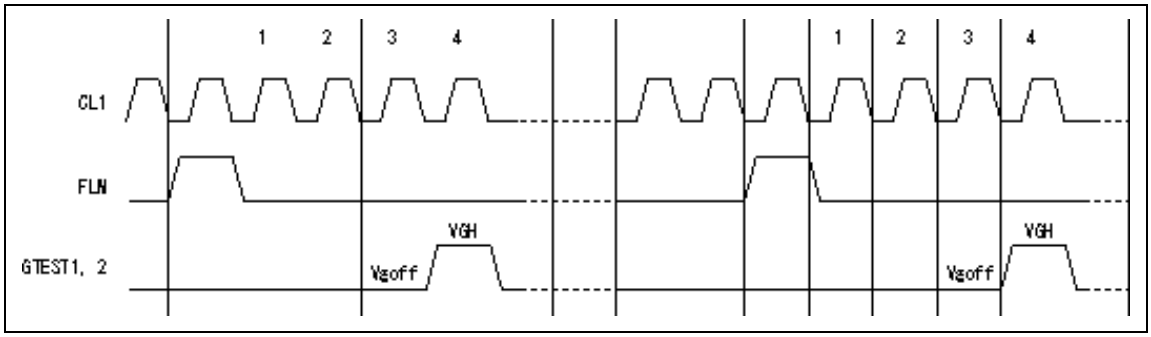


Figure 3 Output Timing for GTEST1 and GTEST2

Table 2 Correspondence between SCN4-0 and Output Start Position

					Output Start Position					
SCN4	SCN3	SCN2	SCN1	SCN0	SCM1=GND SCM2=GND GS=0	SCM1=GND SCM2=GND GS=1	SCM1=Vcc SCM2=GND GS=0	SCM1=Vcc SCM2=GND GS=1	SCM1=Vcc SCM2=Vcc GS=0	SCM1=Vcc SCM2=Vcc GS=1
0	0	0	0	0	G1	—	G120	—	G1	G120
0	0	0	0	1	G9	—	G112	—	G5	G116
0	0	0	1	0	G17	—	G104	—	G9	G112
0	0	0	1	1	G25	—	G96	—	G13	G108
0	0	1	0	0	G33	—	G88	—	G17	G104
0	0	1	0	1	G41	—	G80	—	G21	G100
0	0	1	1	0	G49	—	G72	—	G25	G96
0	1	1	1	1	G57	—	G64	—	G29	G92
0	1	0	0	0	G65	—	G56	—	G33	G88
0	1	0	0	1	G73	—	G48	—	G37	G84
0	1	0	1	0	G81	—	G40	—	G41	G80
0	1	0	1	1	G89	—	G32	—	G45	G76
0	1	1	0	0	G97	—	G24	—	G49	G72
0	1	1	0	1	G105	—	G16	—	G53	G68
0	1	1	1	0	G113	—	G8	—	G57	G64
0	1	1	1	1	—	G120	—	G1	G61	G60
1	0	0	0	0	—	G112	—	G9	G65	G56
1	0	0	0	1	—	G104	—	G17	G69	G52
1	0	0	1	0	—	G96	—	G25	G73	G48
1	0	0	1	1	—	G88	—	G33	G77	G44
1	0	1	0	0	—	G80	—	G41	G81	G40
1	0	1	0	1	—	G72	—	G49	G85	G36
1	0	1	1	0	—	G64	—	G57	G89	G32
1	0	1	1	1	—	G56	—	G65	G93	G28
1	1	0	0	0	—	G48	—	G73	G97	G24
1	1	0	0	1	—	G40	—	G81	G101	G20
1	1	0	1	0	—	G32	—	G89	G105	G16
1	1	0	1	1	—	G24	—	G97	G109	G12
1	1	1	0	0	—	G16	—	G105	G113	G8

Note: When the LSI is set as MS = GND or SCM = Vcc, an output is not started.

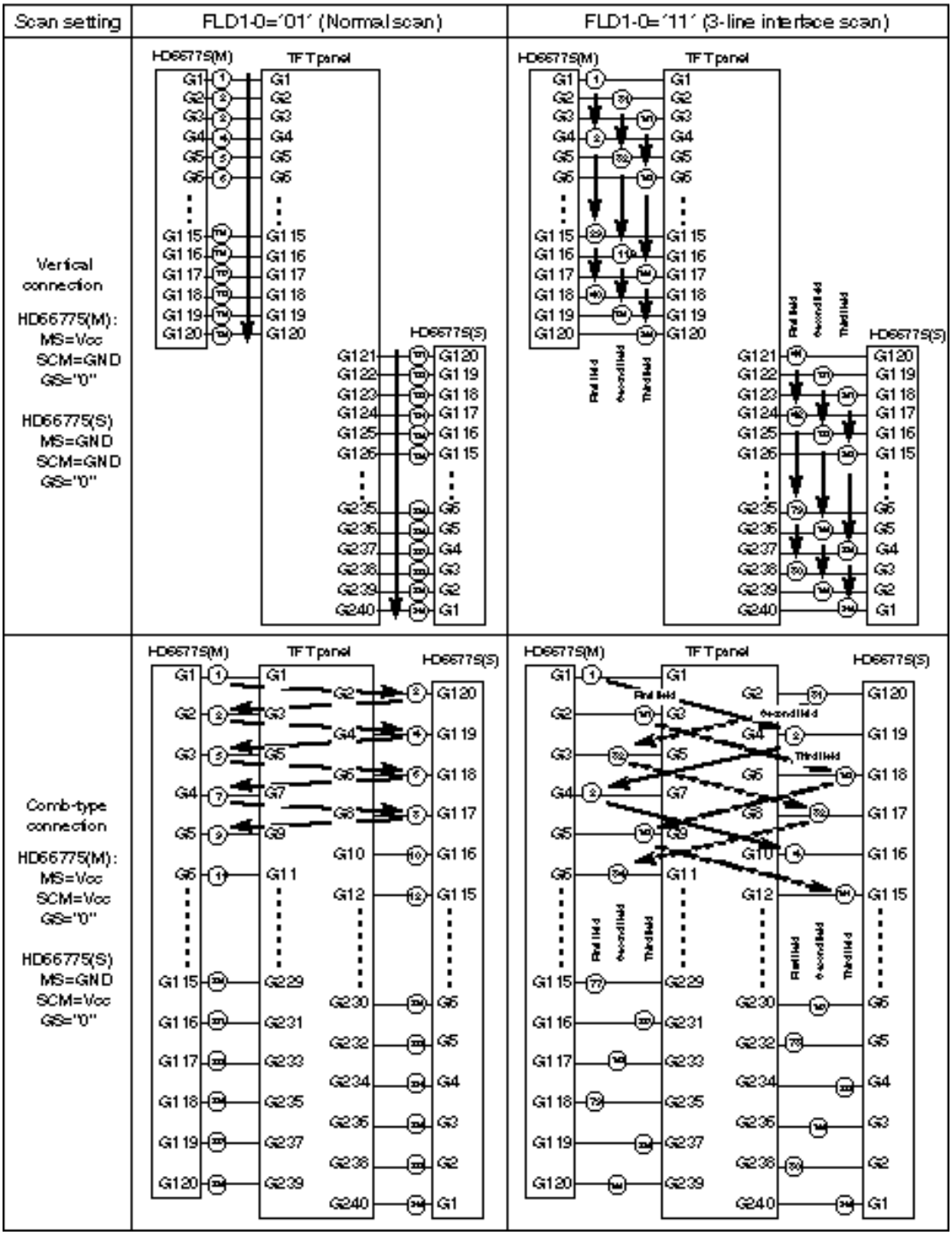
Table 3 Correspondence between NL4-0 and the Number of Valid Lines

NL4	NL3	NL2	NL1	NL0	Number of Valid Lines
0	0	0	0	0	Setting inhibited
0	0	0	0	1	16
0	0	0	1	0	24
0	0	0	1	1	32
0	0	1	0	0	40
0	0	1	0	1	48
0	0	1	1	0	56
0	0	1	1	1	64
0	1	0	0	0	72
0	1	0	0	1	80
0	1	0	1	0	88
0	1	0	1	1	96
0	1	1	0	0	104
0	1	1	0	1	112
0	1	1	1	0	120
0	1	1	1	1	128
1	0	0	0	0	136
1	0	0	0	1	144
1	0	0	1	0	152
1	0	0	1	1	160
1	0	1	0	0	168
1	0	1	0	1	176
1	0	1	1	0	184
1	0	1	1	1	192
1	1	0	0	0	200
1	1	0	0	1	208
1	1	0	1	0	216
1	1	0	1	1	224
1	1	1	0	0	232
1	1	1	0	1	240

Table 4 Correspondence between FLD1-0 and N-Line Interlacing Scan

FLD1	FLD0	Scan Method
0	0	Setting inhibited
0	1	One field
1	0	Setting inhibited
1	1	Three fields

Table 5 N-Line Interlacing Scan Method



Note: The numbers in circles indicate the scanning order.

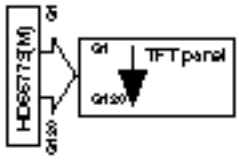
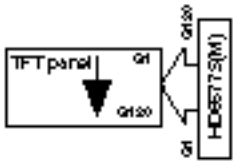
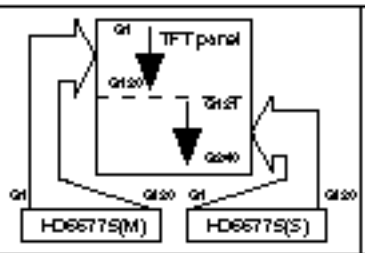
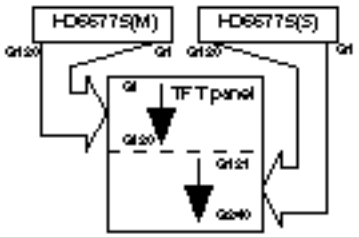
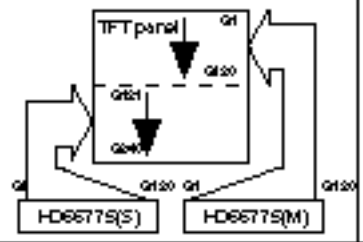
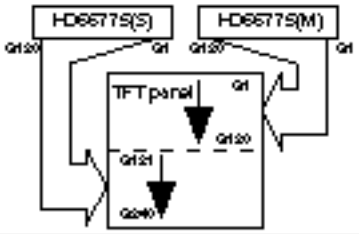
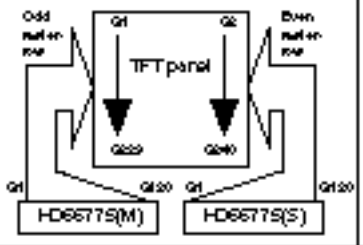
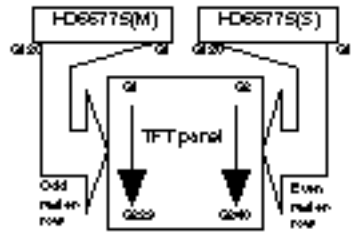
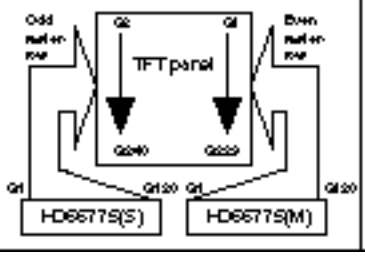
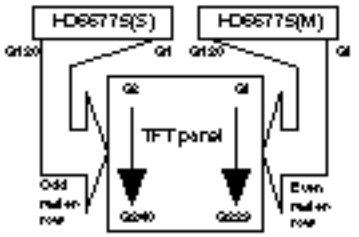
Master/Slave Function and Scan Mode Setting

The master/slave function uses two HD66775s for the 240-output gate driver function. Fix the MS pin of the driver that scans the first line to the Vcc level, and MS pin of the other driver to GND.

Shift direction of the gate signal can be changed by setting the input levels of the SCM pin and the GS bit.

Using the master/slave function with the shift direction enables various types of connections between the liquid crystal display panel and the HD66775. For details, refer to table 6, Master/Slave and Scan Mode Settings.

Table 6 Master/Slave and Scan Mode Settings

	MS	SCM	GS	Mounting example and scan direction
HD66775(M)	VCC	GND	0	
HD66775(M)	VCC	GND	1	
HD66775(M)	VCC	GND	0	 
HD66775(S)	GND			
HD66775(M)	VCC	GND	1	 
HD66775(S)	GND			
HD66775(M)	VCC	VCC	0	 
HD66775(S)	GND			
HD66775(M)	VCC	VCC	1	 
HD66775(S)	GND			

Gate Serial Transfer

The register settings are transferred from HD66770 or HD66772. The interface consists of a chip select (GCS*), a transfer clock (GCL), and data input (GDA) lines.

The data transfer starts when the falling edge of the GCS* line indicates that the data is to be transferred. The transfer ends when the rising edge of the GCS* line indicates that the transfer is over. The bits are transferred in 16-bit units, and the data is transferred in the order from MSB to LSB.

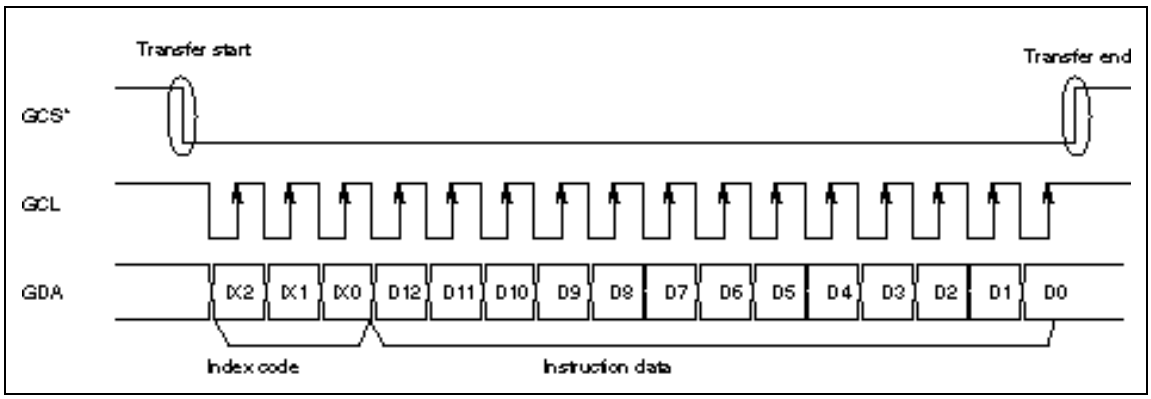


Figure 4 Format for Data Transfer

Reset Functions

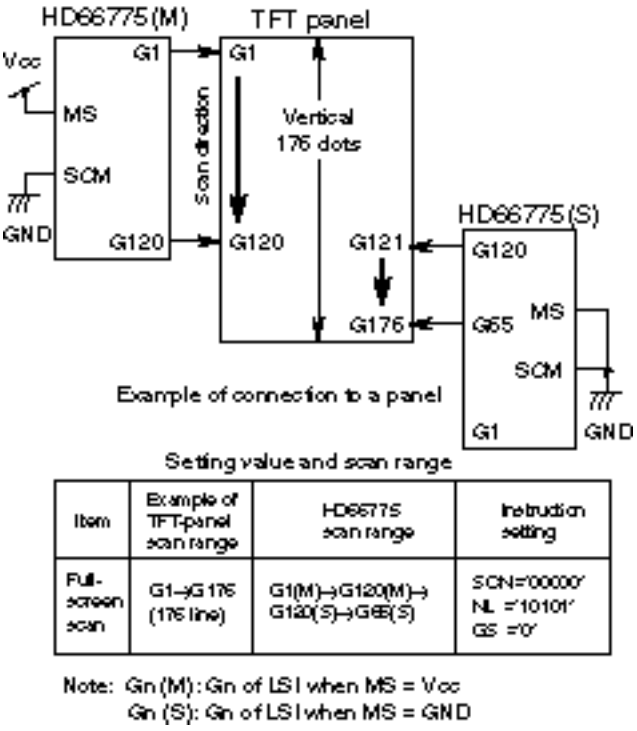
HD66775 sets the internal initialization with the RESET pin. Input a power-on reset signal when the power is applied as in the case with HD66770, HD66772, or HD667P00. Table 7 shows the initial setting values.

Table 7 Initial Setting Values for Registers at Reset

Index Code	Control Bit	Initial Value	Status
R00h	SLP	0	Cancels sleep mode.
	GON	0	Gate output control for display off: GND
R01h	CAD	0	GTEST1 and GTEST2 output Vgoff only
R06h	SCN4-0	00000	Output start position: G1
	NL4-0	11101	Number of valid lines: 240
	GS	0	Scan direction control: G1-G120
R07h	FLD1-0	01	N-line interlacing control: normal scan

Interface between the Liquid Crystal Display Panel

Figures 5 to 8 show the connection example for the configuration of the 176-dot-row TFT-LCD panel using two HD66775s, and SCN, NL, and GS bit settings and the scanning range of gate lines.

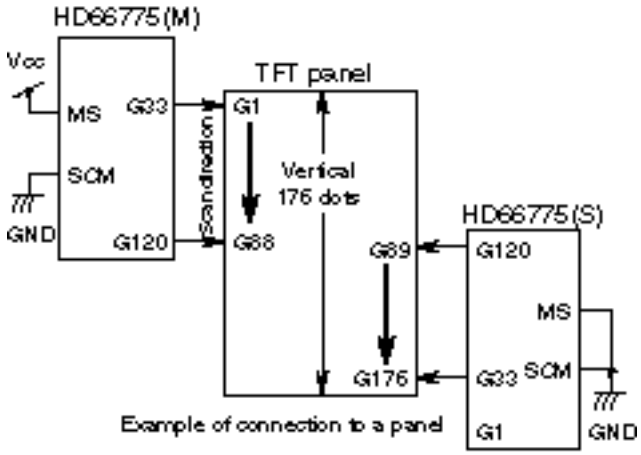


Setting value and scan range

Item	Example of TFT-panel scan range	HD66775 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G1(M)→G120(M)→ G120(S)→G65(S)	SCN='00000' NL ='10101' GS ='0'

Note: Gn (M): Gn of LSI when MS = Vcc
Gn (S): Gn of LSI when MS = GND

Figure 5 Connection Example (1)



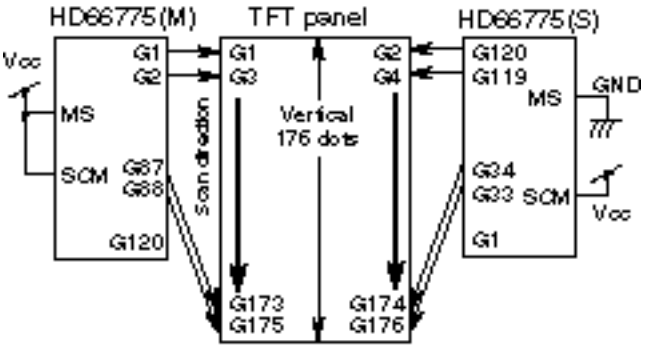
Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66775 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G33(M)→G120(M)→ G120(S)→G33(S)	SCN='00100' NL ='10101' GS ='0'

Note: Gn (M): Gn of LSI when MS = Vcc
Gn (S): Gn of LSI when MS = GND

Figure 6 Connection Example (2)



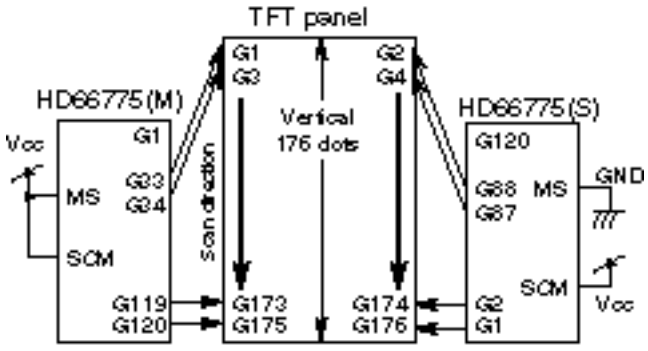
Example of connection to a panel

Setting value and scan range

Item	Example of TFT-panel scan range	HD66775 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G1(M)→G120(S) →・・・→ G88(M)→G33(S)	SCN='00000' NL ='10101' GS ='0'

Note: Gn (M): Gn of LSI when MS = Vcc
Gn (S): Gn of LSI when MS = GND

Figure 7 Connection Example (3)



Setting value and scan range

Item	Example of TFT-panel scan range	HD66775 scan range	Instruction setting
Full-screen scan	G1→G176 (176 line)	G33(M)→G88(S) → · · · →G237→ G120(M)→G1(S)	SCN='01000' NL ='10101' GS ='0'

Note: Gn (M): Gn of LSI when MS = Vcc
Gn (S): Gn of LSI when MS = GND

Figure 8 Connection Example (4)

Example of System Configuration

Figure 9 shows a TFT-LCD panel with 132 (horizontal)-by-176 (vertical) dots, configured by using the HD66770 source driver and the HD667P00 power-supply chip.

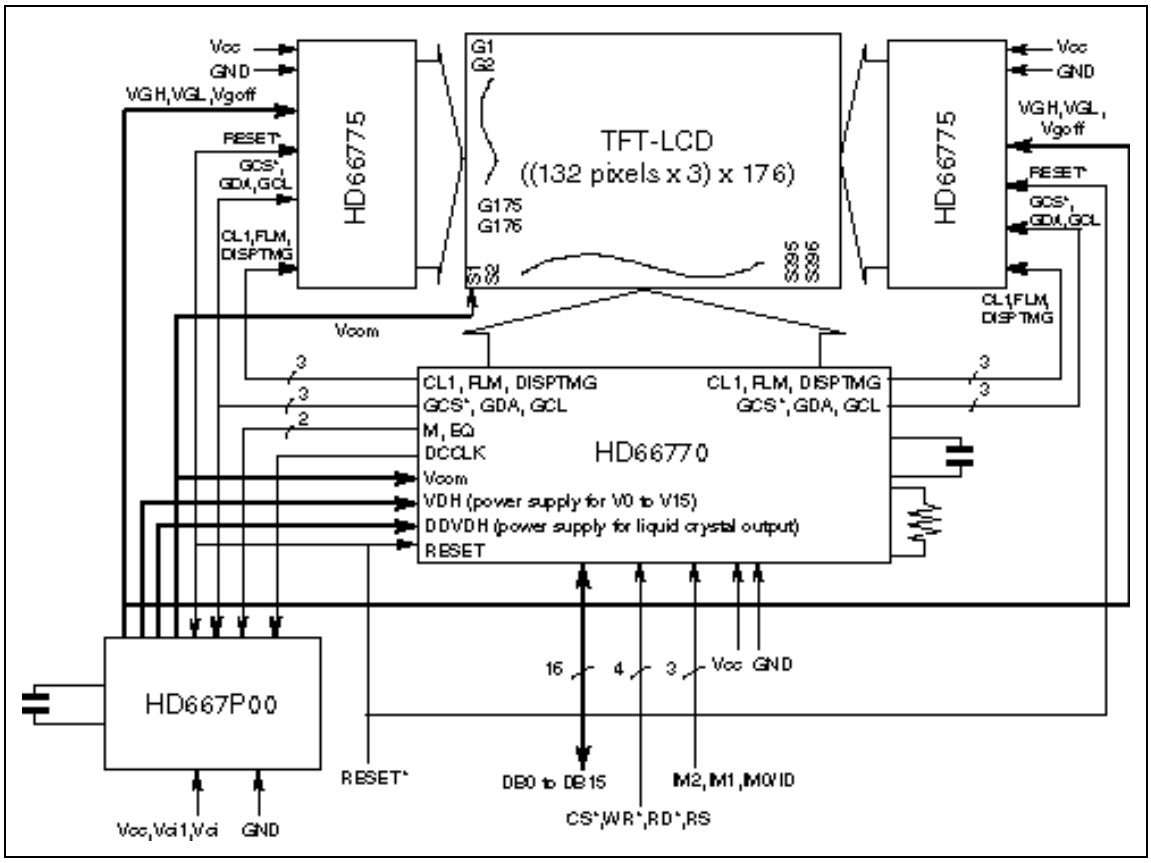
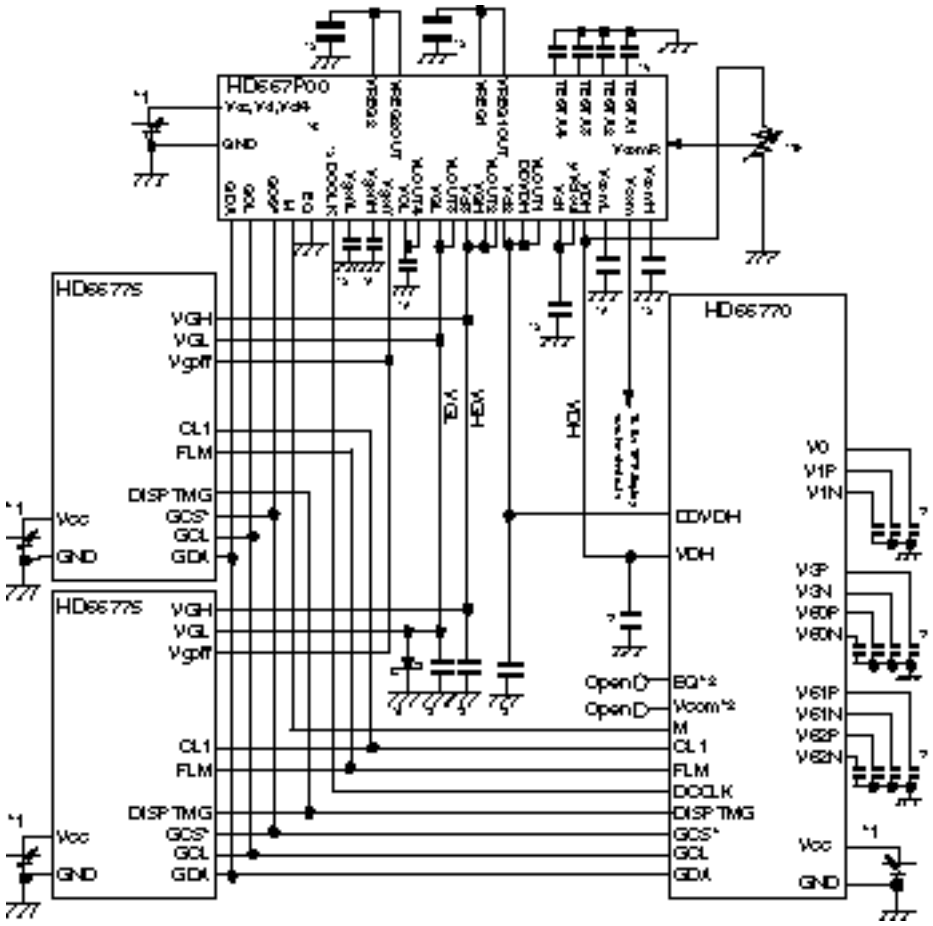


Figure 9 System Configuration

Example of Connection to HD66770 and HD667P00

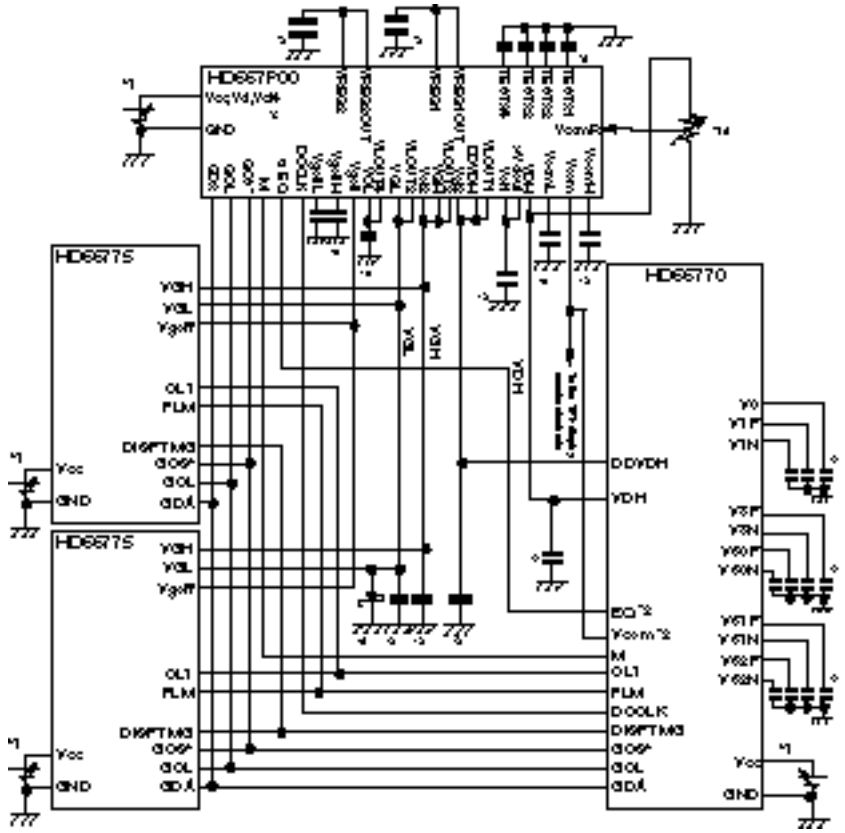
Connection differs according to the voltage setting of Vcom. Figure 10 shows an example of connection to HD66770 source driver and HD667P00 power-supply IC when VcomL < 0 V and 0 V ≤ VcomL < 5.5 V.



Notes:
1. All Vcc and GND input to HD66770, HD66775, and HD667P00 must be the same.
2. Leave the EQ and Vcom pins of HD66770 open. Set the EQ pin of HD667P00 to GND.
3. Use the 1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD667P00. Connect these capacitors according to the HD667P00 pin functions.
5. Apply 2.5 to 3.3 V to Vci by using an external power supply, and connect VciOUT to Vci1 or apply 2.75 V or lower to Vci1 by using an external power supply. Apply 2.5 to 3.3 V or lower to Vci4 by using an external power supply.
6. Conncet the Shottky barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Connect the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.
9. When step-up circuit 4, VcomL, and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.
10. Use 200-kΩ or higher variable resistor.

Figure 10 Example of Connection to HD66770 and HD667P00 when VcomL < 0 V

Figure 11 shows an example of connection to HD66770 source driver and HD667P00 power-supply IC when 0 ≤ VcomL < 5.5 V.



Notes:
1. All Vcc and GND input to HD66770, HD66775, and HD667P00 must be the same.
2. Connect the EQ pins of HD66770 and HD667P00. The Vcom pin must be connected to the Vcom pin of HD667P00. Do not set the Vcom voltage higher than 5.5 V.
3. Use the 1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
4. There is no description of how to connect the capacitors of C11- to C12-, C11+ to C12+, C21- to C23-, C21+ to C23+, C31-, C31+, C41-, and C41+ of HD667P00. Connect these capacitors according to the HD667P00 pin functions.
5. Apply 2.5 to 3.3 V to Vci by using an external power supply, and connect VciOUT to Vci1 or apply 2.75 V or lower to Vci1 by using an external power supply. Apply 2.5 to 3.3 V or lower to Vci4 by using an external power supply.
6. Conncet the Shottky barrier diode when VF = 0.4 V/20 mA and VR ≥ 30 V.
7. Use the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization to be connected.
8. Connect the 0.1-µF capacitor (B characteristics) as a capacitor for stabilization according to the display quality and power consumption.
9. When step-up circuit 4, VcomL, and VgoffH are used, use the 1-µF capacitor (B characteristics) according to the setting mode. When they are not used, leave the pin open.
10. Use 200-kΩ or higher variable resistor.

Figure 11 Example of Connection to HD66770 and HD667P00 when 0 V £ VcomL < 5.5 V

Absolute Maximum Ratings

Item		Symbol	Ratings	Unit	Notes
Power supply voltage	Logic circuit	Vcc	-0.3 to +4.6	V	1
	LCD drive circuit	VGH - GND	-0.3 to +17.5	V	
		VGL - GND	-17.5 to +0.3	V	
Input voltage		VT1	-0.3 to Vcc + 0.3	V	1, 2
Operating temperature		topr	-40 to +85	°C	
Storage temperature		Tstg	-55 to +110	°C	

Notes: 1. Voltage from GND.
2. Applies to the CL1, FLM, GCS*, GDA, GCL, RESET*, DISPTMG, MS, and SCM pins.

Note: If the LSI is used beyond the above maximum ratings, it may be permanently damaged. It should always be used within its specified operating range for normal operation to prevent malfunction or degraded reliability.

Electrical Characteristics

DC Characteristics (VCC = 1.8 to 3.3 V, VGH - VGL = 18 to 33 V, GND = 0 V, Ta = -40 to +85°C)[*1]

Item	Symbol	Test Condition	min.	typ.	max.	Unit	Notes
Input high voltage	VIH		0.8 x Vcc	-	Vcc	V	2
Input low voltage	VIL		0	-	0.2 x Vcc	V	2
Driver on resistance	RONH	VGH – VGL = 33 V, Iload = ±100 μA	-	-	10	kΩ	3
Driver on resistance	RONL	VGH – VGL = 33 V, Iload = ±100 μA	-	-	10	kΩ	3
Input leakage current	IIL	Vin = 0 to VCC	-2.5	-	2.5	μA	2
Operating frequency	fopr		10	-	100	kHz	
Current consumption 1	Icc	1/240 duty, 60-Hz frame frequency, VCC = 3 V, VGH – VGL = 33 V	-	-	T.B.D.	μA	4
Current consumption 2	IGH	1/240 duty, 60-Hz frame frequency, VCC = 3 V, VGH – VGL = 33 V			T.B.D.	μA	4

Notes: 1. For electrical characteristics of the product shipped with the chip, guaranteed at 85°C.
2. Applies to the CL1, FLM, GCS*, GDA, GCL, RESET*, DISPTMG, MS, and SCM pins.
3. Resistance values between the G and V pins (VGH or Vgoff) when the load current flows one of G1 to G120 pins.
The following condition is specified. G1 to G120 pins that are not measured are left open.
VGH = +16.5 V, Vgoff = -16.5 V, Iload = ±100 μA
4. The output pins are not loaded.

AC Characteristics (VCC = 1.8 to 3.3 V, VGH - VGL = 18 to 33 V)

Item	Symbol	Pin	min.	typ.	max.	Unit	Notes
CL1 high-level width	tCWH	CL1	1.0	-	-	µs	
CL1 low-level width	tCWL	CL1	1.0	-	-	µs	
CL1 cycle time	tCYC	CL1	10	-	-	µs	
CL1/GCL rising time	tr	CL1	-	-	100	ns	
CL1/GCL falling time	tf	CL1	-	-	100	ns	
FLM setup time	tFS	FLM, CL1	1.0	-	-	µs	
FLM hold time	tFH	FLM, CL1	1.0	-	-	µs	
GCL cycle time	tcycG	GCL	2.5	-	-	µs	
CCL high-level width	tCWHG	GCL	1.0	-	-	µs	
CCL low-level width	tCWLG	GCL	1.0	-	-	µs	
GDA setup time	tGDS	GCL, GDA	1.0	-	-	µs	
GDA hold time	tGDH	GCL, GDA	1.0	-	-	µs	
GCS low setup time	tGSL	GCL, GCS*	1.0	-	-	µs	
GCS high hold time	tGHH	GCL, GCS*	1.0	-	-	µs	
Output delay time	tDD	CL1, G	-	-	1.0	µs	VGH – VGL = 33 V

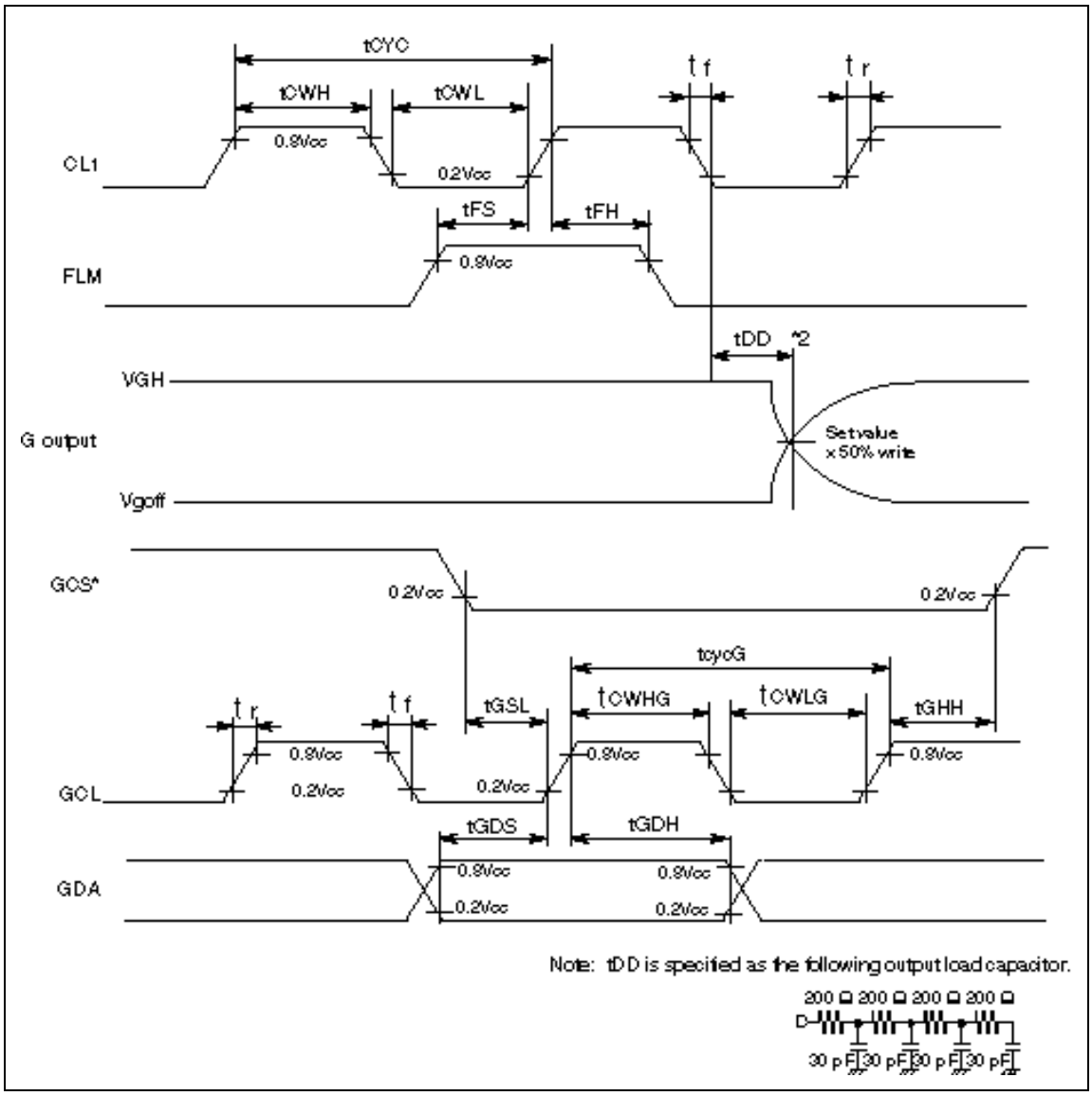


Figure 12 AC Timing