HD66776

Low Temperature poly-silicon TFT Panel 256-channel Source Driver with Internal RAM for 262,144-color display

REJxxxxxxx-xxxxZ
Rev.1.11
Oct.02.2003

Index

Description

The HD66776, a 256-channel source driver LSI, is used in combination with the HD667P20 power-supply IC to display 256 RGB-by-320-dot graphics on TFT color LCD displays in 262,144 colors. As well as the HD6766 is capable, in conjunction with the HD667P20 (power-supply IC), of outputting the signals for the control of low-temperature poly-silicon TFTs.

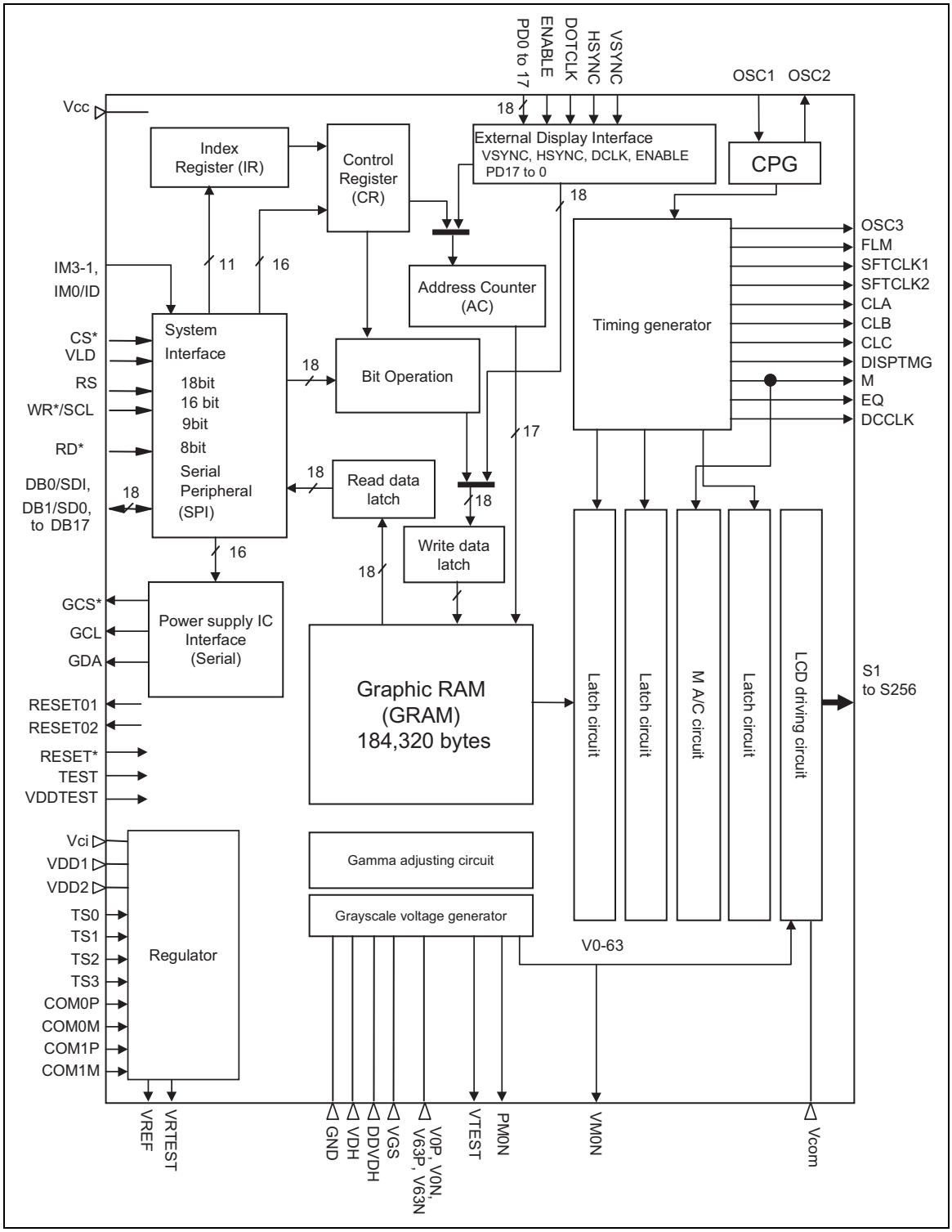
The HD66776's bit-operation functions, 8/9/16/18-bit high-speed bus interface, and high-speed RAM-write functions enable the efficient transfer of data and the high-speed rewriting of data in the graphics RAM. The HD66776's 6/16/18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0) and VSYNC interface (system interface + VSYNC) provide interfaces for use with animated displays. These interfaces provide a window-addressing function that facilitates the construction of a display in any area of the screen and allows the simultaneous display of animated images and the contents of internal RAM without concern for the static image areas.

The HD66776 and HD667P20 have various functions for reducing the power consumption of a LCD system. The HD66776 features low-voltage operation (2.2 V min.) and an internal RAM from which it is able to drive a maximum of 256RGB-by-320-dot color images. HD66776 has voltage-followers to generate the LCD-driving voltage. Since the HD66776 incorporates a circuit that interfaces with the HD667P20, it is capable of setting instructions for the HD667P20. The device supports functions such as the eight-color display function and standby and sleep modes that allow precise power control by software. This LSI is suitable for any medium-sized or small portable product that is battery driven and requires a long battery life, such as digital cellular phones that support a WWW browser and small PDAs.

Features

- 256RGB x 320-dot graphics display LCD controller/driver for 262,144 TFT colors (when used with the HD6677P20)
- Control signals for the low-temperature poly-silicon TFT-panel compatible gate driver (HD66776 + HD667P20)
- System interfaces
  - 8-/9-/16-/18-bit high-speed bus interface
  - Serial peripheral interface (SPI)
- Interfaces for use with animated displays
  - 6-/16-/18-bit RGB-I/F (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17 to 0)
  - VSYNC-I/F (system I/F + VSYNC)
- High-speed burst-RAM write function
- A window-addressing function allows writing to the set of addresses in RAM that corresponds to a window's shape.
  - The interfaces for animated displays facilitate the placing of animated pictures in any area of the screen.
  - Selective transmission to the animated-display area reduces the amount of data transmitted.
  - The contents of internal RAM may be displayed at the same time as the animated display.
- Bit-operations for graphics processing:
  - Write data mask function in bit units
- Various functions for controlling color displays:
- Simultaneous availability of 262,144 colors (γ-correction function)
- Vertical scrolling in raster-row units
- Features for low-power operation include:
  - Vcc = 2.2 to 3.3 V (low-voltage range)
  - DDVDH = 4.0 to 5.9 V (liquid-crystal driving voltage)
  - Power-save functions such as the standby and sleep modes
  - Partial LCD drive that displays two sub-screens in any position
  - Maximum 12-times step-up circuit for the liquid-crystal driving voltage (HD667P20)
  - Voltage followers to decrease the flow of direct current in the LCD drive's bleeder-resistors
- Built-in circuit for interfacing with the HD6677P20 gate-driver/power-supply IC
- Maximum 256RGB-by-320-dot display in combination with the HD6677P20 gate-driver/power-supply IC
- 184,320 bytes of internal RAM
- 256-output liquid-crystal display driver
- n-raster-row AC liquid-crystal drive (can be set to a different polarity each line)
- Internal oscillation and hardware reset
- Reversible direction for the feeding of signals from RAM to the source driver.

Block Diagram



Pin Functions

<table>
<tr><th>Signal</th><th>Number of pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM3-1, IM0/ID</td><td>4</td><td>I</td><td>GND or Vcc</td><td>Settings select the MPU-interface mode as listed below.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th><th>DB pin</th></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>GND</td><td>Setting inhibited</td><td>—</td></tr>
<tr><td>GND</td><td>GND</td><td>GND</td><td>Vcc</td><td>Setting inhibited</td><td>—</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>GND</td><td>80-system 16-bit</td><td>FB17-10, 8-1</td></tr>
<tr><td>GND</td><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 8-bit</td><td>DB17-10</td></tr>
<tr><td>GND</td><td>Vcc</td><td>GND</td><td>ID</td><td>Serial Peripheral Interface</td><td>DB1-0</td></tr>
<tr><td>GND</td><td>Vcc</td><td>Vcc</td><td>*</td><td>Setting inhibited</td><td>—</td></tr>
<tr><td>Vcc</td><td>GND</td><td>GND</td><td>GND</td><td>Setting inhibited</td><td>—</td></tr>
<tr><td>Vcc</td><td>GND</td><td>GND</td><td>Vcc</td><td>Setting inhibited</td><td>—</td></tr>
<tr><td>Vcc</td><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 18-bit</td><td>DB17-0</td></tr>
<tr><td>Vcc</td><td>GND</td><td>Vcc</td><td>Vcc</td><td>80-system 9-bit</td><td>FB17-9</td></tr>
<tr><td>Vcc</td><td>Vcc</td><td>*</td><td>*</td><td>Setting inhibited</td><td>—</td></tr>
</table>
When the serial interface is selected, the iM0 pin is used to set the ID code for the device.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>Selects the HD66776:
Low: the HD66776 is selected and is accessible.
High:HD66776 is not selected and inaccessible
Must be fixed to the GND level when not in use.</td></tr>
<tr><td>VLD</td><td>1</td><td>I</td><td>MPU</td><td>Indicates whether or not the data is valid when writing to the RAM. Low: Valid (writing of data to RAM) High: Invalid (no writing of data to RAM). The RAM address will be updated whether VLD is high or low. Must be fixed to the GND level when no in use. This signal remains available when an external display interface is in use. Polarity of VLD signal is inverted by the setting of VPL register.
<table>
<tr><th>VPL</th><th>CS</th><th>VLD</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Invalid</td><td>Held</td></tr>
</table></td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>Selects the register.
Low: Index High: Control
Fix to the “Vcc” or “GND” level while using SPI.</td></tr>
</table>

<table>
<tr><th>Signal</th><th>Number of pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-system bus interface, serves as a write strobe signal. Data is written on this signal’s low level.
For a synchronous clock interface, serves as the synchronous clock signal.</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>For an 80-system bus interface, serves as a read-strobe signal. Data is read on this signal’s low level. Fix to the “Vcc” or “GND” level while using SPI.</td></tr>
<tr><td>DB0/SD1</td><td>1</td><td>I/O</td><td>MPU</td><td>18-bit bi-directional data bus.
8-bit interface: DB17-DB10
9-bit interface: DB17-DB9
16-bit interface: DB17-DB10 and DB8-DB1
18-bit interface: DB17-DB0
Unused pins must be fixed to the Vcc or GND level.
Serves as the serial data input pin (SDI) of a clock-synchronous serial interface. The input level is read on the rising edge of the SCL signal.</td></tr>
<tr><td>DB1/SD0</td><td>1</td><td>I/O</td><td>MPU</td><td>18-bit bi-directional data bus.
8-bit interface: DB17-DB10
9-bit interface: DB17-DB9
16-bit interface: DB17-DB10 and 8 to 1
18-bit interface: DB17-DB0
Unused pins must be fixed to the Vcc or GND level.
Serves as the serial data output pin (SDO) of a clock-synchronous serial interface. Output is from the falling edge of the SCL signal.</td></tr>
<tr><td>DB2-DB17</td><td>16</td><td>I/O</td><td>MPU</td><td>18-bit bi-directional data bus.
8-bit bus: DB17-DB10
9-bit bus: DB17-DB9
16-bit bus: DB17-DB10 and 8 to 1
18-bit bus: DB17-DB0
Unused pins must be fixed to the Vcc or GND level.</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>Indicates whether or not RAM data is valid when the RGB interface is in use.
Low: Selected (access enabled)
High: Not selected (access disabled)
Must be fixed to the Vcc or GND level when not in use.
Polarity of ENABLE signal is inverted by the setting of EPL register.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>LVD</th><th>RAM Write</th><th>RAM Address</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>*</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>Invalid</td><td>Updated</td></tr>
</table></td></tr>
</table>

Signal	Number of pins	I/O	Connected to	Functions
VSYNC	1	I	MPU	Frame synchronization signal. Polarity is inverted by the setting of VSPL register.

VSPL	VSYNC	Unused
0	Low active	Vcc fixed
1	High active	GND fixed

HSYNC	1	I	MPU	Raster-row synchronization signal. Polarity is inverted by the setting of HSPL register.

HSPL	HSYNC	Unused
0	Low active	Vcc fixed
1	High active	GND fixed

DOTCLK	1	I	MPU	Dot-clock signal. Polarity is inverted by the setting of DPL signal.

DPL	DPTCLK	Unused
0	Data reading at low level	Vcc fixed
1	Data reading at high level	GND fixed

PD0-PD17	18	I	MPU	Serves as 18-bit bus for RGB data. 6-bit interface: DB17 to 12 16-bit interface: DB17 to 13 and DB11 to 1 18-bit interface: DB17 to 0 Must be fixed unused pins to the Vcc or GND level.
S1-S256	256	O	LCD	Outputs voltages for supply to the LCD. The SS bit can change the direction with which segment signals are obtained from RAM. For example, if SS = 0, the data at RAM address “00000” is output on S1. If SS = 1, it is output on S256.
FLM1,2	2	O	HD667P20	Output for the frame-start pulse.
SFTCLK11 SFTCLK12	2	O	HD667P20	Gate shift clock for LTPS. Outputs 2-laster-row pulse.
SFTCLK21 SFTCLK22	2	O	HD667P20	Gate shift clock for LTPS. Outputs 2-laster-row pulse.
CLA1 CLA2	2	O	HD667P20	Signal for control of <R>, <G>, <B> switching.
CLB1 CLB2	2	O	HD67P20	Signal for control of <R>, <G>, <B> switching.
CLC1 CLC2	2	O	HD667P20	Signal for control of <R>, <G>, <B> switching.

Signal	Number of pins	I/O	Connected to	Functions
DISPTMG1 DISPTMG2	2	O	HD667P20	Gate-control signal for LTPS.
M1 M2	2	O	HD667P20	Output for the AC-cycle pulse.
EQ1 EQ2	2	O	HD667P20	Indicates setting of the Vcom output to its high-impedance state during transitions of Vcom when Vcom is being AC-cycled. Low: VcomH or VcomL is being output on the Vcom pin. High: Vcom pin is in high-impedance state.
DCCLK1 DCCLK2	2	O	HD667P20	Outputs the clock signal for the step-up circuit.
GCL1 GCL2	2	O		Clock signal for the serial transfer of register setting to the power-supply IC. Data is output on the falling edges of this signal.
GDA1 GDA2	2	O		Data signal for the serial transfer of register setting to the power-supply IC.
GCS1* GCS2*	2	O		Chip-select signal for the HD667P20. Low: the HD667P20 is selected and can receive serially transferred data. High: the HD667P20is not selected and cannot receive serially transferred data.
DDVDH	1	I		Input for the LCD-driving voltage, which can be provided by the HD667P20. DDVDH: from +4.0 to 5.9 V
VDH	1	I	HD667P20	Reference level for grayscale voltage generation circuit, which can be provided by the HD667P20.
Vcom	1	I	HD67P20	Signal for the equalizer functions. All LCD outputs (S1-S256) are shorted to the Vcom level (high-impedance). When VcomL is lower than 0 V, this signal should not be connected.
Vcc, GND	2	—	Power supply	V_{CC}: + 2.2 V to + 3.3 V; GND (logic): 0 V
AGND	2	—	Power supply	Ground for analog. AGND:0V
OSC1 OSC2	2	I/O	Resistor for the oscillator	For connecting an external resistor for R-C oscillation.
OSC3	1	O	Open	Test pin. Must not be connected.
RESET*	1	I	MPU or external R-C circuit	Reset pin. Setting either pin low initializes the LSI. Must be reset after power is supplied. Input data through RESET1 or RESET2. Unused pins should not be connected.
RESET01 RESET02	2	O	HD667P20	Outputs the same level of voltage of same polarity with RESET*. HD66776 and HD667P20 can be controlled simultaneously by connecting to HD667P20.
VccDUM		O	Input pins	Outputs the internal Vcc level, shorting this pin sets the adjacent input pin to the GND level.
GNDDUM		O	Input pins	Outputs the internal GND level, shorting this pin sets the adjacent input pin to the GND level.

Signal	Number of pins	I/O	Connected to	Functions
DUMMY1 to DUMMY2, DUMMY29 to Dummy33	7	—	Open	Dummy pad. Must be open.
DUMMY 27 DUMMY 28 DYUMM34 DUMMY 35	4	—	Open	Test pin. Must be Open.
DUMMY3 to DUMMY26, DUMMY36 to DUMMY 59	48	—	Open	NC pin. It is possible to use these pins as transfer points for the signal cable when COG mounting.
TEST	1	I	GND	Test pin. Must be fixed to GND level.
V0P, V63P	2	I/O	Capacitor for stabilization	Internal op-amp outputs that produce a positive polarity (V0 can be used for both polarities) when the internal op-amp is on (SAP2-0 ="001", "010", "011", "100", or "101"). For connection to capacitors for stabilization.
V0N, V63N	2	I/O	Capacitor for stabilization	Internal op-amp outputs that produce a negative polarity when the internal op-amp is on (SAP2-0 ="001", "010", "011", "100", or "101"). For connection to capacitors for stabilization.
VGS	1	I	GND or External resistor	Reference level for the grayscale-voltage generation circuit. For connection to a variable resistor that adjusts the source-driver level for a panel.
VTEST	1	O	Open	Test pin. Must be disconnected.
PMON	1	O	Open	Test pin. Must be disconnected.
VMON	1	O	Open	Test pin. Must be disconnected.
VCI	1	—	Power supply	Vci: +2.5V to 3.3V
VDD1	1	I/O	VDD2, Capacitor for stabilization	Internal logic power supply. Do not connect to other than capacitor for stabilization or VDD2.
VDD2	1	I/O	VDD1, Capacitor for stabilization	Internal logic power supply. Do not connect to other than capacitor for stabilization or VDD1.
TS0-TS3	3		Open	Test pin. Must be disconnected.
COM0P, COM0M, COM1P, COM1M	4	I/O	Open	Test pin. Must be disconnected.
VDDTEST	1	I	GND	Test pin. Must be fixed to “GND” level.
VREF	1	O	Open	Test pin. Must be disconnected.
VRTEST	1	O	Open	Test pin. Must be disconnected.

PAD Arrangement

Chip size: 13.89 x 2.94mm

Chip thickness: 400μm (typ.)

Pad coordinate: Pad center

Coordinate original: Chip center

Au bump size

(1) 80μm x 80μm

DUMMY1(No.1) to DUMMY2(No.163)
DUMMY27(No.188) to DUMMY35(No.452)

(2) 56μm x 90μm

RESET01 (No.2) to RESET02 (NO.162)

(3) 80μm x 76μm

DUMMY3(No.164) to DUMMY26(No.187)
DUMMY36 (No.453) to DUMMY59(No.476)

(4) 35μm x 70μm

S1(No.451) to S128 (No.324)
S129 (No.316) to S256(No.189)

(5) 76μm x 80μm

DUMMY28(No.317) to DUMMY34(No.323)

Au bump chip: Refer to pad coordinate

Au bump height: 15μm (typ.)

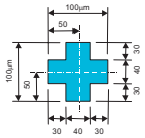
Numbers in a diagram indicate numbers in PAD coordinate.

Alignment mark

(1) PAD coordinate: Two places

(1-a) Coordinate (X,Y) = (-6636.00, -832.50)

(1-b) Coordinate (X,Y) = (6636.00, -832.50)

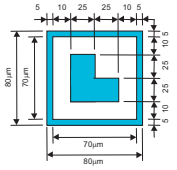


(2) Arrangement coordinate

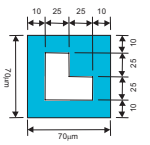
(2-a) Coordinate (X, Y) = (-6686.00, -692.50)

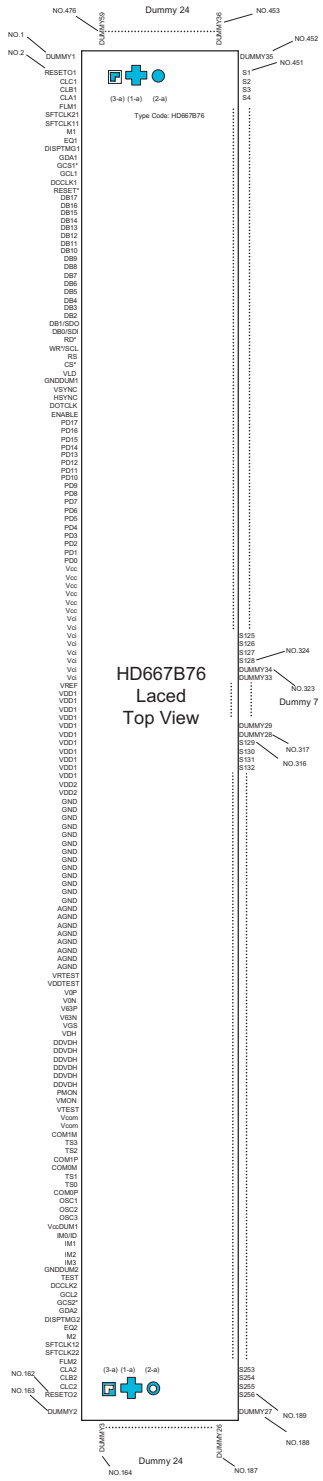
(2-b) Coordinate (X, Y) = (6686.00, -692.50)

(3) Arrangement coordinate
(3-a) Coordinate (X, Y) = (-6686.00, -972.50)



(3-b) Coordinate (X, Y) = (6686.00, -972.50)





Pad Coordinate

No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y	No.	Pad Name	X	Y
1	DUMMY1	-6827.0	-1344.3	51	PD11	-2695.0	-1339.3	101	GND	1435.0	-1339.3	151	GCS2*	5765.0	-1339.3
2	RESETO1	-6645.0	-1339.3	52	PD10	-2615.0	-1339.3	102	GND	1515.0	-1339.3	152	GDA2	5845.0	-1339.3
3	CLC1	-6565.0	-1339.3	53	PD9	-2535.0	-1339.3	103	GND	1595.0	-1339.3	153	DISPTMG2	5925.0	-1339.3
4	CLB1	-6485.0	-1339.3	54	PD8	-2455.0	-1339.3	104	AGND	1675.0	-1339.3	154	EQ2	6005.0	-1339.3
5	CLA1	-6405.0	-1339.3	55	PD7	-2375.0	-1339.3	105	AGND	1755.0	-1339.3	155	M2	6085.0	-1339.3
6	FLM1	-6325.0	-1339.3	56	PD6	-2295.0	-1339.3	106	AGND	1835.0	-1339.3	156	SFTCLK12	6165.0	-1339.3
7	SFTCLK21	-6245.0	-1339.3	57	PD5	-2215.0	-1339.3	107	AGND	1915.0	-1339.3	157	SFTCLK22	6245.0	-1339.3
8	SFTCLK11	-6165.0	-1339.3	58	PD4	-2135.0	-1339.3	108	AGND	1995.0	-1339.3	158	FLM2	6325.0	-1339.3
9	M1	-6085.0	-1339.3	59	PD3	-2055.0	-1339.3	109	AGND	2075.0	-1339.3	159	CLA2	6405.0	-1339.3
10	EQ1	-6005.0	-1339.3	60	PD2	-1975.0	-1339.3	110	AGND	2155.0	-1339.3	160	CLB2	6485.0	-1339.3
11	DISPTMG1	-5925.0	-1339.3	61	PD1	-1895.0	-1339.3	111	AGND	2235.0	-1339.3	161	CLC2	6565.0	-1339.3
12	GDA1	-5845.0	-1339.3	62	PD0	-1815.0	-1339.3	112	VRTEST	2355.0	-1339.3	162	RESETO2	6645.0	-1339.3
13	GCS1*	-5765.0	-1339.3	63	VCC	-1665.0	-1339.3	113	VDDTEST	2495.0	-1339.3	163	DUMMY2	6827.0	-1344.3
14	GCL1	-5685.0	-1339.3	64	VCC	-1585.0	-1339.3	114	V0P	2675.0	-1339.3	164	DUMMY3	6827.0	-1150.0
15	DCCLK1	-5605.0	-1339.3	65	VCC	-1505.0	-1339.3	115	V0N	2755.0	-1339.3	165	DUMMY4	6827.0	-1050.0
16	RESET*	-5525.0	-1339.3	66	VCC	-1425.0	-1339.3	116	V63P	2835.0	-1339.3	166	DUMMY5	6827.0	-950.0
17	DB17	-5415.0	-1339.3	67	VCC	-1345.0	-1339.3	117	V63N	2915.0	-1339.3	167	DUMMY6	6827.0	-850.0
18	DB16	-5335.0	-1339.3	68	VCC	-1265.0	-1339.3	118	VGS	2995.0	-1339.3	168	DUMMY7	6827.0	-750.0
19	DB15	-5255.0	-1339.3	69	VCI	-1185.0	-1339.3	119	VDH	3075.0	-1339.3	169	DUMMY8	6827.0	-650.0
20	DB14	-5175.0	-1339.3	70	VCI	-1105.0	-1339.3	120	DDVDH	3175.0	-1339.3	170	DUMMY9	6827.0	-550.0
21	DB13	-5095.0	-1339.3	71	VCI	-1025.0	-1339.3	121	DDVDH	3255.0	-1339.3	171	DUMMY10	6827.0	-450.0
22	DB12	-5015.0	-1339.3	72	VCI	-945.0	-1339.3	122	DDVDH	3335.0	-1339.3	172	DUMMY11	6827.0	-350.0
23	DB11	-4935.0	-1339.3	73	VCI	-865.0	-1339.3	123	DDVDH	3415.0	-1339.3	173	DUMMY12	6827.0	-250.0
24	DB10	-4855.0	-1339.3	74	VCI	-785.0	-1339.3	124	DDVDH	3495.0	-1339.3	174	DUMMY13	6827.0	-150.0
25	DB9	-4775.0	-1339.3	75	VCI	-705.0	-1339.3	125	DDVDH	3575.0	-1339.3	175	DUMMY14	6827.0	-50.0
26	DB8	-4695.0	-1339.3	76	VCI	-625.0	-1339.3	126	PMON	3675.0	-1339.3	176	DUMMY15	6827.0	50.0
27	DB7	-4615.0	-1339.3	77	VREF	-525.0	-1339.3	127	VMON	3755.0	-1339.3	177	DUMMY16	6827.0	150.0
28	DB6	-4535.0	-1339.3	78	VDD1	-425.0	-1339.3	128	VTEST	3835.0	-1339.3	178	DUMMY17	6827.0	250.0
29	DB5	-4455.0	-1339.3	79	VDD1	-345.0	-1339.3	129	VCOM	3915.0	-1339.3	179	DUMMY18	6827.0	350.0
30	DB4	-4375.0	-1339.3	80	VDD1	-265.0	-1339.3	130	VCOM	3995.0	-1339.3	180	DUMMY19	6827.0	450.0
31	DB3	-4295.0	-1339.3	81	VDD1	-185.0	-1339.3	131	COM1M	4095.0	-1339.3	181	DUMMY20	6827.0	550.0
32	DB2	-4215.0	-1339.3	82	VDD1	-105.0	-1339.3	132	TS3	4175.0	-1339.3	182	DUMMY21	6827.0	650.0
33	DB1/SDO	-4135.0	-1339.3	83	VDD1	-25.0	-1339.3	133	TS2	4255.0	-1339.3	183	DUMMY22	6827.0	750.0
34	DB0/SDI	-4055.0	-1339.3	84	VDD1	55.0	-1339.3	134	COM1P	4335.0	-1339.3	184	DUMMY23	6827.0	850.0
35	RD*	-3975.0	-1339.3	85	VDD1	135.0	-1339.3	135	COM0M	4415.0	-1339.3	185	DUMMY24	6827.0	950.0
36	WR*/SCL	-3895.0	-1339.3	86	VDD1	215.0	-1339.3	136	TS1	4495.0	-1339.3	186	DUMMY25	6827.0	1050.0
37	RS	-3815.0	-1339.3	87	VDD1	295.0	-1339.3	137	TS0	4575.0	-1339.3	187	DUMMY26	6827.0	1150.0
38	CS*	-3735.0	-1339.3	88	VDD1	375.0	-1339.3	138	COM0P	4655.0	-1339.3	188	DUMMY27	6827.0	1344.6
39	VLD	-3655.0	-1339.3	89	VDD2	455.0	-1339.3	139	OSC1	4805.0	-1339.3	189	S256	6521.4	1349.6
40	GNDDUM1	-3575.0	-1339.3	90	VDD2	535.0	-1339.3	140	OSC2	4885.0	-1339.3	190	S255	6473.2	1249.6
41	VSYNC	-3495.0	-1339.3	91	GND	635.0	-1339.3	141	OSC3	4965.0	-1339.3	191	S254	6425.0	1349.6
42	HSYNC	-3415.0	-1339.3	92	GND	715.0	-1339.3	142	VCCDUM1	5045.0	-1339.3	192	S253	6376.8	1249.6
43	DOTCLK	-3335.0	-1339.3	93	GND	795.0	-1339.3	143	IM0/ID	5125.0	-1339.3	193	S252	6328.6	1349.6
44	ENABLE	-3255.0	-1339.3	94	GND	875.0	-1339.3	144	IM1	5205.0	-1339.3	194	S251	6280.4	1249.6
45	PD17	-3175.0	-1339.3	95	GND	955.0	-1339.3	145	IM2	5285.0	-1339.3	195	S250	6232.2	1349.6
46	PD16	-3095.0	-1339.3	96	GND	1035.0	-1339.3	146	IM3	5365.0	-1339.3	196	S249	6184.0	1249.6
47	PD15	-3015.0	-1339.3	97	GND	1115.0	-1339.3	147	GNDDUM2	5445.0	-1339.3	197	S248	6135.8	1349.6
48	PD14	-2935.0	-1339.3	98	GND	1195.0	-1339.3	148	TEST	5525.0	-1339.3	198	S247	6087.6	1249.6
49	PD13	-2855.0	-1339.3	99	GND	1275.0	-1339.3	149	DCCLK2	5605.0	-1339.3	199	S246	6039.4	1349.6
50	PD12	-2775.0	-1339.3	100	GND	1355.0	-1339.3	150	GCL2	5685.0	-1339.3	200	S245	5991.2	1249.6

No.	Pad Name	X	Y
201	S244	5943.0	1349.6
202	S243	5894.8	1249.6
203	S242	5846.6	1349.6
204	S241	5798.4	1249.6
205	S240	5750.2	1349.6
206	S239	5702.0	1249.6
207	S238	5653.8	1349.6
208	S237	5605.6	1249.6
209	S236	5557.4	1349.6
210	S235	5509.2	1249.6
211	S234	5461.0	1349.6
212	S233	5412.8	1249.6
213	S232	5364.6	1349.6
214	S231	5316.4	1249.6
215	S230	5268.2	1349.6
216	S229	5220.0	1249.6
217	S228	5171.8	1349.6
218	S227	5123.6	1249.6
219	S226	5075.4	1349.6
220	S225	5027.2	1249.6
221	S224	4979.0	1349.6
222	S223	4930.8	1249.6
223	S222	4882.6	1349.6
224	S221	4834.4	1249.6
225	S220	4786.2	1349.6
226	S219	4738.0	1249.6
227	S218	4689.8	1349.6
228	S217	4641.6	1249.6
229	S216	4593.4	1349.6
230	S215	4545.2	1249.6
231	S214	4497.0	1349.6
232	S213	4448.8	1249.6
233	S212	4400.6	1349.6
234	S211	4352.4	1249.6
235	S210	4304.2	1349.6
236	S209	4256.0	1249.6
237	S208	4207.8	1349.6
238	S207	4159.6	1249.6
239	S206	4111.4	1349.6
240	S205	4063.2	1249.6
241	S204	4015.0	1349.6
242	S203	3966.8	1249.6
243	S202	3918.6	1349.6
244	S201	3870.4	1249.6
245	S200	3822.2	1349.6
246	S199	3774.0	1249.6
247	S198	3725.8	1349.6
248	S197	3677.6	1249.6
249	S196	3629.4	1349.6
250	S195	3581.2	1249.6

No.	Pad Name	X	Y
251	S194	3533.0	1349.6
252	S193	3484.8	1249.6
253	S192	3436.6	1349.6
254	S191	3388.4	1249.6
255	S190	3340.2	1349.6
256	S189	3292.0	1249.6
257	S188	3243.8	1349.6
258	S187	3195.6	1249.6
259	S186	3147.4	1349.6
260	S185	3099.2	1249.6
261	S184	3051.0	1349.6
262	S183	3002.8	1249.6
263	S182	2954.6	1349.6
264	S181	2906.4	1249.6
265	S180	2858.2	1349.6
266	S179	2810.0	1249.6
267	S178	2761.8	1349.6
268	S177	2713.6	1249.6
269	S176	2665.4	1349.6
270	S175	2617.2	1249.6
271	S174	2569.0	1349.6
272	S173	2520.8	1249.6
273	S172	2472.6	1349.6
274	S171	2424.4	1249.6
275	S170	2376.2	1349.6
276	S169	2328.0	1249.6
277	S168	2279.8	1349.6
278	S167	2231.6	1249.6
279	S166	2183.4	1349.6
280	S165	2135.2	1249.6
281	S164	2087.0	1349.6
282	S163	2038.8	1249.6
283	S162	1990.6	1349.6
284	S161	1942.4	1249.6
285	S160	1894.2	1349.6
286	S159	1846.0	1249.6
287	S158	1797.8	1349.6
288	S157	1749.6	1249.6
289	S156	1701.4	1349.6
290	S155	1653.2	1249.6
291	S154	1605.0	1349.6
292	S153	1556.8	1249.6
293	S152	1508.6	1349.6
294	S151	1460.4	1249.6
295	S150	1412.2	1349.6
296	S149	1364.0	1249.6
297	S148	1315.8	1349.6
298	S147	1267.6	1249.6
299	S146	1219.4	1349.6
300	S145	1171.2	1249.6

No.	Pad Name	X	Y
301	S144	1123.0	1349.6
302	S143	1074.8	1249.6
303	S142	1026.6	1349.6
304	S141	978.4	1249.6
305	S140	930.2	1349.6
306	S139	882.0	1249.6
307	S138	833.8	1349.6
308	S137	785.6	1249.6
309	S136	737.4	1349.6
310	S135	689.2	1249.6
311	S134	641.0	1349.6
312	S133	592.8	1249.6
313	S132	544.6	1349.6
314	S131	496.4	1249.6
315	S130	448.2	1349.6
316	S129	400.0	1249.6
317	DUMMY28	300.0	1344.6
318	DUMMY29	200.0	1344.6
319	DUMMY30	100.0	1344.6
320	DUMMY31	0.0	1344.6
321	DUMMY32	-100.0	1344.6
322	DUMMY33	-200.0	1344.6
323	DUMMY34	-300.0	1344.6
324	S128	-400.0	1349.6
325	S127	-448.2	1249.6
326	S126	-496.4	1349.6
327	S125	-544.6	1249.6
328	S124	-592.8	1349.6
329	S123	-641.0	1249.6
330	S122	-689.2	1349.6
331	S121	-737.4	1249.6
332	S120	-785.6	1349.6
333	S119	-833.8	1249.6
334	S118	-882.0	1349.6
335	S117	-930.2	1249.6
336	S116	-978.4	1349.6
337	S115	-1026.6	1249.6
338	S114	-1074.8	1349.6
339	S113	-1123.0	1249.6
340	S112	-1171.2	1349.6
341	S111	-1219.4	1249.6
342	S110	-1267.6	1349.6
343	S109	-1315.8	1249.6
344	S108	-1364.0	1349.6
345	S107	-1412.2	1249.6
346	S106	-1460.4	1349.6
347	S105	-1508.6	1249.6
348	S104	-1556.8	1349.6
349	S103	-1605.0	1249.6
350	S102	-1653.2	1349.6

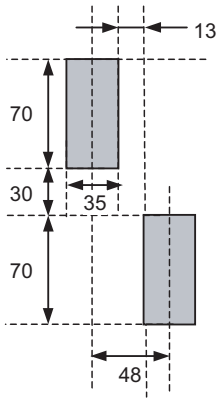
No.	Pad Name	X	Y
351	S101	-1701.4	1249.6
352	S100	-1749.6	1349.6
353	S99	-1797.8	1249.6
354	S98	-1846.0	1349.6
355	S97	-1894.2	1249.6
356	S96	-1942.4	1349.6
357	S95	-1990.6	1249.6
358	S94	-2038.8	1349.6
359	S93	-2087.0	1249.6
360	S92	-2135.2	1349.6
361	S91	-2183.4	1249.6
362	S90	-2231.6	1349.6
363	S89	-2279.8	1249.6
364	S88	-2328.0	1349.6
365	S87	-2376.2	1249.6
366	S86	-2424.4	1349.6
367	S85	-2472.6	1249.6
368	S84	-2520.8	1349.6
369	S83	-2569.0	1249.6
370	S82	-2617.2	1349.6
371	S81	-2665.4	1249.6
372	S80	-2713.6	1349.6
373	S79	-2761.8	1249.6
374	S78	-2810.0	1349.6
375	S77	-2858.2	1249.6
376	S76	-2906.4	1349.6
377	S75	-2954.6	1249.6
378	S74	-3002.8	1349.6
379	S73	-3051.0	1249.6
380	S72	-3099.2	1349.6
381	S71	-3147.4	1249.6
382	S70	-3195.6	1349.6
383	S69	-3243.8	1249.6
384	S68	-3292.0	1349.6
385	S67	-3340.2	1249.6
386	S66	-3388.4	1349.6
387	S65	-3436.6	1249.6
388	S64	-3484.8	1349.6
389	S63	-3533.0	1249.6
390	S62	-3581.2	1349.6
391	S61	-3629.4	1249.6
392	S60	-3677.6	1349.6
393	S59	-3725.8	1249.6
394	S58	-3774.0	1349.6
395	S57	-3822.2	1249.6
396	S56	-3870.4	1349.6
397	S55	-3918.6	1249.6
398	S54	-3966.8	1349.6
399	S53	-4015.0	1249.6
400	S52	-4063.2	1349.6

No.	Pad Name	X	Y
401	S51	-4111.4	1249.6
402	S50	-4159.6	1349.6
403	S49	-4207.8	1249.6
404	S48	-4256.0	1349.6
405	S47	-4304.2	1249.6
406	S46	-4352.4	1349.6
407	S45	-4400.6	1249.6
408	S44	-4448.8	1349.6
409	S43	-4497.0	1249.6
410	S42	-4545.2	1349.6
411	S41	-4593.4	1249.6
412	S40	-4641.6	1349.6
413	S39	-4689.8	1249.6
414	S38	-4738.0	1349.6
415	S37	-4786.2	1249.6
416	S36	-4834.4	1349.6
417	S35	-4882.6	1249.6
418	S34	-4930.8	1349.6
419	S33	-4979.0	1249.6
420	S32	-5027.2	1349.6
421	S31	-5075.4	1249.6
422	S30	-5123.6	1349.6
423	S29	-5171.8	1249.6
424	S28	-5220.0	1349.6
425	S27	-5268.2	1249.6
426	S26	-5316.4	1349.6
427	S25	-5364.6	1249.6
428	S24	-5412.8	1349.6
429	S23	-5461.0	1249.6
430	S22	-5509.2	1349.6
431	S21	-5557.4	1249.6
432	S20	-5605.6	1349.6
433	S19	-5653.8	1249.6
434	S18	-5702.0	1349.6
435	S17	-5750.2	1249.6
436	S16	-5798.4	1349.6
437	S15	-5846.6	1249.6
438	S14	-5894.8	1349.6
439	S13	-5943.0	1249.6
440	S12	-5991.2	1349.6
441	S11	-6039.4	1249.6
442	S10	-6087.6	1349.6
443	S9	-6135.8	1249.6
444	S8	-6184.0	1349.6
445	S7	-6232.2	1249.6
446	S6	-6280.4	1349.6
447	S5	-6328.6	1249.6
448	S4	-6376.8	1349.6
449	S3	-6425.0	1249.6
450	S2	-6473.2	1349.6

No.	Pad Name	X	Y
451	S1	-6521.4	1249.6
452	DUMMY35	-6827.0	1344.6
453	DUMMY36	-6827.0	1150.0
454	DUMMY37	-6827.0	1050.0
455	DUMMY38	-6827.0	950.0
456	DUMMY39	-6827.0	850.0
457	DUMMY40	-6827.0	750.0
458	DUMMY41	-6827.0	650.0
459	DUMMY42	-6827.0	550.0
460	DUMMY43	-6827.0	450.0
461	DUMMY44	-6827.0	350.0
462	DUMMY45	-6827.0	250.0
463	DUMMY46	-6827.0	150.0
464	DUMMY47	-6827.0	50.0
465	DUMMY48	-6827.0	-50.0
466	DUMMY49	-6827.0	-150.0
467	DUMMY50	-6827.0	-250.0
468	DUMMY51	-6827.0	-350.0
469	DUMMY52	-6827.0	-450.0
470	DUMMY53	-6827.0	-550.0
471	DUMMY54	-6827.0	-650.0
472	DUMMY55	-6827.0	-750.0
473	DUMMY56	-6827.0	-850.0
474	DUMMY57	-6827.0	-950.0
475	DUMMY58	-6827.0	-1050.0
476	DUMMY59	-6827.0	-1150.0

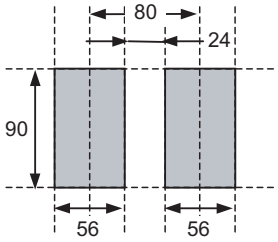
Bump Arrangement

SI to 256 (Laced)



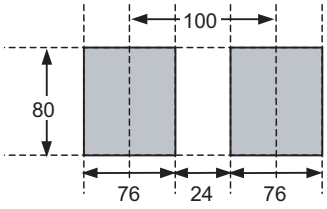
Unit: m

RESET01 to RESET02



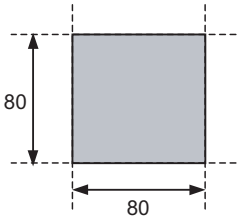
Unit: m

DUMMY3 to 26, 28 to 34, 36 to 59



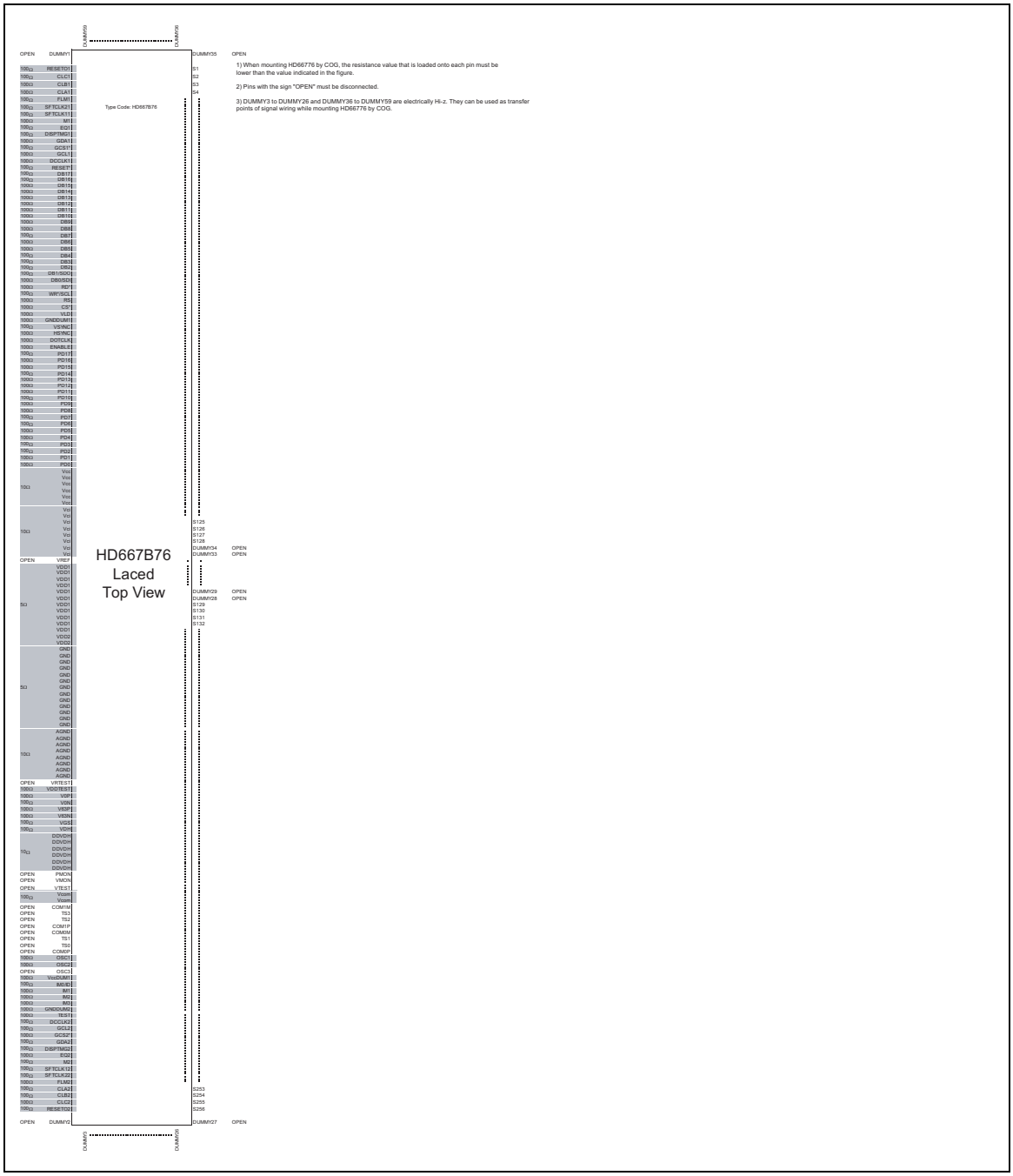
Unit: m

DUMMY1, 2, 27, 35



Unit: m

Pin connecting resistance recommended value



Block Function Descriptions

System interface

The HD66776 has five high-speed system interfaces: an 80-system 18-bit/16-bit/9-bit/8-bit bus and a clocked serial peripheral (SPI: Serial Peripheral Interface) port. The interface mode is selected by the IM3-0 pins.

The HD66776 has three registers: a 16-bit index register (IR), an 18-bit write-data register (WDR), and an 18-bit read-data register (RDR). The IR stores index information from the control registers and the GRAM. The WDR temporarily stores data to be written into control registers and the GRAM, and the RDR temporarily stores data read from the GRAM. Data written into the GRAM from the MPU is first written into the WDR and then is automatically written into the GRAM by internal operation. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are normal.

Execution time for instruction excluding oscillation start is 0 clock cycle and instructions can be written in succession.

Register Selection (8/9/16/18 Parallel interface)

80-system Bus			
WR*	**RD***	**RS**	**Operation**
0	1	0	Writes index to IR.
1	0	0	Setting inhibited.
0	1	1	Writes to control registers and GRAM through WDR.
1	0	1	Reads data from GRAM through RDR.

Values of CS and VLD during RAM Write

VPL	CS*	VLD	Operations
0	0	0	Data is written to the GRAM. RAM address is updated.
	1	0	Data is not written to the GRAM. RAM address is not updated.
	0	1	Data is not written to the GRAM. RAM address is updated.
	1	1	Data is not written to the GRAM. RAM address is not updated.
1	0	0	Data is not written to the GRAM, RAM address is updated.
	1	0	Data is not written to the GRAM. RAM address is not updated.
	0	1	Data is written to the GRAM. RAM address is updated.
	1	1	Data is not written to the GRAM. RAM address is not updated.

Note: The value of VLD only has a meaning for the RAM write instructions.

Register selection (Serial peripheral interface)

Start bytes		
R/W-bit	RS-bit	Operations
0	0	Writes an index into IR.
1	0	Setting inhibited.
0	1	Writes data to control registers and GRAM through WDR.
1	1	Reads data from GRAM through RDR.

External Display Interface (RGB-I/F, VSYNC-I/F)

The HD66776 incorporates RGB and VSYNC interfaces as external interfaces for the reproduction of animated displays. When the RGB-I/F is selected, the synchronization signals, which are VSYNC, HSYNC, and DOTCLK and are supplied from the external interfaces, are available for use in operating the display. The data for display (PD17-0) are written according to the values of the data enable signal (ENABLE) and data valid signal (VLD) in synchronization with the VSYNC, HSYNC, and DOTCLK signals. This allows flicker-free updating of the screen. When the VSYNC-I/F is selected, operations other than frame synchronization by the VSYNC signal are synchronized with the internal clock. The data for display is written to the GRAM via the system interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

Switching from and to the system interface is done by instructions. The interface, therefore, can be selected according to whether the screen is displaying moving or still pictures. All data written via the RGB-I/F are written to the GRAM. Therefore, data is only transferred when the screen is updated, which reduces the amount of data transferred and the consumption of power when moving pictures are being displayed.

Bit Operations

The HD66772 is equipped with a write data mask function that selects and writes data into the GRAM. For details, see the section on the graphics operation functions.

Address Counter (AC)

The address counter (AC) assigns addresses to the GRAM. When an address set instruction is written into the IR, the address information is sent from the IR to the AC.

After writing into the GRAM, the AC is automatically incremented by 1 (or decremented by 1). After reading from the data, the AC is not updated. A window address function allows for data to be written only to a window area specified by GRAM.

Graphics RAM (GRAM)

The graphics RAM (GRAM) has 18 bits/pixel and stores the bit-pattern data of 256 x 320 bytes.

Grayscale Voltage Generation Circuit

The grayscale voltage generation circuit generates LCD-driving voltages according to the grayscale data set in the γ-correction register. 262,144 colors are simultaneously available for display. For details, see the section on the γ-correction register.

Timing Generator

The timing generator generates timing signals for the operation of internal circuits such as the GRAM. The RAM read timing for display and internal operation timing by MPU access is generated separately to avoid interference with one another. The timing generator generates the interface signals (M, FLM, SFTCLK, SFTCLK2, CLA, CLB, CLC, EQ, DISPTMG, and DCCLK) for the power-supply IC.

Oscillation Circuit (OSC)

The HD66776 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pins. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

Liquid Crystal Display Driver Circuit

The liquid crystal display driver circuit consists of 256 source drivers (S1 to S256).

The shift direction of 256-bit data can be changed by the SS bit by selecting an appropriate direction for the device mounting configuration.

Interface with Power supply IC

A serial interface circuit provides an interface with the HD667P20. When sending an instruction setting from the HD66776 to the HD667P20, a register setting value from within the HD66776 is transferred via the serial interface circuit. A transfer is started by setting a serial transfer enable in the HD66776. However, transfer to and reading from the HD6677P20 are not possible during standby. For details, see the Gate serial transfer to and from the gate driver.

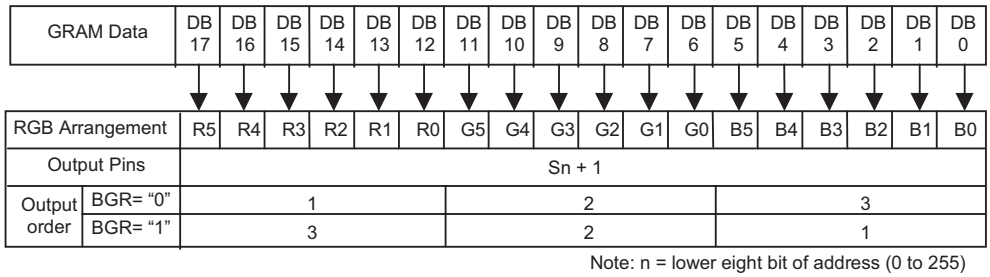
GRAM Address Map

Relation between GRAM Addresses and Screen Position (SS = "0")

S Pin/Display line	S1	S2	S3	S4	S5	.....	S255	S256
	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0		PD17 ----- PD0	PD17 ----- PD0
Line 1	"00000"H	"00001"H	"00002"H	"00003"H	"00004"H	.....	"000FE"H	"000FF"H
Line 2	"00100"H	"00101"H	"00102"H	"00103"H	"00104"H	.....	"001FE"H	"001FF"H
Line 3	"00200"H	"00201"H	"00202"H	"00203"H	"00204"H	.....	"002FE"H	"002FF"H
Line 4	"00300"H	"00301"H	"00302"H	"00303"H	"00304"H	.....	"003FE"H	"003FF"H
Line 5	"00400"H	"00401"H	"00402"H	"00403"H	"00404"H	.....	"004FE"H	"004FF"H
Line 6	"00500"H	"00501"H	"00502"H	"00503"H	"00504"H	.....	"005FE"H	"005FF"H
Line 7	"00600"H	"00601"H	"00602"H	"00603"H	"00604"H	.....	"006FE"H	"006FF"H
Line 8	"00700"H	"00701"H	"00702"H	"00703"H	"00704"H	.....	"007FE"H	"007FF"H
Line 9	"00800"H	"00801"H	"00802"H	"00803"H	"00804"H	.....	"008FE"H	"008FF"H
Line 10	"00900"H	"00901"H	"00902"H	"00903"H	"00904"H	.....	"009FE"H	"009FF"H
Line 11	"00A00"H	"00A01"H	"00A02"H	"00A03"H	"00A04"H	.....	"00AFE"H	"00AFF"H
Line 12	"00B00"H	"00B01"H	"00B02"H	"00B03"H	"00B04"H	.....	"00BFE"H	"00BFF"H
Line 13	"00C00"H	"00C01"H	"00C02"H	"00C03"H	"00C04"H	.....	"00CFE"H	"00CFF"H
Line 14	"00D00"H	"00D01"H	"00D02"H	"00D03"H	"00D04"H	.....	"00DFE"H	"00DFF"H
Line 15	"00E00"H	"00E01"H	"00E02"H	"00E03"H	"00E04"H	.....	"00EFE"H	"00EFF"H
Line 16	"00F00"H	"00F01"H	"00F02"H	"00F03"H	"00F04"H	.....	"00FFE"H	"00FFF"H
Line 17	"01000"H	"01001"H	"01002"H	"01003"H	"01004"H	.....	"010FE"H	"010FF"H
Line 18	"01100"H	"01101"H	"01102"H	"01103"H	"01104"H	.....	"011FE"H	"011FF"H
Line 19	"01200"H	"01201"H	"01202"H	"01203"H	"01204"H	.....	"012FE"H	"012FF"H
Line 20	"01300"H	"01301"H	"01302"H	"01303"H	"01304"H	.....	"013FE"H	"013FF"H
⋮	⋮	⋮	⋮	⋮	⋮	.....	⋮	⋮
Line 319	"13E00"H	"13E01"H	"13E02"H	"13E03"H	"13E04"H	.....	"13EFE"H	"13EFF"H
Line 320	"13F00"H	"13F01"H	"13F02"H	"13F03"H	"13F04"H	.....	"13FFE"H	"13FFF"H

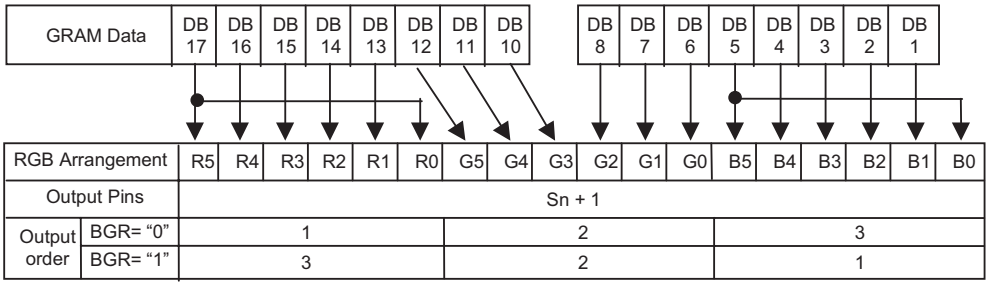
Relation between GRAM data and Display contents (SS = "0")

80-system 18-bit interface



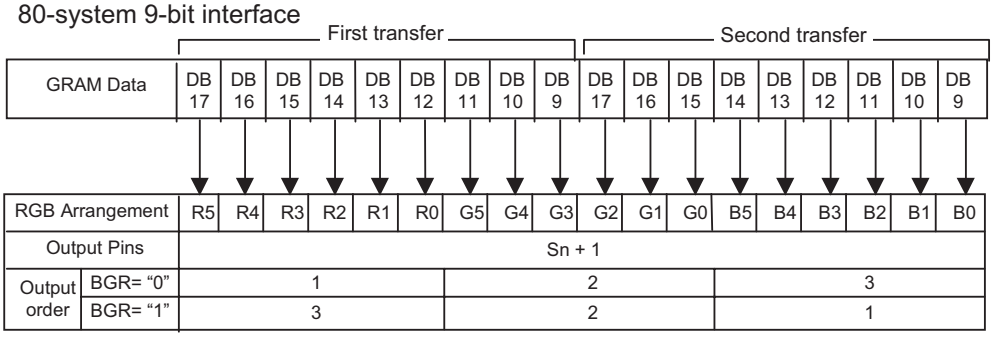
Note: n = lower eight bit of address (0 to 255)

80-system 16-bit interface



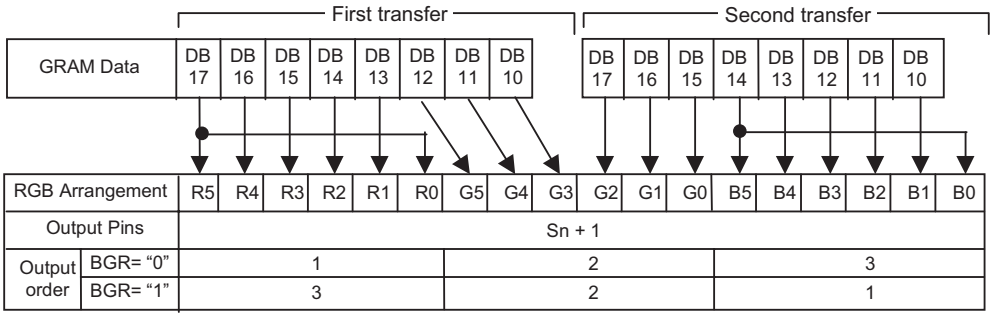
Note: n = lower eight bit of address (0 to 255)

80-system 9-bit interface



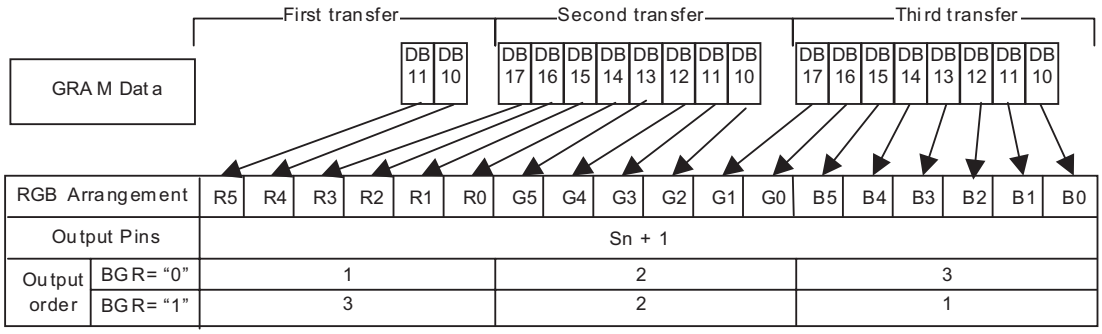
Note: n = lower eight bit of address (0 to 255)

80-system 8-bit interface (1) (two times transfer/pixel)



Note: n = lower eight bit of address (0 to 255)

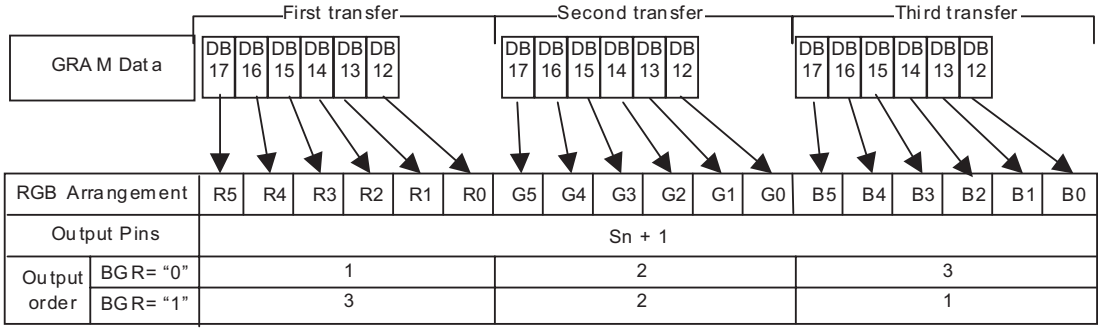
80-system 8-bit interface (2) (three times transfer/pixel)



RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR= "0"	1						2						3					
Output order BGR= "1"	3						2						1					

Note: n = lower eight bit of address (0 to 255)

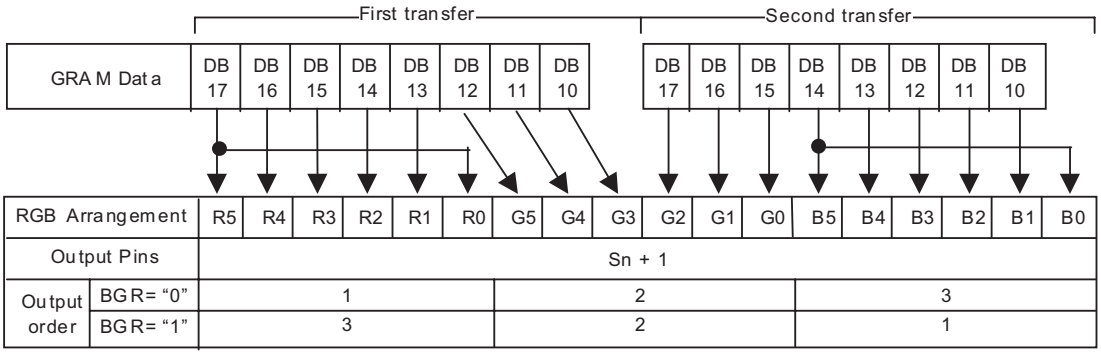
80-system 8-bit interface (3) (three times transfer/pixel)



RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR= "0"	1						2						3					
Output order BGR= "1"	3						2						1					

Note: n = lower eight bit of address (0 to 255)

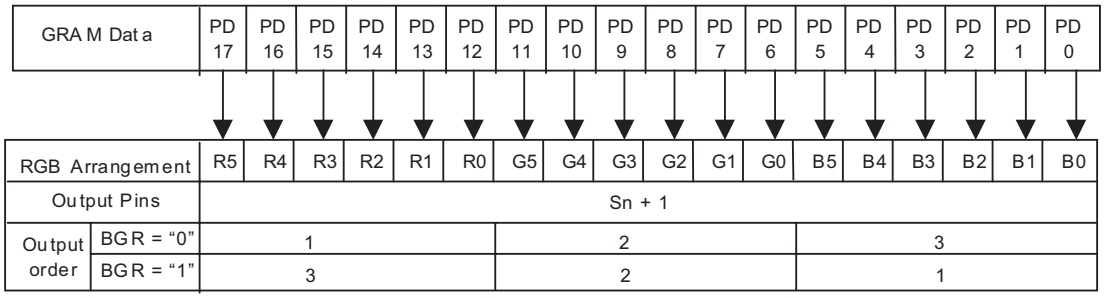
SPI (two times transfer/pixel)



RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR= "0"	1						2						3					
Output order BGR= "1"	3						2						1					

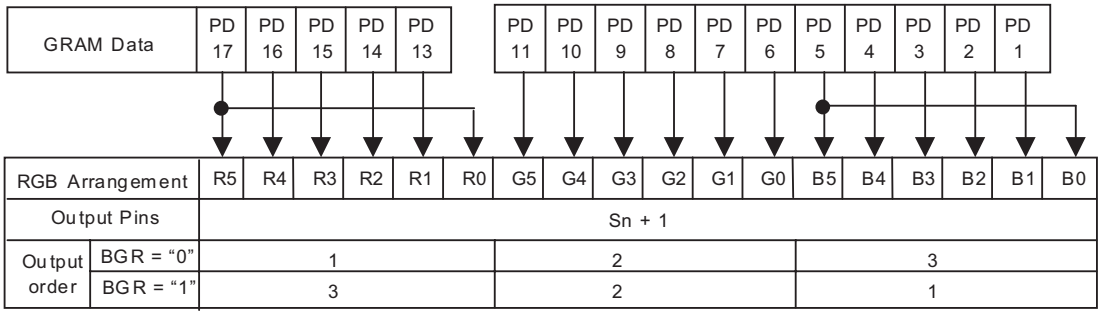
Note: n = lower eight bit of address (0 to 255)

18-bit RGB interface



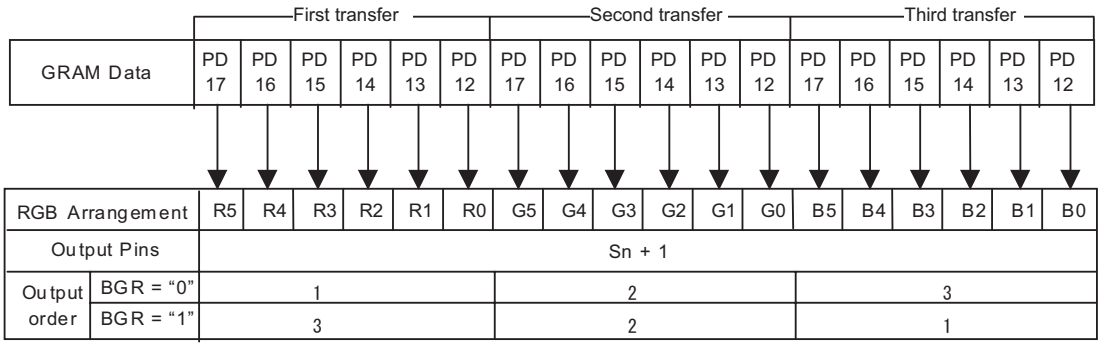
GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

16-bit RGB interface



GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

6-bit RGB interface



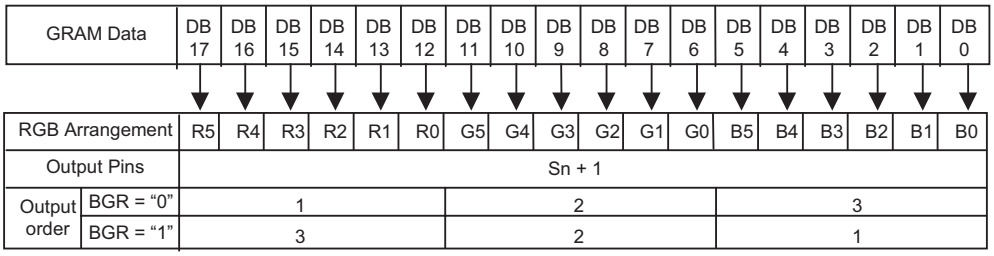
	First transfer						Second transfer						Third transfer					
GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

Relation between GRAM Addresses and Screen Position (SS = "1")

S Pin/Display line	S1	S2	S3	S4	S5	.....	S255	S256
	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0	PD17 ----- PD0		PD17 ----- PD0	PD17 ----- PD0
Line 1	"000FF"H	"000FE"H	"000FD"H	"000FC"H	"000EB"H	.....	"00001"H	"00000"H
Line 2	"001FF"H	"001FE"H	"001FD"H	"001FC"H	"001EB"H	.....	"00101"H	"00100"H
Line 3	"002FF"H	"002FE"H	"002FD"H	"002FC"H	"002EB"H	.....	"00201"H	"00200"H
Line 4	"003FF"H	"003FE"H	"003FD"H	"003FC"H	"003EB"H	.....	"00301"H	"00300"H
Line 5	"004FF"H	"004FE"H	"004FD"H	"004FC"H	"004EB"H	.....	"00401"H	"00400"H
Line 6	"005FF"H	"005FE"H	"005FD"H	"005FC"H	"005EB"H	.....	"00501"H	"00500"H
Line 7	"006FF"H	"006FE"H	"006FD"H	"006FC"H	"006EB"H	.....	"00601"H	"00600"H
Line 8	"007FF"H	"007FE"H	"007FD"H	"007FC"H	"007EB"H	.....	"00701"H	"00700"H
Line 9	"008FF"H	"008FE"H	"008FD"H	"008FC"H	"008EB"H	.....	"00801"H	"00800"H
Line 10	"009FF"H	"009FE"H	"009FD"H	"009FC"H	"009EB"H	.....	"00901"H	"00900"H
Line 11	"00AFF"H	"00AFE"H	"00AFD"H	"00AFC"H	"00AEB"H	.....	"00A01"H	"00A00"H
Line 12	"00BFF"H	"00BFE"H	"00BFD"H	"00BFC"H	"00BEB"H	.....	"00B01"H	"00B00"H
Line 13	"00CFF"H	"00CFE"H	"00CFD"H	"00CFC"H	"00CEB"H	.....	"00C01"H	"00C00"H
Line 14	"00DFF"H	"00DFE"H	"00DFD"H	"00DFC"H	"00DEB"H	.....	"00D01"H	"00D00"H
Line 15	"00EFF"H	"00EFE"H	"00EFD"H	"00EFC"H	"00EEB"H	.....	"00E01"H	"00E00"H
Line 16	"00FFF"H	"00FFE"H	"00FFD"H	"00FFC"H	"00FEB"H	.....	"00F01"G	"00F00"H
Line 17	"010FF"H	"010FE"H	"010FD"H	"010FC"H	"010EB"H	.....	"01001"H	"01000"H
Line 18	"011FF"H	"011FE"H	"011FD"H	"011FC"H	"011EB"H	.....	"01101"H	"01100"H
Line 19	"012FF"H	"012FE"H	"012FD"H	"012FC"H	"012EB"H	.....	"01201"H	"01200"H
Line 20	"013FF"H	"013FE"H	"013FD"H	"013FC"H	"013EB"H	.....	"01301"H	"01300"H
⋮	⋮	⋮	⋮	⋮	⋮	.....	⋮	⋮
Line 319	"13EFF"H	"13EFE"H	"13EFD"H	"13EFC"H	"13EEB"H	.....	"13E01"H	"13E00"H
Line 320	"13FFF"H	"13FFE"H	"13FFD"H	"13FFC"H	"13FEB"H	.....	"13F01"H	"13F00"H

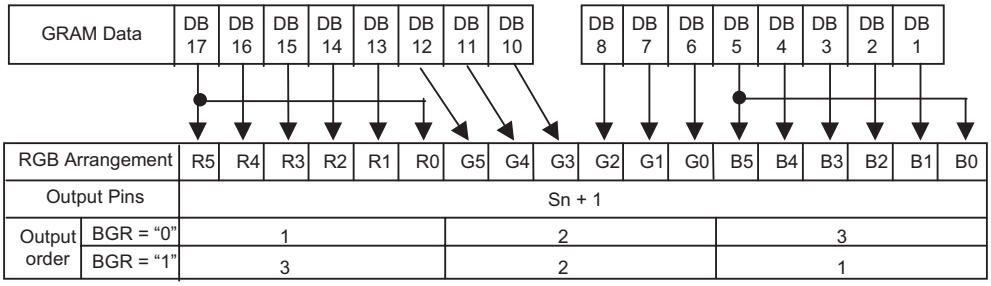
Relation between GRAM data and Display contents (SS = “1”)

80-system 18-bit interface



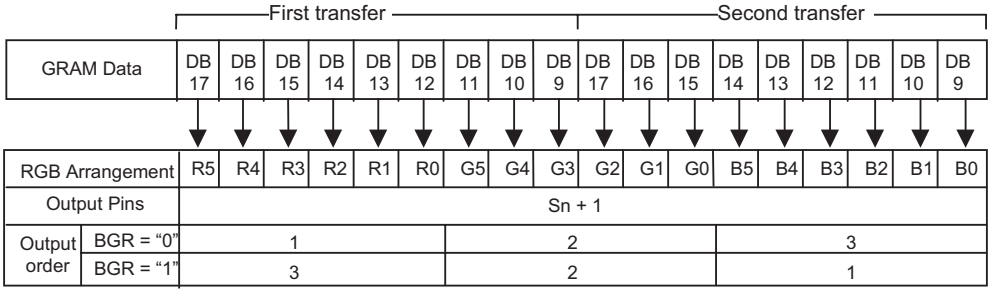
Note: n = lower eight bit of address (255 to 0)

80-system 16-bit interface



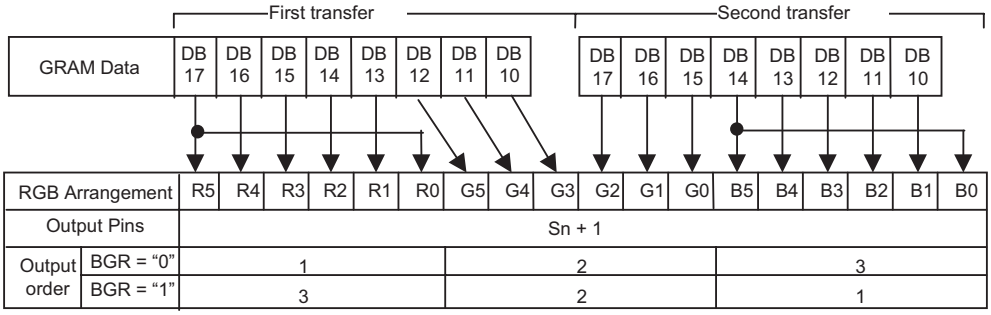
Note: n = lower eight bit of address (255 to 0)

80-system 9-bit interface



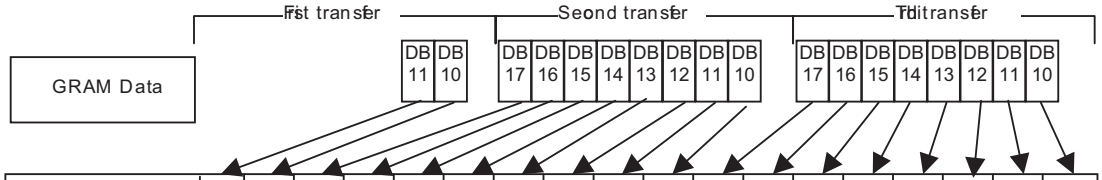
Note: n = lower eight bit of address (255 to 0)

80-system 8-bit interface (1) (Two timas transfer/pixel)



Note: n = lower eight bit of address (255 to 0)

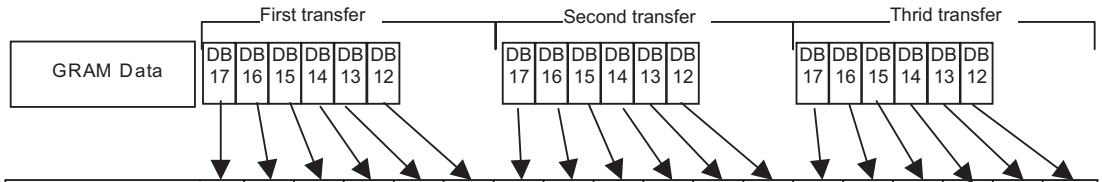
80-system 8-bit interface (2) (Three timas transfer/pixel)



RGB Arrangement		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins		Sn + 1																	
Output order	BGR = "0"	1						2						3					
	BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

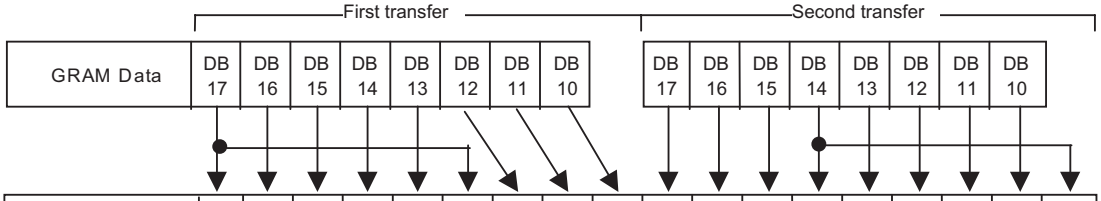
80-system 8-bit interface (3) (Three timas transfer/pixel)



RGB Arrangement		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins		Sn + 1																	
Output order	BGR = "0"	1						2						3					
	BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

SPI (Two times transfer/pixel)



RGB Arrangement		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins		Sn + 1																	
Output order	BGR = "0"	1						2						3					
	BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

18-bit RGB interface

GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1	PD 0
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

16-bit RGB interface

GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 11	PD 10	PD 9	PD 8	PD 7	PD 6	PD 5	PD 4	PD 3	PD 2	PD 1
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

6-bit RGB interface

	First transfer						Second transfer						Third ransfer					
GRAM Data	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12	PD 17	PD 16	PD 15	PD 14	PD 13	PD 12
RGB Arrangement	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Output Pins	Sn + 1																	
Output order BGR = "0"	1						2						3					
Output order BGR = "1"	3						2						1					

Note: n = lower eight bit of address (255 to 0)

Instructions

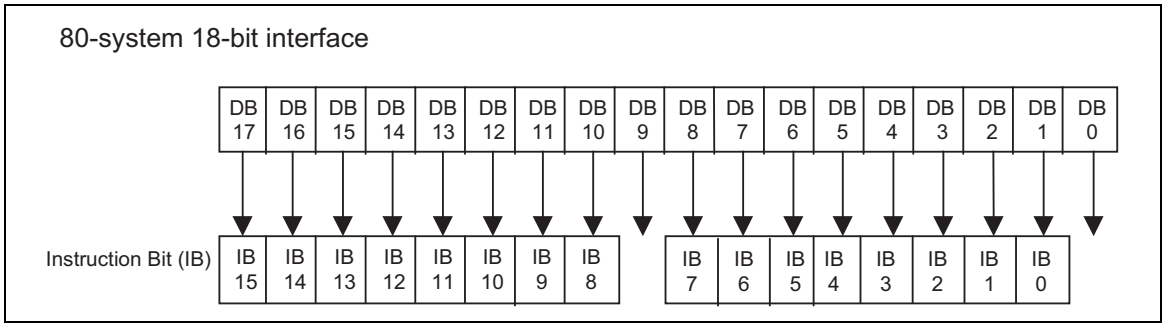
Outline

The HD66776 has an 18-bit bus architecture. Before the internal operation of the HD67766 starts, control information is temoralily sotred in the registers descreibed below to allow high-speed interfaceing with a high-performance microcomputer. The internla operation of the HD66776 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/”), and the internal 16-bit data bus signals (DB15 to DB0), make up the HD6776 instructions. The accesses to the GRAM use the internal 180bit data bus. There are nine categories of instructions.

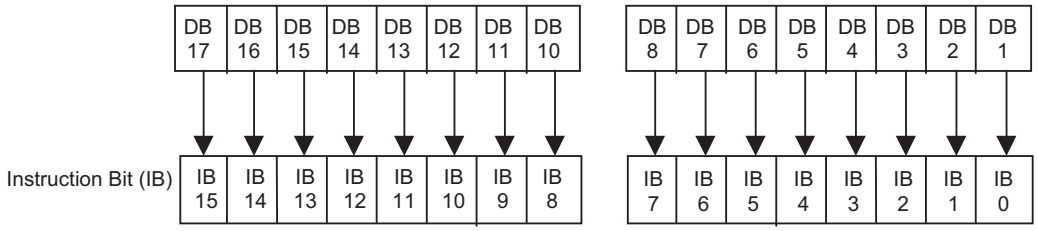
- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale γ-adjustment
- Interface with the gate driver and power supply IC

Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can reduce the amount of transferred data and lighten the microcomputer program load with the window address function.

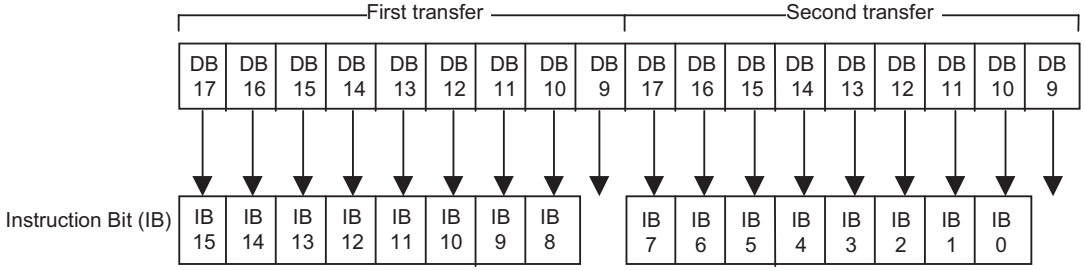
The 16-bit instruction assignments (IB15-0) differ according to the interface as is shown below. Issuing of instructions should be in accord with the data format in use.



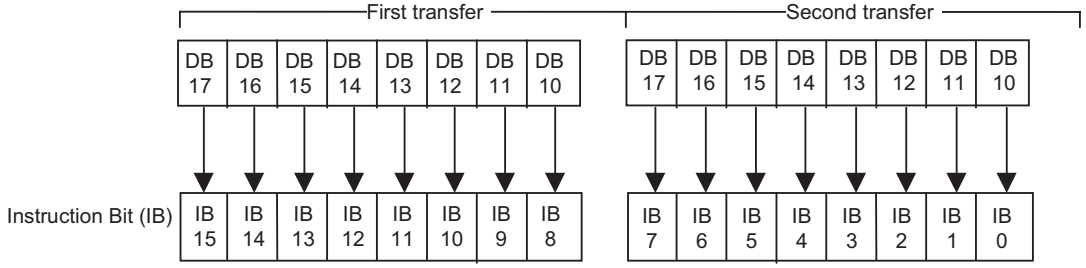
80-system 16-bit nterface



80-system 9-bit nterface



80-system 8-bit nterface



Instruction Description

Ensure that you are aware of the assignments of instruction bits (IB15-0) for each interface that are illustrated below.

General Settings

Index

The index instruction specifies the RAM control indexes (R000h to R40Fh). It sets the register number in the range of “00000000000” to “10000001111” in binary form. Those instruction bits of the index register which are not allocated to the index register should not be accessed.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	ID10	ID9	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Start Oscillation (R000h)

The start oscillation instruction restarts the oscillator from the halt state in the standby mode. After issuing this instruction, wait at least 10 ms for oscillation to stabilize before issuing the next instruction. (See the Standby Mode section.)

If this register is read forcibly, 0776H is read.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	0

Driver Output Conrol (R001h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SS	0	0	NL5	NL4	NL3	NL2	NL1	NL0

SS: Selects the output shift direction of the source driver. When SS = 0, the sequence is from S1 to S256. When SS = 1, the sequence is from S256 to S1. In addition, SS and BGR bits should be specified when the bit order for R, G, and B are changed. When BGR = 0, the output order is R, G, and B. When BGR = 1, the output order is R, G, and B. Rewrite data to the RAM whenever you change the SS and BGR bits.

NL5-0: Specify the number of raster–rows to be driven. The number is adjusted in units of eight. Mapping of addresses in the GRAM is independent of this setting. The selected size should be larger than the panel to be driven.

NL Bits

NL5	NL4	NL3	NL2	NL1	NL0	Display Size	LCD Raster-Rows
0	0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	0	1	256 x 16 dots	16
0	0	0	0	1	0	256 x 24 dots	24
0	0	0	0	1	1	256 x 32 dots	32
0	0	0	1	0	0	256 x 40 dots	40
0	0	0	1	0	1	256 x 48 dots	48
0	0	0	1	1	0	256 x 56 dots	56
0	0	0	1	1	1	256 x 64 dots	64
0	0	1	0	0	0	256 x 72 dots	72
			. . .			. . .	. . .
1	0	0	0	1	0	256 x 280 dots	280
1	0	0	0	1	1	256 x 288 dots	288
1	0	0	1	0	0	256 x 296 dots	296
1	0	0	1	0	1	256 x 304 dots	304
1	0	0	1	1	0	256 x 312 dots	312
1	0	0	1	1	1	256 x 320 dots	320

Note: A front porch period (set in the FP register) and back porch period (set in the BP register) will respectively be inserted as blank periods (all gates output Vgoff level) before and after the driver scans through all of the gates.

LCD-Driving-Waveform Control (R002h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

B/C: When B/C = “0”, a frame-AC waveform is generated and the LCD-driving signal alternates frame by frame. When B/C = “1”, an n-raster-row AC waveform is generated and its polarity alternates on each raster-row specified by bits EOR and NW5–NW0 of the LCD-driving-waveform control register. For details, see the section on the n-raster-row reversed AC drive.

EOR: When the C-pattern waveform is set (B/C = “1”) and EOR = “1”, the odd/even frame-select signals and the n-raster-row reversed signals are EORed for alternating drive. EOR is used when the LCD is not alternated the set values of the LCD drive duty ratio and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows n that will alternate at the C-pattern waveform setting (B/C = "1"). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Entry Mode (R003h)

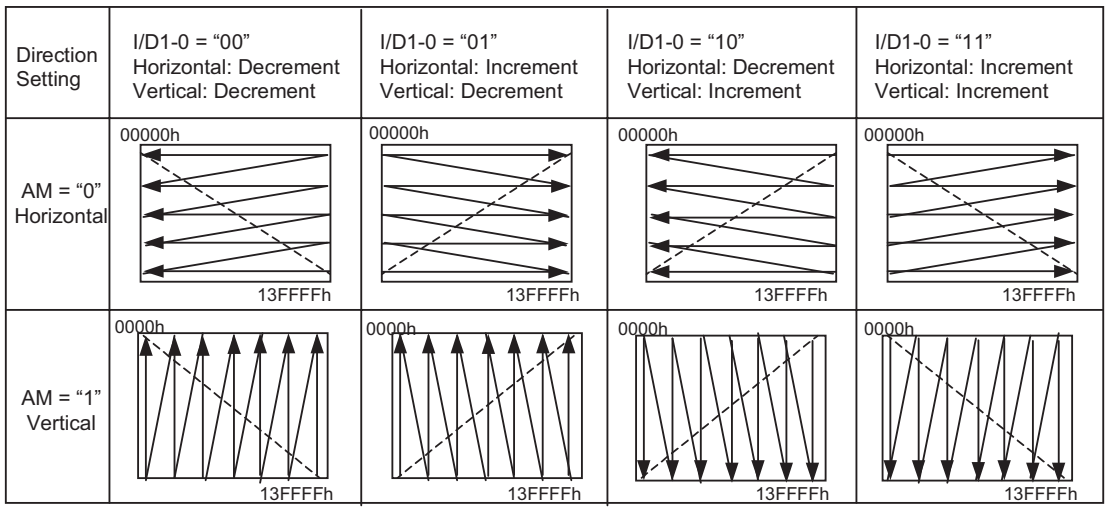
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DEM	0	BGR	0	0	HWM 1	HWM 0	0	0	I/D 1	I/D 0	AM	0	0	0

The write data sent from the microcomputer is modified in the HD66776 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

HWM1-0: When HWM=11, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to RAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see High-Speed RAM Write Mode section.

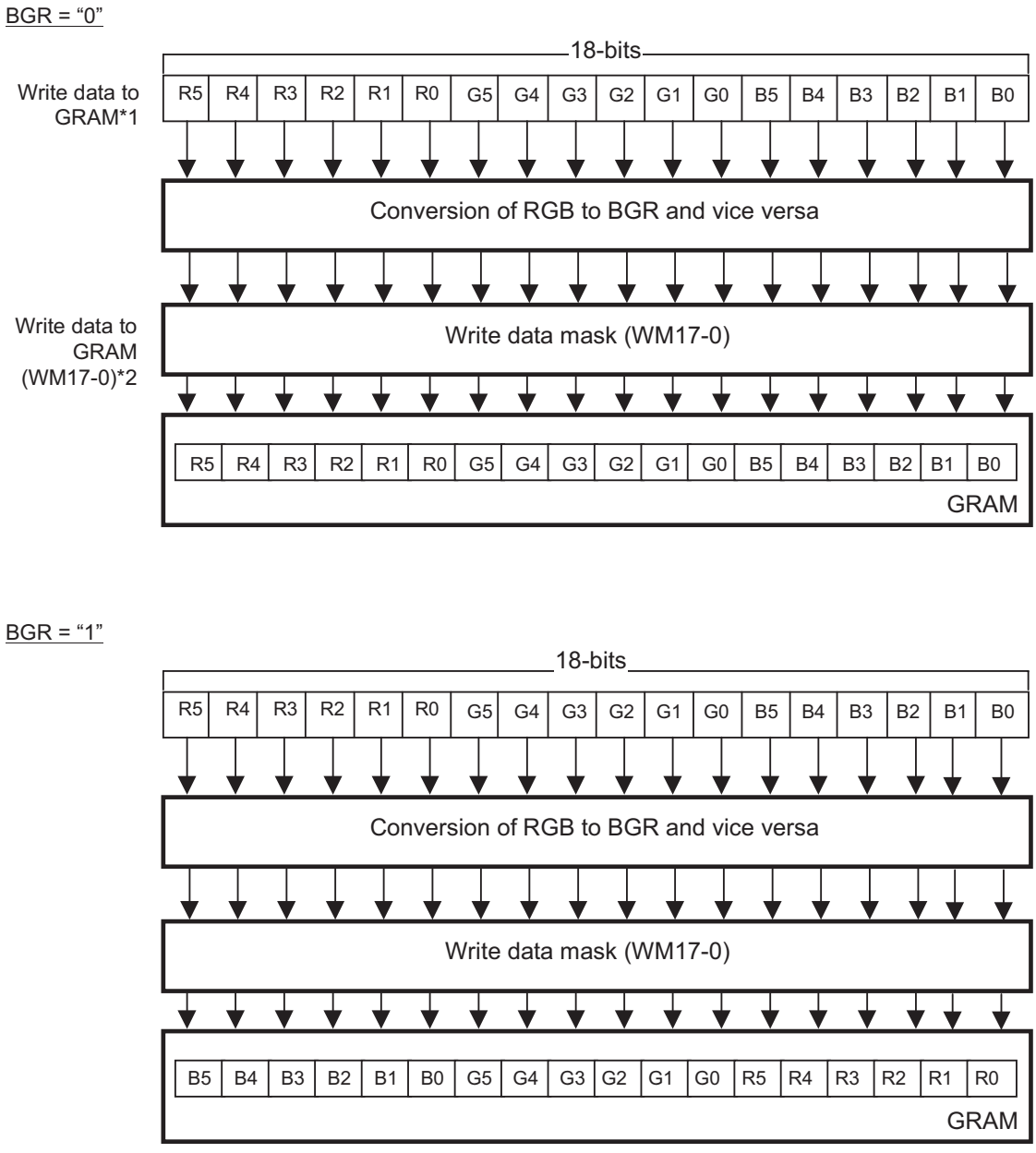
I/D1-0: When I/D1-0 = "1", the address counter (AC) is automatically incremented by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decremented by 1 after the data is written to the GRAM. The increment/decrement setting of the address counter by I/D1-0 is done independently for the upper (AD16-8) and lower (AD7-0) addresses. The direction of moving through the addresses when the GRAM is written to is set by the AM bit.

AM: Sets the automatic update method of the AC after the data is written to the GRAM. When AM = "0", the data is continuously written horizontally. When AM = "1", the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.



Address direction setting

BGR: In the writing of 18 bits of data to RAM, this bit may be used to reverse the bit order from R, G, and B to B, G, and R. Please be aware that setting BGR to 1 will convert the order of the CP17-0 and WM17-0 bits in the same way.



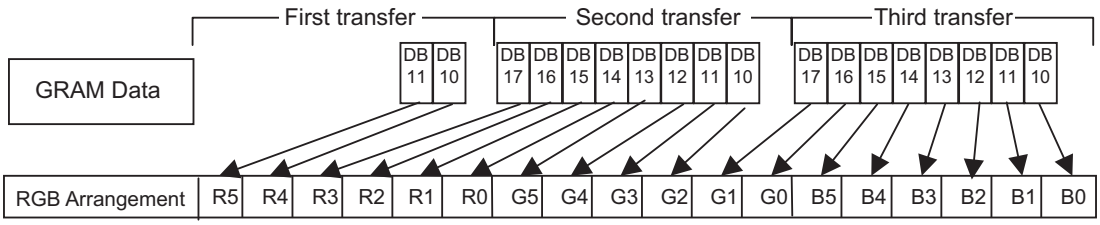
Note1: Data is written to the GRAM in 18-bit units. Logical and compare operations are also performed in 18-bit units. For bit assignment for each interface, see the section parallel transfer.

Note2: The write data mask (WM17-0) is set by the register in the RAM write data mask section.

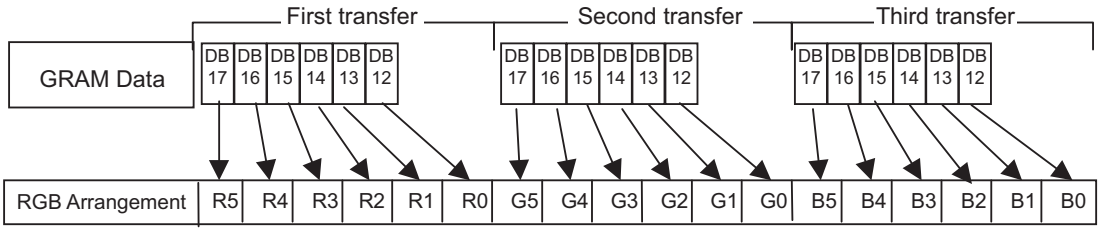
TRI: Set transforming method for 80 system 8-bit bus interface.

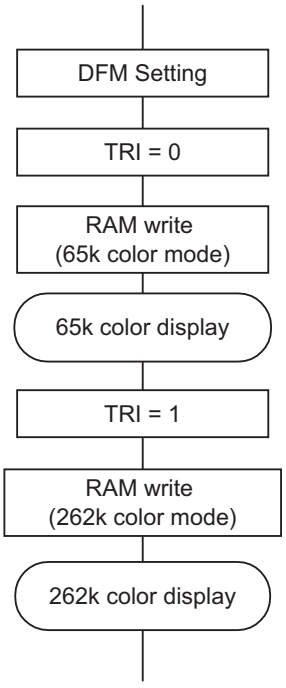
DFM: Set data format of TRI = “1” for 80 system 8-bit bus interface.

TRI = "1", DFM = "0"



TRI = "1", DFM = "1"





Pin setting (8-bit two times transfer/three times transfer)
IM3 =GND
IM2 =GND
IM1 =Vcc
IM0 = Vcc

Note
1.Setting Index and Common are two-times transfer no matter if it is set as three-times transfer mode.
2.It does not read data when it is set as three-times transfer mode.

8-bit two-times transfer/three-times transfer setting flow

Display Control (1) (R007h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	COL	0	0	0	0	VLE2	VLR1	SPT	PT1	PT0	GON	DTE	0	REV	D1	D0

VLE2–1: When VLE = “1”, the first screen is vertically scrolled. When VLE2 = “1”, the 2nd screen is vertically scrolled.

Note: This function is not available when the external display interface is in use. When using an external display interface, VLE2-1must be set to “00”.

VLE Bits

VLE2	VLE1	Image on 1st Screen	Image on 2nd Screen
0	0	Stationary	Stationary
0	1	Stationary	Scrolled
1	0	Scroll	Stationary
1	1	Scroll	Scroll

COL: When COL = “1”, selects the eight color display mode. For details, see the section on the eight-color dipslay mode.

CL Bits

COL	Number of Colors
o	262,144
1	8

SPT: SPT = “1” selects the two-division driving of the LCD. For details, see the section on the screen-division driving function.

Note: This function is not available when the external display interface is in use. When using an external display interface, SPT must be set to “0”.

REV: REV = 1 selects the inversion of the display of all characters and graphics. For details, see the section on the inverted display function. Making it possible to invert the grayscale levels allows the display of the same data on both normally white and normally black panels.

The output on the source lines during the periods of the front and back porch and blanking of the partial display is determined by PT1-0.

REV	GRAM Data	Source Output in the Display Area*	
		Positive Polarity	Negative Polarity
0	18'h00000	V63	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V63
1	18'h00000	V0	V63
	⋮	⋮	⋮
	18'h3FFFF	V63	V0

Note: The output on the source lines during the periods of the front and back porch and blanking of the partial display is determined by PT1-0.

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven. For details, see the section on screen-division driving function.

PT Bits

PT1	PT0	Source Output for Non-Display Area		DISPTMG Output for Non-Display Area
		Positive Polarity	Negative Polarity	
0	0	V63	V0	Normal Drive
0	1	V63	V0	"Low"
1	0	GND	GND	"Low"
1	1	High impedance	High impedance	"Low"

GON: When GON = "0", the gate-off level and Vcom level will be GND.

DTE: When DTE = "0", the DISPTMG output will be fixed to GND.

DTE Bits

DTE	DISPTMG Output
0	Halt (GND)
1	Operation (Vcc/GND)

D1–0: The display is on when D1 = 1 and off when D1 = 0. When the display is off, the data for display is retained in the GRAM, and can instantly be redisplayed by setting D1 = 1. When D1 is 0 (i.e., the display is off) all of the source outputs are set to the GND level. This allows the HD66776 to control the charging current for the LCD during AC driving. When D1–0 = 01, the internal display operations of the HD66776 continue although the actual display is off.

When D1-0 = 00, the internal display operations halt and the display is also switched off. These bits, in combination with GON and DTE, control the display. For details, see the section on the flow for setting instructions.

D1-0 Bits

D1	D0	Source Output	HD67776 Internal Operations	Power supply IC and LCD panel Control Signals (FLM, SFTCLK1/2, CLA/B/C, DCCLK, EQ)
0	0	GND	Halt	Halt
0	1	GND	Operate	Operate
1	0	Unlit display	Operate	Operate
1	1	Display	Operate	Operate

Note: Data can be written to the GRAM from the microcomputer regardless of the contents of D1-0.

Note: The GON bit is used to set the power supply IC. Control by the power supply is according to this bit's value. For details, see the data sheet for the power supply IC.

Display Control 2 (R008h)

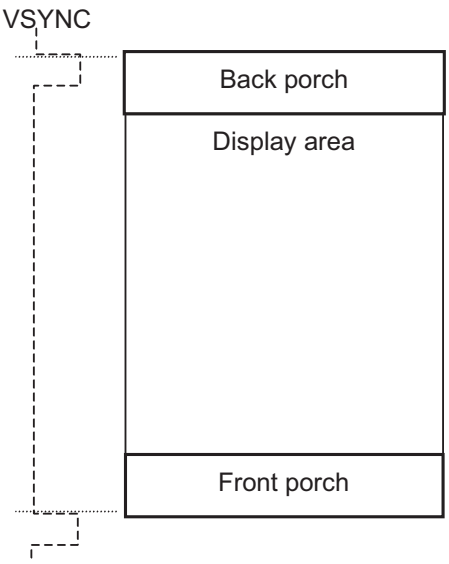
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

FP3-0/BP3-0: Set the periods of blanking (the front and back porch), which are placed at the beginning and end of the display. FP3-0 are for a front porch and BP3-0 are for a back porch.

When the external display interface is in use, the front porch (FP) will start on the falling edge of the VSYNC signal and display operation commences at the end of the front-porch period. The back porch (BP) will start when data for the number of raster-rows specified by the NL bits has been displayed. During the period between the completion of the back-porch period and the next VSYNC signal, the display will remain blank.

FP and BP Bits

FP3	FP2	FP1	FP0	Number of Raster Periods in the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of Raster Periods in the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
	.			.
	.			.
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	Setting disabled



Note: The output timing to LCD panels displayed two raster-rows after the input synchronization signal.

Instruction for setting BP/FP

Set BP and FP within the range indicated below.

Internal clock operation	BP >= 2 lines	FP >= 2 lines	FP + BP <= 16 lines
RGB interface	BP >= 2 lines	FP >= 2 lines	FP + BP <= 16 lines
VSYNC interface	BP >= 2 lines	FP >= 2 lines	FP + BP = 16 lines

Gate Driver Interface Control (R00Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0
R	1	0	0	0	0	0	0	0	TE	0	0	0	0	0	IDX2	IDX1	IDX0

IDX2-0: Index bits that select instructions for the gate-driver/power-supply IC. The instruction that corresponds to the setting made here is transferred, with the index, to the gate-driver/power-supply IC via the serial interface. These instructions are transferred in bit rows as shown below. The upper 3 bits correspond to IDX2-0. The IDX2-0 setting at the time of transfer selects the instruction for the gate-driver/power-supply IC as listed below.

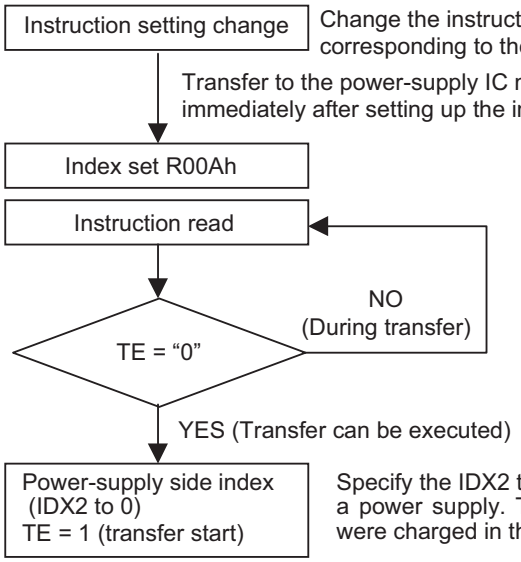
To change an instruction setting on the gate-driver/power-supply IC, first change the instruction bit on the HD66776, select the instruction, which includes the changed instruction bit, from the list below, by setting IDX2-0 as required. The instruction is transferred to the gate-driver/power-supply IC as the transfer starts (TE=1), and is the executed**.**

TE: Serial transfer enable for the gate-driver/power-supply IC. When TE=0, serial transfer is possible. Do not change the instruction during transfer. When TE=1, transfer starts. TE returning to 0 indicates the end of the transfer. Note that, serial transfer to the gate-driver/power-supply IC requires 18 clock cycles at most. Do not change the instruction during the transfer.

* New instructions should be transferred to the gate-driver/power-supply IC soon after they have been set on the HD66776.

HD667P20 Instruction chart

IDX2	IDX1	IDX0	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	GON	VCOMG	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP
0	0	1	0	(VRL3)0	VRL2	VRL1	VRL0	PON	VRH3	VRH2	VRH1	VRH0	VC2	VC1	VC0
			0	(VRL3)1	0	0	DK0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	VDV4	VDV3	VDV2	VDV1	VDV0	VCM4	VCM3	VCM2	VCM1	VCM0
0	1	1	Setting inhibited												
1	0	0	Setting inhibited												
1	0	1	Setting inhibited												
1	1	0	Setting inhibited												
1	1	1	0	0	VGL4	VGL3	VGL2	VGL1	VGL0	0	VGH4	VGH3	VGH2	VGH1	VGH0



Power supply IC interface: Serial transfer sequence

Notes 1: Transfer to the power-supply IC must take place immediately after setting up the instruction.

2: The serial transfer period takes a maxim of 1/fosc x 18clock cycles (sec).

3: Serial transfer cannot be executed in standby mode. If the chip enters standby mode during transfer, the serial transfer is forcibly suspended. Transfer must be executed again because correct transfer, tis not guaranteed in this situation.

4: Serial transfer can be forcibly suspended by writing TE = 0. Transfer must be executed again because correct transfer is not guaranteed in this situation.

5. Do not enter standby mode during transfer forcibly terminate transfer except incase of emergency. Before executing, confirm that the transfer is completed.

External Display Interface Control 1) (R00Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1–0: Specify the RGB I/F mode when the RGB interface is used. Specifically, this setting specifies the mode when the bits of DM and RM are set to RGBI/F. These bits should be set before display operation through the RGB I/F and should not be set during operation.

RIM Bits

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one-time transfer/pixel)
0	1	16-bit RGB interface (one-time transfer/pixel)
1	0	6-bit RGB interface (three-time transfers/pixel)
1	1	Setting disabled

DM1–0:.Specify the display operation mode. The interface can be set based on the bits of DM1-0. This setting enables switching interfaces between internal operation and the external display interface. Switching between two external display interfaces (RGB-I/F and VSYNC-I/F) should not be done.

DM Bits

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Specifies the interface for RAM accesses. RAM accesses can be performed through the interface specified by the bits of RM1-0. When the display data is written via the RGB-I/F, 1 should be set. This bit and the DM bits can be set independently. The display data can be rewritten via the system interface by clearing this bit while the RGB interface is used.

RM Bits

RM	Interface for RAM Access
0	System interface/VSYNC interface
1	RGB interface

Depending on the external display interface settings, different interfaces for use can be specified to match the displaying state. While displaying moving pictures (RGB-I/F/VSYNC-I/F), the data for display can be written in high-speed write mode (HWM = “11”), which achieves both low power consumption and high-speed access.

Display state and interfaces

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still pictures	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving pictures	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying moving pictures.	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving pictures	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1:The instruction register can only be set through the system interface.
2:Switching between RGB-I/F and VSYNC-I/F cannot be done.
3:The RGB-I/F mode should not be changed during RGB I/F operation.
4:For the transition flow for each operation mode, see the External Display Interface section.
5:RGB-I/F and VSYNC-I/F should be used in high-speed write mode (HWM1-0 = “11”).

Internal clock operation mode

All the display operations are controlled by signals generated by the internal clock in internal clock operation mode. All inputs through the external display interface are invalid. The internal RAM can be accessed only via the system interface.

RGB interface mode (1)

The display operations are controlled by the frame synchronization clock (VSYNC), raster-row synchronization signal (VSYNC), and dot clock (DCLK) in RGB interface mode. These signals should be supplied during display operation in this mode. The display data is transferred to the internal RAM via PD17-0 for each pixel. Combining the function of the high-speed write mode and the window address enables display of both the moving picture area and the internal RAM area simultaneously. In this method, data is only transferred when the screen is updated, which reduces the amount of data transferred. The periods of the front (FP) and back (BP) porch and the display are automatically generated in the HD66776 by counting the raster-row synchronization signal (HSYNC) based on the frame synchronization signal (VSYNC). When pixel data is transferred via PD 17 to 0, the transfer should be operated according to the settings above.

RGB interface mode (2)

When RGB-I/F is in use, data can be written to RAM via the system interface. This write operation should be performed while data for display is not being transferred via RGB-I/F (ENABLE = High). Before the next data transfer for display via RGB-I/F, the setting above should be changed, and then the address and index (R202h) should be set.

VSYNC interface mode

The internal display operation is synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When data is written to the internal RAM with the required speed after the falling edge of VSYNC, moving pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface. In VSYNC-I/F mode, only the VSYNC input is valid. The other input signals for the external display interface are invalid. The periods of the front porch (FP), back porch (BP), and display period (NL) are automatically generated by the frame synchronization signal (VSYNC) according to the settings of the HD66776 registers.

Frame Cycle Control (1) (R00Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVI 1	DIVI 0	0	0	0	RTNI 4	RTNI 3	RTNI 2	RTNI 1	RTNI 0

RTNI4-0: Set the 1H period (1 raster-row).

DIVI1-0: Set the division ratio of clocks for internal operation (DIVI1-0). Internal operations are driven by clocks, which are frequency divided according to the DIVI1-0 setting. Frame frequency can be adjusted along with the 1H period (RTNI4-0). When changing the number of raster-rows, adjust the frame frequency. For details, see the frame frequency adjustment Function section.

RTNI Bits and Clock Cycles

RTNI4	RTNI3	RTNI2	RTNI1	RTNI0	Clock number for one line
0	0	0	0	0	Setting disabled
		⋮			
0	1	1	1	1	
1	0	0	0	0	16 clock
1	0	0	0	1	17 clock
1	0	0	1	0	18 clock
		⋮			
1	1	1	1	0	30 clock
1	1	1	1	1	31 clock

DIVI Bits and Clock Frequency

DIVI1	DIVI0	Division Ratio	Internal Operating Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

* fosc = R-C oscillation frequency

Formula for the frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line + FP + BP)}} \text{ [Hz]}$$

fosc: R-C oscillation frequency
Line: number of driven raster-rows (NL bit)
FP: Front porch
BP: Back porch
Division ratio: DIVI bit
Clock cycles per raster-row: RTNI bit

External Display Interface Control (2) (R00Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	DIVE 1	DIVE 0	RTNE 7	RTNE 6	RTNE 5	RTNE 4	RTNE 3	RTNE 2	RTNE 1	RTNE 0

RTNE7-0: Sets the 1H period (1-raster-row). Sets DOTCLK for 1H divided by division ratio.

RTNE7	RTNE6	RTNE5	RTNE4	RTNE3	RTNE2	RTNE1	RTNE0	Number of Clock for 1 period
0	0	0	0	0	0	0	0	Setting inhibited
				:				
				:				
0	0	0	0	1	1	1	1	
0	0	0	1	0	0	0	0	16 clock
0	0	0	1	0	0	0	1	17 clock
0	0	0	1	0	0	1	0	18 clock
				:				:
				:				:
1	1	1	1	1	1	1	0	254 clock
1	1	1	1	1	1	1	1	255 clock

DIVE1-0: Set the internal division ratio of DOTCLK clocks (DIVE1-0). Internal operations are driven by clocks which frequency are divided according ot the DIVE1-0.

DIVE1	DIVE0	Division Ratio	Frequency of internal DOTCLK	
			18/16 bit RGB interface	6 bit RGB interface
0	0	2	Setting inhibited	Setting inhibited
0	1	4	fdotclk ÷ 4	fdotclk ÷ 12
1	0	8	fdotclk ÷8	fdotclk ÷24
1	1	16	fdotclk ÷16	fdotclk ÷48

* fdotclk : R-C oscillation frequency

External Display Interface Control (3) (R00Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	VSPL	HSPL	VPL	EPL	DPL

DPL: Sets the signal polarity of DOTCLK pin.
DPL = “0”: Read data at rising edge of DOTCLK.
DPL = “1”: Read data at falling edge of DOTCLK.

EPL: Sets the signal polarit of ENABLE pins.
EPL = “0”: When ENABLE =”low”, it is available to write data of PD17-0.
When ENABLE = “high”, it is not available to write data of PD17-0.
EPL = “1”: When ENABLE = “high”, it is available to write data of PD17-0.
When ENBALE = “low”, it is not available to write data of PD17-0.

VPL: Sets te signal polarity of VLD pin.
VPL = “0”: When VLD = “Low”, RAM writing is available.
When VLD = “High”, RAM writing is not available.
VPL = “1”: When VLD = “high”, RAM writing is available.
When VLD =”low”, RAM writing is not available.

HSPL: Sets the signal polarity of HSYNC pin.
HSPL = “0”: “Low” is active.
HSPL = “1”: “High” is active

VSPL: Set the signal polarity of VSYNC pin.
VSPL = “0”: “Low” is active.
VSPL = “1”: “High” is active.

LTPS Interface Control (1) (R010h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	FWI5	FWI4	FWI3	FWI2	FWI1	FWI0	0	0	0	0	0	FTI2	FTI1	FTI0

FTI2-0: Defines the FLM rising position.

FWI5-0: Sets the "High" width of FLM.

FTI2	FTI1	FTI0	FLM rising position
0	0	0	0 clock
0	0	1	0.5 clock
0	1	0	1 clock
0	1	1	1.5 clock
1	0	0	2.0 clock
1	0	1	2.5 clock
1	1	0	3 clock
1	1	1	3.5 clcok

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

FWI5	FWI4	FWI3	FWI2	FWI1	FWI0	FLM "High" period
0	0	0	0	0	0	0 clock
0	0	0	0	0	1	0.5 clock
0	0	0	0	1	0	1 clock
0	0	0	0	1	1	1.5 clock
0	0	0	1	0	0	2 clock
0	0	0	1	0	1	2.5 clock
0	0	0	1	1	0	3 clock
0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	31.5 clock

LTPS Interface Control (2) (R011h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	SWI5	SWI4	SWI3	SWI2	SWI1	SWI0	0	0	0	0	0	STI2	STI1	STI0

STGI2-0: Defines the SFTCLK1 and 2 rising position.

SWI5-0: Sets the "High" width of SFTCLK1 and 2.

STI2	STI1	STI0	SFTCLK rising position
0	0	0	0 clock
0	0	1	0.5 clock
0	1	0	1.0 clock
0	1	1	1.5 clock
1	0	0	2.0 clock
1	0	1	2.5 clock
1	1	0	3 clock
1	1	1	3.5 clcok

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

SWI5	SWI4	SWI3	SWI2	SWI1	SWI0	SFTCLK "High" period
0	0	0	0	0	0	0 clock
0	0	0	0	0	1	0.5 clock
0	0	0	0	1	0	1 clock
0	0	0	0	1	1	1.5 clock
0	0	0	1	0	0	2 clock
0	0	0	1	0	1	2.5 clock
0	0	0	1	1	0	3 clock
0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	31.5 clock

LTPS Interface Control (3) (R012h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	CLWI4	CLWI3	CLWI2	CLWI1	CLWI0	0	0	0	0	CLTI3	CLTI2	CLTI1	CLTI0

CLTI3-0: Defines the CLA rising position.

CLW

CLTI3	CLTI2	CLTI1	CLTI1	CLA rising position
0	0	0	0	Setting disabled
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
0	0	1	1	1.5 clock
0	1	0	0	2.0 clock
⋮	⋮	⋮	⋮	⋮
⋮	⋮	⋮	⋮	⋮
1	1	1	1	7.5 clcok

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

CLWI4	CLWI3	CLWI2	CLWI1	CLWI0	CLA/B/C “High” period
0	0	0	0	0	0 clock
0	0	0	0	1	0.5 clock
0	0	0	1	0	1 clock
0	0	0	1	1	1.5 clock
0	0	1	0	0	2 clock
0	0	1	0	1	2.5 clock
0	0	1	1	0	3 clock
0	0	1	1	1	3.5 clock
:	:	:	:	:	:
:	:	:	:	:	:
1	1	1	1	1	15.5 clock

LTPS Interface Control (4) (R013h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	CLWI4	CLWI3	CLWI2	CLWI1	CLWI0	0	0	0	0	CLTI3	CLTI2	CLTI1	CLTI0

DPTI2-0: Defines the DISPTMG rising position.

DPWI5-0: Sets the "High" width of DISPTMG.

DPTI2	DPTI1	DPTI0	DISPTMG rising position
0	0	0	0 clock
0	0	1	0.5 clock
0	1	0	1.0 clock
0	1	1	1.5 clock
1	0	0	2.0 clock
:	:	:	:
1	1	1	3.5 clcok

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

DPWI5	DPWI4	DPWI3	DPWI2	DPWI1	DPWI0	CLA/B/C "High" period
0	0	0	0	0	0	0 clock
0	0	0	0	0	1	0.5 clock
0	0	0	0	1	0	1 clock
0	0	0	0	1	1	1.5 clock
0	0	0	1	0	0	2 clock
0	0	0	1	0	1	2.5 clock
0	0	0	1	1	0	3 clock
0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	31.5 clock

LTPS Interface Control (5) (R014h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	MCPI2	MCPI1	MCPI0	0	0	0	0	0	0	SHI1	SHI0

SHI1-0: Defines the hold time from the falling edge of CLA/B/C source output.

MCPI2-0: Sets the changing position of AC signal M.

SHI1	SHI0	Source hold time
0	0	0 clock
0	1	0.5 clock
1	0	1.0 clock
1	1	1.5 clock

Note) Setting values above are clocks from the falling edge of CLA, CLB, and CLC signals.

MCPI2	MCPI1	MCPI0	M alternating point
0	0	0	0 clock
0	0	1	0.5 clock
0	1	0	1 clock
0	1	1	1.5 clock
1	0	0	2 clock
1	0	1	2.5 clock
1	1	0	3 clock
1	1	1	3.5 clock

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

LTPS Interface Control (6) (R015h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	EQWI1	EQWI0	0	0	0	0	0	EQTI2	EQTI1	EQTI0

ETQI2-0: Defines the equalize starting position.

EQWI1-0: Sets "High" width of EQ.

EQTI2	EQTI1	EQTI0	Equalize starting position
0	0	0	0 clock
0	0	1	0.5 clock
0	1	0	1.0 clock
0	1	1	1.5 clock
1	0	0	2 clock
1	0	1	2.5 clock
1	1	0	3 clock
1	1	1	3.5 clock

Note) Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

EQWI1	EQWI0	EQ "High" period
0	0	0 clock
0	1	0.5 clock
1	0	1 clock
1	1	1.5 clock

LTPS Interface Control (7) (R016h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	FEW7	FEW6	FEW5	FEW4	FEW3	FEW2	FEW1	FEW0	0	0	0	FTE4	FTE3	FTE2	FTE1	FTE0

FTE4-0: Defines the FLM rising position.

FWE7-0: Sets the "High" width of FLM.

FTE4	FTE3	FTE2	FTE1	FTE0	FLM rising position
0	0	0	0	0	0 clock
0	0	0	0	1	0.5 clock
0	0	0	1	0	1.0 clock
0	0	0	1	1	1.5 clock
0	0	1	0	0	2.0 clock
:	:	:	:	:	:
1	1	1	1	1	15.5 clcok

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2). Numbers in the above chart show the rising position of FLM signal from 0 clock when setting SFTCLK rising point on 0 clock.

FWE7	FWE6	FWE5	FWE4	FWE3	FWE2	FWE1	FWE0	FLM "High" period
0	0	0	0	0	0	0	0	0 clock
0	0	0	0	0	0	0	1	0.5 clock
0	0	0	0	0	0	1	0	1 clock
0	0	0	0	0	0	1	1	1.5 clock
0	0	0	0	0	1	0	0	2 clock
0	0	0	0	0	1	0	1	2.5 clock
0	0	0	0	0	1	1	0	3 clock
0	0	0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	127.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

LTPS Interface Control (8) (R017h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	SWE0	0	0	0	STE4	STE3	STE2	STE1	STE0

STE4-0: Defines the rising position of SFTCLK1, 2.

SWE7-0: Sets the "High" width of SFTCLK1, 2.

STE4	STE3	STE2	STE1	STE0	SFTCLK rising position
0	0	0	0	0	0 clock
0	0	0	0	1	0.5 clock
0	0	0	1	0	1.0 clock
0	0	0	1	1	1.5 clock
0	0	1	0	0	2.0 clock
:	:	:	:	:	:
1	1	1	1	1	15.5 clcok

Note) Numbers in the above chart is the clocks from the reference point.
The reference point is the rising point when setting SFTCLK rising point on 0 clock.

SWE7	SWE6	SWE5	SWE4	SWE3	SWE2	SWE1	SWE0	SFTCLK "High" period
0	0	0	0	0	0	0	0	0 clock
0	0	0	0	0	0	0	1	0.5 clock
0	0	0	0	0	0	1	0	1 clock
0	0	0	0	0	0	1	1	1.5 clock
0	0	0	0	0	1	0	0	2 clock
0	0	0	0	0	1	0	1	2.5 clock
0	0	0	0	0	1	1	0	3 clock
0	0	0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	127.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

LTPS Interface Control (9) (R018h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	CLWE5	CLWE4	CLWE3	CLWE2	CLWE1	CLWE0	0	0	0	CLTE4	CLTE3	CLTE2	CLTE1	CLTE0

CLTE4-0: Defines the CLA rising position.

CLWE5-0: Sets the "High" width of CLA/B/C.

CLTE4	CLTE3	CLTE2	CLTE1	CLTE0	CLA rising position
0	0	0	0	0	0 clock
0	0	0	0	1	0.5 clock
0	0	0	1	0	1.0 clock
0	0	0	1	1	1.5 clock
0	0	1	0	0	2.0 clock
:	:	:	:	:	:
1	1	1	1	1	15.5 clcok

Note) Numbers in the above chart is the clocks from the reference point.
The reference point is the rising point when setting SFTCLK rising point on 0 clock.

CLWE5	CLWE4	CLWE3	CLWE2	CLWE1	CLWE0	CLA/B/C "High" period
0	0	0	0	0	0	0 clock
0	0	0	0	0	1	0.5 clock
0	0	0	0	1	0	1 clock
0	0	0	0	1	1	1.5 clock
0	0	0	1	0	0	2 clock
0	0	0	1	0	1	2.5 clock
0	0	0	1	1	0	3 clock
0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:
:	:	:	:	:	:	:
1	1	1	1	1	1	31.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

LTPS Interface Control (10) (R019h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DPWE7	DPWE6	DPWE5	DPWE4	DPWE3	DPWE2	DPWE1	DPWE0	0	0	0	DPTE4	DPTE3	DPTE2	DPTE1	DPTE0

DPTE4-0: Defines the DISPTMG rising position.

DPWE7-0: Sets the "High" width of DISPTMG.

DPTE4	DPTE3	DPTE2	DPTE1	DPTE0	DISPTMG rising position
0	0	0	0	0	0 clock
0	0	0	0	1	0.5 clock
0	0	0	1	0	1.0 clock
0	0	0	1	1	1.5 clock
0	0	1	0	0	2.0 clock
:	:	:	:	:	:
1	1	1	1	1	15.5 clcok

Note) Numbers in the above chart is the clocks from the reference point.
The reference point is the rising point when setting SFTCLK rising point on 0 clock.

DPWE 7	DPWE 6	DPWE 5	DPWE 4	DPWE 3	DPWE 2	DPWE 1	DPWE 0	DISPTMG "High" period
0	0	0	0	0	0	0	0	0 clock
0	0	0	0	0	0	0	1	0.5 clock
0	0	0	0	0	0	1	0	1 clock
0	0	0	0	0	0	1	1	1.5 clock
0	0	0	0	0	1	0	0	2 clock
0	0	0	0	0	1	0	1	2.5 clock
0	0	0	0	0	1	1	0	3 clock
0	0	0	0	0	1	1	1	3.5 clock
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
1	1	1	1	1	1	1	1	127.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

LPTS Interface Control (11) (R01Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	MCPE3	MCPE2	MCPE1	MCPE0	0	0	0	0	SHE3	SHE2	SHE1	SHE0

SHE3-0: Defines the hold time from the falling edge of CLA/B/C source output.

MCPE3-0: Sets the changing position of AC signal M.

SHE3	SHE2	SHE1	SHE0	Source hold time
0	0	0	0	0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
0	0	1	1	1.5 clock
0	1	0	0	2.0 clock
:	:	:	:	:
1	1	1	1	15.5 clcok

Note) Numbers in the above chart is the clocks from the reference point.
The reference point is the rising point when setting SFTCLK rising point on 0 clock.

MCPE3	MCPE2	MCPE1	MCPE0	M alternating position
0	0	0	0	0 clock
0	0	0	1	0.5 clock
0	0	1	0	1 clock
0	0	1	1	1.5 clock
0	1	0	0	2 clock
:	:	:	:	:
:	:	:	:	:
1	1	1	1	15.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

LTPS Interface Control (12) (R01Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	EQWE3	EQWE2	EQWE1	EQWE0	0	0	0	0	EQTE3	EQTE2	EQTE1	EQTE0

EQTE3-0: Defines the equlize starting position.

EQWE3-0: Sets “High” width of EQ.

EQTE3	EQTE2	EQTE1	EQTE0	Equalize starting position
0	0	0	0	0 clock
0	0	0	1	0.5 clock
0	0	1	0	1.0 clock
0	0	1	1	1.5 clock
1	1	0	0	2.0 clock
:	:	:	:	:
1	1	1	1	7.5 clcok

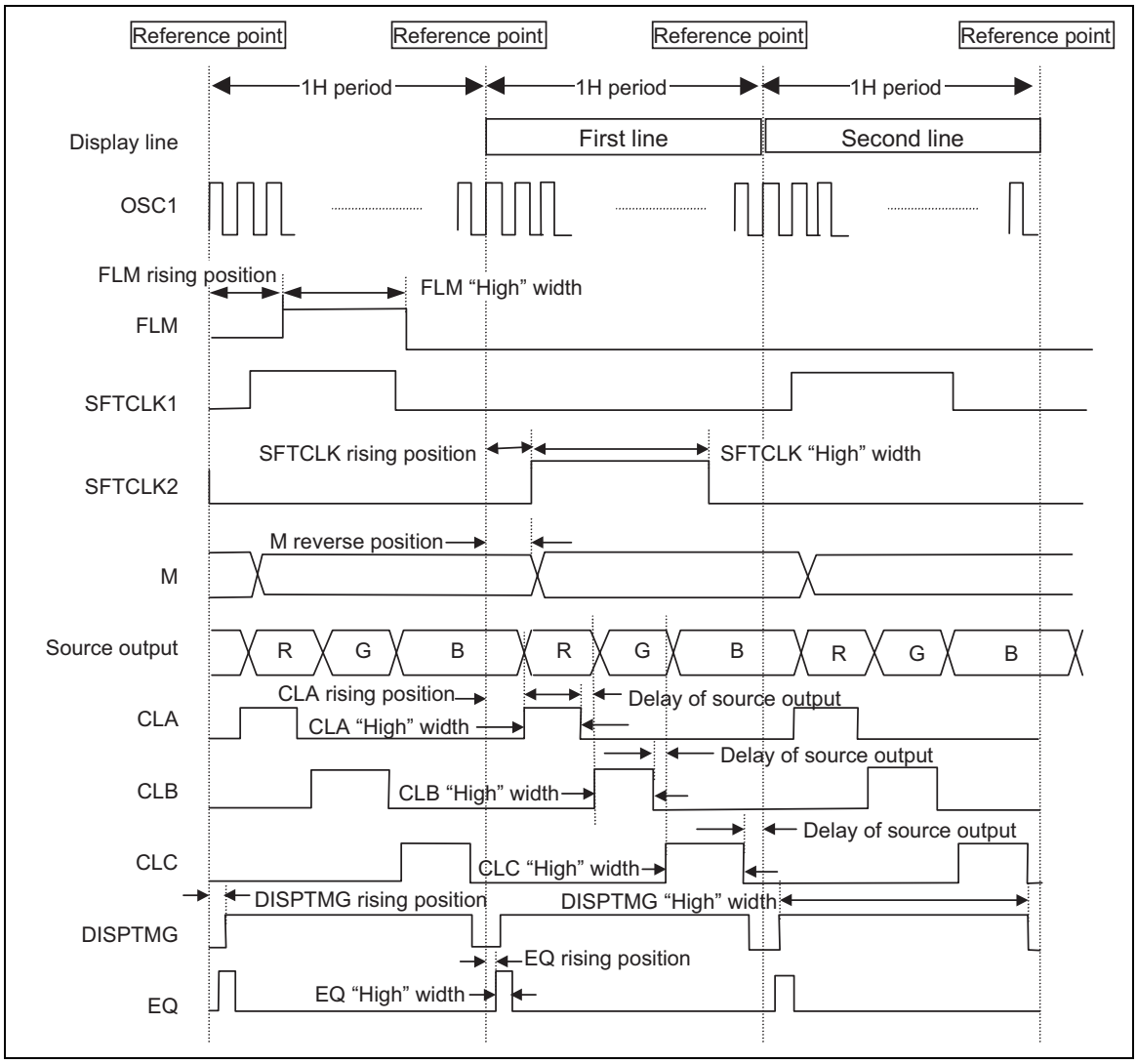
Note) Numbers in the above chart is the clocks from the reference point.
The reference point is the rising point when setting SFTCLK rising point on 0 clock.

MCPE3	MCPE2	MCPE1	MCPE0	M alternating position
0	0	0	0	0 clock
0	0	0	1	0.5 clock
0	0	1	0	1 clock
0	0	1	1	1.5 clock
0	1	0	0	2 clock
:	:	:	:	:
:	:	:	:	:
1	1	1	1	7.5 clock

Note) Number of clock is the setting value of DIVE1 - 0 of external display interface (2).

Specification of LTPS panel control signal

The following is the timing chart of control signal.



Limitations

Internal clock drive mode	Internal clock drive mode
(CLTI) + 3 x (CLWI) + 3 x SHI < (RTNI)	(CLTE) + 3 x (CLWE) + 3 x SHE < (RTNE)
(STI) + (SWI) < (RTNI)	(STE) + (SWE) < (RTNE)
(FTI) + (FWI) < (RTNI)	(FTE) + (FEW) < (RTNE)
(DPTI) + (DPWI) < (RTNI)	(DPTE) + (DPWE) < (RTNE)

Power control system instruction

Power Control 1 (R100h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB	SLP	STB

SLP: When SLP = "1", the HD66776 enters sleep mode, in which the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only serial transfer to a power-supply IC and the following instructions can be executed during sleep mode.

(i) Power control (BS2–0, DC2–0, AP2–0, SLP, STB, VC2-0, CAD, VR3-0, VRL3-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits)
(ii) Common interface control (TE, IDX)

During sleep mode, other GRAM data and instructions cannot be updated, although they are retained.

STB: When STB = "1", the HD66776 enters standby mode, in which display operation completely stops, halting the internal R-C oscillator. In addition, no external clock pulses are supplied. For details, see the Standby Mode section.

Only the following instructions can be executed during standby mode.

(i) Standby mode cancel (STB = "0")
(ii)Start oscillation

During standby mode, serial transfer to the power-supply IC is not possible. Transfer the data again after standby mode is canceled.

DSTB: When DSTB = "1", HD66776 enters deep standby mode. During Deep standby mode, it is more power saving compared to the standby mode, because HD66767switch off the logic power supply dering the standby mode. While it is in deep standby mode, contents of GRAM data and instruction set will be broken. Reset GRAM data and instruction set after deep standby mode is canceled. During deep standby mode, serial transfer to the gate driver is not possible. Transfer the data again after standby mode is canceled.

Note: The SLP bit is for setting the power-supply IC. Control based on the bits' values is executed by the common driver. For details, see the data sheet for the power supply IC.

Power Control 2 (R101h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	DC4	DC3	SAP2	SAP1	SAP0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	0	0

SAP2-0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the LCD. When the amount of fixed current is large,LCD driving capability increases, and it rises picture quality.. But the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption. During operation with no display, when SAP2–0 = 000, the current consumption can be reduced by halting the operational amplifier and step-up circuit operation.

SAP Bits

SAP2	SAP1	SAP0	Op-amp Current
0	0	0	Halt
0	0	1	0.65
0	1	0	0.80
0	1	1	1.00

SAP2	SAP1	SAP0	Op-amp Current
1	0	0	1.35
1	0	1	1.60
1	1	0	Setting disabled
1	1	1	Setting disabled

BT2–0: Switch the output factor for step-up. Adjust scale factor of the step-up circuit to meet the voltage used. Lower amplification of the step-up circuit consumes less current.

DC4-3: Sets frequency of step-up clock DCCLK.

DC4	DC3	DCCLK operation frequency
0	0	fosc ÷ 4
0	1	fosc ÷ 8
1	0	fosc ÷ 16
1	1	fosc ÷ 32

DC2–0: Select the operating frequency for the step-up circuit. When this frequency is high, the driving ability of the step-up circuit and the display quality are high, but the current consumption is increased. Adjust the frequency by considering both the display quality and the current consumption.

AP2–0: Adjust the amount of fixed current from the fixed current source in the operational amplifier for the LCD. When the amount of fixed current is large, the LCD driving ability and the display quality are high, but the current consumption is increased. Adjust the fixed current by considering both the display quality and the current consumption. During operation with no display, when AP2–0 = “000”, the current consumption can be reduced by ending the operational amplifier and step-up circuit operation.

Note: The BS2-0, DC2-0, and AP2-0 bits are for setting the power-supply IC. Control based on the bits’ values in executed by the common driver. For details, see the data sheet for the power supply IC.

Power Control 3 (R102h)
Power Control 4 (R103h)
Power Control 5 (R104h)
Power Control 6 (R105h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	VGL4	VGL3	VGL2	VGL1	VGL0	0	VGH4	VGH3	VGH2	VGH1	VGH0
W	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
W	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VGH4-0: Sets the output level of VGH regulator. It is possible to set 2.82 times to 4.06 times REGP voltage.

VGL4-0: Sets the output level of VGL regulator. It is possible to set –2.26 times to –4.0 times REGP voltage.

VC2-0: Adjust VciOUT output and VREG1OUT input on the basis of Vci.

VRL3: When VRL3 =”0”, sets PON, VRH3-0, and VC2-0 for HD667P20. When VRL3-0 = “1”, sets DK0 for HD667P20.

VRL2: Transferred to a power supply IC. VRL2 is not used in HD667P20.

VRL1: Transferred to a power supply IC. VRL2 is not used in HD667P20.

VRL0: Assigned to DK0 when VRL3=1.

PON: Set operation/stop of VLOUT3. PON = 0 is to stop and PON = 1 is to start operation.

VRH3-0: Sets an amplification factor for VREG1OUT. The amplification factor can be set to 1.25 to 1.90 times the REGP input.

VCOMG: When VCOMG = “1”, instruction (VDV) becomes valid because output level of VcomL can be set to any level. VCOMG = “1” is valid when PON = “1”. When VCOMG = “0”, VcomL is at GND level and setting for instruction (VDV) becomes invalid. When VCOMG = “0”, output of VLOUT 4, a power supply for Vcoml, stops. Set VCOMG according to the sequence of a power supply setting flow because VCOMG setting is related to the power supply starting sequence.

VDV4-0: Sets amplification factors for Vcom and Vgoff while Vcom AC drive is being performed. The amplification factors can be set to 0.6 to 1.25 times the VREG1 input. When Vcom AC drive is not performed, the settings are invalid.

VCM4-0: Sets the VcomH voltage, which is positive when Vcom AC drive is being performed. The amplification factor can be set to 0.41 to 1.00 times the VREG1 input. Setting VCM4-0 to "1" stops the internal resistor adjustment, and the external resistor connected to VcomR can be used to adjust VcomH.

Note: The VGH4-0, VGL4-0, VC2-0, PON, VRH3-0, VCOMG, VDV4-0, and VCM4-0 bits are for the power supply IC. Control according to the bits’ values is executed by the power-supply IC. for details, see the data sheet for the power-supply IC.

RAM access system instruction

RAM Address Set (R200h)
RAM Address Set (R201h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
W	1	0	0	0	0	0	0	0	AD16	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8

AD16–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting the addresses. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in standby mode. Ensure that the address is set within the specified window address. When RGB-I/F is in use (RM = "1"), AD16-0 will be set at the falling edge of the VSYNC signal. When the internal clock operation and VSYNC-I/F (RM = "0") are in use, AD16-0 will be set upon execution of an instruction.

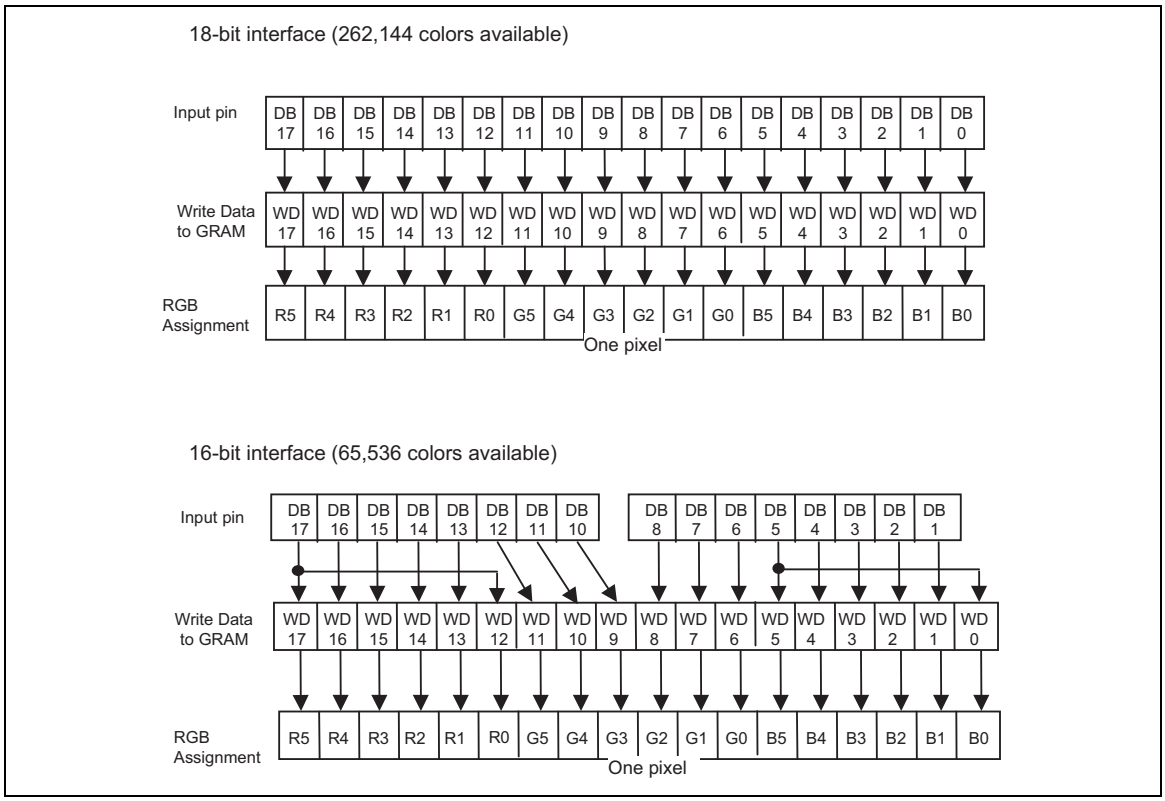
GRAM Address Range

AD16–AD0	GRAM Setting
"00000"H – "000FF"H	Bitmap data for Line 1
"00100"H – "001FF"H	Bitmap data for Line 2
"00200"H – "002FF"H	Bitmap data for Line 3
"00300"H – "003FF"H	Bitmap data for Line 4
:	:
"13C00"H – "13CFF"H	Bitmap data for Line 317
"13D00"H – "13DFF"H	Bitmap data for Line 318
"13E00"H – "13EFF"H	Bitmap data for Line 319
"13F00"H – "13FFF"H	Bitmap data for Line 320

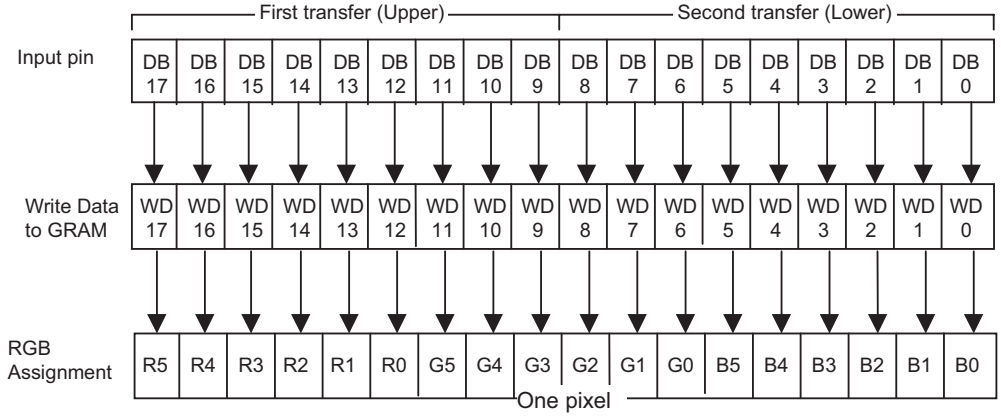
Write Data to GRAM (R202h)

R/W	RS																		
W	1		RAM write data (WD17-0). The pin assignment for DB17-0 varies for each interface (see below)																
		PD17	PD16	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Whe RGB-I/F is in use		WD 17	WD 16	WD 15	WD 14	WD 13	WD 12	WD 11	WD 10	WD 9	WD 8	WD 7	WD 6	WD 5	WD 4	WD 3	WD 2	WD 1	WD 0

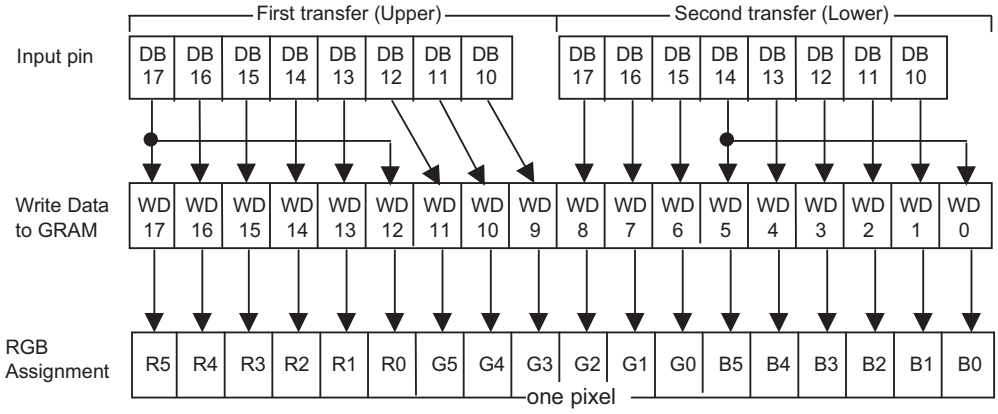
WD17–10: GRAM data is expanded to 18 bits to be written. Please keep in mind that the expansion format varies for each interface. The grayscale level is determined by the GRAM data. The address is automatically updated by the bits of AM and I/D after GRAM writing. GRAM cannot be accessed in standby mode. When the 8- or 16-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the RB data to its LSB. When data is written to RAM used by RGB-I/F via the system interface, please make sure that write data conflicts do not occur. When the 18-bit RGB-I/F is in use, 18-bit data is written to RAM via PD17-0 and 262,144 colors are available. When the 16-bit RGB-I/F is in use, the MSB is written to its LSB and 65,536 colors are available.



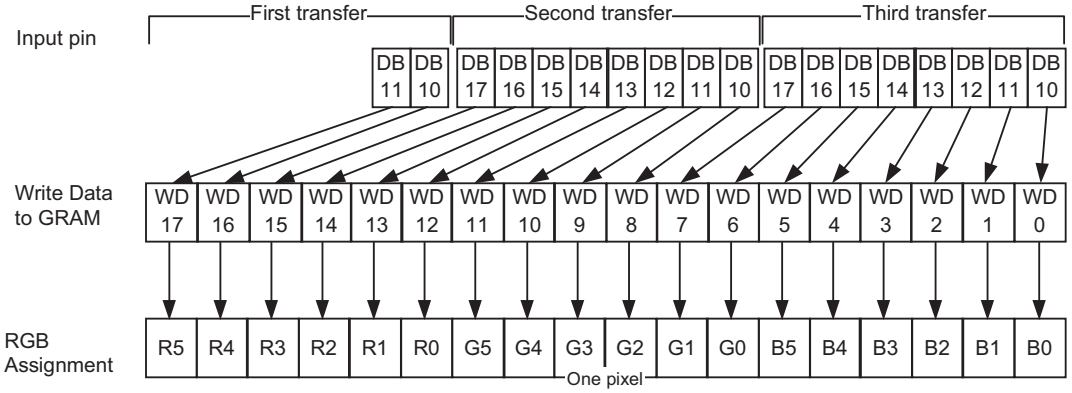
9-bit interface (262,144 colors available)



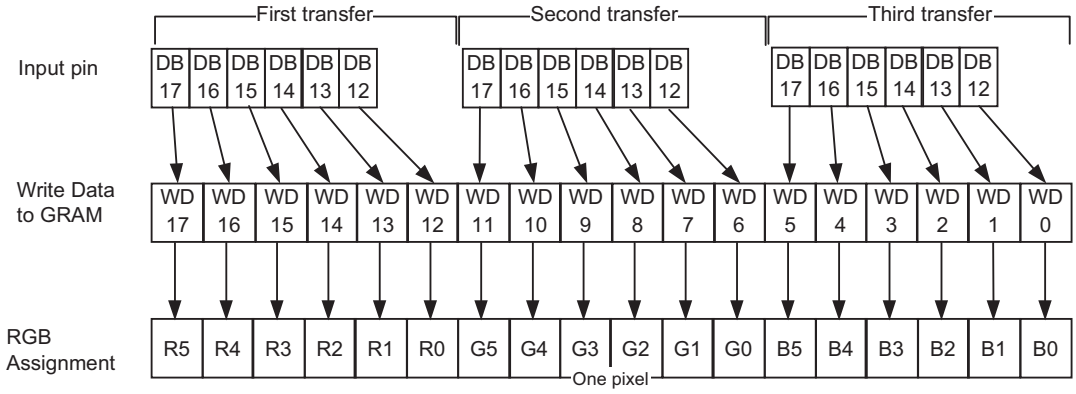
8-bit interface (1) (65,536 colors available)



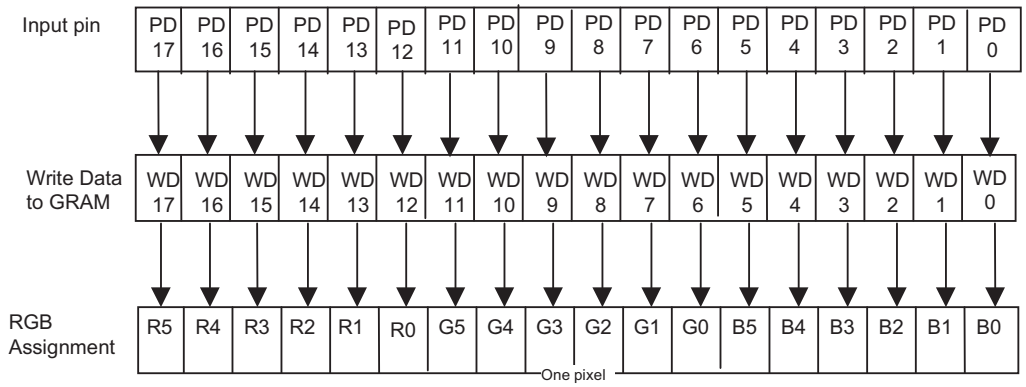
8-bit interfacer (2) (262,144 colors available)



8-bit interfacer (3) (262,144 colors available)

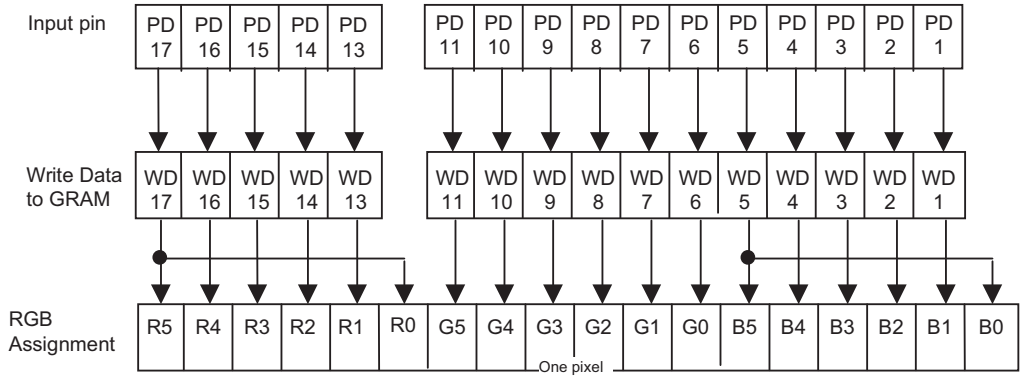


18-bit RGB interface (262,144 colcors available)



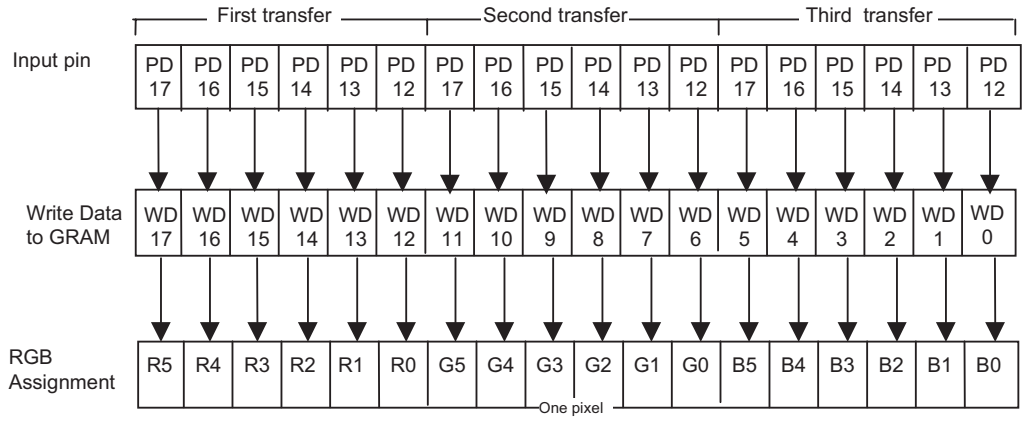
The index register should be set when data for display is written in RGB-I/F.

16-bit RGB interface (65,536 colcors available)



The index register should be set when data for display is written in RGB-I/F.

6-bit RGB interface (262,144 colcors available)



The index register should be set when data for display is written in RGB-I/F.

GRAM Data and LCD Output

REV = 0

GRAM Data Setting	Grayscale Polarity		GRAM Data Setting	Grayscale Polarity	
RGB	Negative	Positive	RGB	Negative	Positive
000000	V0	V63	100000	V32	V31
000001	V1	V62	100001	V33	V30
000010	V2	V61	100010	V34	V29
000011	V3	V60	100011	V35	V28
000100	V4	V59	100100	V36	V27
000101	V5	V58	100101	V37	V26
000110	V6	V57	100110	V38	V25
000111	V7	V56	100111	V39	V24
001000	V8	V55	101000	V40	V23
001001	V9	V54	101001	V41	V22
001010	V10	V53	101010	V42	V21
001011	V11	V52	101011	V43	V20
001100	V12	V51	101100	V44	V19
001101	V13	V50	101101	V45	V18
001110	V14	V49	101110	V46	V17
001111	V15	V48	101111	V47	V16
010000	V16	V47	110000	V48	V15
010001	V17	V46	110001	V49	V14
010010	V18	V45	110010	V50	V13
010011	V19	V44	110011	V51	V12
010100	V20	V43	110100	V52	V11
010101	V21	V42	110101	V53	V10
010110	V22	V41	110110	V54	V9
010111	V23	V40	110111	V55	V8
011000	V24	V39	111000	V56	V7
011001	V25	V38	111001	V57	V6
011010	V26	V37	111010	V58	V5
011011	V27	V36	111011	V59	V4
011100	V28	V35	111100	V60	V3
011101	V29	V34	111101	V61	V2
011110	V30	V33	111110	V62	V1
011111	V31	V32	111111	V63	V0

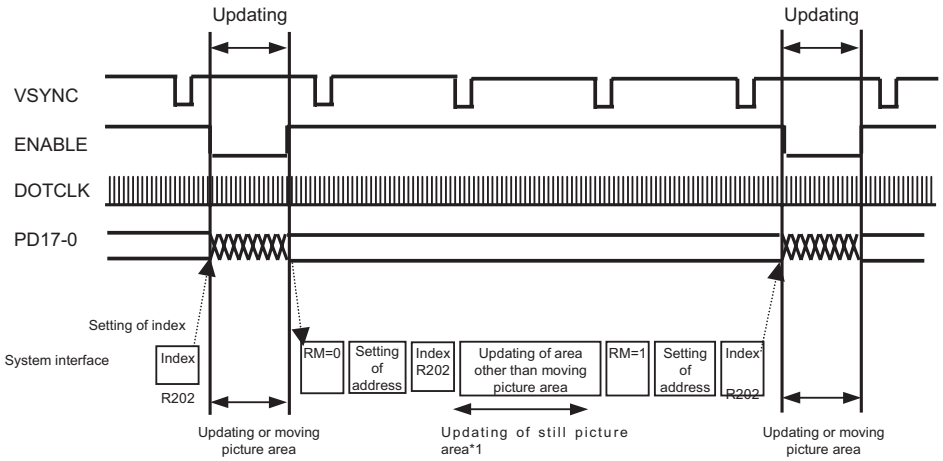
REV = 1

GRAM Data Setting	Grayscale Polarity		GRAM Data Setting	Grayscale Polarity	
RGB	Negative	Positive	RGB	Negative	Positive
000000	V63	V0	100000	V31	V32
000001	V62	V1	100001	V30	V33
000010	V61	V2	100010	V29	V34
000011	V60	V3	100011	V28	V35
000100	V59	V4	100100	V27	V36
000101	V58	V5	100101	V26	V37
000110	V57	V6	100110	V25	V38
000111	V56	V7	100111	V24	V39
001000	V55	V8	101000	V23	V40
001001	V54	V9	101001	V22	V41
001010	V53	V10	101010	V21	V42
001011	V52	V11	101011	V20	V43
001100	V51	V12	101100	V19	V44
001101	V50	V13	101101	V18	V45
001110	V49	V14	101110	V17	V46
001111	V48	V15	101111	V16	V47
010000	V47	V16	110000	V15	V48
010001	V46	V17	110001	V14	V49
010010	V45	V18	110010	V13	V50
010011	V44	V19	110011	V12	V51
010100	V43	V20	110100	V11	V52
010101	V42	V21	110101	V10	V53
010110	V41	V22	110110	V9	V54
010111	V40	V23	110111	V8	V55
011000	V39	V24	111000	V7	V56
011001	V38	V25	111001	V6	V57
011010	V37	V26	111010	V5	V58
011011	V36	V27	111011	V4	V59
011100	V35	V28	111100	V3	V60
011101	V34	V29	111101	V2	V61
011110	V33	V30	111110	V1	V62
011111	V32	V31	111111	V0	V63

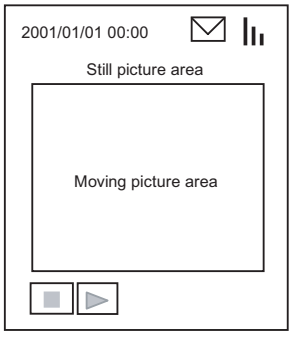
RAM Access via RGB-I/F and System I/F

All the data for display is written to the internal RAM in the HD66776 when RGB-I/F is in use. In this method, data, including that in both the moving picture area and the screen update frame, can only be transferred via RGB-I/F. In addition to using the high-speed write mode (HWM1-0 = "11") and the window address function, the power consumption can be reduced and high-speed access can be achieved while moving pictures are being displayed. Data for display that is not in the moving picture area or the screen update frame can be rewritten via the system interface.

RAM can be accessed via the system interface when RGB-I/F is in use. When data is written to RAM during RGB-I/F mode, the ENABLE bit should be high to stop data writing via RGB-I/F, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is low. After this RAM access via the system interface, a waiting time is needed for a write/read bus cycle before the next RAM access starts via RGB-I/F. When a RAM write conflict occurs, data writing is not guaranteed.



Note 1: When RGB-I/F is in use, an address is set at every falling edge of VSYNC.
2: An address and an index (R202h) should be set before RAM is accessed via RGB-I/F.
3: The high-speed write mode (HWM1-0 = "11") should be used in RGB-I/F and VSYNC-I/F.

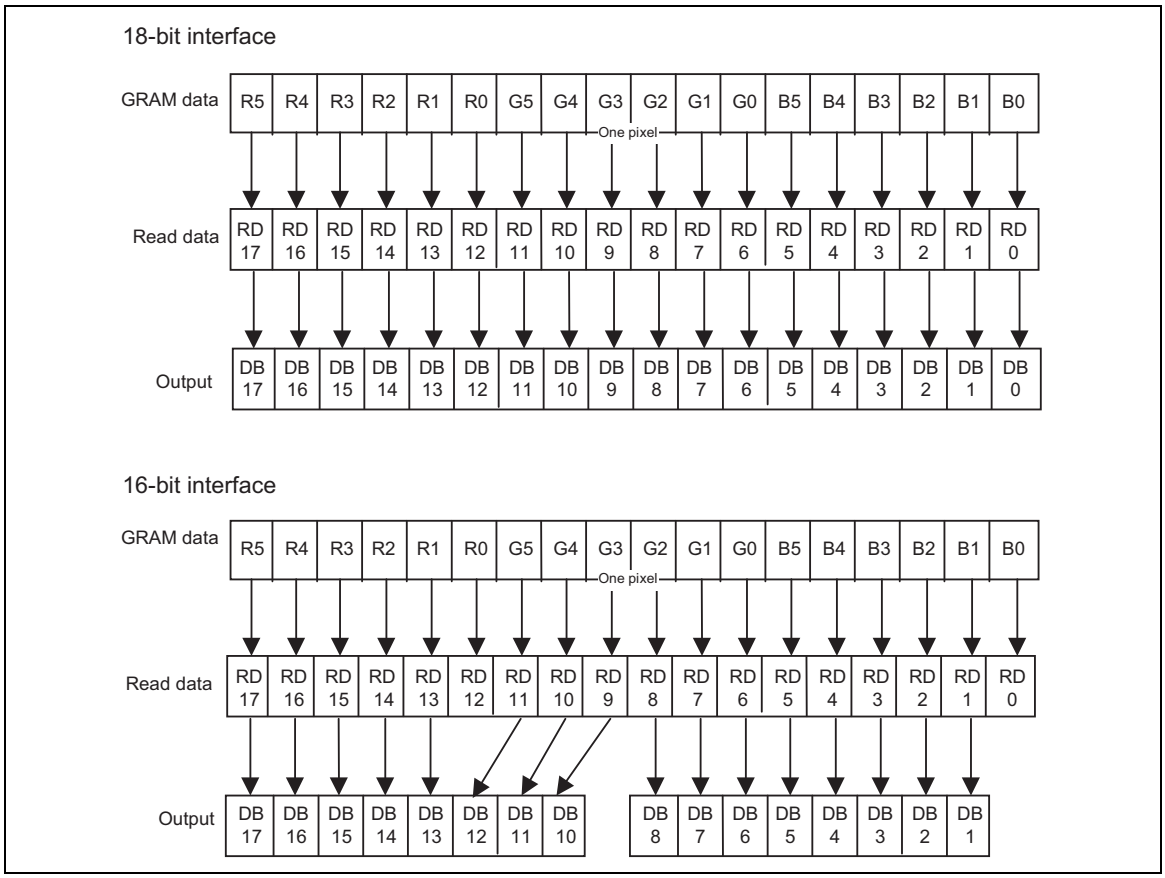


Example of Updating Still Picture Area during Diaplaying Moving Picture

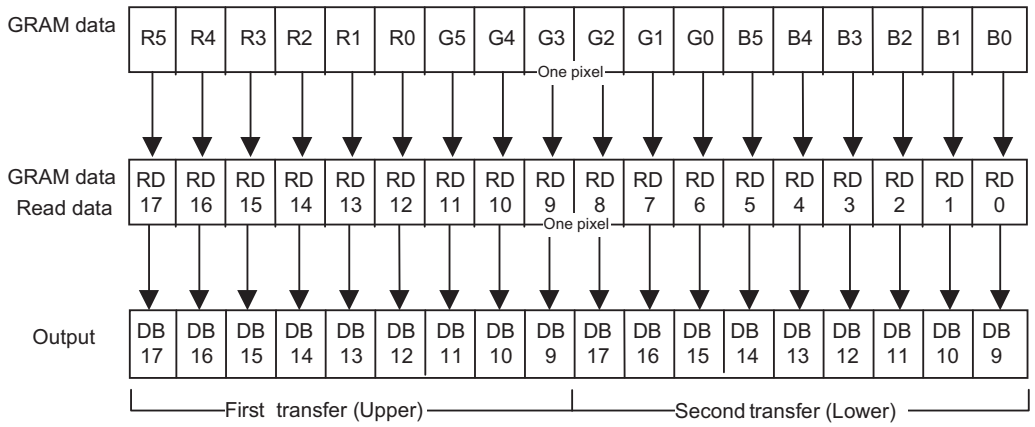
Read Data from GRAM (R203h)

R/W	RS		
R	1		RAM read data (RD17-0) The pin assignment for DB17-0 varies for eachinterface (see below).

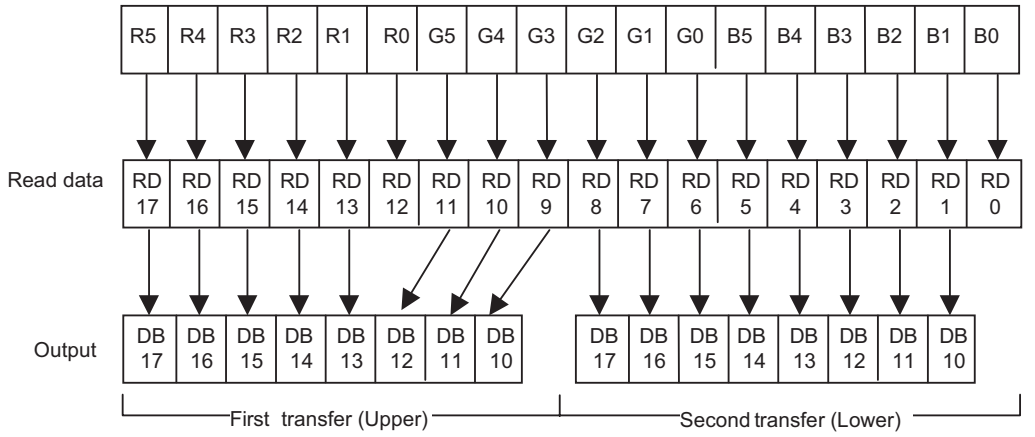
RD17–0: Read 18-bit data from GRAM. When the data is read to the microcomputer, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data in the data bus (DB17–0) becomes invalid and the second-word read is normal. When bit processing, such as a logical operation, is performed by the HD66776, only one read can be processed since the latched data in the first word is used. Please make sure bit processing is performed in 18-bit units. When the 8-/16-bit interface is in use, the LSB of RB write data will not be read. When RGB-I/F is in use, this function is not available.

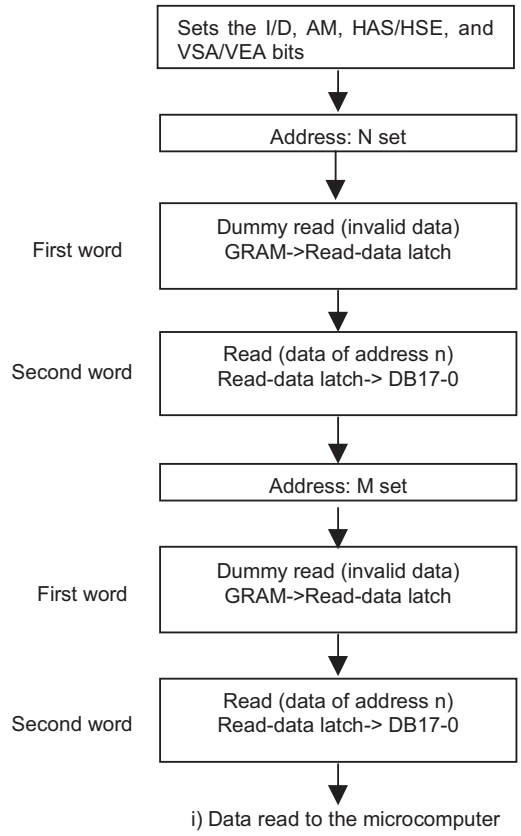


9-bit interface



8-bit interface / SPI





GRAM read sequence

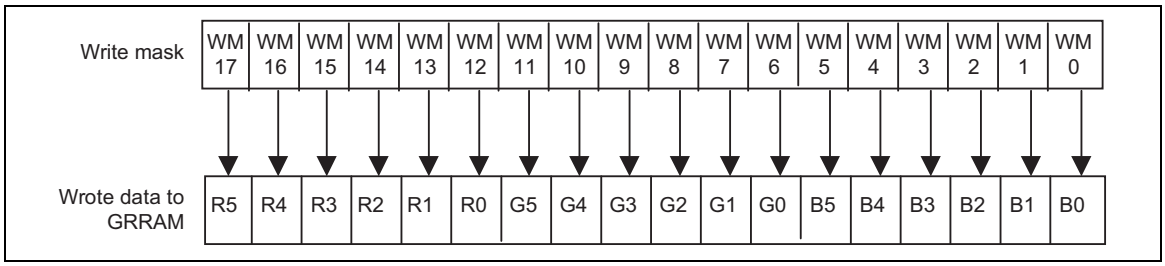
RAM Write Data Mask (R203h)

RAM Write Data Mask (R204h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	0	0	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0
W	1	0	0	0	0	0	1	1	1	0	1	WM 17	WM 16	WM 15	WM 14	WM 13	WM 12

WM17–0: In writing to GRAM, these bits mask the writing in a bit unit. When WM17 = "1", this bit masks the MSB of the write data and does not write to GRAM. Similarly, the WM16–0 bits mask the data written to GRAM in a bit unit. For details, see the Graphics Operation Function section.

Please make sure the write data to GRAM (18-bit data) is masked. When RGB-I/F is in use, this function is not available.



γ Control Instructions

γ Control (R300h to R309h)

	R/W	RS	IB15	IB14	IB13	IB12	IB1	BI10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R300	W	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R301	W	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R302	W	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R303	W	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R304	W	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 2	VRP 01	VRP 00
R305	W	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R306	W	1	0	0	0	0	0	PKN 32	PKN 31	PKIN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R307	W	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R308	W	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R309	W	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52-00: The γ fine adjustment registers for positive polarity
PRP12-00: The γ gradient adjustment registers for positive polarity
VRP14-00: The γ amplitude adjustment registers for positive polarity
PKN42-00: The γ fine adjustment registers for negative polarity
PRN12-00: The γ gradient adjustment registers for negative polarity
VRN14-00: The γ amplitude adjustment registers for negative polarity

For details, see the section on the γ adjustment.

Position Control Instructions

Vertical Scroll Control (R400h)
Vertical Scroll Control (R401h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10
W	1	0	0	0	0	0	0	0	VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20

VL18–10: Specify the amount of scroll in the display to enable smooth vertical scrolling. Any raster-row from 0 to 319 can be displayed with scrolling. After the 320th raster-row is displayed, the display restarts from the 1st raster-row. The display-start raster-row (VL18–10) is valid only when VLE1 = "1" or VLE2 = "1". The raster-row display is fixed when VLE1 = "0".
*: When the external display interface is in use, this function is not available.

VL Bits and Display-start Raster-row

VL18	VL17	VL16	VL15	VL14	VL13	VL12	VL11	VL10	Amount of Scrolling (Number of raster-row)
0	0	0	0	0	0	0	0	0	Line 0
0	0	0	0	0	0	0	0	1	Line 1
0	0	0	0	0	0	0	1	0	Line 2
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	0	Line 318
1	0	0	1	1	1	1	1	1	Line 319

Note: Do not set to over 319 ("13F"H) raster-rows.

VL28–20: Specify the amount of scroll in the 2nd display to enable smooth vertical scrolling. Any raster-row from 0 to 319 can be displayed with scrolling. After the 320th raster-row is displayed, the display restarts from the 1st raster-row. The display-start raster-row (VL28–20) is valid only when VLE2 = "1". The raster-row display is fixed when VLE2 = "0".
*: When the external display interface is in use, this function is not available.

VL Bits and Display-start Raster-row

VL28	VL27	VL26	VL25	VL24	VL23	VL22	VL21	VL20	Amount of Scrolling (Number of raster-row)
0	0	0	0	0	0	0	0	0	Line 0
0	0	0	0	0	0	0	0	1	Line 1
0	0	0	0	0	0	0	1	0	Line 2
:	:	:	:	:	:	:	:	:	:
1	0	0	1	1	1	1	1	0	Line 318
1	0	0	1	1	1	1	1	1	Line 319

Note: Do not set to over 319 ("13F"H) raster-rows.

1st-screen driving position (1) (R402h)
1st-screen driving position (2) (R403h)
2nd-screen driving position (1) (R404h)
2nd-screen driving position (2) (R405h)

R/W	RS	IB15	IB14	IB13	IB12	IB1	BI10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	SS 18	SS 17	SS 16	SS 15	SS 14	SS 13	SS 12	SS 11	SS 10
W	1	0	0	0	0	0	0	0	SE 18	SE 17	SE 16	SE 15	SE 14	SE 13	SE 12	SE 11	SE 10
W	1	0	0	0	0	0	0	0	SS 28	SS 27	SS 26	SS 25	SS 24	SS 23	SS 22	SS 21	SS 20
W	1	0	0	0	0	0	0	0	SE 28	SE 27	SE 26	SE 25	SE 24	SE 23	SE 22	SE 21	SE 20

SS18–0: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver.

SE18–0: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS18–10 = “07”H and SE18–10 = “10”H are set, the LCD driving is performed from G8 to G17, and non-selection driving is performed for G1 to G7, G18, and others. Ensure that SS18–10 ≤ SE18–10 ≤ “13F”H. For details, see the Screen-division Driving Function section.

SS28–0: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver. The second screen drives when SPT = “1”.

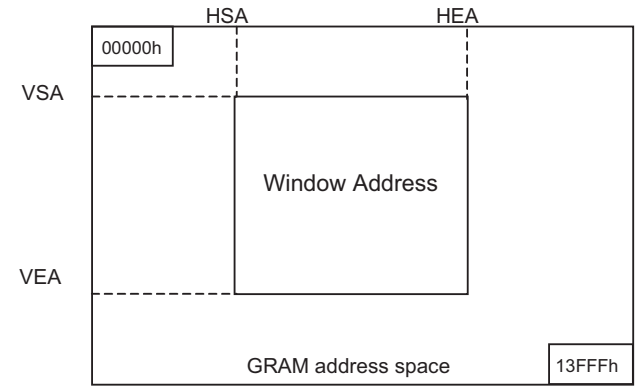
SE28–0: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SPT = “1”, SS28–20 = “20”H, and SE28-20 = “4F”H are set, the LCD driving is performed from G33 to G80. Ensure that SS18–10 ≤ SE18–10 < SS28-20 ≤ SE28-20 ≤”13F”H. For details, see the Screen-division Driving Function section.

Horizontal RAM address position (R406h)
Vertical RAM address position (R407h)
Horizontal RAM address position (R408h)
Vertical RAM address position (R409h)

R/W	RS	IB15	IB14	IB13	IB12	IB1	BI10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
W	1	0	0	0	0	0	0	0	0	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0
W	1	0	0	0	0	0	0	0	VSA 8	VSA 7	VSA 6	VSA 5	VSA 4	VSA 3	VSA 2	VSA 1	VSA 0
W	1	0	0	0	0	0	0	0	VEA 8	VEA 7	VEA 6	VEA 5	VEA 4	VEA 3	VEA 2	VEA 1	VEA 0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written to. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ “FF”h.

VSA8-0/VEA8-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA8-0 from the address specified by VSA8-0. Note that an address must be set before RAM is written to. Ensure “000”h ≤ VSA8-0 ≤ VEA8-0 ≤”13F”h.



Note: Ensure that the window address area is within the GRAM address space.

Instruction List

Major Division		Minor Division		Upper code								Lower code								Note
Index upper		Index	Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index	-	Index	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	
SR	Status read	-	Status read	0	0	0	0	0	0	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	
0**	Display control	000h	Display control	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
			Device code read	0	0	0	0	0	1	1	1	0	1	1	1	0	1	1	0	
		001h	Driver output control	0	0	0	0	0	0	0	SS (0)	0	0	NL5 (1)	NL4 (0)	NL3 (0)	NL2 (1)	NL1 (1)	NL0 (1)	
		002h	LCD drive AC control	0	0	0	0	0	0	B/O (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
		003h	Entry mode	0	0	0	BGR (0)	0	0	HWM1 (0)	HWM0 (0)	0	0	ID1 (1)	ID0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
		004h	Setting inhibited																	
		005h	Setting inhibited																	
		006h	Setting inhibited																	
		007h	Display control (1)	COL (0)	0	0	0	0	VLE2 (0)	VLE1 (0)	SPT (0)	PT1 (0)	PT0 (0)	GON (0)	DTE (0)	0	REV (0)	D1 (0)	D0 (0)	
		008h	Display control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
		009h	Setting inhibited																	
		00Ah	Power supply IC interface contro	0	0	0	0	0	0	0	TE (0)	0	0	0	0	0	IDX2 (0)	IDX1 (0)	IDX0 (0)	
		00Bh	Setting inhibited																	
		00Ch	External display interface control (0	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
		00Dh	Frame frequency adjustment control	0	0	0	0	0	0	DIVI1 (0)	DIVI0 (1)	0	0	0	RTNI4 (1)	RTNI3 (0)	RTNI2 (0)	RTNI1 (0)	RTNI0 (0)	
		00Eh	External display interace control (0	0	0	0	0	0	0	DIVE1 (1)	DIVE0 (0)	RTNE 7 (0)	RTNE 6 (0)	RTNE5 (0)	RTNE4 (1)	RTNE3 (1)	RTNE2 (1)	RTNE1 (1)	RTNE0 (0)	
		00Fh	External desplay interface control	0	0	0	0	0	0	0	0	0	0	0	VSPL (0)	HSPL (0)	VPL (0)	EPL (0)	DPL (0)	
		010h	ITP interface control (1)	0	0	FWI5 (0	FWI4 (0)	FWI3 (0)	FWI2 (0)	FWI1 (0)	FWI0 (0)	0	0	0	0	0	FTI2 (0)	FTI1 (0)	FTI0 (0)	
		011h	LTPS interace control (2)	0	0	SWI5 (0)	SWI4 (0)	SWI4 (0)	SWI2 (0)	SWI1 (0)	SWI0 (0)	0	0	0	0	0	STI2 (0)	STI1 (0)	STI0 (0)	
		012h	LTPS interface control (3)	0	0	0	CLWI4 (0)	CLWI3 (0)	CLWI2 (0)	CLWI1 (0)	CLWI0 (0)	0	0	0	0	CLTI3 (0)	CLTI2 (0)	CLTI1 (0)	CLTI0 (0)	
		013h	LTPS interface control (4)	0	0	DPWI5 (0	DPWI4 (0)	DPWI3 (0)	DPWI2 (0)	DPWI1 (0)	DPWI0 (0)	0	0	0	0	0	DPTI2 (0)	DPTI1 (0)	DPTI0 (0)	
		014h	LTPS interface control (5)	0	0	0	0	0	MCPI2 (0)	MCPI1 (0)	MCPI0 (0)	0	0	0	0	0	0	SHI1 (0)	SHI0 (0)	
		015h	LTPS interface control (6)	0	0	0	0	0	0	EQWI1 (0)	EQWI0 (0)	0	0	0	0	0	EQTI2 (0)	EQTI1 (0)	EQTI0 (0)	
		016h	LTPS interface control (7)	FWE7 (0)	FWE6 (0)	FWE5 (0)	FWE4 (0)	FWE3 (0)	FWE2 (0)	FWE1 (0)	FWE0 (0)	0	0	0	FTE4 (0)	FTE3 (0)	FTE2 (0)	FTE1 (0)	FTE0 (0)	
		017h	LTPS interface control (8)	SWE7 (0)	SWE6 (0)	SWE5 (0	SWE4 (0)	SWE3 (0)	SWE2 (0)	SWE1 (0)	SWE0 (0)	0	0	0	STE4 (0)	STE3 (0)	STE2 (0)	STE1 (0)	STE0 (0)	
		018h	LTPS interface control (9)	0	0	CLWE5 (0)	CLWE4 (0)	CLWE3 (0)	CLWE2 (0)	CLWE1 (0)	CLWE0 (0)	0	0	0	CLTE4 (0)	CLTE3 (0)	CLTE2 (0)	CLTE1 (0)	CLTE0 (0)	
		019h	LTPS interface control (10)	DPWE7 (0)	DPWE6 (0)	DPWE5 (0)	DPWE4 (0)	DPWE3 (0)	DPWE2 (0)	DPWE1 (0)	DPWE0 (0)	0	0	0	DPTE4 (0)	DPTE3 (0)	DPTE2 (0)	DPTE1 (0)	DPTE0 (0)	
		01Ah	LTPS interface control (11)	0	0	0	0	MCPE3 (0)	MCPE2 (0)	MCPE1 (0)	MCPE0 (0)	0	0	0	0	SHE3 (0)	SHE2 (0)	SHE1 (0)	SHE0 (0)	
		01Bh	LTPS interface control (12)	0	0	0	0	EQWE3 (0)	EQWE2 (0)	EQWE1 (0)	EQWE0 (0)	0	0	0	0	EQTE3 (0)	EQTE2 (0)	EQTE1 (0)	EQTE0 (0)	
		01Fh	LTPS interface control (13)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
		020h-0FFh	Setting inhibited																	
1**	Power control	100h	Power control (1)	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTB (0)	SLP (0)	STB (0)	
		101h	Power control (2)	DC4 (0)	DC3 (0	SAP2 (0)	SAP1 (0)	SAP0 (0)	BT2 (0)	BT1 (0)	BT0 (0)	DC2 (0)	DC1 (0)	DC0 (0)	AP2 (0)	AP1 (0)	AP0 (0)	0	0	
		102h	Setting inhibited																	
		103h	Power control (4)	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2 (0)	VC1 (0)	VC0 (0)	
		104h	Power control (5)	0	0	0	0	VRL3 (0)	VRL2 (0)	VRL1 (0)	VRL0 (0)	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
		105h	Power control (6)	0	0	VCOMG (0)	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
		107h-1FFh	Setting inhibited																	
2**	RAM access	200h	RAM address set (1)	0	0	0	0	0	0	0	0	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
		201h	RAM address set (2)	0	0	0	0	0	0	0	AD16 (0)	AD15 0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	A10 (0)	AD9 (0)	AD8 (0)	
		202h	RAM data write/read	RAM write data (WD17-0)/RAM read data (RD17-0) *Bit assignment changes according to the selected interface																
		203h	RAM write data mask (1)	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
		204h	RAM write data mask (2)	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
		205h-2FFh	Setting inhibited																	
3**	control	300h	control (1)	0	0	0	0	0	PKP12 (0)	PKP11 (0)	PKP10 (0)	0	0	0	0	0	PKP02 (0)	PKP01 (0)	PKP00 (0)	
		301h	control (2)	0	0	0	0	0	PKP32 (0)	PKP31 (0)	PKP30 (0)	0	0	0	0	0	PKP22 (0)	PKP21 (0)	PKP20 (0)	
		302h	control (3)	0	0	0	0	0	PKP52 (0)	PKP51 (0)	PKP50 (0)	0	0	0	0	0	PKP42 (0)	PKP41 (0)	PKP40 (0)	
		303h	control (4)	0	0	0	0	0	PRP12 (0)	PRP11 (0)	PRP10 (0)	0	0	0	0	0	PRP02 (0)	PRP01 (0)	PRP00 (0)	
		304h	control (5)	0	0	0	VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)	0	0	0	0	VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)	
		305h	control (6)	0	0	0	0	0	PKN12 (0)	PKN11 (0)	PKN10 (0)	0	0	0	0	0	PKN02 (0)	PKN01 (0)	PKN00 (0)	
		306h	control (7)	0	0	0	0	0	PKN32 (0)	PKN31 (0)	PKN30 (0)	0	0	0	0	0	PKN22 (0)	PKN21 (0)	PKN20 (0)	
		307h	control (8)	0	0	0	0	0	PKN52 (0)	PKN51 (0)	PKN50 (0)	0	0	0	0	0	PKN42 (0)	PKN41 (0)	PKN40 (0)	
		308h	control (9)	0	0	0	0	0	PRN12 (0)	PRN11 (0)	PRN10 (0)	0	0	0	0	0	PRN02 (0)	PRN01 (0)	PRN00 (0)	
		309h	control (10)	0	0	0	VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)	0	0	0	0	VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)	
		30Ah	Setting inhibited																	
		30Bh	Setting inhibited																	
		90Ch	Setting inhibited																	
		30Dh	Setting inhibited																	
		30Eh	Setting inhibited																	
		30Fh	Setting inhibited																	
		310h-3FFh	Setting inhibited																	
4**	Coordinate contro	400h	Vertical scroll control (1)	0	0	0	0	0	0	0	VL18 (0)	VL17 (0)	VL16 (0)	VL15 (0)	VL14 (0)	VL13 (0)	VL12 (0)	VL11 (0)	VL10 (0)	
		401h	Vertical scroll control (2)	0	0	0	0	0	0	0	0	VL27 (0)	VL26 (0)	VL25 (0)	VL24 (0)	VL23 (0)	VL22 (0)	VL21 (0)	VL20 (0)	
		402h	Frist screen driving position (1)	0	0	0	0	0	0	0	SS18 (0)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	
		403h	Frist screen driving position (2)	0	0	0	0	0	0	0	SE18 (1)	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	
		404h	Second screen driving position (1)	0	0	0	0	0	0	0	SS28 (0)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
		405h	Second screen driving position (2)	0	0	0	0	0	0	0	SE28 (1)	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	
		406h	Horizontal RAM address position	0	0	0	0	0	0	0	0	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
		407h	Horizontal RAM address position	0	0	0	0	0	0	0	0	HEA7 (1)	HEA6 (1)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	
		408h	Vertical RAM address position (1)	0	0	0	0	0	0	0	VSA8 (0)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	
		409h	Vertical RAM address position (2)	0	0	0	0	0	0	0	VEA8 (1)	VEA7 (0)	VEA6 (0)	VEA5 (1)	VEA4 (1)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	
		40Ah-4FFh	Setting inhibited																	
5**		*	Setting inhibited																	
6**		*	Setting inhibited																	
7**		*	Setting inhibited																	
F**		*	Setting inhibited																	

Reset Function

The HD66776 is internally initialized by RESET input inside the HD66776 is in busy state during the reset period and no instruction or GRAM data access from the MPU is accepted. Reset the power-supply IC as its settings are not automatically reinitialized when the HD66776 is reset. The reset input must be held for at least 1ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10ms).

Instruction set initialization

Indicated in the liwer row of each cell in Table 57.

GRAM Data Initialization

This is not automatically initialized by reset input but must be initialized by software while display is off (D1–0 = “00”).

Output Pin Initialization

1. LCD driver output pins (source outputs): Output GND level
2. Oscillator output pin (OSC2): Outputs oscillation signal
3. Power supply IC interface signals (GCS*, GCL, and GDA): Halt
4. Timing signals: Halt (M, FLM, SFTCLK1, SFTCLK2, CLA, CLB, CLC, DISPTMG, DCCLK, EQ)

Interface Specifications

The HD66776 incorporates a system interface, which is used to set instructions, and an external display interface, which is used to display moving pictures. Selecting these interfaces to match the screen data (moving or still enables efficient transfer of data for display.

The external display interface includes RGB-I/F and VSYNC-I/F. This allows flicker-free screen update.

When RGB-I/F is selected, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for use in operating the display. The data for display (PD17-0) is written according to the values of the data enable signal (ENABLE) and data valid signal (VLD), in synchronization with the VSYNC, HSYNC, and DOTCLK signals. The data for display is written to GRAM, so that data transfer is reduced only when switching the screen. In addition, using the window address function enables rewriting only to the internal RAM area to display moving pictures. Using this function also enables simultaneously display of the moving picture are and the RAM data that was written. While displaying moving pictures, the data for display should be written in high-speed access via RGB-I/F or VSYNC-I/F.

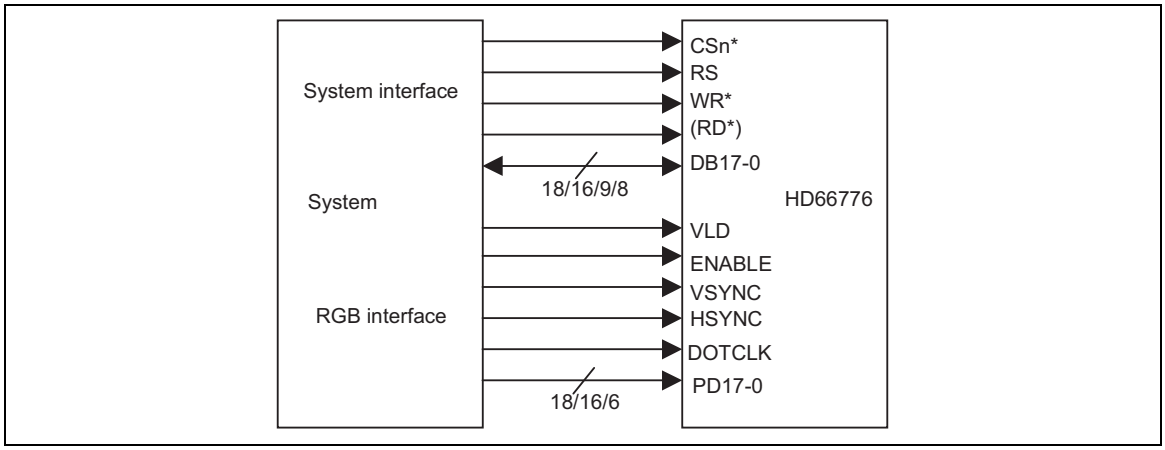
The internal display operation I synchronized with the frame synchronization signal (VSYNC) in VSYNC interface mode. When writing to the internal RAM is done within the required time after the falling edge of VSYNC, moving pictures can be displayed via the conventional interface. There are some limitations on the timing and methods of writing to RAM. See the section on the external display interface.

The HD66776has four operation modes for each display state. These settings are specified by control instructions for external display interface. Transitions between modes should follow the transition flow.

Operation mode and interface

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still picture)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving picture)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still picture while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1:Instruction registers can only be set via system interface.
2:RGB-I/F and VSYNC-I/F cannot be used at the same time.
3:RGB-I/F mode (RIM-0) cannot be set while RGB I/F is operating.
4:For mode transitions see the section on the external display interface.
5:RGB-I/F and VSYNC-I/F modes should be used in high-speed write mode (HWM1-0 = 11).



System Interface

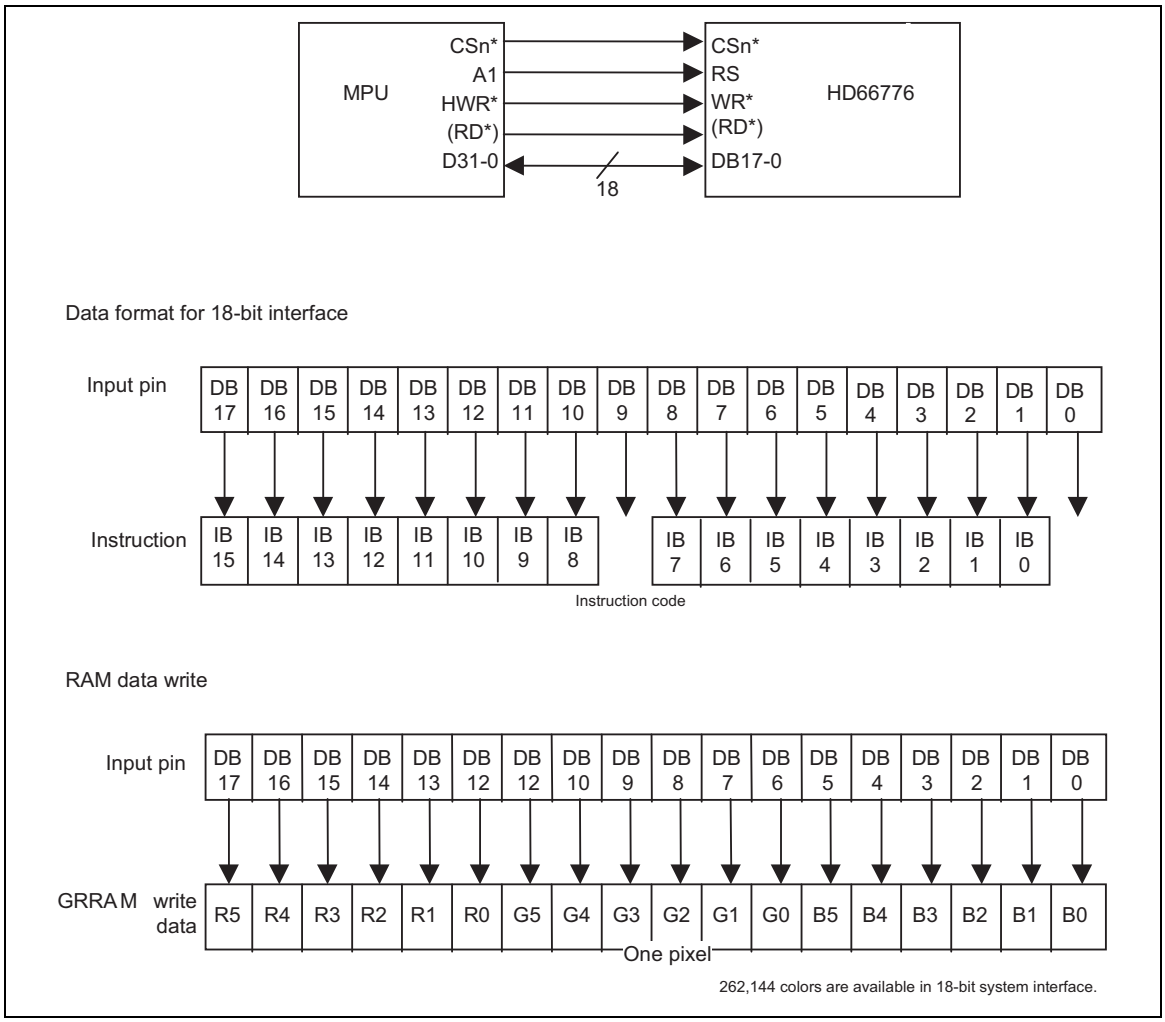
The following interfaces are available as sytem interface. It is determined by setting bits of IM3-0. Instructions and RAM accesses can be performed via the system interface.

IM bits

IM3	IM2	IM1	IM0	System Interface	DB Pin
0	0	0	0	Setting disabled	
0	0	0	1	Setting disabled	
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8 to 1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Clocked serial peripheral interface (SPI)	DB1 to 0
0	1	1	*	Setting disabled	
1	0	0	0	Setting disabled	
1	0	0	1	Setting disabled	
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled	

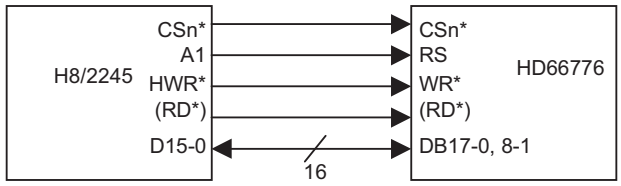
80-system 18-bit bus interface

80-system 18-bit parallel data transfer can be used by setting IM3/2/1/0 pins to Vcc/GND/Vcc/GND levels.



80-system 16-bit bus interface

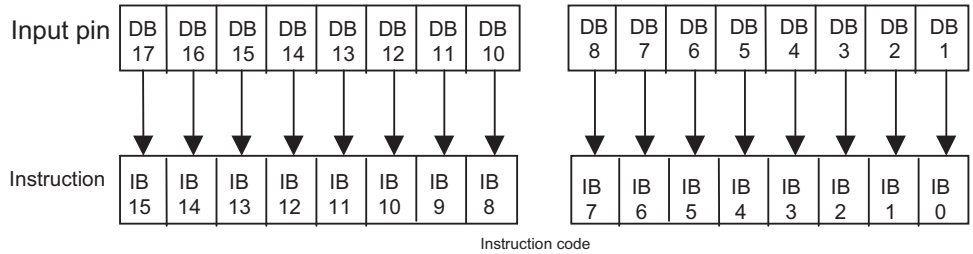
80-system 16-bit parallel data transfer can be used by setting IM3/2/1/0 pins to GND/GND/Vcc/GND levels



Example of interface with 16-bit microcomputer

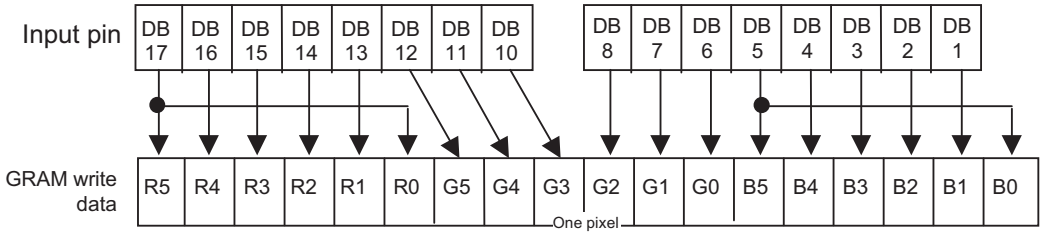
Data format for 16-bit interface

Instruction



Instruction code

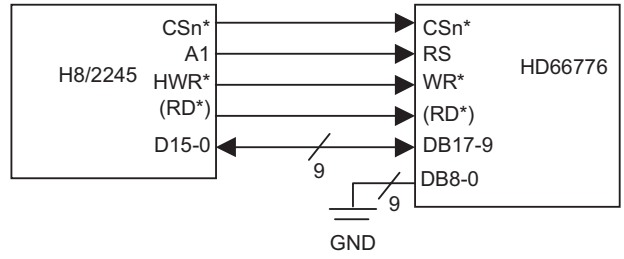
RAM data write



65,536 colors are available in 16-bit system interface.

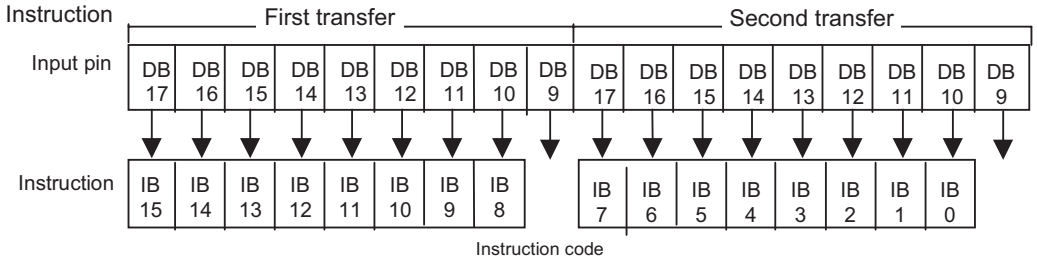
80-system 9-bit bus interface

80-system 9-bit parallel data transfer can be used by setting IM3/2/1/0 pins to Vcc/GND/Vcc/Vcc levels. 16-bit instruction is divided into two parts, which are lower and upper, and the upper eight bits are first transferred. The LSB of the bus is not used. RAM data is also divided into two parts, which are lower and upper, and the upper nine bits are first transferred. Unused pins (DB8-0) must be fixed to the Vcc or GND level. Ensure that upper bytes have to be written when writing the index register.

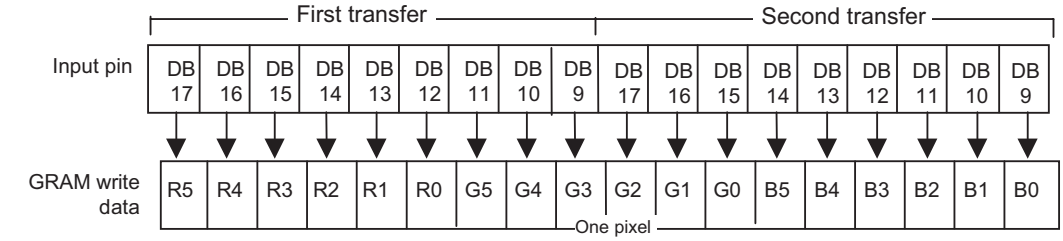


Example of interface with 8-bit microcomputer

Data format for 8-bit interface (1)

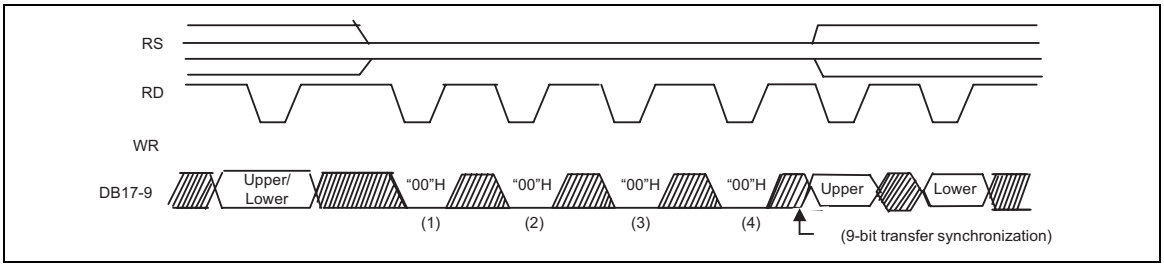


RAM data write



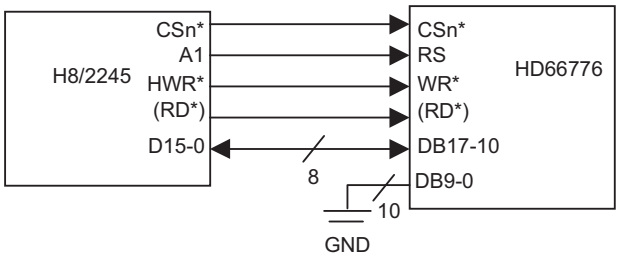
Note: Transfer synchronization function for 9-bit bus interface.

The HD66776 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit bus interface. Noise causing transfer mismatch between the nine upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.



80-system 8-bit bus interface

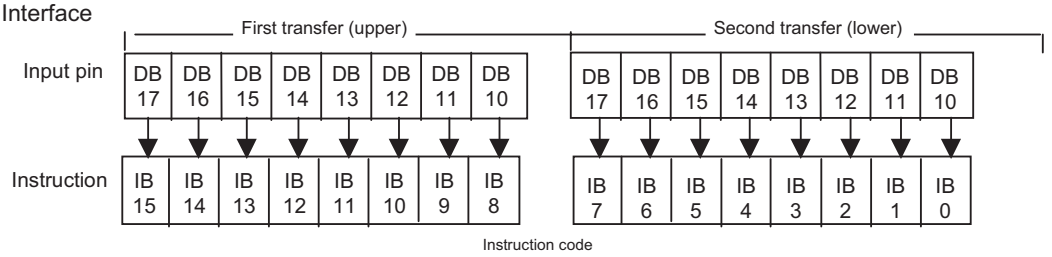
80-system 8-bit parallel data transfer can be used by setting IM3/2/1/0 pins to GND/GND/Vcc/Vcc levels. 16-bit instruction is divided into two parts, which are lower and upper, and the upper eight bits are first transferred. According to the setting of TRI, RAM data for one word are divided into two or three for two time transfer or three time transfer. The LSB of the bus is not used. RAM data is also divided into two parts, which are lower and upper, and the upper nine bits are first transferred. Data for RAM write is expanded to 18-bit data in this LSI. Unused pins (DB9-0) must be fixed to the Vcc or GND level. Ensure that upper bytes have to be written when writing the index register.



Example of interface with 8-bit microcomputer

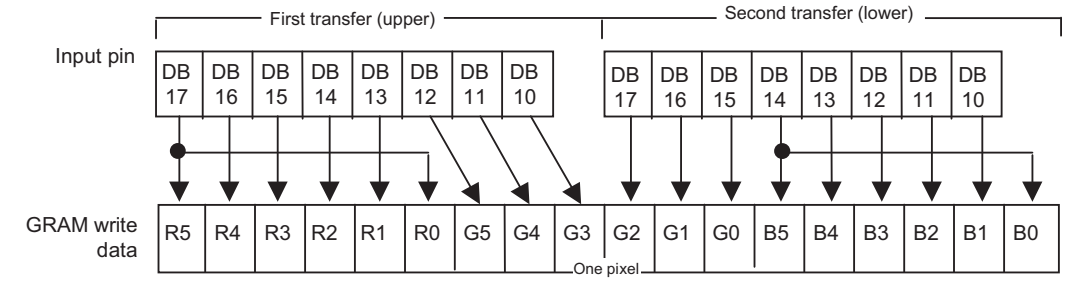
Data format for 8-bit interface (1)

Interface



Instruction code

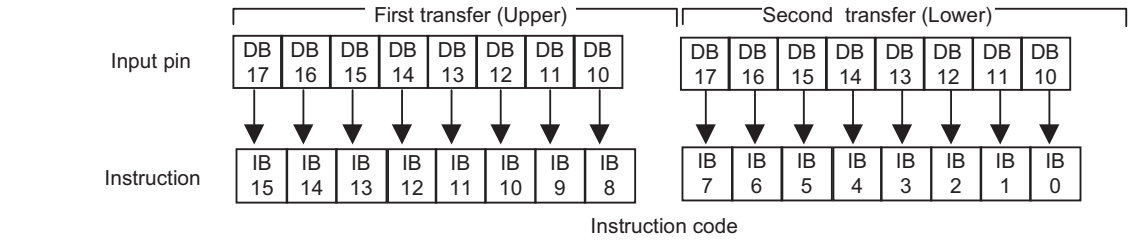
RAM data write



65,536 colors are available in 8-bit system interface.

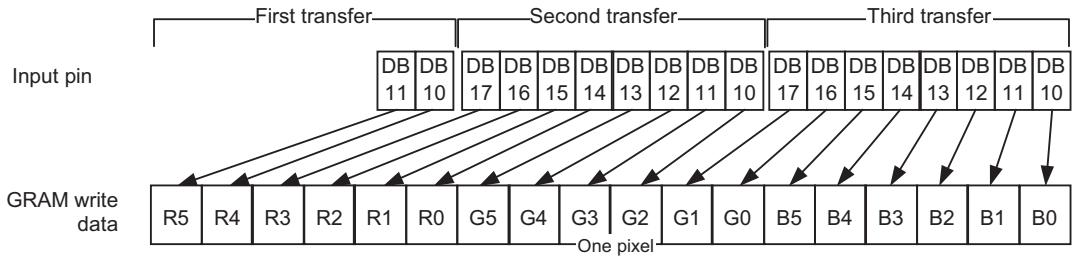
Data format for 8-bit interface (2)

Instruction



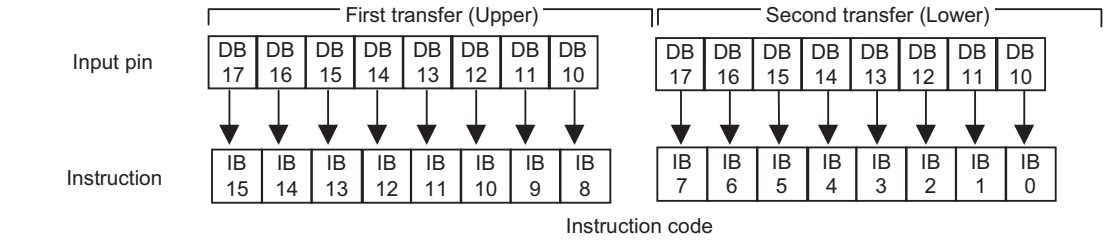
Instruction code

RAM data write



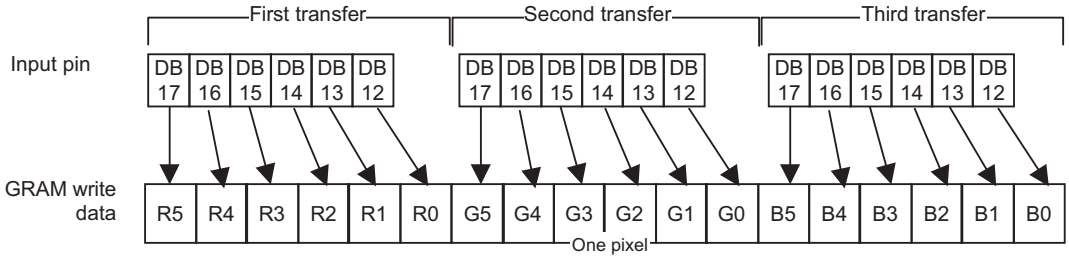
Data format for 8-bit interface (3)

Instruction



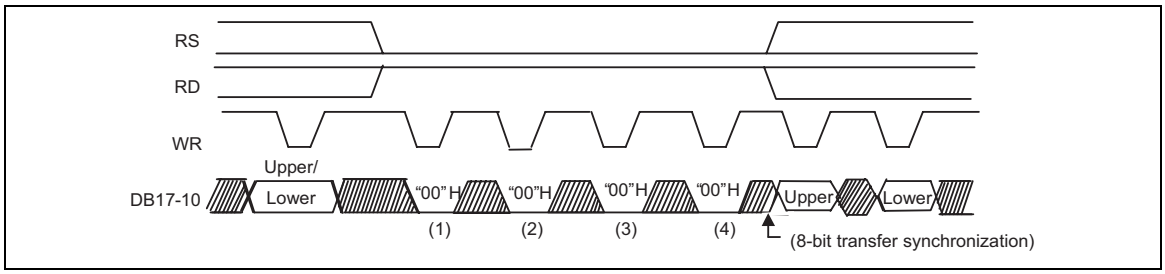
Instruction code

RAM data write



Note: Transfer synchronization function for an 8-bit bus interface

The HD66776 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a 00H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system.



Serial clock synchronized interface (SPI)

Setting the IM3 pin to the GND level, the IM2 pin to the Vcc level, the IM1 pin to the GND level allows standard clock-synchronized serial data (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB15-2 pins which are not used must be fixed at Vcc or GND.

The HD66776 initiates serial data transfer by transferring the start byte at the falling edge of CS* input. It ends serial data transfer at the rising edge of CS* input.

The HD66776 is selected when the 6-bit chip address in the start byte transferred from the transmitting device matches the 6-bit device identification code assigned to the HD66776. The HD66776, when selected, receives the subsequent data string. The least significant bit of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single HD66776 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.

When writing to RAM via this serial interface, the data is written to the GRAM after two-byte data has been transferred. The MSB of RB data is added to its LSB so that data to be written to the RAM will be 18 bits.

After receiving the start byte, the HD66776 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All HD66776 instructions are 16 bits. Two bytes are received with the MSB first (DB15 to 0), then the instructions are internally executed. Data for RAM write is expanded to 18-bit data in this LSI.) After the start byte has been received, the first byte is fetched internally as the upper eight bits of the instruction and the second byte is fetched internally as the lower eight bits of the instruction.

Four bytes of RAM read data after the start byte are invalid. The HD66776 starts to read correct RAM data from the fifth byte.

Start Byte Format

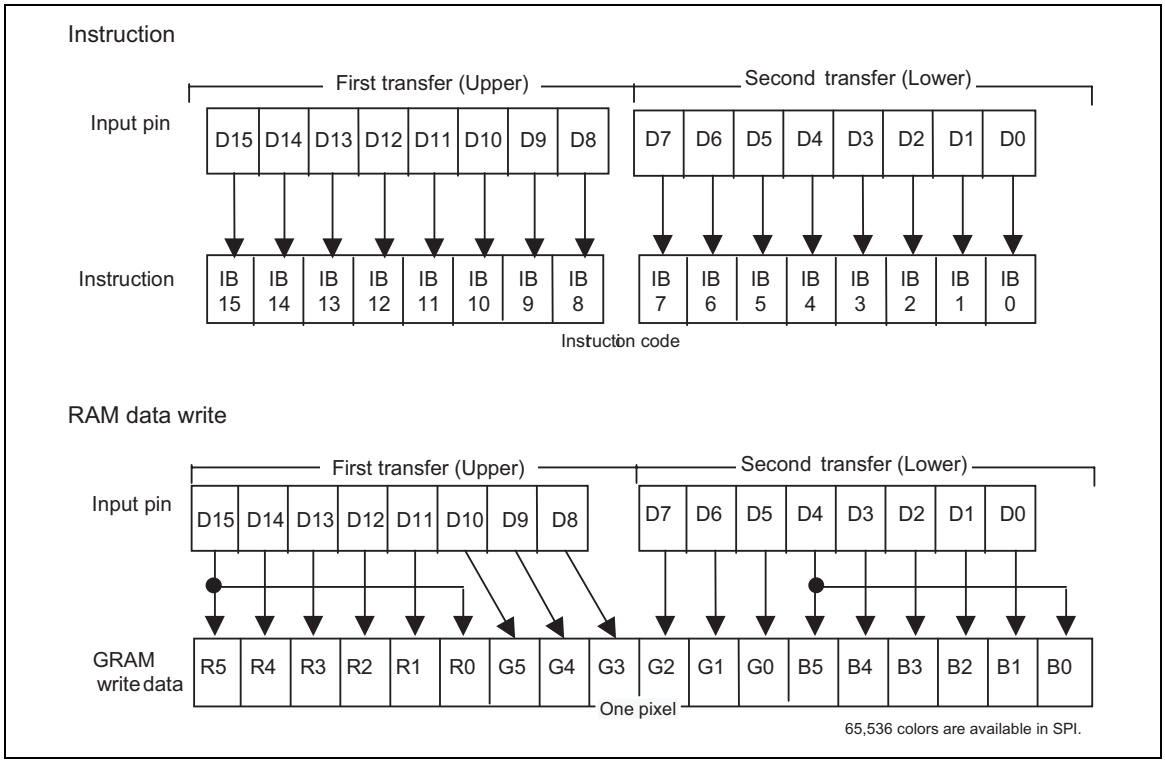
Transfer Bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

Note: ID bit is selected by the IM0/ID pin.

RS and R/W Bis Function

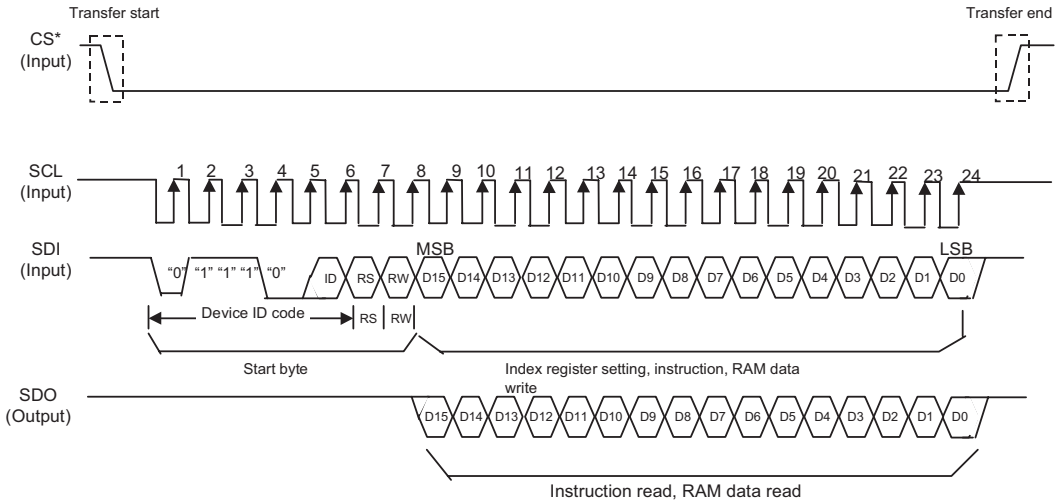
RS	R/W	Function
0	0	Sets index register
0	1	Reads status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

Data format for serial interface

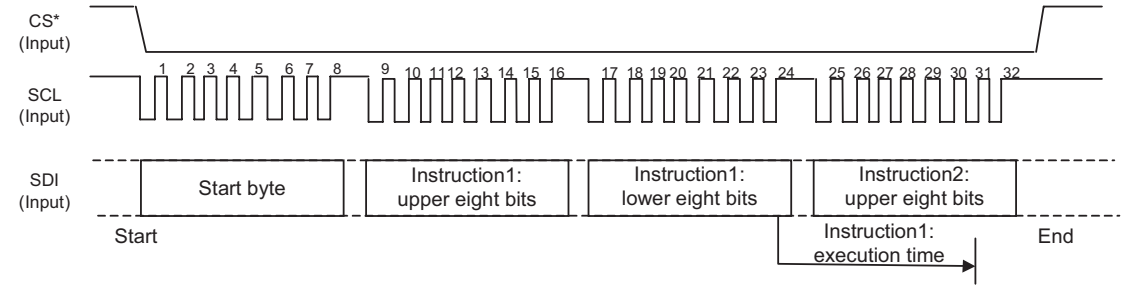


Procedure for Transfer on Clock-Synchronized Serial Bus Interface

a)Timing if Basic Data-transfer through Clock-Synchronized Serial Bus Interface

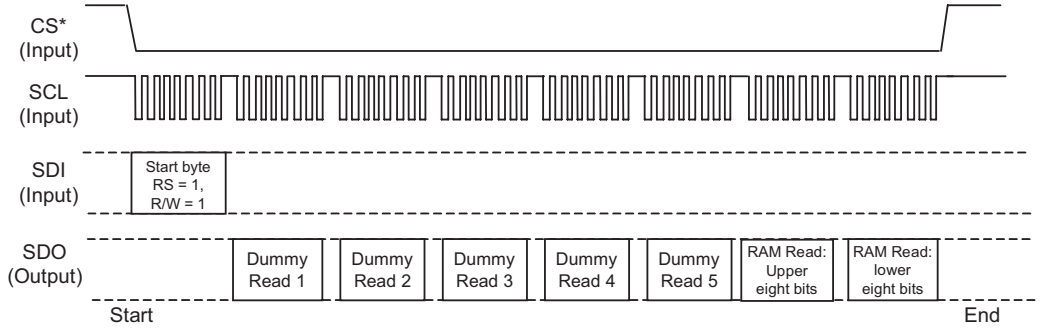


b) Timing of consecutive Data-Transfer through Clock-Synchronized Serial Bus Interface



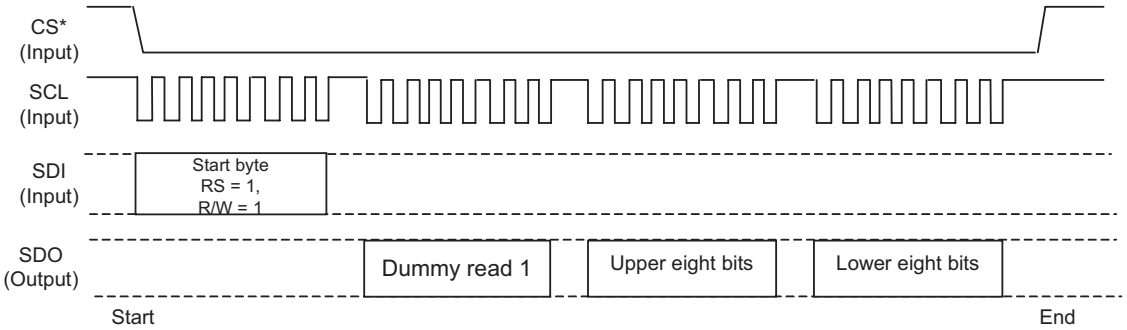
Procedure for Transfer on Clock-Synchronized Serial Bus Interface (cont)

c) RAM Data/Instruction Read



Note: Fifth bytes of the RAM read data after the start byte are invalid. The HD66776 starts to read the correct RAM data from the sixth byte.

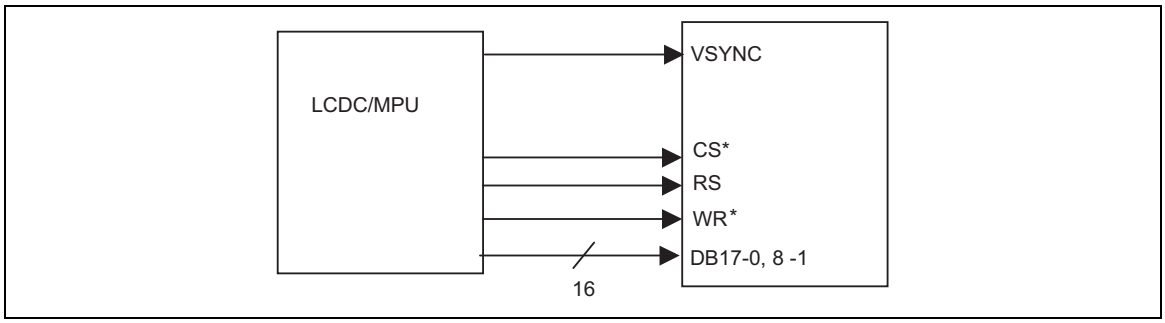
d) Status Read/Instruction Read



Note: One byte of the read data after the start byte are invalid. The HD66776 starts to read the correct data from the second byte.

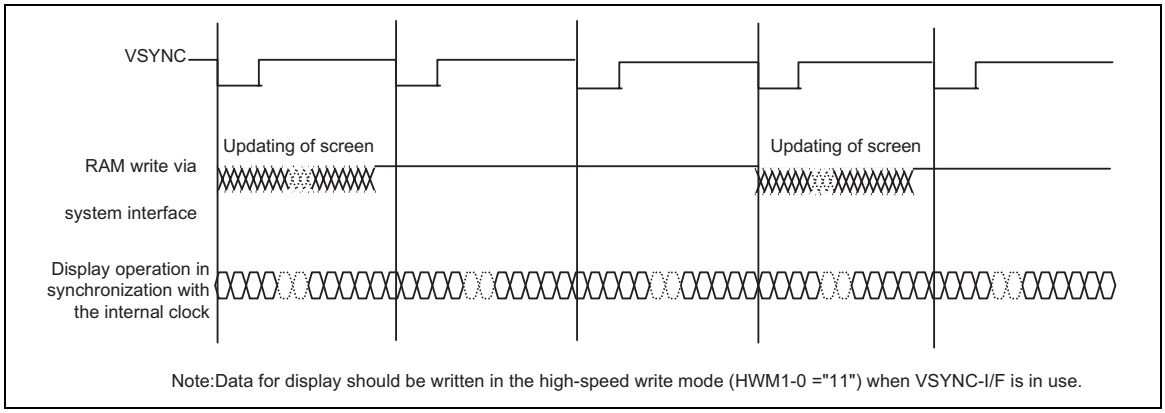
VSYNC Interface

The HD66776 incorporates VSYNC-I/F, which enables moving pictures to be displayed with only the system interface and the frame synchronization signal (VSYNC). This interface requires minimal changes from the system interface to display moving pictures.



When DM1-0 = “10” and RM = “0”, VSYNC-I/F is available. In this interface the internal display operation is synchronized with VSYNC. Data for display is written to RAM via the system interface with higher speed than for internal display operation. This method enables flicker-free display of moving pictures with the system interface.

Display operation can be achieved by using the internal clock generated by the internal oscillator and the VSYNC input. Because all the data for display is written to RAM, only the data to be rewritten is transferred. This method reduces the amount of data transferred during moving picture display operation. The high-speed write mode (HWM1-0 = “11”) achieves both low power consumption and high-speed access.



VSYNC-I/F requires taking the minimum speed for RAM writing via the system interface and the frequency of the internal clock into consideration. RAM writing should be performed with higher speed than the result obtained from the calculation shown below.

- Internal clock frequency (fosc) [Hz] = Frame frequency × (Display raster-row (NL) + Front porch (FP) + Back porch (BP)) × 16 Clock × Fluctuation
- Minimum speed for RAM writing [Hz] > 256 × Display raster-row (NL) / {((Back porch (BP) + Display raster-row (NL) - Margin) × 16 clock) / fosc}

Note: When RAM writing does not start immediately after the falling edge of VSYNC, the time between the falling edge of VSYNC and the RAM writing start timing must also be considered.

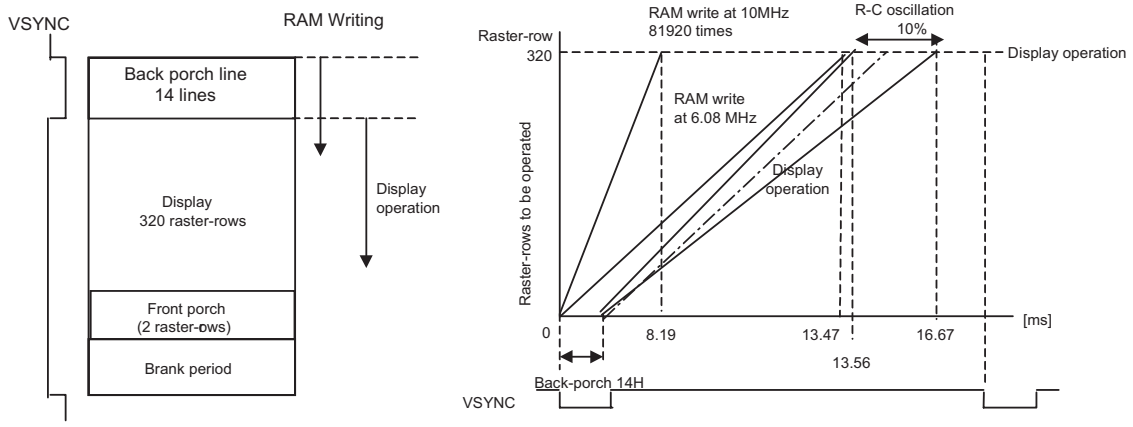
An example is shown below.
Example
Display size 256 RGB × 320 raster-rows
Display raster-row 320 raster-rows (NL = 100111)
Back/front porch 14/2 raster-rows (BP = 1110/FP = 0010)
Frame frequency 60 Hz

Internal clock frequency (fosc) Hz = 60 Hz × (320 + 2 + 14) × 16 Clock × 1.1 / 0.9 = 394 kHz

Note 1: Calculating the internal clock frequency requires considering the fluctuation. In the above case a 10% fluctuation within the VSYNC period is assumed.
Note 2: The fluctuation includes LSI production variation and air temperature fluctuation. Other fluctuations, including those for the external resistors and the supplied power, are not included in this example. Please keep in mind that a margin for these factors is also needed.

Minimum speed for RAM writing Hz > 256 × 320 / {((14 + 320 - 2) raster-rows × 16 clock) / 394 kHz} = 6.08 MHz

Note 3: In this case RAM writing starts immediately after the falling edge of VSYNC.
Note 4: The margin for display raster-row should be two raster-rows or more at the completion of RAM writing for one frame.

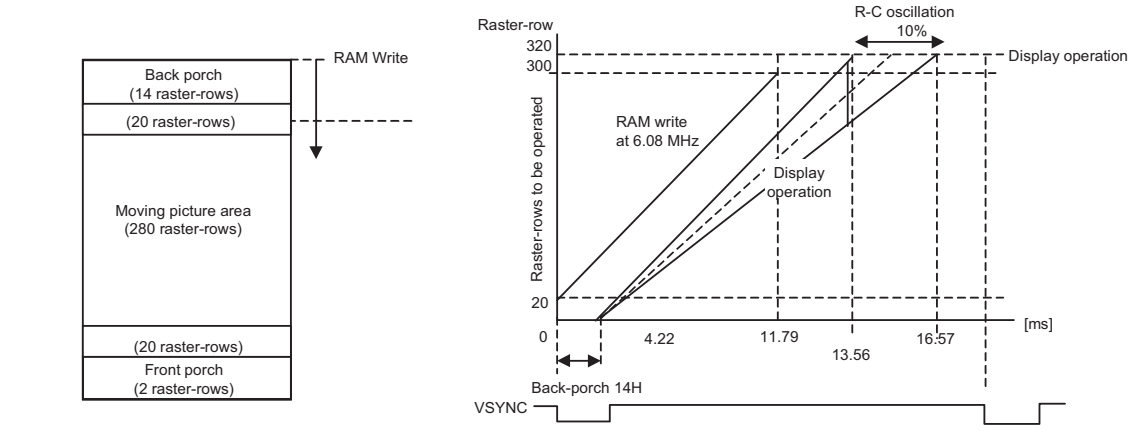


Operation for VSYNC Interface

Usage on VSYNC Interface

1. The Example above is a calculated value. Please keep in mind that a margin for these factors is also needed. Because production variation of the internal oscillator requires consideration.

2. The example above is a calculated value of rewriting the whole screen. A limitation of the moving picture area generates a margin for the RAM write speed.



Limitation of Moving Picture Area

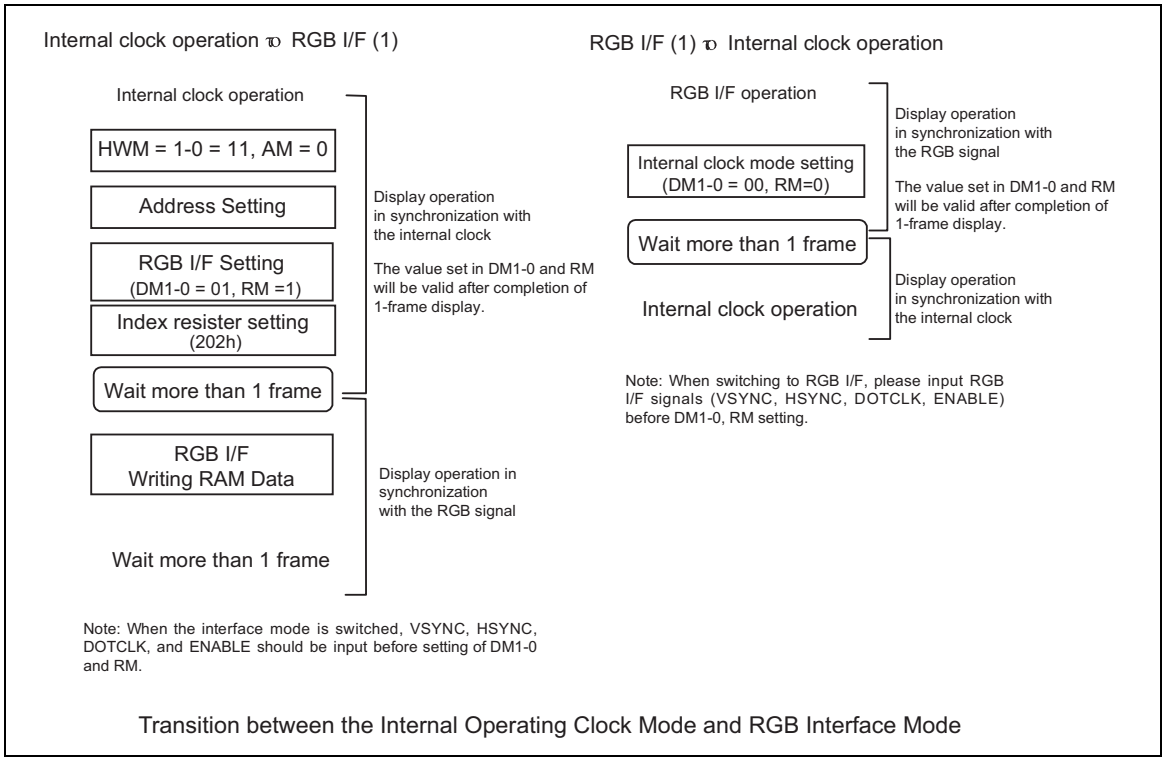
3. During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

4. Transition between the internal clock operation mode (DM1-0 = 00) and VSYNC interface mode will be valid after the completion of the screen which is displayed when the instruction is set.

5. Partial display, vertical scroll, and interlaced driving functions are not available on VSYNC interface mode.

6. The VSYNC interface is performed by the method above, therefore, AM bit should be 0.

7. Data for display should be written in high-speed write mode (HWM1-0 = 11) when the VSYNC interface is in use.



Transition between the Internal Operating Clock Mode and RGB Interface Mode

External Display Interface

The following interfaces are available as external display interface. It is determined by setting bits of RIM1-0. RAM accesses can be performed via the RGB interface.

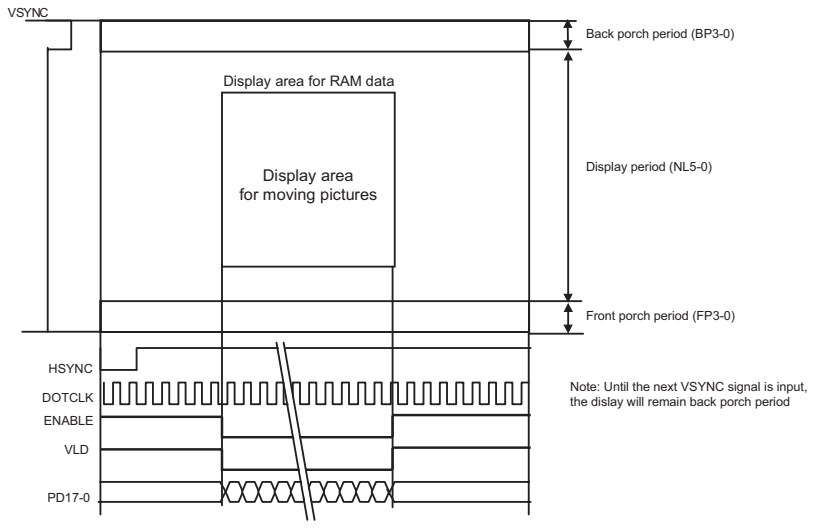
RIM Bits

RIM1	RIM0	RGB Interface	PD Pin
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface	PD17-12
1	1	Setting disabled	

Note: Multiple interfaces cannot be used.

RGB interface

The RGB-I/F is performed in synchronization with VSYNC, HSYNC, and DOTCLK. Combining the function of the high-speed write mode (HWM1-0 = 11) and the window address enables transfer only the screen to be updated and reduce the power consumption.



VSYNC:Frame synchronization signal
HSYNC:Raster-row synchronization signal
DOTCLK:Dot clock

ENABLE:Data enable signal
VLD: Data valid signal
PD17-0: Display data for RGB (6:6:6)

Back porch period (BPP):14H>=BP3-0>=2H
Front porch period (FPP):14H>FP3-0>=2H
FPP + BPP = 16H
Display operation period:NL5-0=<320H
The number of raster-rows of 1 frame: FPP + DP + BPP

VLD and ENABLE signals

The relationship between VLD and ENABLE signals is shown below.

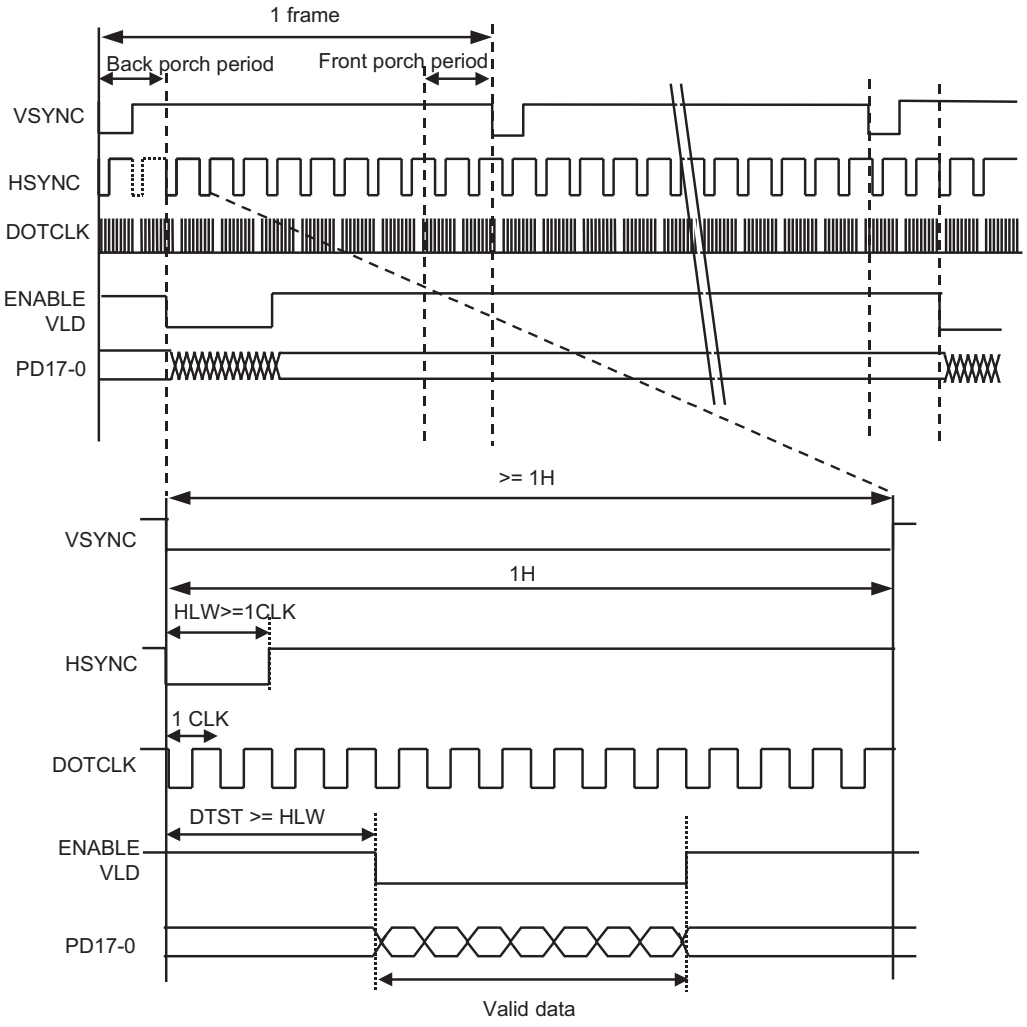
Relationship between VLD and ENABLE

ENABLE	VLD	RAM Write	RAM Address
0	0	Valid	Updated
0	1	Invalid	Updated
1	*	Invalid	Hold

RGB interface timing

16/18-bit RGB interface timing

Timing chart for RGB-I/F is shown below.

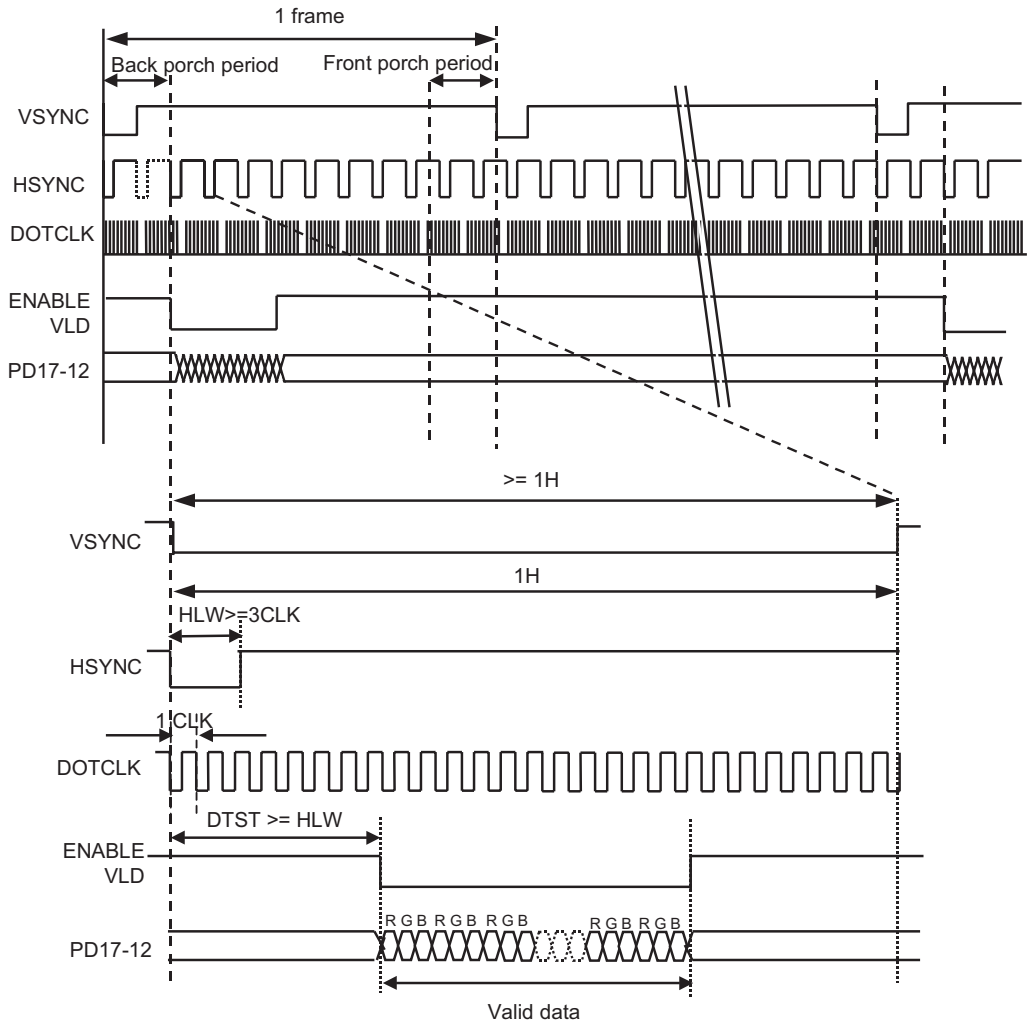


VLW: The period in which VSYNC is low level
HLW: The period in which HSYNC is low level
DTST: Set up time for data transfer

Note: Data for display should be written in the high-speed write mode (HWM1-0=11) in RGB-I/F is in use.

6-bit RGB interface timing

Timing chart for RGB-I/F is shown below.



VLW: The period in which VSYNC is low level
HLW: The period in which HSYNC is low level
DTST: Set up time for data transfer

Note 1:These clocks are regarded as one pixel for transfer when data is transferred in 6-bit interface.
2: VSYNC,. HSYNC., EVABLE, DOTCLK, VLC, and PD17-2 should be transferred in units of three clocks.
3: Data for display should be written in the high-speed write mode (HWM1-0=11) in RGB-I/F is in use.

Moving picture display

The HD66776 incorporates RGB interface to display moving pictures and RAM to store data for display. For displaying moving pictures, the HD66772 has the following features.

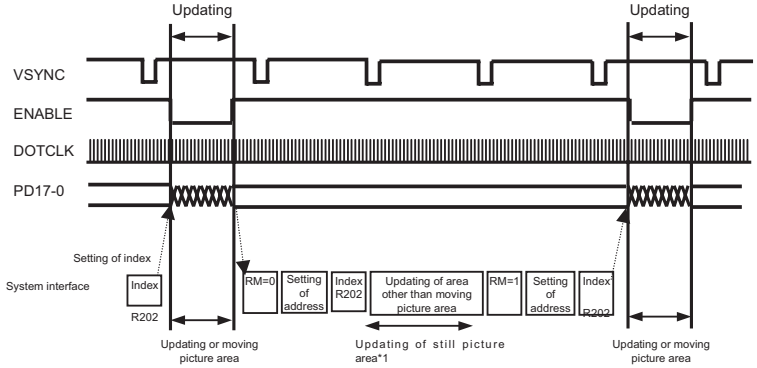
- Moving picture area can only be transferred by the window address function
- The high-speed write mode achieves both low power consumption and high-speed access
- Moving picture area to be rewritten can only be transferred.
- Reducing the amount of data transferred enables reduce the power consumption to the whole system.

Still picture area, such as an icon, can be updated while displaying moving pictures combining with the system interface.

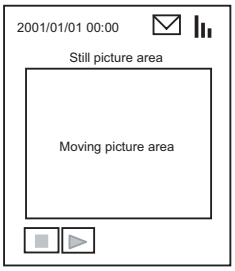
RAM access via the system interface when RGB-I/F is in use

RAM can be accessed via the system interface when RGB-I/F is in use. When data is written to RAM during RGB-I/F mode, the ENABLE bit should be high to stop data writing via RGB-I/F, because RAM writing is always performed in synchronization with the DOTCLK input when ENABLE is low. When RM = “0”, RAM access via the system interface is available. Before the next RAM access via RGB-I/F, set RM = “1” and index to R202h after waiting some time for a write/read bus cycle. When a RAM write conflict occurs, data writing is not guaranteed.

Example of display moving picture via RGB-I/F and updating still picture via the system interface are shown below.



Note 1: When RGB-I/F is in use, an address is set at every falling edge of VSYNC.
2: An address and an index (R202h) should be set before RAM is accessed via RGB-I/F.
3: The high-speed write mode (HWM1-0 = "11") should be used in RGB-I/F and VSYNC-I/F.

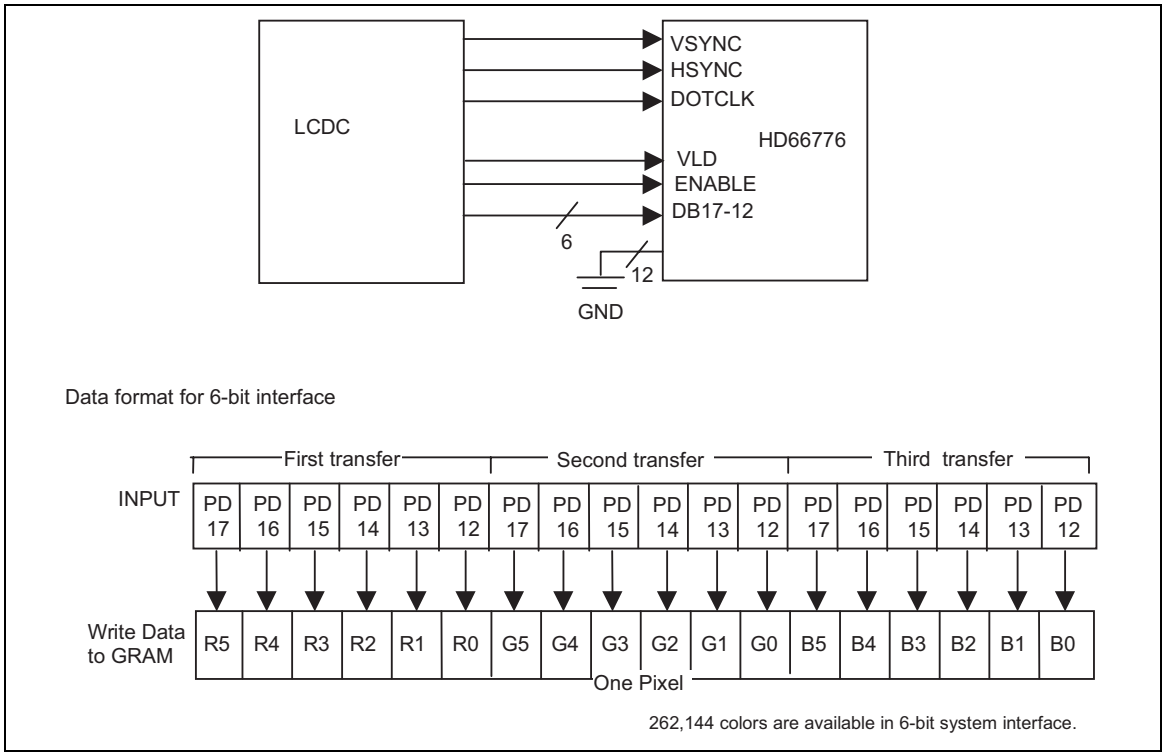


Example of Updating Still Picture Area during Diaplaying Moving Picture

6-bit RGB interface

6-bit RGB interface can be used by setting RIM1-0 to 10. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM via 6-bit RGB data bus (PD17-12), the data valid signal (VLD), and the data enable signal (ENABLE). Unused pins (DB11 to 0) must be fixed to the Vcc or GND level.

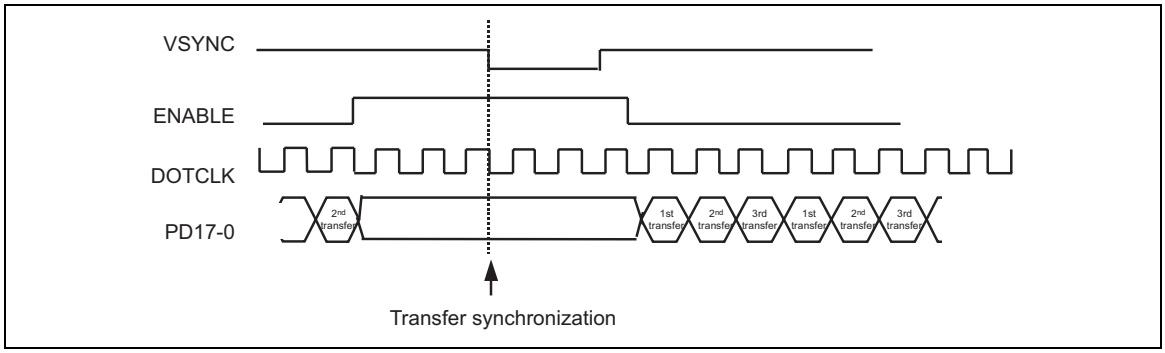
Note: Instructions should be set via the system interface.



Note: Transfer synchronization function for a 6-bit bus interface

The HD66776 has the transfer counter to count 1st, 2nd and 3rd data transfer in the 6-bit bus interface. The transfer counter is reset on the falling edge of VSYNC and enters the 1st data transmission state. Transfer mismatch can be corrected by a reset triggered on the falling edge of VSYNC, which means the beginning of a frame. The next transfer restarts correctly. In this method, when data is consecutively transferred such as displaying moving pictures, the effect of transfer mismatch will be reduced and recover normal operation.

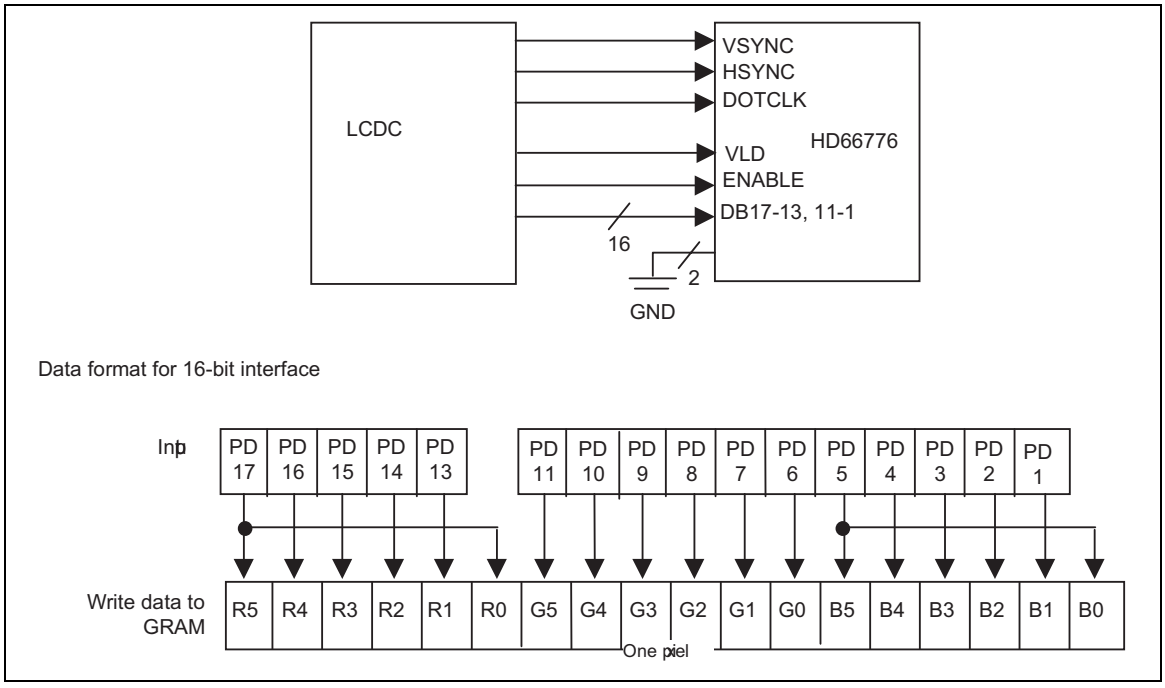
Note: The internal display is operated in units of three DOTCLK. When the DOTCLK is not input in units of pixels, clock mismatch occurs and the frame which is operated and the next frame are not displayed correctly.



16-bit RGB interface

16-bit RGB interface can be used by setting RIM1-0 to “01”. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM in synchronization with display operation via 16-bit RGB data bus (PD17-13 and 11-1), the data valid signal (VLD) and data enable signal (ENABLE).

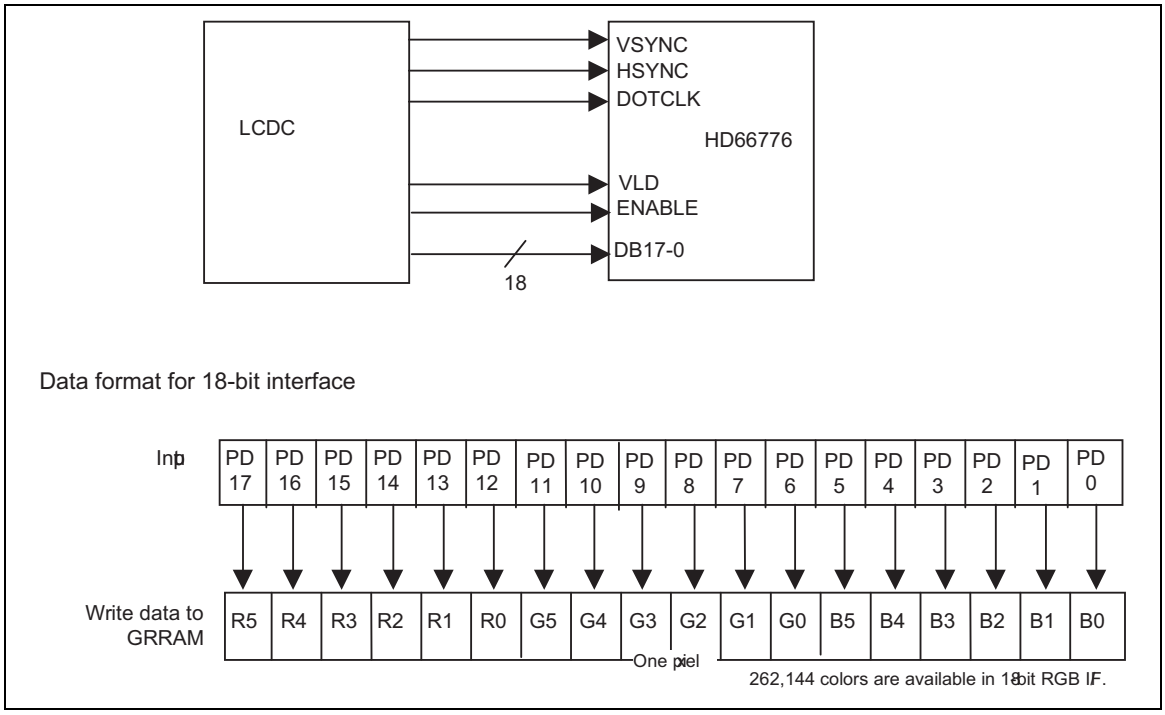
Note: Instructions should be set via the system interface.



18-bit RGB interface

18-bit RGB interface can be used by setting RIM1-0 to “00”. Display operation is synchronized with VSYNC, HSYNC, and DOTCLK signals. Data for display is transferred to the internal RAM in synchronization with display operation via 18-bit RGB data bus (PD17-0), the data valid signal (VLD) and data enable signal (ENABLE).

Note: Instructions should be set via the system interface.



Usage on external display interface

a) When external display interface is in use, the following functions are not available.

Relationship between VLD and ENABLE

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Graphics operation function	Not available	Available

b) VSYNC, HSYNC, and DOTCLK signals should be supplied during display operation via RGB-I/F.

c) RGB data is transferred for three clock cycles in 6-bit RGB-I/F. Data transferred, therefore, should be transferred in units of RGB.

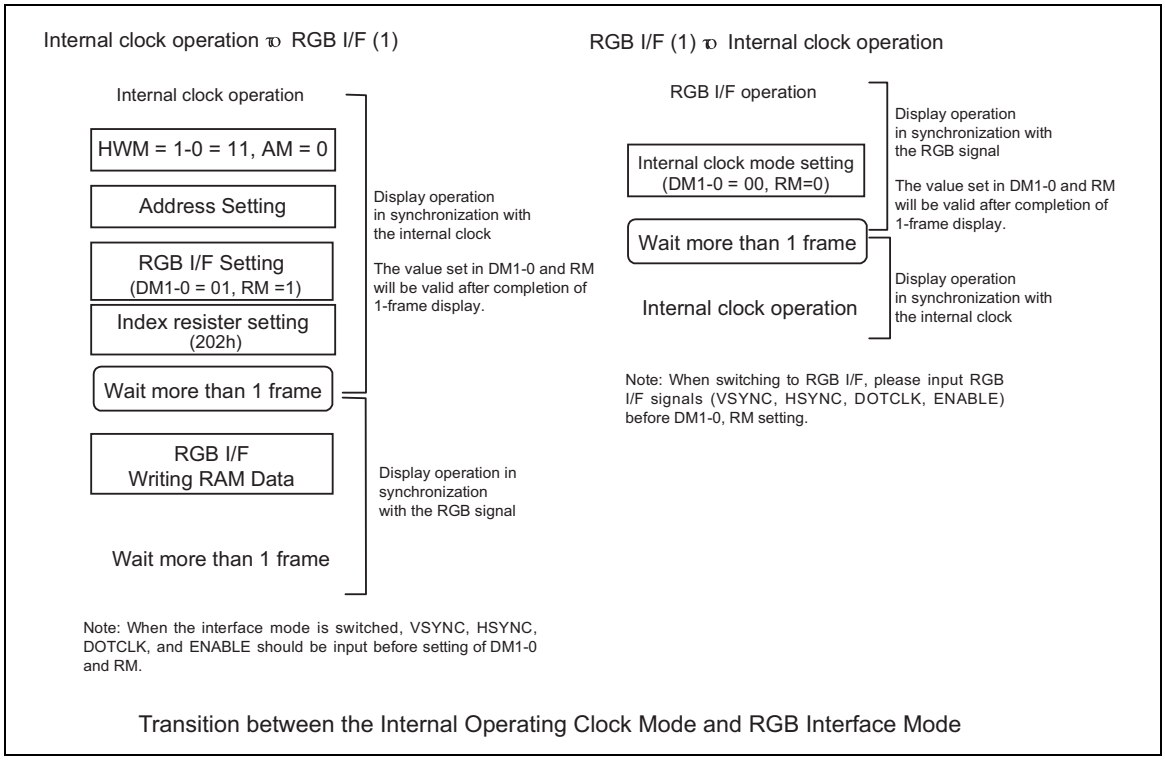
d) Interface signals, VSYNC, HSYNC, DOTCL, ENABLE, VLD,6-bit RGB-I/F and PD17-12 should be set in units of RGB (pixels) to match RGB transfer.

e) Transitions between internal operation mode and external display interface should follow the mode transition sequence shown below.

f) During the period between the completion of displaying one frame data and the next VSYNC signal, the display will remain front porch period.

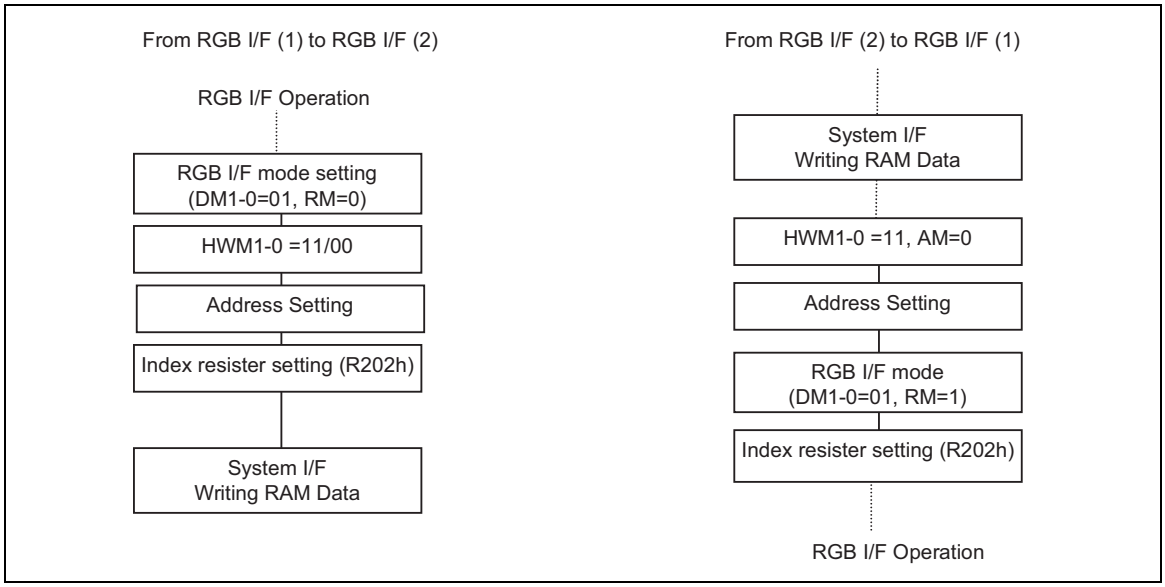
g) RGB-I/F should be used in high-speed write mode (HWM1-0 = 11).

h) An address set is done on the falling edge of VSYNC every frame in RGB-I/F.



Transition between the Internal Operating Clock Mode and RGB Interface Mode

Writing RAM data from system I/F during displaying RGB I/F

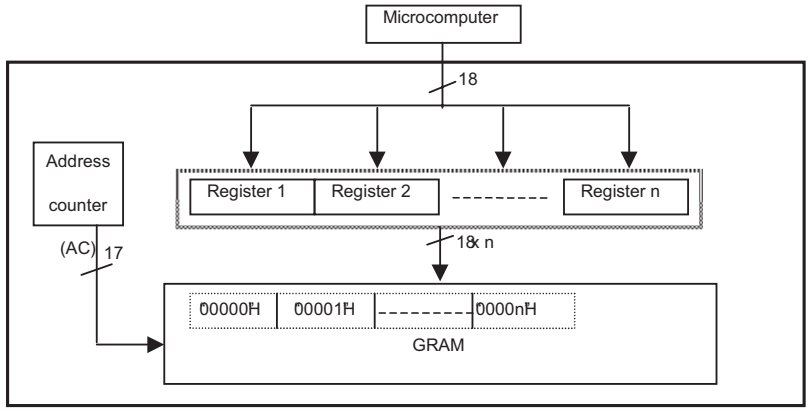


High-Speed Burst RAM Write Function

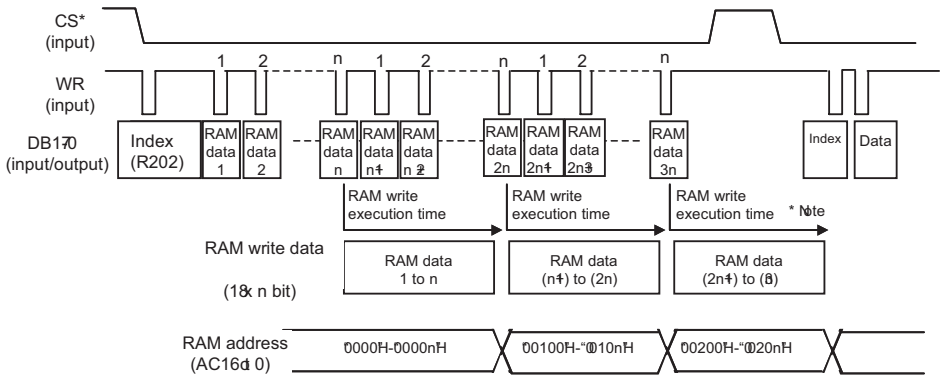
The HD66776 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications which require the high-speed rewriting of the display data, for example, display of color animations, etc.

When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the HD66776 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.

a) Action flow of high-speed consecutive RAM writing



b) Wxample of high-speed consecutive RAM writing



Note: When a high-speed RAM wirte is canceled, the next instruction must only be executed after the RAM write execution time has elapsed (Bus cycle fire (tCYC) at normal write mode).

When high-speed RAM write mode is used, note the following.

Notes: 1. RAM writing is executed by one-raster-row. And data is not written into RAM when writing is finished before data fills the horizontal window setting area.
2. When the index register and RAM data write (202H) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM1-0 must be set to "00" while RAM is being read.
3. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.

Comparison between Normal and High-Speed RAM Write Operations

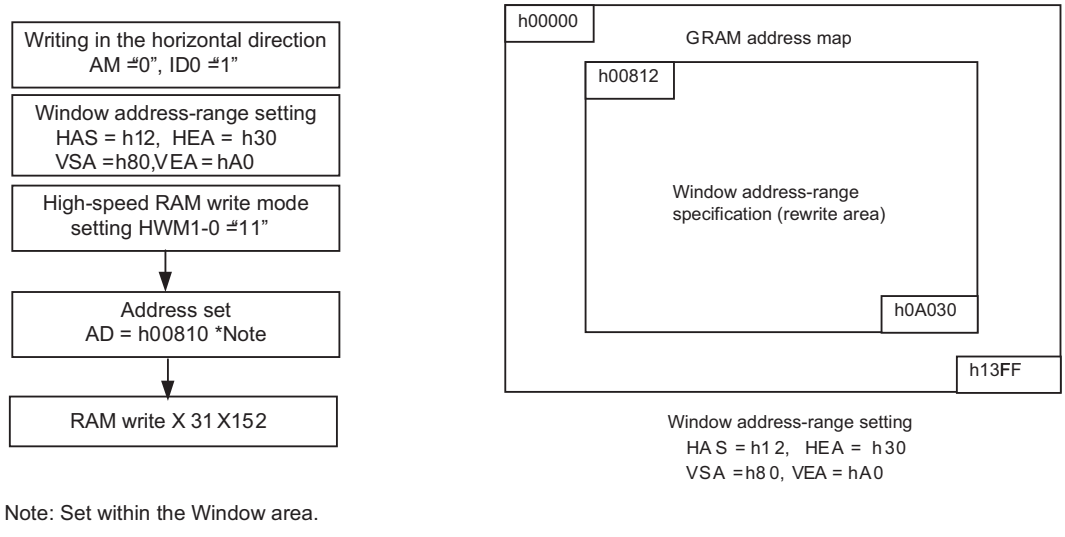
	Normal RAM Write (HWM1-0= "00")	**High-Speed RAM Write (HWM1-0= "11")**
BGR function	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word unit	Can be specified by word unit
RAM read	Can be read by word unit	Can not be used
RAM write	Can be written by word unit	Can be written by every raster-row
Window address	Can be set by word unit (Minimum range: 1 word x 1 line)	More than eight words are needs to be set. Can be set by word unit. (Minimum range: 8 word x 1 line)
External display interface	Can be used	Can be used

High-Speed RAM Write in the Window Address

When a window address range is specified, RAM data which is in an optional window area can be rewritten consecutively and quickly.

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be rewritten to consecutively and quickly by using the window address-range specification bits (HSA7 to 0, HEA7 to 0).



Note: Set within the Window area.

Example of the High-Speed RAM Write with a Window Address-Range Specification

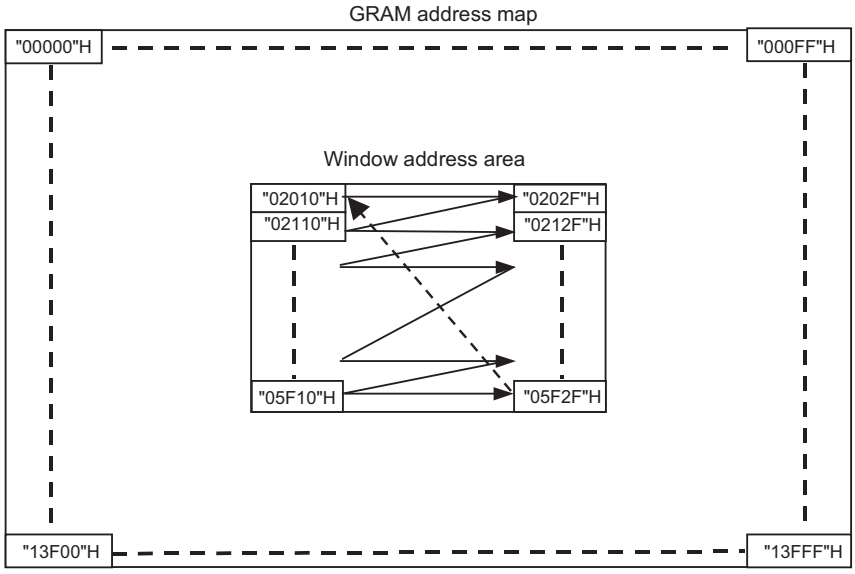
Window Address Function

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7 to 0, end: HEA 7 to 0) or the vertical address register (start: VSA8 to 0, end: VEA8 to 0) can be written to consecutively.

Data is written to addresses in the direction specified by the AM bit (increment/decrement). When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.

The window must be specified to be within the GRAM address area described below. Addresses must be set within the window address.

[Restriction on window address-range settings]
(Horizontal direction) 00H ≤ HEA7 to 0 ≤ HEA7 to 0 ≤ “FF”H
(Vertical direction) 00H ≤ VSA8 to 0 ≤ VEA8 to 0 ≤ “13F”H
[Restriction on address settings during the window address]
(RAM address) HSA7 to 0 ≤ AD7 to 0 ≤ HEA7 to 0
VSA8 to 0 ≤ AD16 to 8 ≤ VEA8 to 0



Window address-range specification area
HSA7 to 0 = "10"H, HEA 7 to 0 = "2F"H
VSA8 to 0 = "020"H, VEA8 to 0 = "05F"H
I/D = "1" (increment)
AM = "0" (horizontal writing)

Example of Address Operation in the Window Address Specification

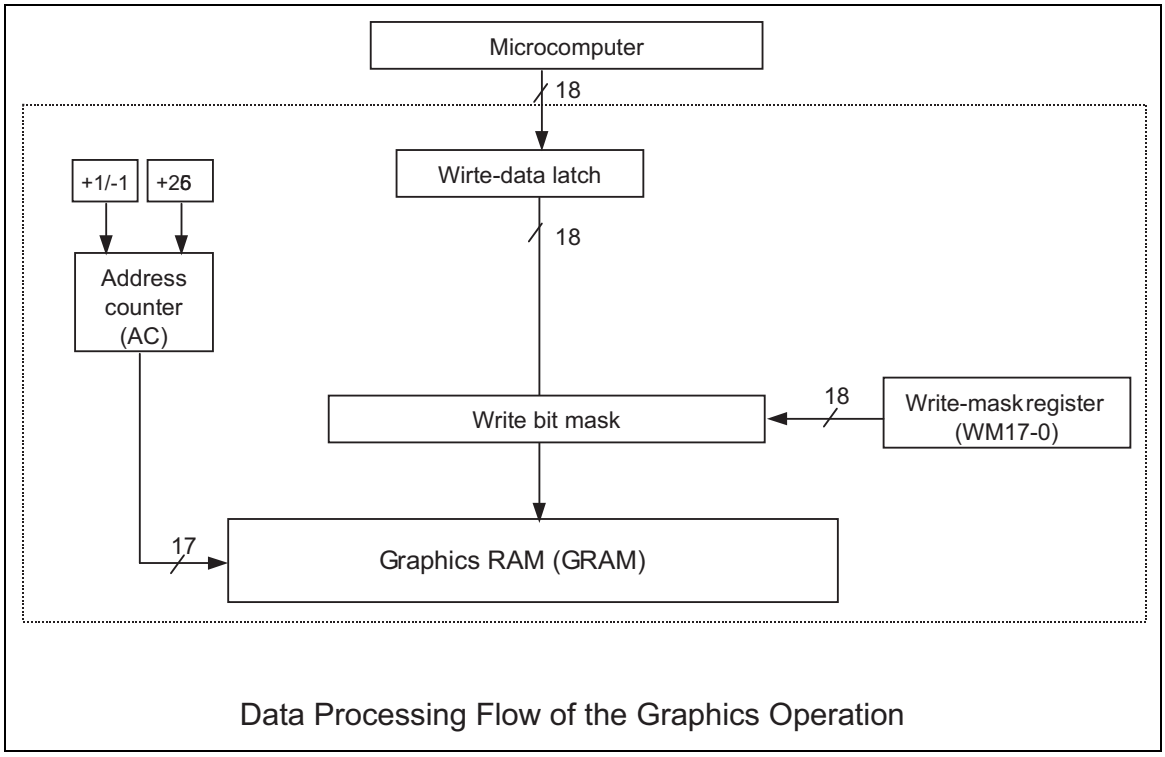
Graphics Operation Function

The HD66776 can greatly reduce the load of the microcomputer graphics software processing through the 18-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 18-bit write data.
The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the write from the microcomputer.

Graphics Operation

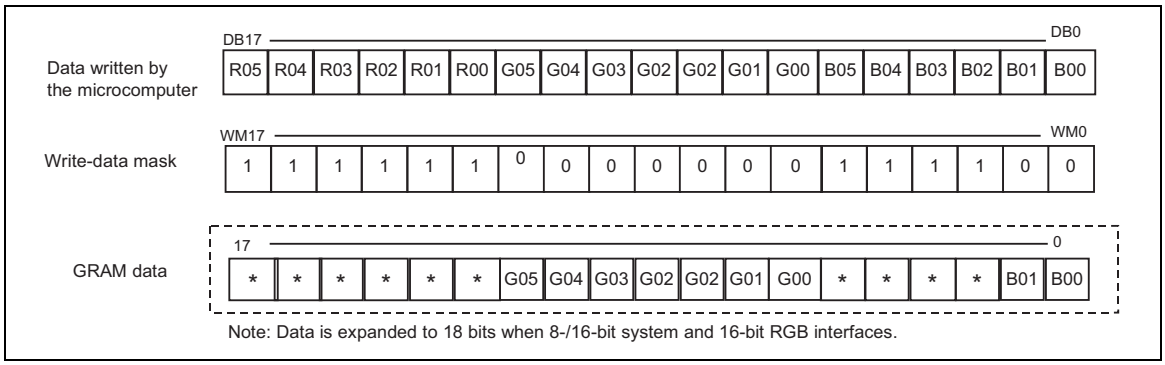
Operation Mode	I/D	AM	Operation and Usage
Write mode 1	0/1	0	Horizontal data replacement
Write mode 2	0/1	1	Vertical data replacement



Data Processing Flow of the Graphics Operation

Write-data Mask Function

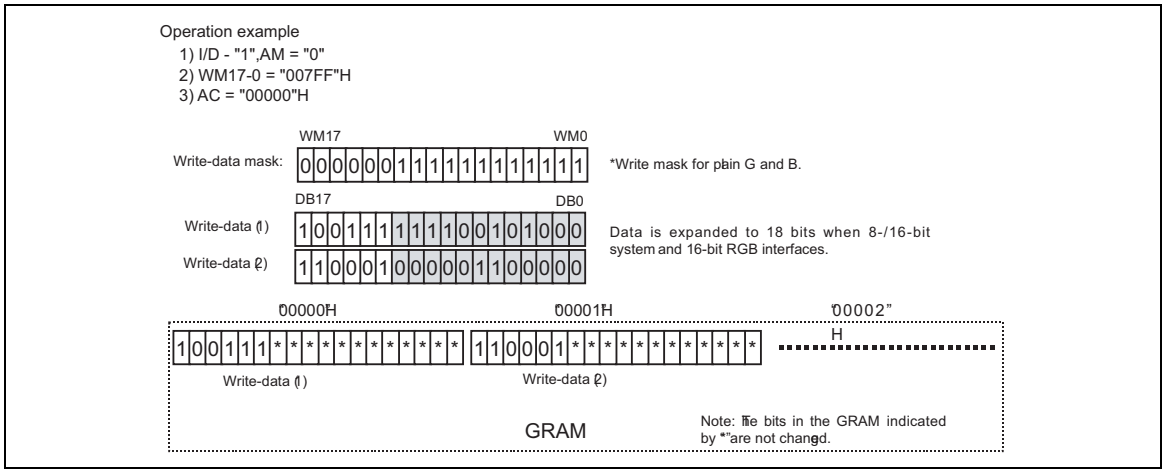
The HD66776 expands 16-bit data sent from the microcomputer to 18-bit data (when 18-bit interface is in use, data is not expanded). A bit-wise write-data mask function controls writing the 18-bit data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM17–0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is retained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.



Graphics Operation Processing

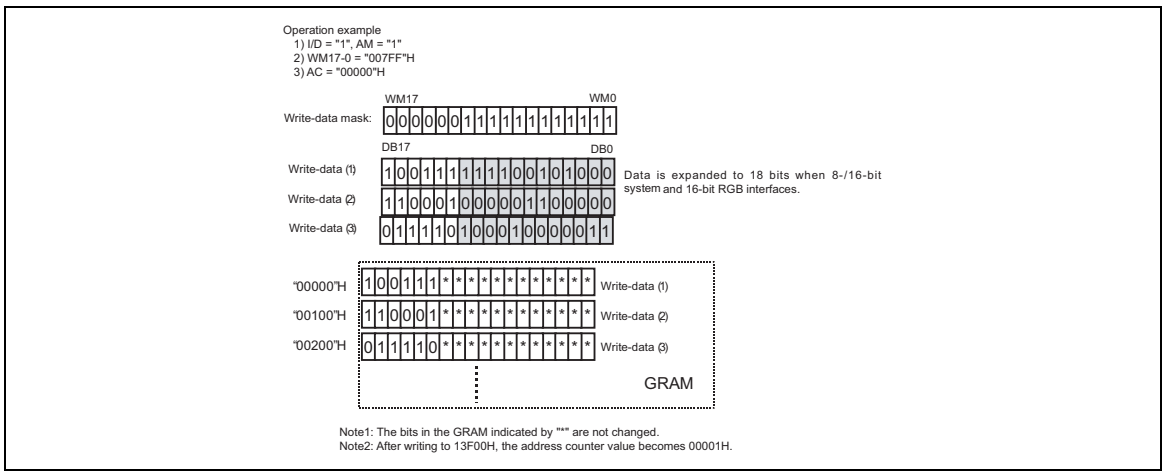
1. Write mode 1: AM = “0”

   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM17–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = “1”) or decrements by -1 (I/D = “0”), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.



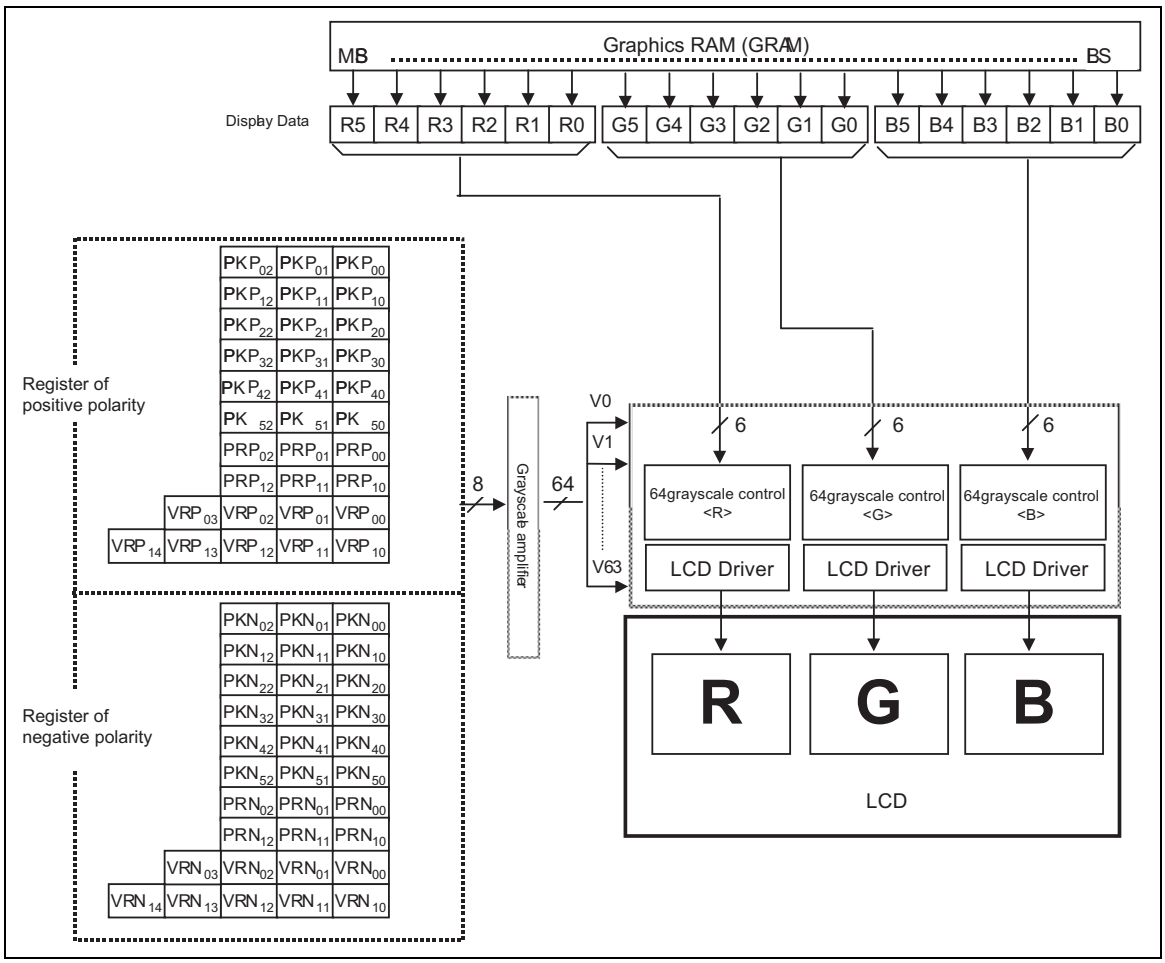
2. Write mode 2: AM = “1”

   This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM17–0) are also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = “1”) or upper-left edge (I/D = “0”) following the I/D bit after it has reached the lower edge of the GRAM.



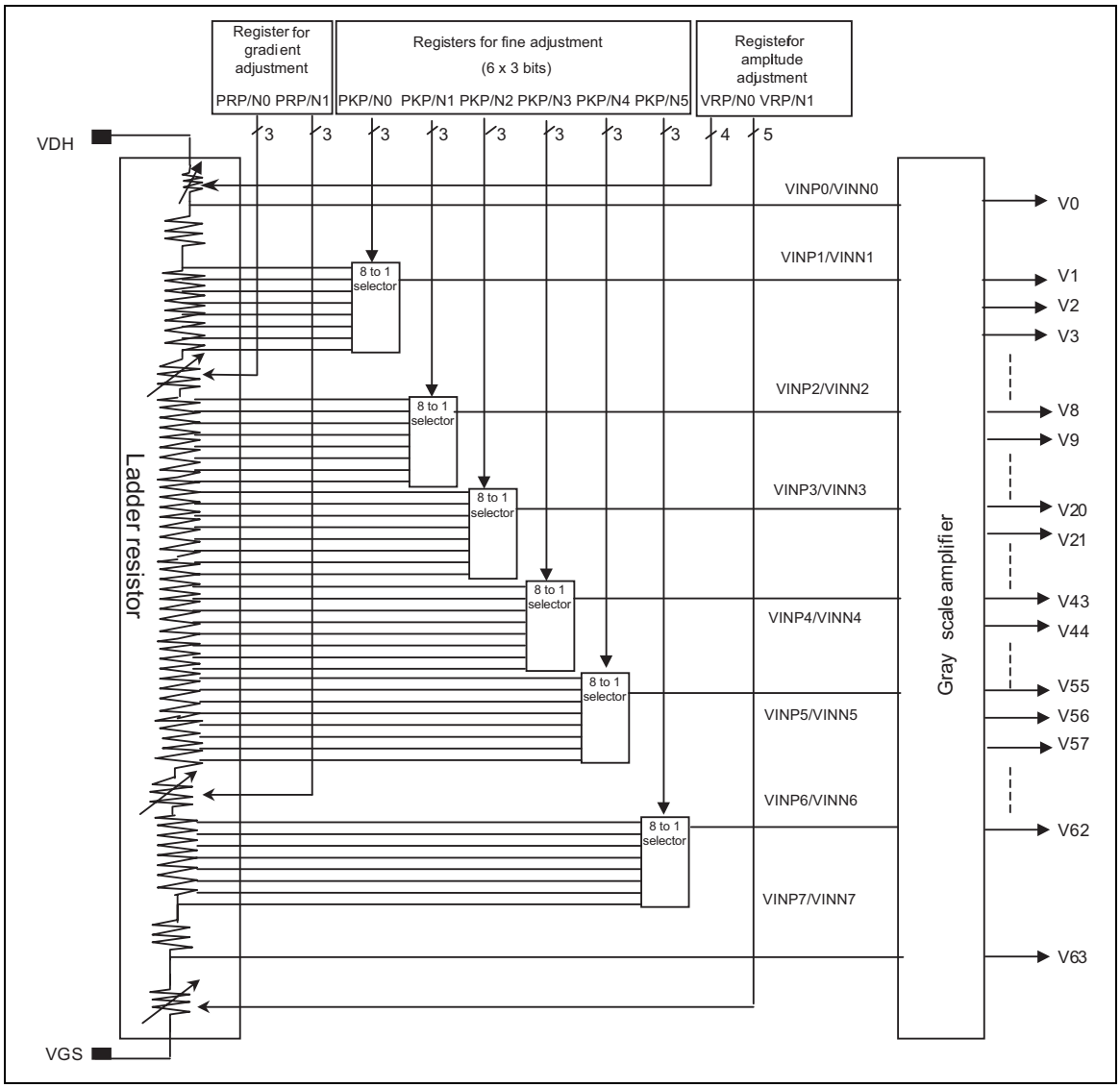
γ-Correction Function

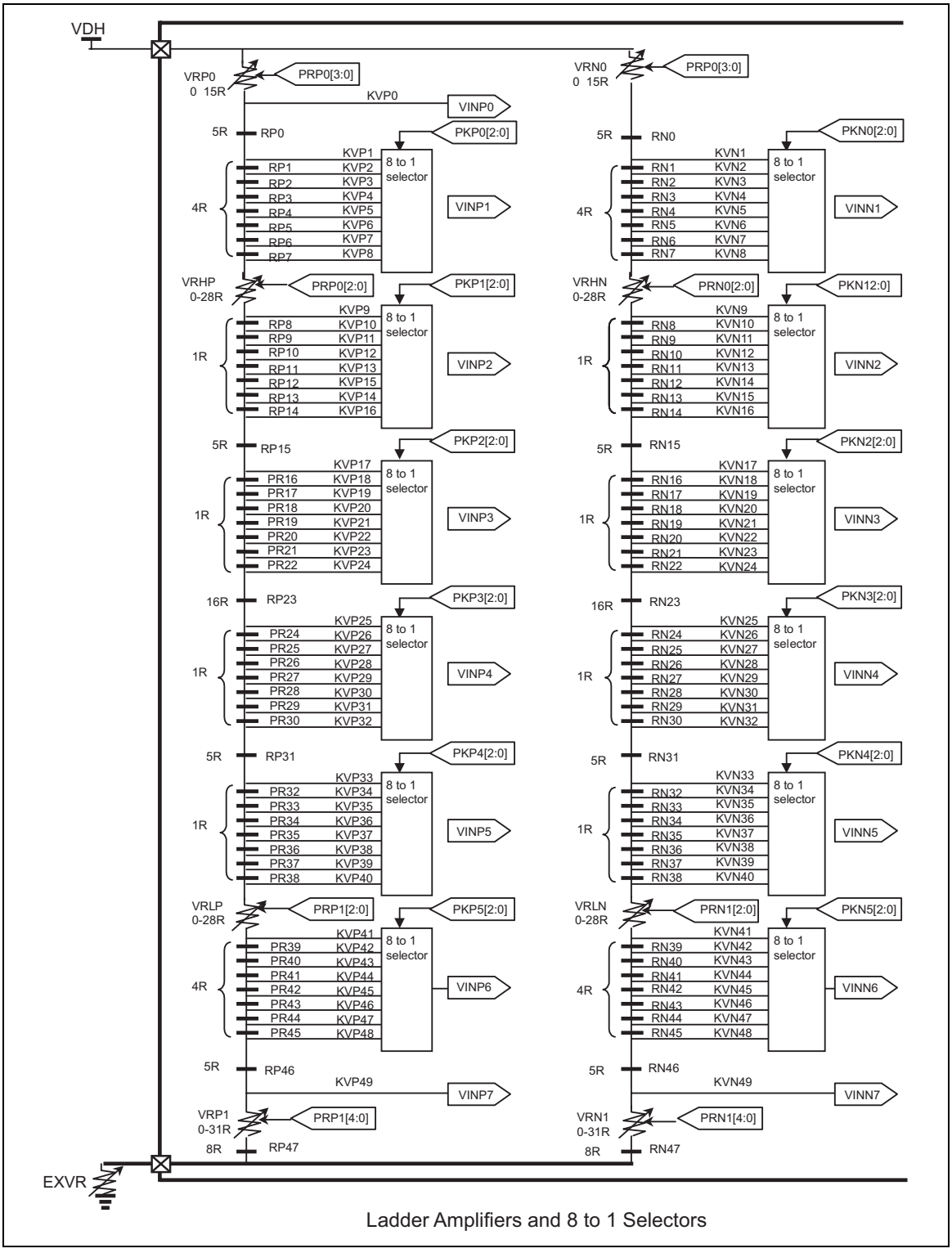
The HD66776 incorporates a γ-correction function to simultaneously display 262,144 colors. The γ-correction operation specifies eight levels of grayscale with gradient-adjustment and fine-adjustment registers. Select the polarity of these registers to match the LCD panel used. These registers are available for both polarities.



Configuration of Grayscale Amplifier

Eight levels (VIN0-7) are specified by the gradient-adjustment and fine-adjsutment registers. 64-levels (V0-63) are generated by ladder resistors, which divide each level specified by the registers into more detailed levels.

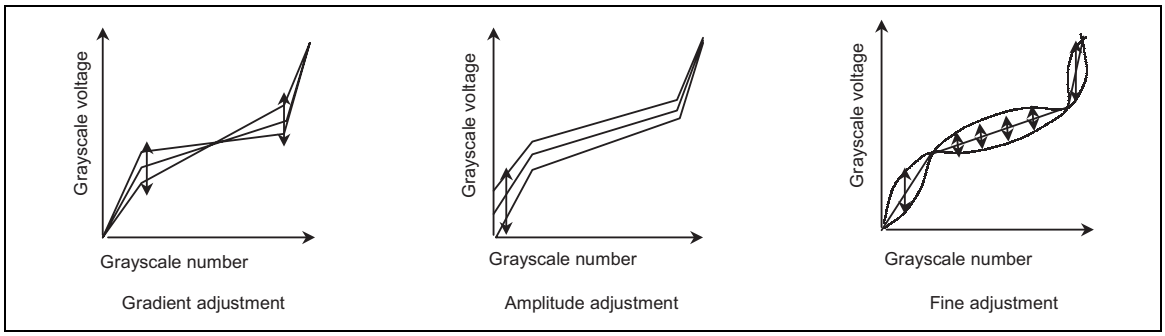




Ladder Amplifiers and 8 to 1 Selectors

γ-Correction Registers

This block has register groups for specifying a grayscale voltage that meets the γ-characteristics for the LCD panel used. These registers are divided into three groups, which correspond to the gradient, amplitude, and fine adjustment of the grayscale characteristics for the voltage. The polarity of each register can be specified independently (R, G, and B are common.).



1. Gradient adjustment registers

   The gradient adjustment registers are used to adjust the gradient in the middle of the grascale characteristics for the voltage without changing the dynamic range. This function is implemented by controlling the variable resistor (VRHP (N)0/VRL(N)1) in the ladder resistor block for grayscale voltage generation. A register can be separated into positive/negative polarities to perform an asymmetric drive.

2. Amplitude adjustment registers

   The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. This function is implemented by controlling the variable resistor (VRP (N)/0VRP(N)1) under the ladder resistor block for grayscale voltage generation. The VDH level can be adjusted higher. There is an independent register on the positive/negative polarities as well as the gradient adjustment register.

3 Fine adjustment registers

   The fine adjustment register is no make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent register on the positive/negative polarities as well as other adjustment registers.

Correction Registers

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 2 to 0	PRN0 2 to 0	Variable resistor VRHP (N)
	PRP1 2 to 0	PRN1 2 to 0	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 3 to 0	VRN0 3 to 0	Variable resistor VRP (N)0
	VRP1 4 to 0	VRN1 4 to 0	Variable resistor VRP (N) 1
Fine adjustment	PKP0 2 to 0	PKN0 2 to 0	8-to-1 selector (voltage level of grayscale 1)
	PKP1 2 to 0	PKN1 2 to 0	8-to-1 selector (voltage level of grayscale 8)
	PKP2 2 to 0	PKN2 2 to 0	8-to-1 selector (voltage level of grayscale 20)
	PKP3 2 to 0	PKN3 2 to 0	8-to-1 selector (voltage level of grayscale 43)
	PKP4 2 to 0	PKN4 2 to 0	8-to-1 selector (voltage level of grayscale 55)
	PKP5 2 to 0	PKN5 2 to 0	8-to-1 selector (voltage level of grayscale 62)

Ladder resistors and 8 to 1 selector

Block configuration

The block consists of two ladder resistors including variable one, and 8 to 1 selector which selects one voltage level generated by the ladder resistors and outputs the reference voltage for grayscale voltage. Furthermore, the block has pins to connect a variable resistor. It can adjust the variation between panels.

Variable resistor

The variable resistors are two types, gradient adjustment (VRHP(N)/VRLP(N)), and amplitude adjustment (VRP(N)0/VRP(N)1). The resistances are set by the gradient adjustment and amplitude adjustment registers. Their relationship is shown below.

Gradient Adjustment (1)	
Register value PRP(N)0[2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Gradient Adjustment (1)	
Register value PRP(N)1[2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Gradient Adjustment (1)	
Register value VRP(N)0[3:0]	Resistance value VRP(N)0
0000	0R
0001	1R
0010	2R
:	:
:	:
1101	13R
1110	14R
1111	15R

Gradient Adjustment (1)	
Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

8 to 1 selector

In the 8 to 1 selector, the voltage level can be selected from the levels which are generated by ladder resistors, and be output the six types of the reference voltage, the VIN1 to VIN6. The following figure explains the relationship between the fine adjustment register and the selecting voltage.

KVPP and KVPN

Contents of Register	**Selected Voltage**					
PKP(N)2-0	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels V0~V63 are calculated by the following formula.

Voltage formula (positive polarity)

Pins	Formula	Micro-adjsting register	Reference
KVP0	VDH- ΔV*VRP0/SUMRP	-	VINP0
KVP1	VDH- ΔV*(VRP0+5R)/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VDH- ΔV*(VRP0+9R)/SUMRP	PKP02-00 = "001"	
KVP3	VDH- ΔV*(VRP0+13R)/SUMRP	PKP02-00 = "010"	
KVP4	VDH- ΔV*(VRP0+17R)/SUMRP	PKP02-00 = "011"	
KVP5	VDH- ΔV*(VRP0+21R)/SUMRP	PKP02-00 = "100"	
KVP6	VDH- ΔV*(VRP0+25R)/SUMRP	PKP02-00 = "101"	
KVP7	VDH- ΔV*(VRP0+29R)/SUMRP	PKP02-00 = "110"	
KVP8	VDH- ΔV*(VRP0+33R)/SUMRP	PKP02-00 = "111"	
KVP9	VDH- ΔV*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VDH- ΔV*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VDH- ΔV*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VDH- ΔV*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VDH- ΔV*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VDH- ΔV*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VDH- ΔV*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VDH- ΔV*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VDH- ΔV*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VDH- ΔV*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VDH- ΔV*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VDH- ΔV*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VDH- ΔV*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VDH- ΔV*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VDH- ΔV*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VDH- ΔV*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VDH- ΔV*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VDH- ΔV*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VDH- ΔV*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VDH- ΔV*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VDH- ΔV*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VDH- ΔV*(VRP0+73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VDH- ΔV*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VDH- ΔV*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VDH- ΔV*(VRP0+80R+VRHP)/SUMRP	PKP42-00 = "000"	VINP5
KVP34	VDH- ΔV*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VDH- ΔV*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VDH- ΔV*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VDH- ΔV*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VDH- ΔV*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VDH- ΔV*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VDH- ΔV*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VDH- ΔV*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VDH- ΔV*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VDH- ΔV*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VDH- ΔV*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VDH- ΔV*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VDH- ΔV*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VDH- ΔV*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VDH- ΔV*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VDH- ΔV*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
SUMRN: Total of th enegative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1
ΔV: Voltage difference between VDH-VGS

Voltage Formula-2 (positive polarity)

grayscale voltage	Formula
V0	VINP0
V1	VINP1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINP2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINP3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINP4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINP5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINP6
V63	VINP7

Voltage Formula (Negative polarity)

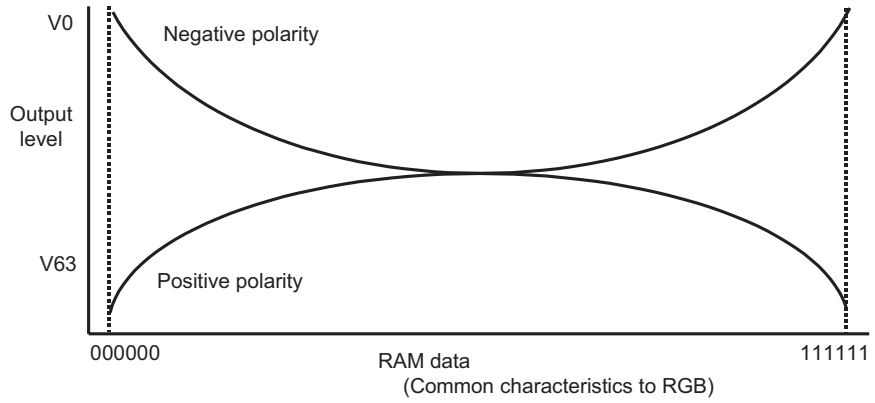
Pins	Formula	Micro-adjsting register	Reference
KVN0	VDH- ΔV*VRN0/SUMRN	-	VINN0
KVN1	VDH- ΔV*(VRN0+5R)/SUMRN	PKN02-00 = "000"	VINN1
KVN2	VDH- ΔV*(VRN0+9R)/SUMRN	PKN02-00 = "001"	
KVN3	VDH- ΔV*(VRN0+13R)/SUMRN	PKN02-00 = "010"	
KVN4	VDH- ΔV*(VRN0+17R)/SUMRN	PKN02-00 = "011"	
KVN5	VDH- ΔV*(VRN0+21R)/SUMRN	PKN02-00 = "100"	
KVN6	VDH- ΔV*(VRN0+25R)/SUMRN	PKN02-00 = "101"	
KVN7	VDH- ΔV*(VRN0+29R)/SUMRN	PKN02-00 = "110"	
KVN8	VDH- ΔV*(VRN0+33R)/SUMRN	PKN02-00 = "111"	
KVN9	VDH- ΔV*(VRN0+33R+VRHN)/SUMRN	PKN12-10 = "000"	VINN2
KVN10	VDH- ΔV*(VRN0+33R+VRHN)/SUMRN	PKN12-10 = "001"	
KVN11	VDH- ΔV*(VRN0+35R+VRHN)/SUMRN	PKN12-10 = "010"	
KVN12	VDH- ΔV*(VRN0+36R+VRHN)/SUMRN	PKN12-10 = "011"	
KVN13	VDH- ΔV*(VRN0+37R+VRHN)/SUMRN	PKN12-10 = "100"	
KVN14	VDH- ΔV*(VRN0+38R+VRHN)/SUMRN	PKN12-10 = "101"	
KVN15	VDH- ΔV*(VRN0+39R+VRHN)/SUMRN	PKN12-10 = "110"	
KVN16	VDH- ΔV*(VRN0+40R+VRHN)/SUMRN	PKN12-10 = "111"	
KVN17	VDH- ΔV*(VRN0+45R+VRHN)/SUMRN	PKN22-20 = "000"	VINN3
KVN18	VDH- ΔV*(VRN0+46R+VRHN)/SUMRN	PKN22-20 = "001"	
KVN19	VDH- ΔV*(VRN0+47R+VRHN)/SUMRN	PKN22-20 = "010"	
KVN20	VDH- ΔV*(VRN0+48R+VRHN)/SUMRN	PKN22-20 = "011"	
KVN21	VDH- ΔV*(VRN0+49R+VRHN)/SUMRN	PKN22-20 = "100"	
KVN22	VDH- ΔV*(VRN0+50R+VRHN)/SUMRN	PKN22-20 = "101"	
KVN23	VDH- ΔV*(VRN0+51R+VRHN)/SUMRN	PKN22-20 = "110"	
KVN24	VDH- ΔV*(VRN0+52R+VRHN)/SUMRN	PKN22-20 = "111"	
KVN25	VDH- ΔV*(VRN0+68R+VRHN)/SUMRN	PKN32-30 = "000"	VINN4
KVN26	VDH- ΔV*(VRN0+69R+VRHN)/SUMRN	PKN32-30 = "001"	
KVN27	VDH- ΔV*(VRN0+70R+VRHN)/SUMRN	PKN32-30 = "010"	
KVN28	VDH- ΔV*(VRN0+71R+VRHN)/SUMRN	PKN32-30 = "011"	
KVN29	VDH- ΔV*(VRN0+72R+VRHN)/SUMRN	PKN32-30 = "100"	
KVN30	VDH- ΔV*(VRN0+73R+VRHN)/SUMRN	PKN32-30 = "101"	
KVN31	VDH- ΔV*(VRN0+74R+VRHN)/SUMRN	PKN32-30 = "110"	
KVN32	VDH- ΔV*(VRN0+75R+VRHN)/SUMRN	PKN32-30 = "111"	
KVN33	VDH- ΔV*(VRN0+80R+VRHN)/SUMRN	PKN42-00 = "000"	VINN5
KVN34	VDH- ΔV*(VRN0+81R+VRHN)/SUMRN	PKN42-00 = "001"	
KVN35	VDH- ΔV*(VRN0+82R+VRHN)/SUMRN	PKN42-00 = "010"	
KVN36	VDH- ΔV*(VRN0+83R+VRHN)/SUMRN	PKN42-00 = "011"	
KVN37	VDH- ΔV*(VRN0+84R+VRHN)/SUMRN	PKN42-00 = "100"	
KVN38	VDH- ΔV*(VRN0+85R+VRHN)/SUMRN	PKN42-00 = "101"	
KVN39	VDH- ΔV*(VRN0+86R+VRHN)/SUMRN	PKN42-00 = "110"	
KVN40	VDH- ΔV*(VRN0+87R+VRHN)/SUMRN	PKN42-00 = "111"	
KVN41	VDH- ΔV*(VRN0+87R+VRHN+VRLN)/SUMRN	PKN52-50 = "000"	VINN6
KVN42	VDH- ΔV*(VRN0+91R+VRHN+VRLN)/SUMRN	PKN52-50 = "001"	
KVN43	VDH- ΔV*(VRN0+95R+VRHN+VRLN)/SUMRN	PKN52-50 = "010"	
KVN44	VDH- ΔV*(VRN0+99R+VRHN+VRLN)/SUMRN	PKN52-50 = "011"	
KVN45	VDH- ΔV*(VRN0+103R+VRHN+VRLN)/SUMRN	PKN52-50 = "100"	
KVN46	VDH- ΔV*(VRN0+107R+VRHN+VRLN)/SUMRN	PKN52-50 = "101"	
KVN47	VDH- ΔV*(VRN0+111R+VRHN+VRLN)/SUMRN	PKN52-50 = "110"	
KVN48	VDH- ΔV*(VRN0+115R+VRHN+VRLN)/SUMRN	PKN52-50 = "111"	
KVN49	VDH- ΔV*(VRN0+120R+VRHN+VRLN)/SUMRN	-	VINN7

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0 + VRP1
SUMRN: Total of th enegative polarity ladder resistance = 128R + VRHN + VRLN + VRN0 + VRN1
ΔV: Voltage difference between VDH-VGS

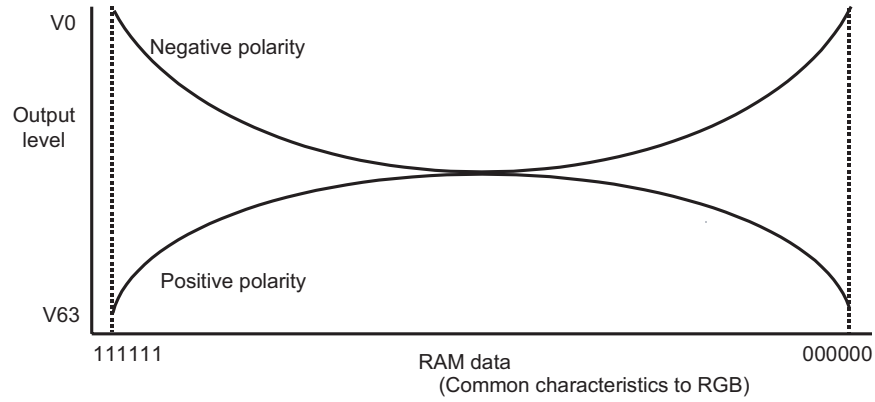
Voltage formula –2 (Negative formula)

grayscale voltage	Formula
V0	VINN0
V1	VINN1
V2	V8+(V1-V8)*(30/48)
V3	V8+(V1-V8)*(23/48)
V4	V8+(V1-V8)*(16/48)
V5	V8+(V1-V8)*(12/48)
V6	V8+(V1-V8)*(8/48)
V7	V8+(V1-V8)*(4/48)
V8	VINN2
V9	V20+(V8-V20)*(22/24)
V10	V20+(V8-V20)*(20/24)
V11	V20+(V8-V20)*(18/24)
V12	V20+(V8-V20)*(16/24)
V13	V20+(V8-V20)*(14/24)
V14	V20+(V8-V20)*(12/24)
V15	V20+(V8-V20)*(10/24)
V16	V20+(V8-V20)*(8/24)
V17	V20+(V8-V20)*(6/24)
V18	V20+(V8-V20)*(4/24)
V19	V20+(V8-V20)*(2/24)
V20	VINN3
V21	V43+(V20-V43)*(22/23)
V22	V43+(V20-V43)*(21/23)
V23	V43+(V20-V43)*(20/23)
V24	V43+(V20-V43)*(19/23)
V25	V43+(V20-V43)*(18/23)
V26	V43+(V20-V43)*(17/23)
V27	V43+(V20-V43)*(16/23)
V28	V43+(V20-V43)*(15/23)
V29	V43+(V20-V43)*(14/23)
V30	V43+(V20-V43)*(13/23)
V31	V43+(V20-V43)*(12/23)
V32	V43+(V20-V43)*(11/23)
V33	V43+(V20-V43)*(10/23)
V34	V43+(V20-V43)*(9/23)
V35	V43+(V20-V43)*(8/23)
V36	V43+(V20-V43)*(7/23)
V37	V43+(V20-V43)*(6/23)
V38	V43+(V20-V43)*(5/23)
V39	V43+(V20-V43)*(4/23)
V40	V43+(V20-V43)*(3/23)
V41	V43+(V20-V43)*(2/23)
V42	V43+(V20-V43)*(1/23)
V43	VINN4
V44	V55+(V43-V55)*(22/24)
V45	V55+(V43-V55)*(20/24)
V46	V55+(V43-V55)*(18/24)
V47	V55+(V43-V55)*(16/24)
V48	V55+(V43-V55)*(14/24)
V49	V55+(V43-V55)*(12/24)
V50	V55+(V43-V55)*(10/24)
V51	V55+(V43-V55)*(8/24)
V52	V55+(V43-V55)*(6/24)
V53	V55+(V43-V55)*(4/24)
V54	V55+(V43-V55)*(2/24)
V55	VINN5
V56	V62+(V55-V62)*(44/48)
V57	V62+(V55-V62)*(40/48)
V58	V62+(V55-V62)*(36/48)
V59	V62+(V55-V62)*(32/48)
V60	V62+(V55-V62)*(25/48)
V61	V62+(V55-V62)*(18/48)
V62	VINN6
V63	VINN7

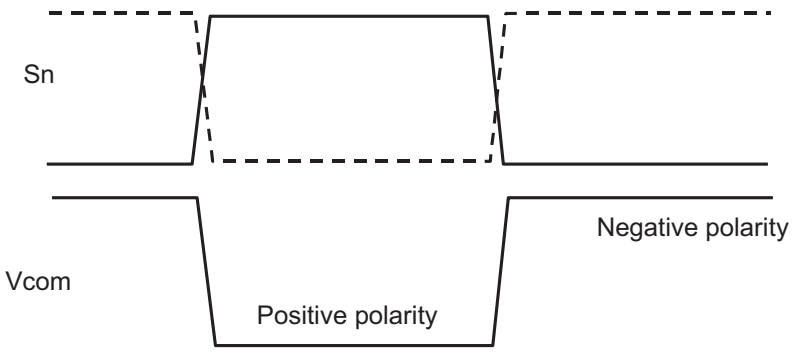
Relation between RAM Data and Output level



Relationship between RAM data and output level (REV = 0)



Relationship between RAM data and output level (REV =1)



Relationship between Source Output and Vcom

8-Color Display Mode

The HD66776 incorporates an 8-color display mode as low power consumption display mode. The grayscale level to be used is indicated below, and the unused levels are stopped. This, therefore, achieved to reduce the power consumption.

COL	Number of display color
0	262,144
1	8

Active amplifer on each mode (● Where amplifier is active.)

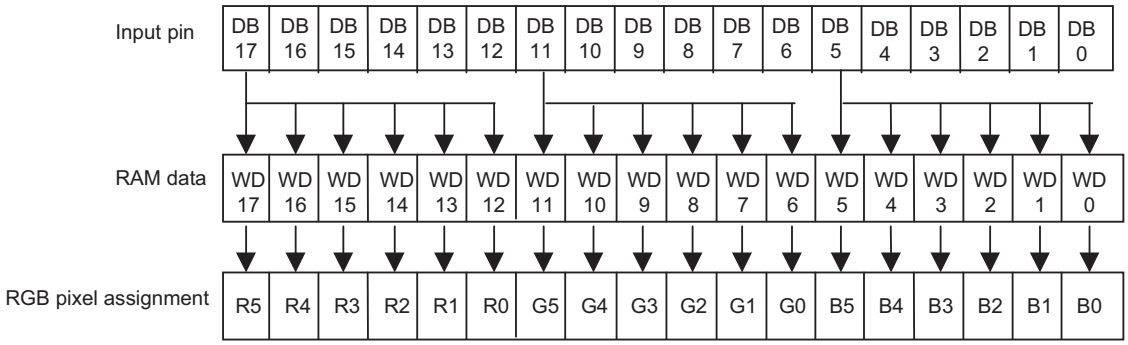
	Number of display color		
Amplifier	262K	8	RAM data
V0	●	●	111111
V1	●		111110
V2	●		111101
V3	●		111100
V4	●		111011
V5	●		111010
V6	●		111001
V7	●		111000
V8	●		110111
V9	●		110110
V10	●		110101
V11	●		110100
V12	●		110011
V13	●		110010
V14	●		110001
V15	●		110000
V16	●		101111
V17	●		101110
V18	●		101101
V19	●		101100
V20	●		101011
V21	●		101010
V22	●		101001
V23	●		101000
V24	●		100111
V25	●		100110
V26	●		100101
V27	●		100100
V28	●		100011
V29	●		10010
V30	●		100001
V31	●		100000

	Number of display color		
Amplifier	262K	8	RAM data
V32	●		011111
V33	●		011110
V34	●		011101
V35	●		011100
V36	●		011011
V37	●		011010
V38	●		011001
V39	●		011000
V40	●		010111
V41	●		010110
V42	●		010101
V43	●		010100
V44	●		010011
V45	●		010010
V46	●		010001
V47	●		010000
V48	●		001111
V49	●		001110
V50	●		001101
V51	●		001100
V52	●		001011
V53	●		001010
V54	●		001001
V55	●		001000
V56	●		000111
V57	●		000110
V58	●		000101
V59	●		000100
V60	●		000011
V61	●		000010
V62	●		000001
V63	●	●	000000

When HD66776 is operated in low power consumption mode, the process below is executed while RAM data writing, and HD66776 automatically selects the active amplifier.

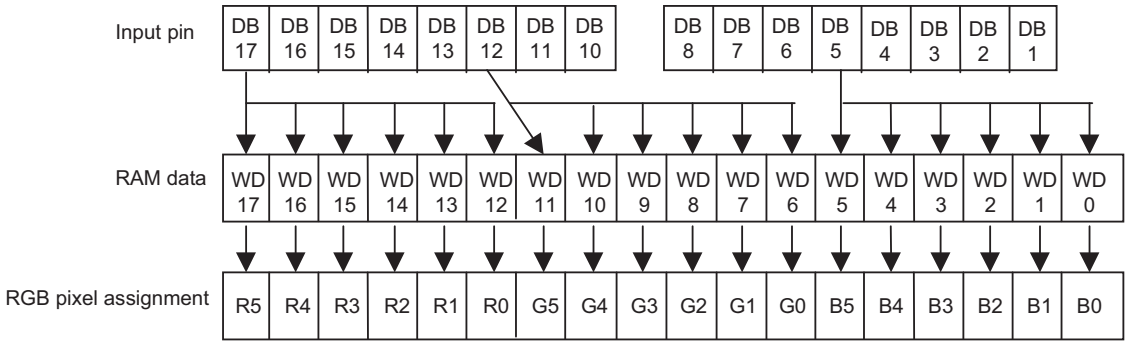
- 18-bit interface mode

8-color mode



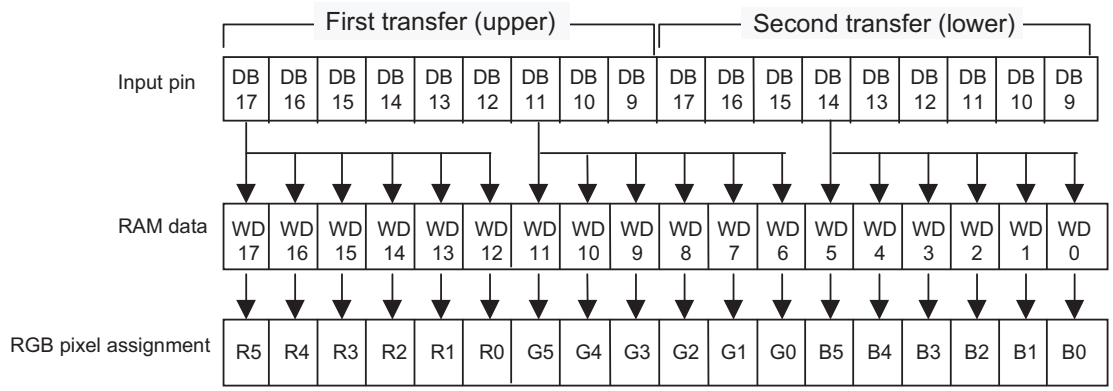
- 16-bit interface mode

8-color mode



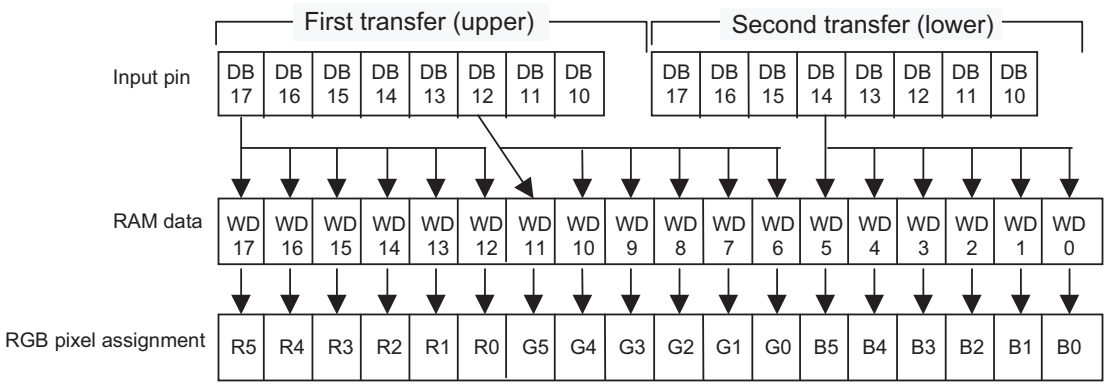
● 9-bit interface mode

8-color mode



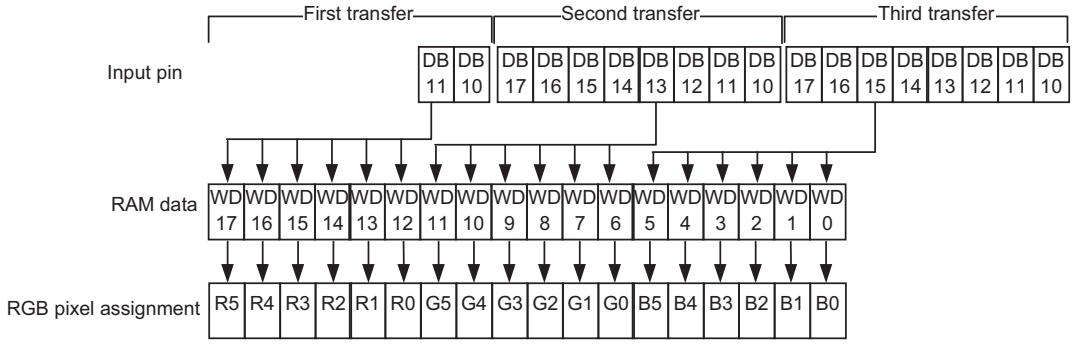
● 8-bit interface mode

8-color mode



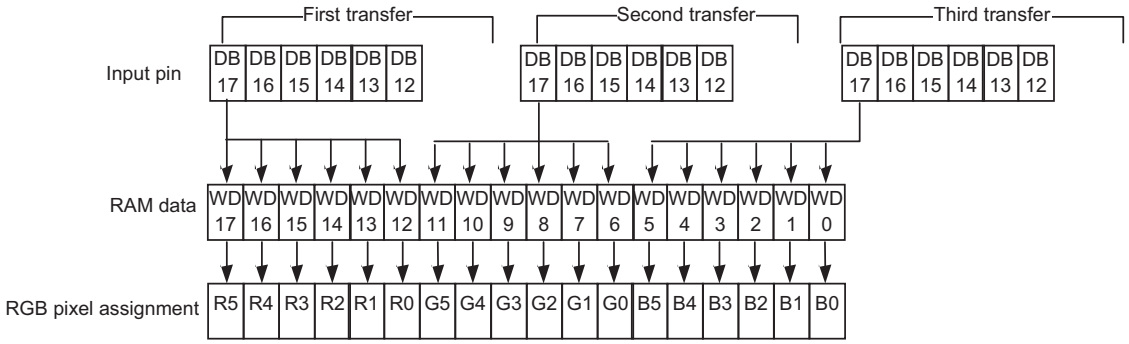
● 8-bit interface mode (2)

8-color mode



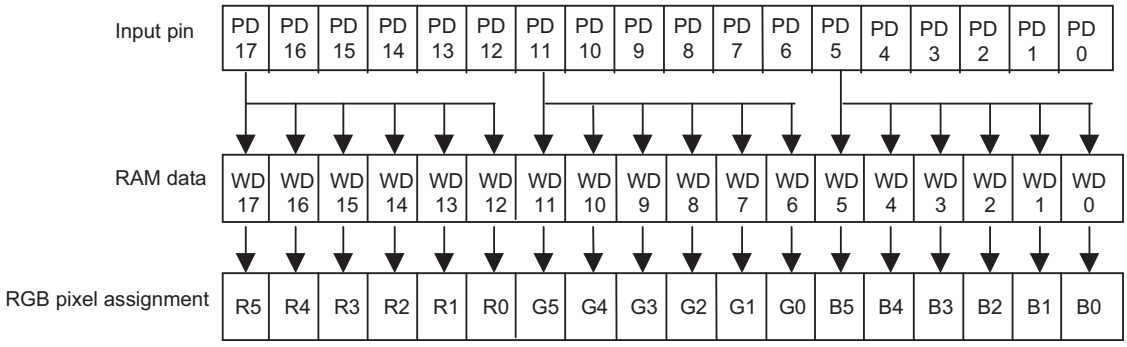
● 8-bit interface mode (3)

8-color mode



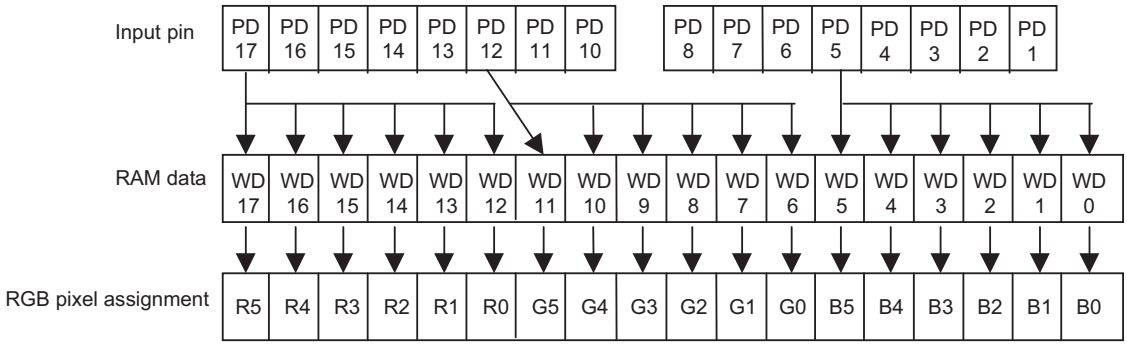
● RGB interface (18-bit) mode

8-color-mode



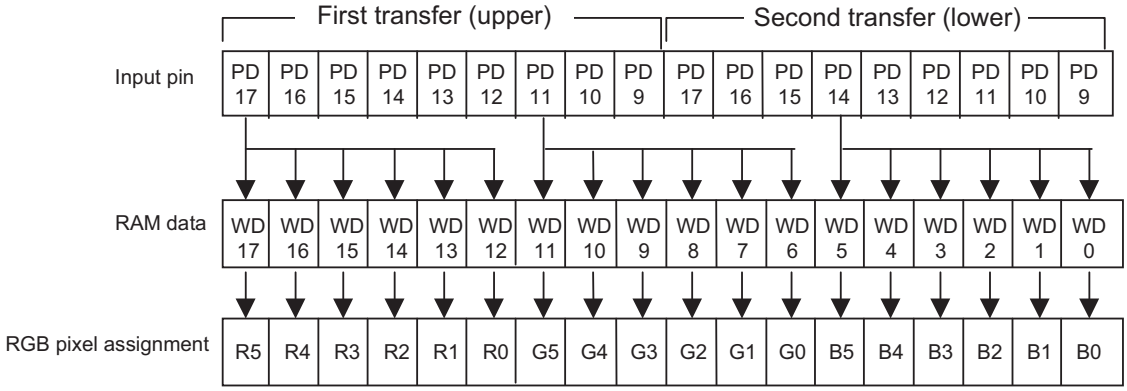
● RGB interface (16-bit) mode

8-color-mode



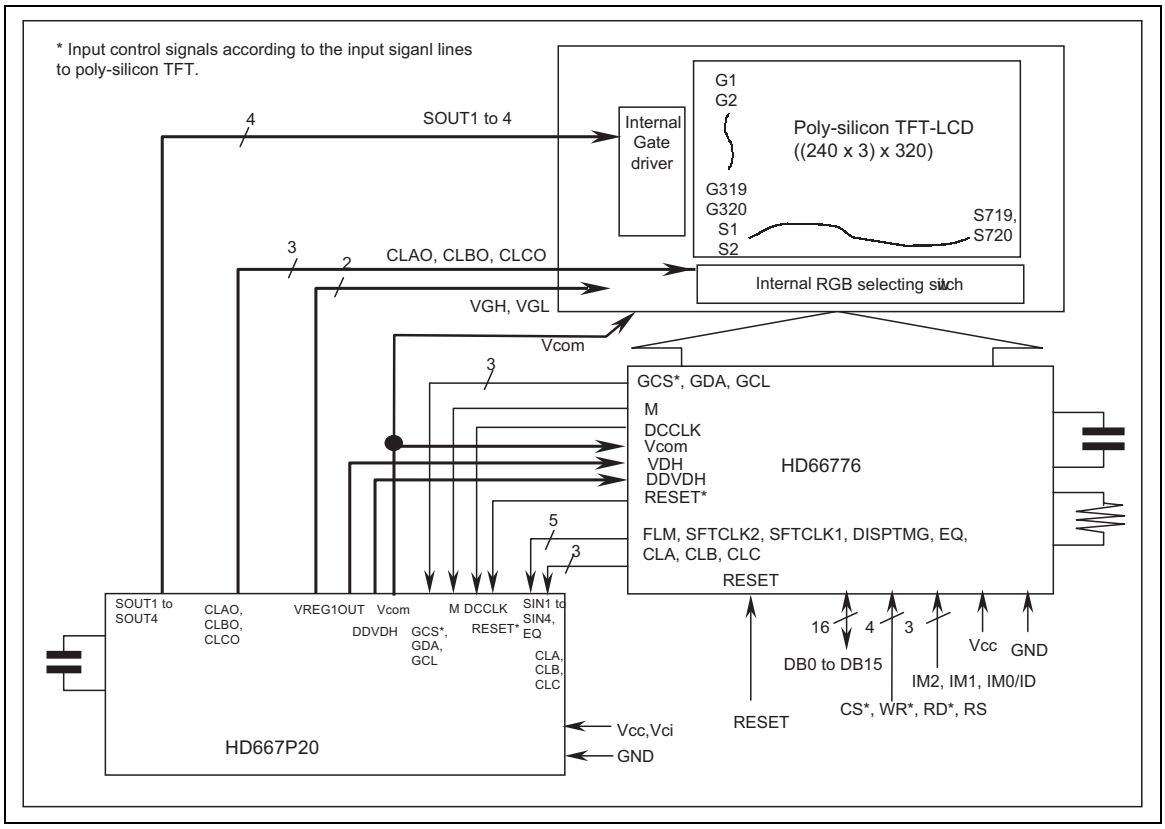
● RGB interface (9bit) mode

8-color-mode



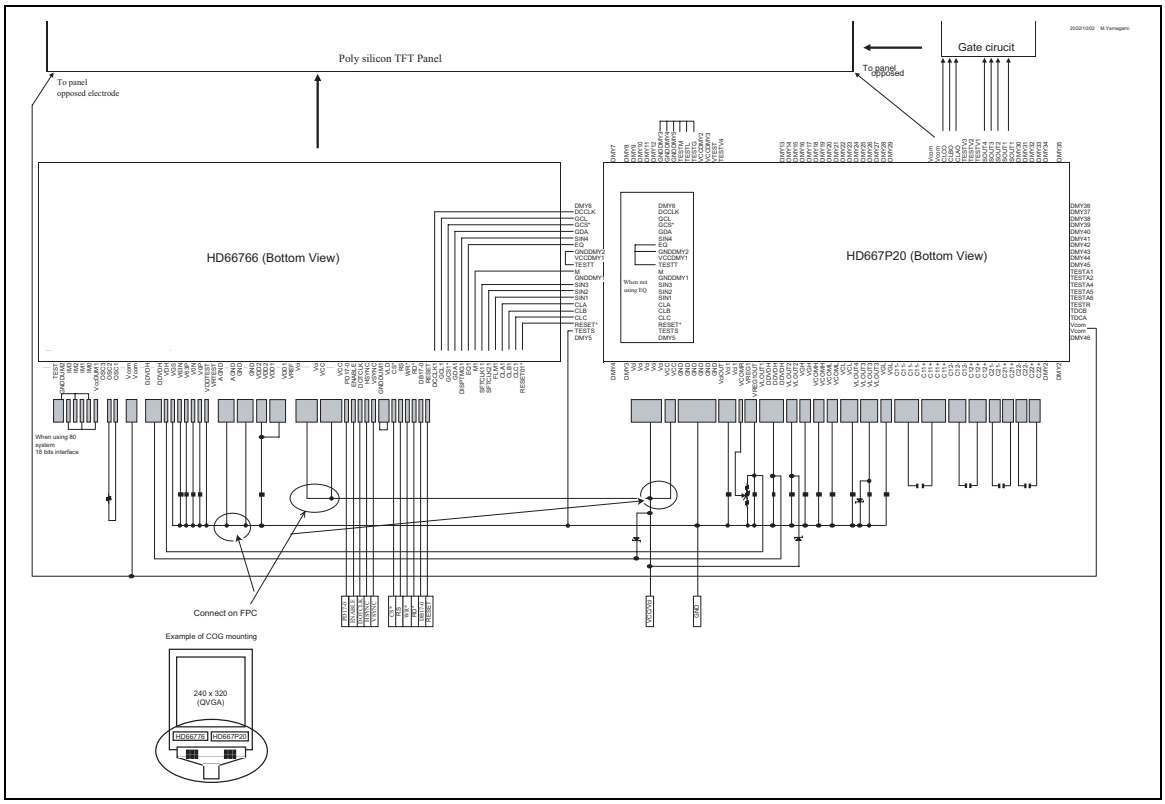
Example of System Configuration of TFT display

The following diagram indicates a connection example of HD66776 and HD667P20 (power supply IC) when consisting the 256RGB x 320dot poly-silicon TFT-LCD panel with internal gate driver's System Configuration of TFT display



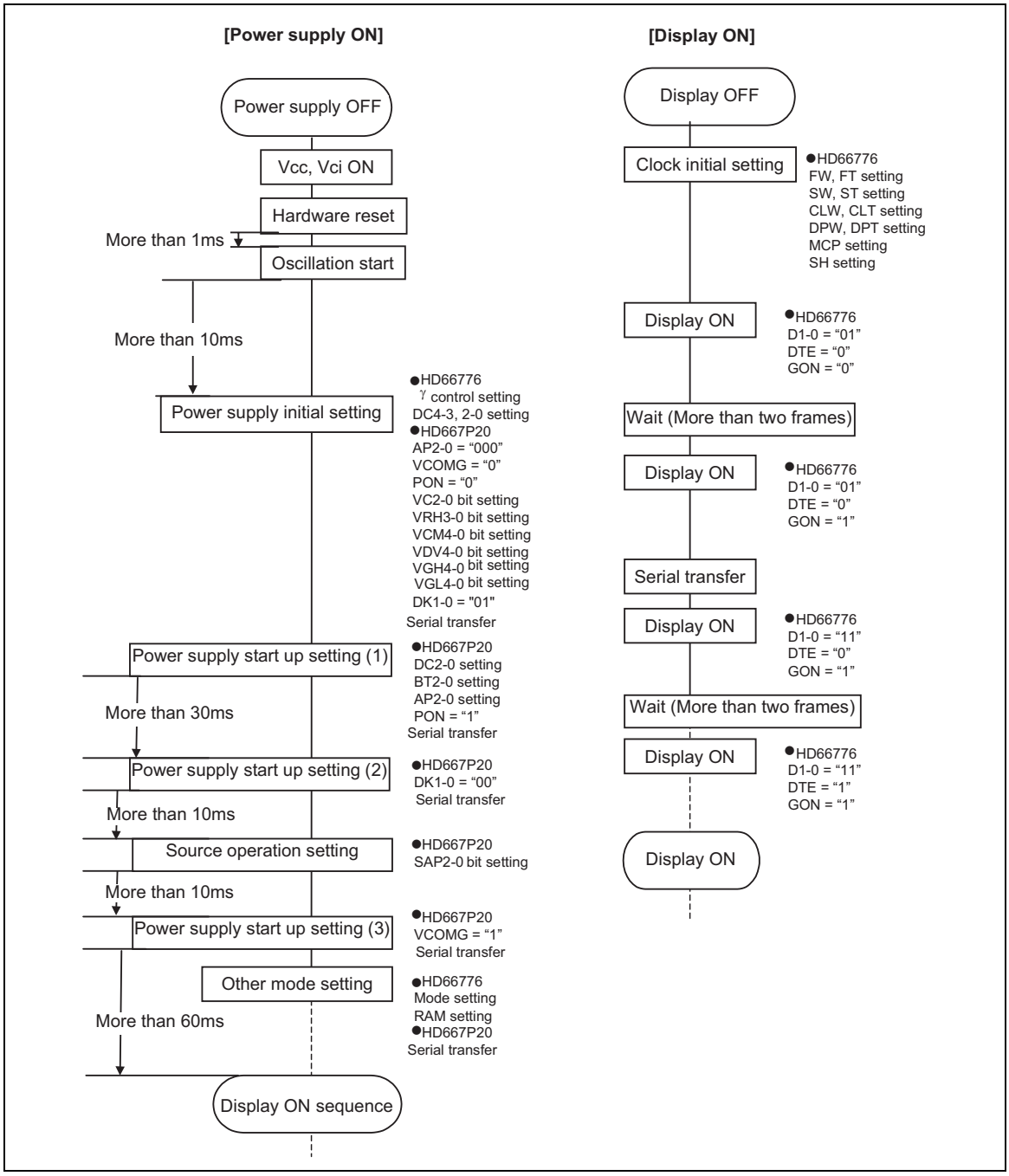
Example of Chip set connecting

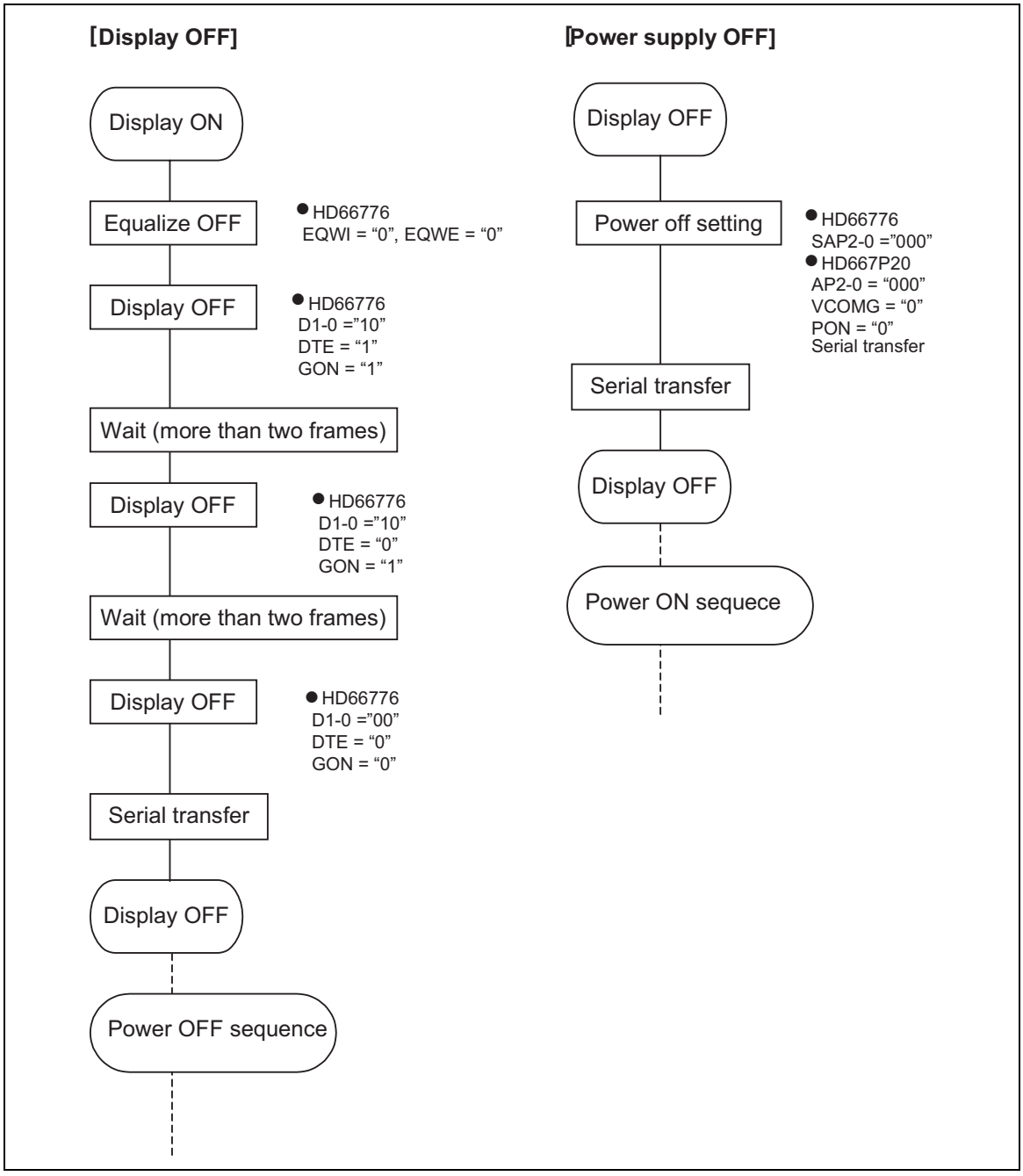
Figure indicates the example of connection between source driver HD66776 and power supply IC HD667P20.

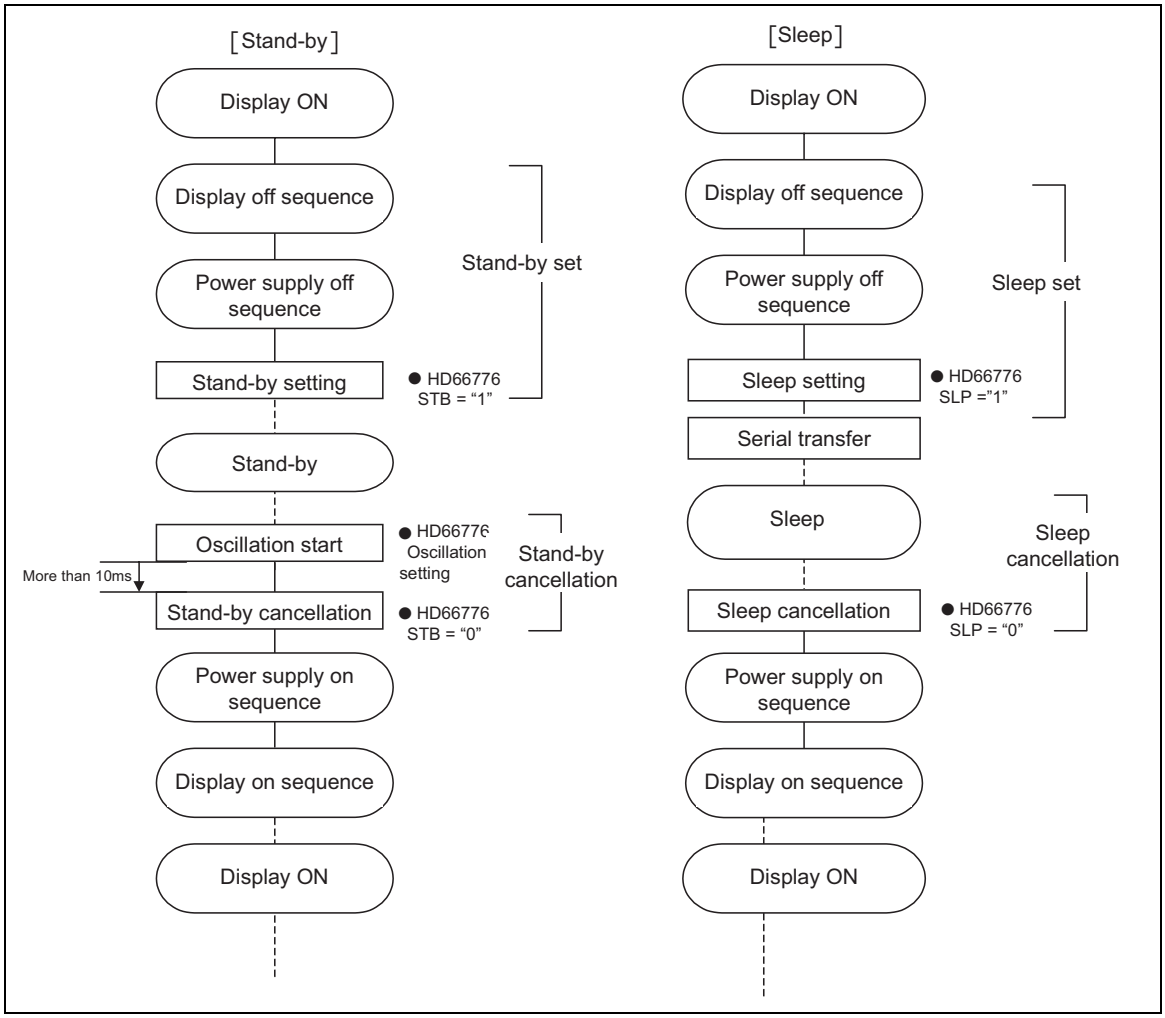


Instruction Setting Flow

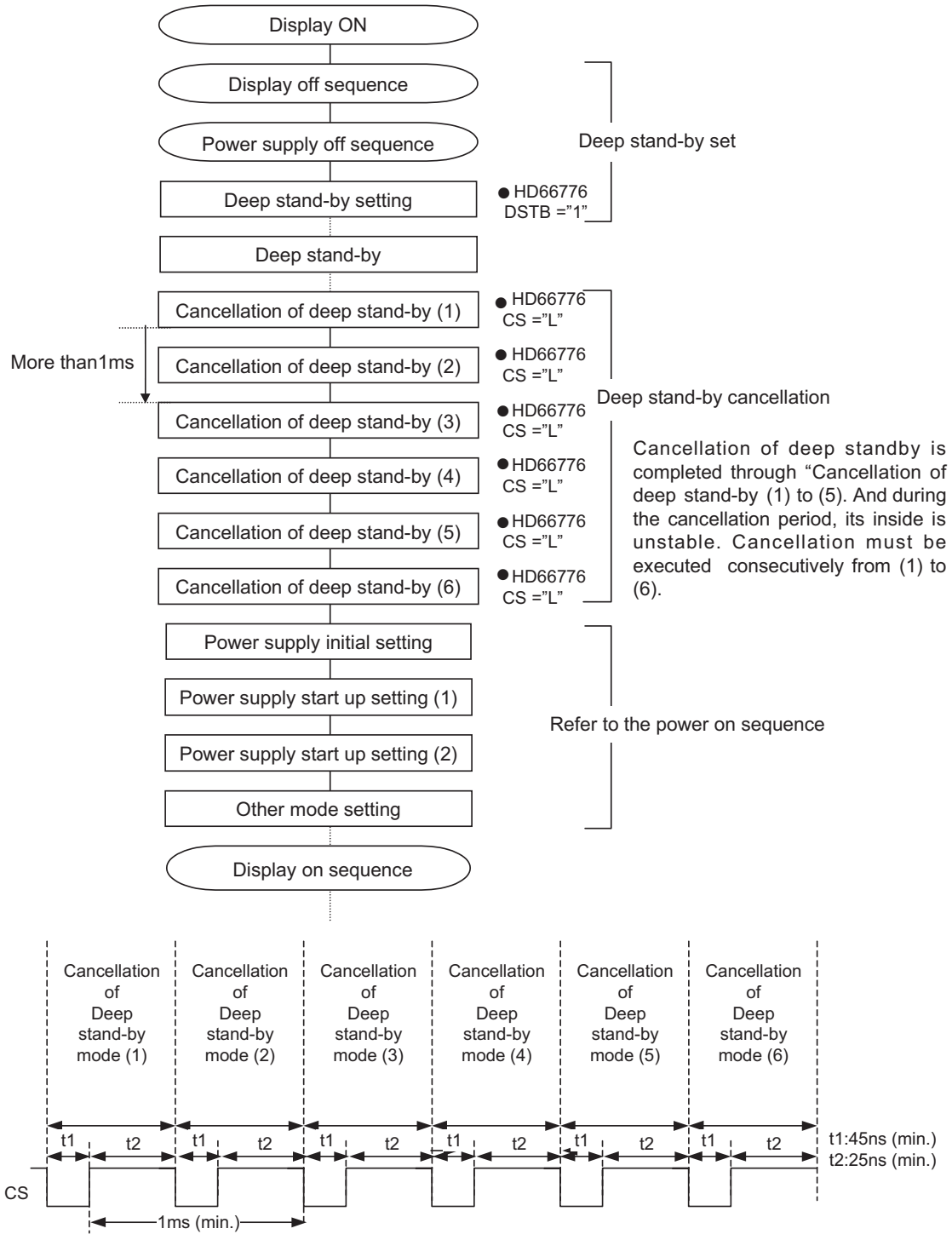
The following chart is the example of setting instructions for starting up HD66776/HD667P10. The instruction setting for the HD67P10 is executed by the serial interface. Execute the serial transfer command right after setting the instruction of HD66776.



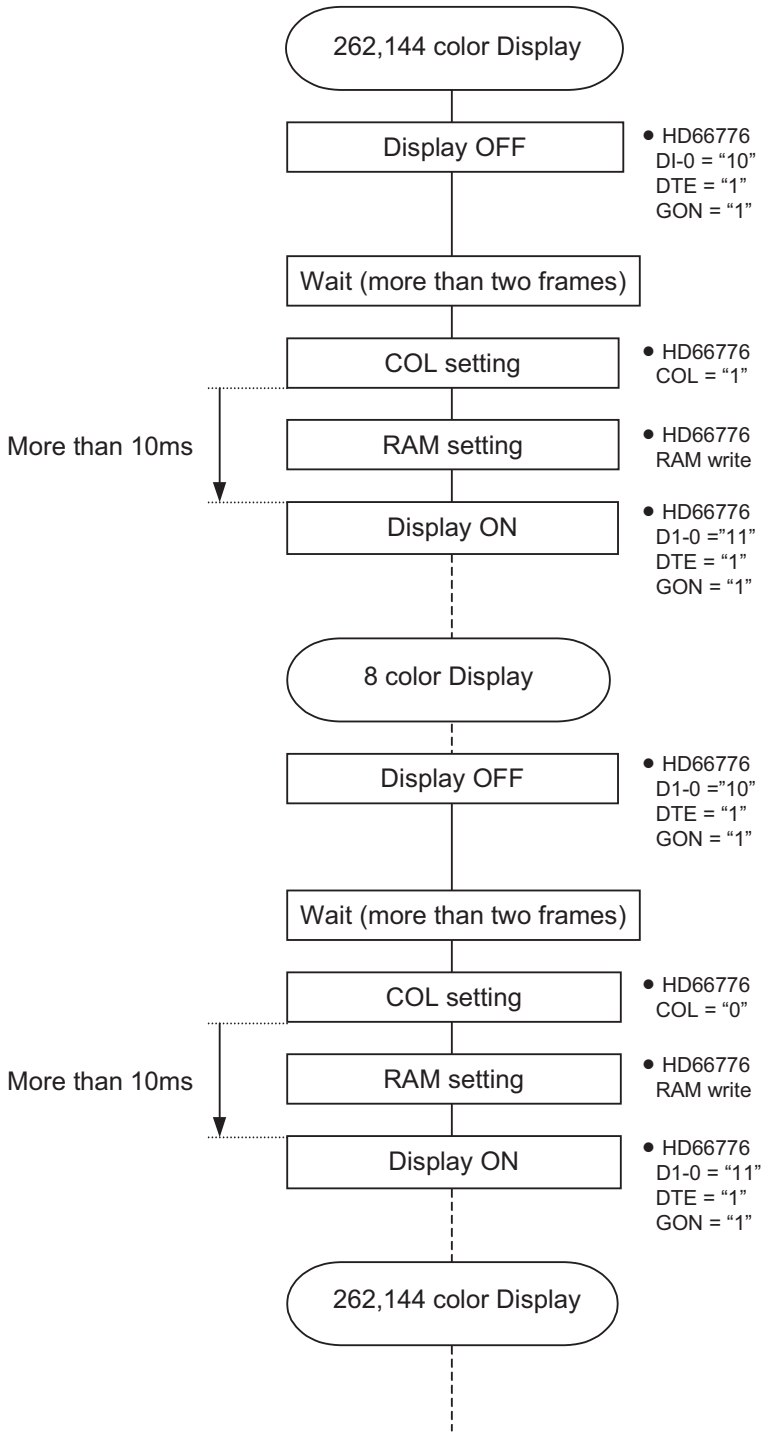

[Display OFF]
Display ON
Equalize OFF
● HD66776
EQWI = “0”, EQWE = “0”
Display OFF
● HD66776
D1-0 =”10”
DTE = “1”
GON = “1”
Wait (more than two frames)
Display OFF
● HD66776
D1-0 =”10”
DTE = “0”
GON = “1”
Wait (more than two frames)
Display OFF
● HD66776
D1-0 =”00”
DTE = “0”
GON = “0”
Serial transfer
Display OFF
Power OFF sequence
[Power supply OFF]
Display OFF
Power off setting
● HD66776
SAP2-0 =”000”
● HD667P20
AP2-0 = “000”
VCOMG = “0”
PON = “0”
Serial transfer
Serial transfer
Display OFF
Power ON sequece

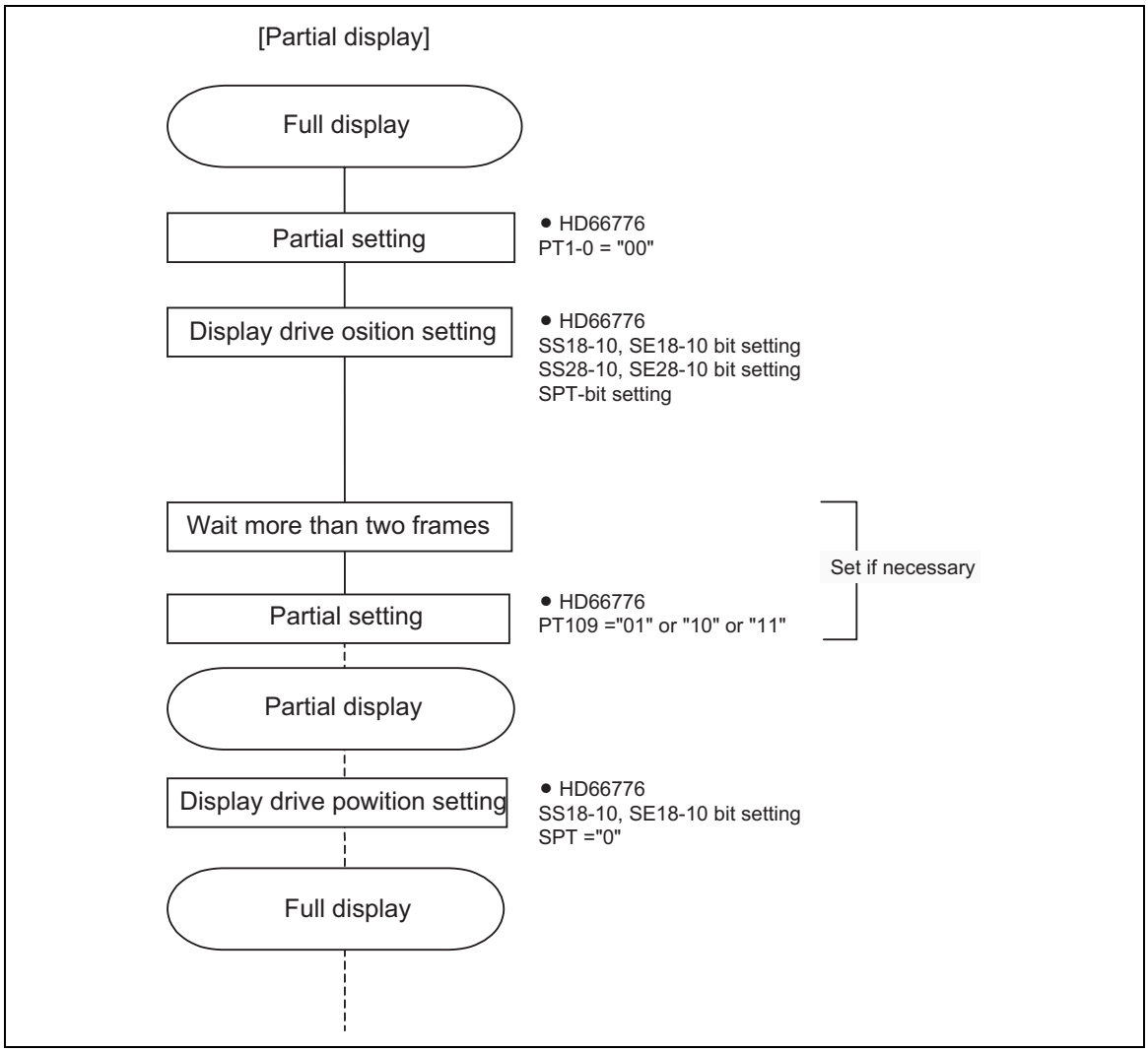

[Stand-by]
Display ON
Display off sequence
Power supply off sequence
Stand-by setting
● HD66776 STB = "1"
Stand-by set
Stand-by
Oscillation start
● HD66776 Oscillation setting
More than 10ms
Stand-by cancellation
● HD66776 STB = "0"
Stand-by cancellation
Power supply on sequence
Display on sequence
Display ON
[Sleep]
Display ON
Display off sequence
Power supply off sequence
Sleep setting
● HD66776 SLP ="1"
Sleep set
Serial transfer
Sleep
Sleep cancellation
● HD66776 SLP = "0"
Sleep cancellation
Power supply on sequence
Display on sequence
Display ON

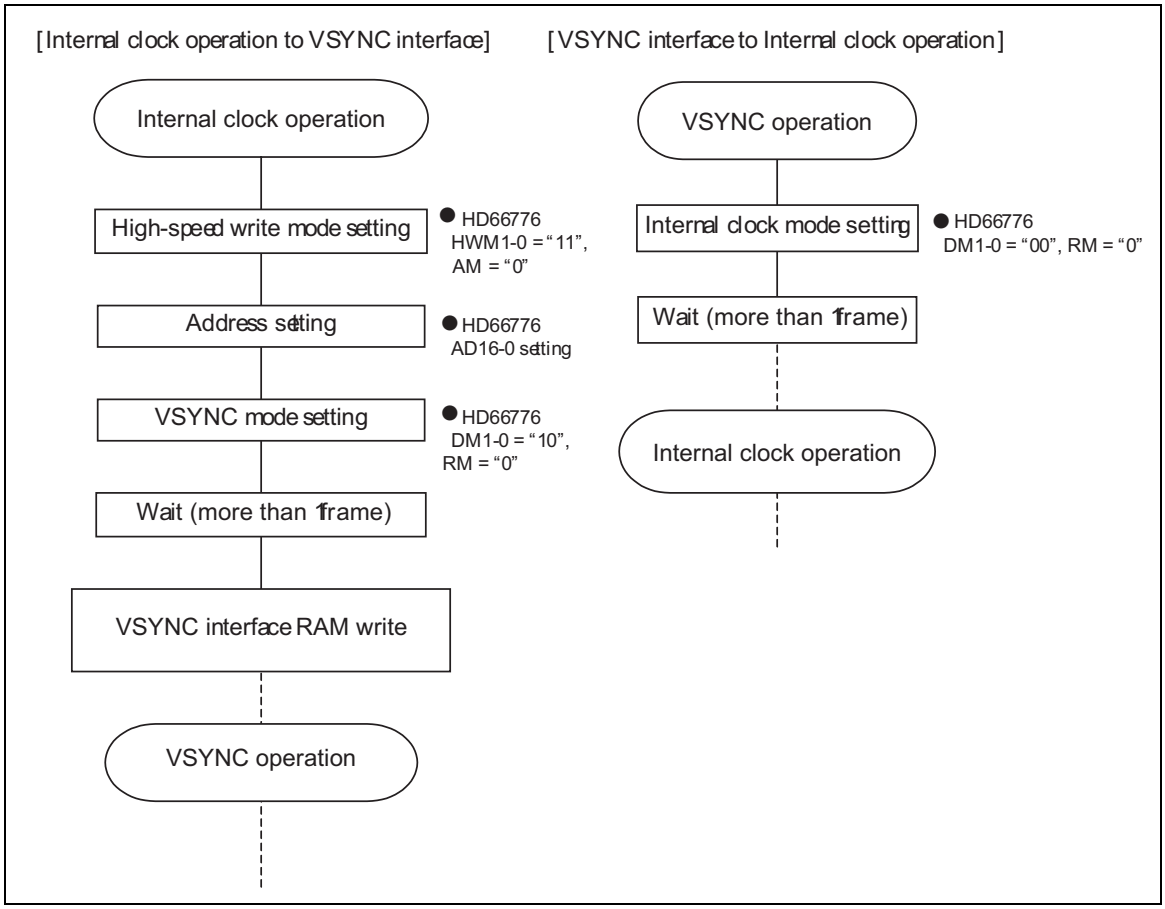
[Deep Stand-by]



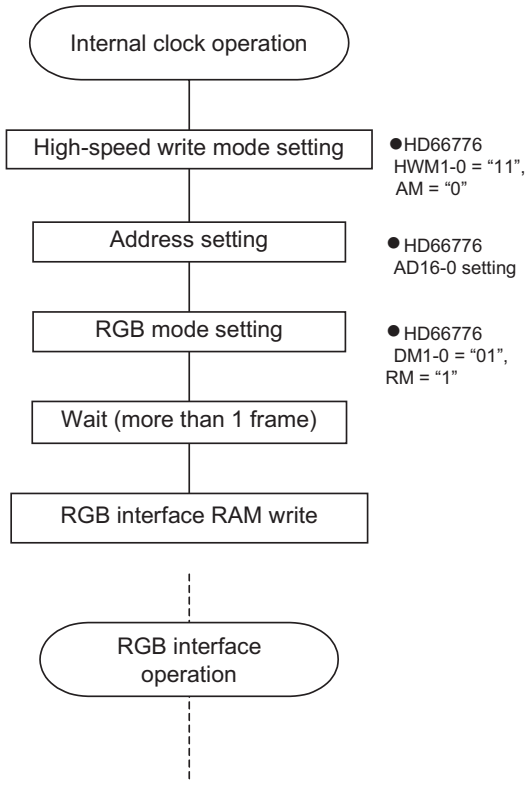
[262,144 to 8 color mode color mode]
[8 color mode to 262,144 color mode]



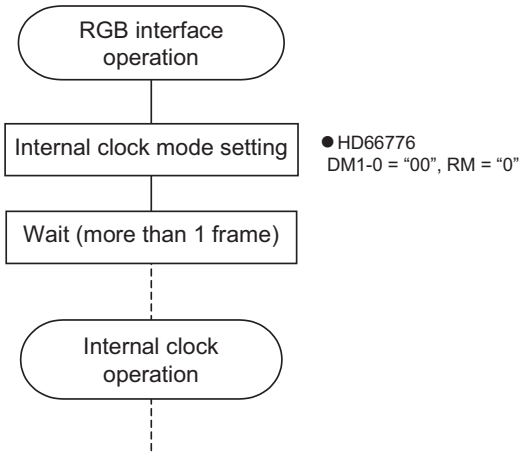

[Partial display]
Full display
Partial setting
● HD66776
PT1-0 = "00"
Display drive osition setting
● HD66776
SS18-10, SE18-10 bit setting
SS28-10, SE28-10 bit setting
SPT-bit setting
Wait more than two frames
Set if necessary
Partial setting
● HD66776
PT109 ="01" or "10" or "11"
Partial display
Display drive powition setting
● HD66776
SS18-10, SE18-10 bit setting
SPT ="0"
Full display


[Internal clock operation to VSYNC interface]
Internal clock operation
High-speed write mode setting
HD66776
HWM1-0 = "11",
AM = "0"
Address setting
HD66776
AD16-0 setting
VSYNC mode setting
HD66776
DM1-0 = "10",
RM = "0"
Wait (more than 1frame)
VSYNC interface RAM write
VSYNC operation
[VSYNC interface to Internal clock operation]
VSYNC operation
Internal clock mode setting
HD66776
DM1-0 = "00", RM = "0"
Wait (more than 1frame)
Internal clock operation

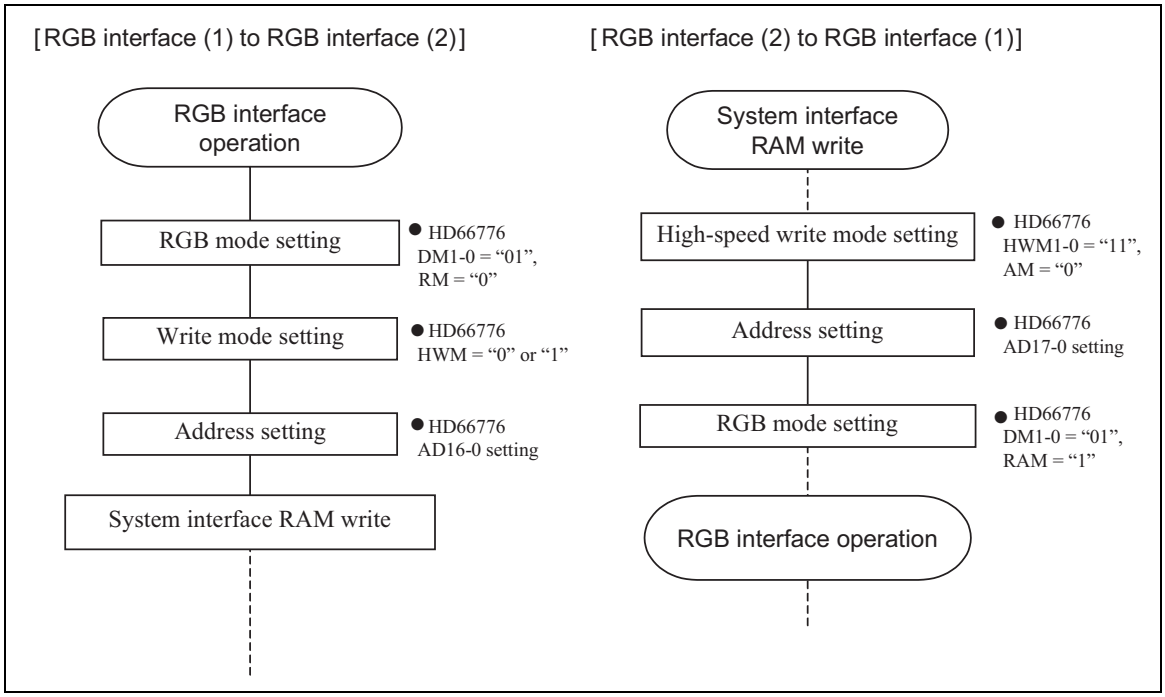
[Internal clock operation to RGB interface (1)]



[RGB interface (1) to Internal clock operation]

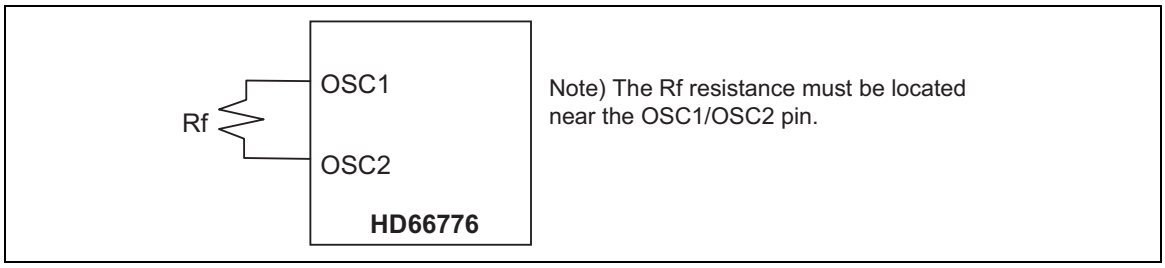


RAM data writing flow from system interface displaying RGB interfaced.



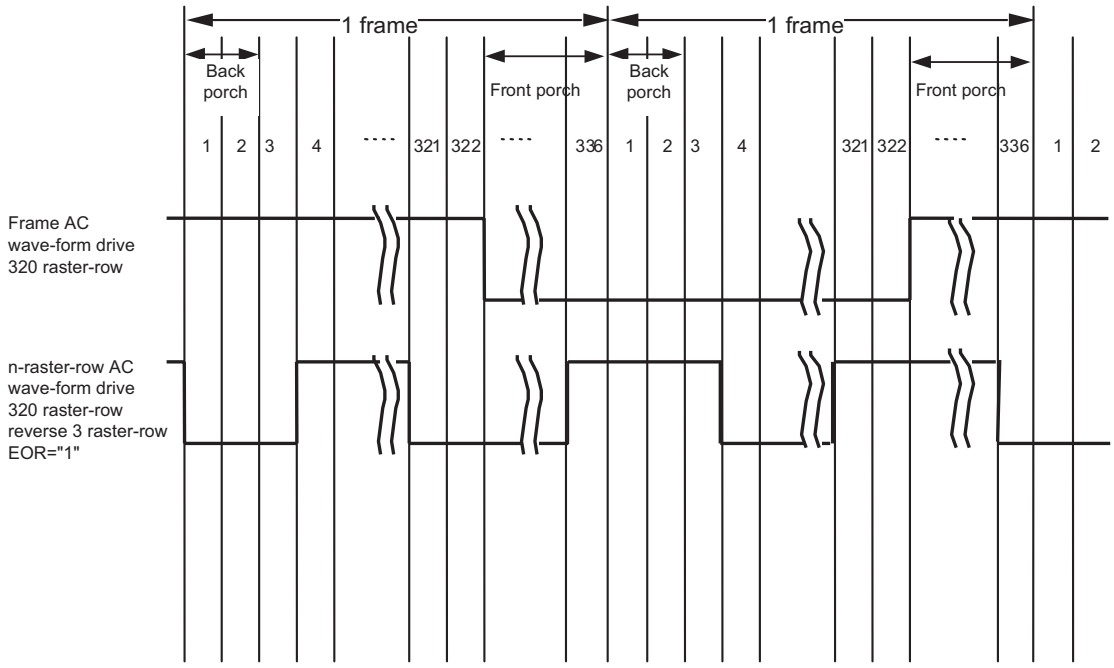
Oscillation circuit

The HD66776 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according ot the external resistance value, writing length, or operating power-supply voltage. If Rf is increased or power supply voltage is decreases, the oscillation frequency decreases. For the relation ship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.



n-raster-row Reversed AC Drive

The HD66776 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64-raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality. Determine the number of the raster-rows n (NW bit set value+1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge of discharge current is increased in the LCD cells.

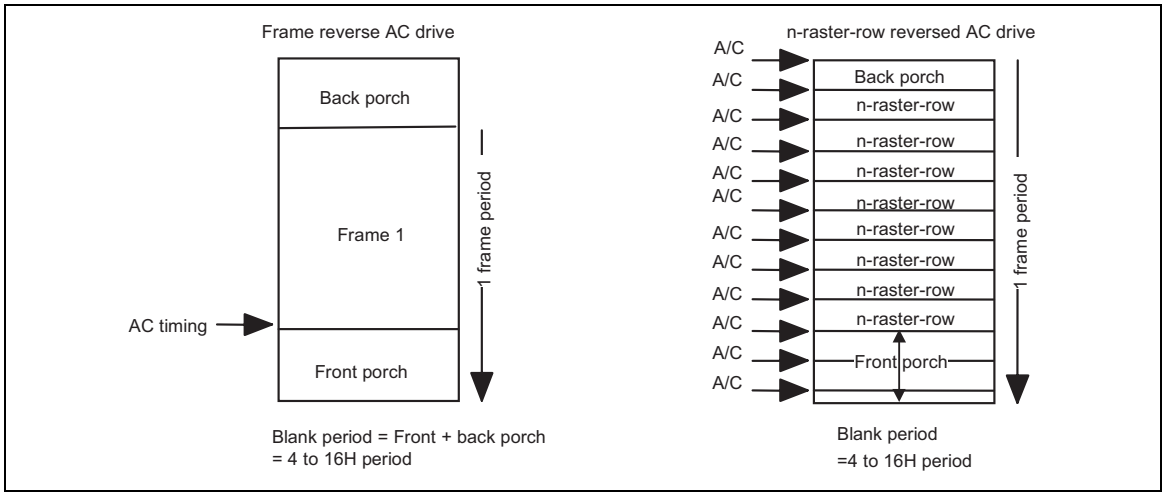


Note: In an n-raster-row driving EOR should be "1" so that DC bias voltage is not applied.

Example of an AC Signal under n-raster-row Reversed AC Drive

AC Drive Timing

Following diagram indicates the timing of changing polarity on the each A/C drive method. LCD drive polarity is changed after every frame. After the A/C this timing, the blank (all outputs from the gate Vgoff output) in 4 to 16H period is inserted. When the reversed n-raster-row is driving, a blank period of the 4 to 16H periods is inserted after all screens are drawn.



Frame Frequency Adjusting Function

The HD66776 has an on-chip frame-frequency adjustment function when it selects the internal clock action mode. The frame frequency can be adjusted by the instruction setting (DIVI, RTNI) during the LCD driver as the oscillation frequency is always same. If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

Relationship between LCD Drive Duty and Frame Frequency

The relationship between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTNI) and in the operation clock division bit (DIVI) by the instruction.

(Formula for the frame frequency)

$$\text{Frame Frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (Line + FP+BP)}} \text{ [Hz]}$$

fosc: R-C oscillation frequency
Line: Numbers of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit
FP: Front porch
BP: Back porch

Example of Calculation

In case of maximum frame frequency = 60 Hz:
Driver raster-row: 320

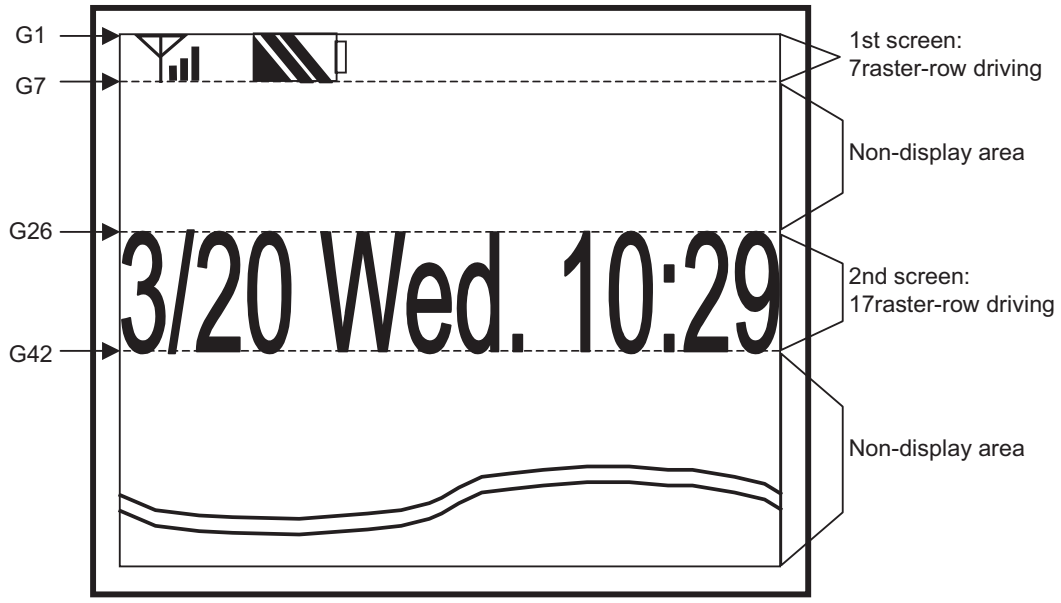
1H periods 16 clock (RTN3 to 0 = “10000”)
Operation clock division ratio:1 division

fosc = 60Hz x 16 clock x 1 division x (320 +16) lines = 323[kHz]

In this case, the CR oscillation frequency becomes 323 kHz. The external resistance value of the R-C oscillator must be adjusted to be 323 kHz.

Screen-division Driving Function

The HD66776 can select and drive two screens at arbitrary positions with the screen-driving position registers (R402 to R405). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption. For the 1st division screen, start lies (SS18 to 10) and end lines (SE18 to 10) are specified by the 1st screen-driving position register (R402 and R403). For the 2nd division screen, start line (SS28 to 20) and end lines (SE28 to 20) are specified by the 2nd screen-driving position register (R404 and R405). The 2nd screen control is effective when the SPT bit is 1. The total count of selection –driving lines for the 1st and 2nd screens must be the number of LCD drive raster-rows or less.



Driving raster-row: NL5-0="100111" (320 lines)
1st screen setting: SS18-10 = "00"H, SE18-10 = "06H"
2nd screen setting: SS28-20 = "19"H, SE28-20 = "29"H, SPT = "1"

Display Example of Two-Screen Division Driving

It is possible to set the driver output of non-display area during partial display. Select the setting value according to the characteristic of LCD panel.

PT1	PT0	Source output of non-display area		DISPTMG output of non-display are
0	0	V63	V0	Normal operation
0	1	V63	V0	"Low"
1	0	GND	GND	"Low"
1	1	Hi-z	Hi-z	"Low"

Restrictions on the 1st/2nd Screen Driving Position Register Settings

The following restrictions must be satisfied when setting the start line(SS18 to 10) and end line (SE18 to 10) of the 1st screen driving position register (R402, R403) and the start line (SS28 to 20) and end line (SE 28 to 20) of the 2nd screen driving position register (R404, R405) for the HD66776. Note that incorrect display may occur if the restrictions are not satisfied.

Restrictions on the 1st /2nd Screen Driving Position Register Settings

1st Screen Driving (SPT = 0)

Register setting	Display operation
(SE18 to 10) – (SS18 to 10) = NL	Full screen display Normally displays (SE18 to 10) to (SS18 to 10)
(SE18 to 10) – (SS18 to 10) < NL	Partial display Normally displays (SE18 to 10) to (SS18 to 10) RAM data in other areas are not displayed.
(SE18 to 1) – (SS18 to 10) > NL	Setting disabled

Note 1: SS18 to 10 <= SE18 to 10 <= “13F”H
Note 2: Setting SE28 to 20 and SS28 to 20 are invalid.

2nd Screen Driving (SPT = 1)

Register setting	Display operation
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28-20)) = NL	Full screen display Normally displays (SE27 to 10) to (SE17 to 10)
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28 to 20)) < NL	Partial display Normally displays (SE27 to 20) to (SS17 to 10) RAM data in other areas are not displayed.
((SE18 to 10) – (SS18 to 10)) + ((SE28 to 20) – (SS28 to 20)) > NL	Setting disabled

Note 1: SS18 to 10 <= SE18 to 10 < SS28 to 20 <= SE28 to 20 <= “13F”H
Note 2: (SE28 to 20) – (SS18 to 10) <= NL

Absolute Maximum Ratings

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc	V	-0.3 to + 4.6	1, 2
Power supply voltage (2)	Vci	V	-0.3 to + 4.6	1, 3
Power supply voltage (3)	DDVDH-GND	V	-0.3 to + 6.5	1, 4
Input voltage	Vt	V	-0.3 to Vcc + 0.3	1
Operating temperature	Topr	°C	-40 to + 85	1, 5
Storage temperature	Tstg	°C	-55 to + 110	1, 6

Notes: 1. If the LSI is used above these absolute maximum ratings, it may become permanently damaged. Using the LSI within the following electrical characteristic limit is strongly recommended for normal operation. If these electrical characteristic conditions are also exceeded, the LSI will malfunction and cause poor reliability.

2. Vcc ≥ GND must be maintained.

3. Vci ≥ GND must be maintained.

4. DDVDH ≥ GND must be maintained.

5.For die and wafer products, specified up to 85 °C.

DC Characteristics (Vcc= 2.2 to 3.3V, Ta = -40 to +85°C[*1])

Item		Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage		V_{IH}	V	V_{CC} = 2.2 to 3.3 V	0.8 V_{CC}	—	V_{CC}	2, 3
Input low voltage (1)		V_{IL}	V	V_{CC} = 2.2 to 3.3 V	–0.3	—	0.2V_{CC}	2, 3
Output high voltage		V_{OH1}	V	I_{OH} = –0.1 mA	0.75V_{CC}	—	—	2
Output low voltage (1)		V_{OL1}	V	V_{CC} = 2.2 to 3.3 V, I_{OL} = 0.1 mA	—	—	0.2 V_{CC}	2
I/O leakage current		I_{Li}	µA	Vin = 0 to V_{CC}	–1	—	1	4
Current consumption (1) (Vcc–GND)	Normal operation mode	I_{OP}	µA	R-C oscillation; fosc = 325kHz (320line) V_{CC} = 3V, Ta = 25°C, RAM data 0000h	—	70	130	5,6
	Stand-by mode	I_{ST}	µA	Vcc = 3V, Ta<=25°C	—	0.1	5	5
	Deep stand-by mode	I_{DST}	µA	Vcc = 3V, Ta>50°C	—	0.1	5	5
Current consumption (2) (Vcc-GND)	Normal operation mode	I_{CIOP}	µA	R-C oscillation; fosc = 325kHz (320line) V_{CC} = 3V, Ta = 25°C, RAM data 0000h	—	140	210	5, 6
	Stand-by mode	I_{CIST}	µA	Vci = 3V, Ta<=25°C	—	30	100	5
	Deep stand-by mode	I_{CIDST}	µA	Vci = 3V, Ta<=25°C	—	0.1	5	5
LCD Power Current (DDVDH-GND)		I_{LCD}	µA	Vcc=3V, VLCD=5.5V, VDH=5.0V, CR Oscillation; fosc=325kHz(320line), Ta=25°C, RAMdata:0000h, REV= “0”, SAP= “001”, VRN4-0= “0”, VRP4-0 = “0” PKP52-00 =”0”, PRP12-00 = “0”, VRP14-00 = “0”, PKN52-00 = “0”, PRN12-00 = “0”, VRN14-00 = “0”	—	600	1000	5,6
LCD Driving Voltage (DDVDH-GND)		V_{LCD}	V	—	4.0	—	5.9	—
Output Voltage deviation		∠Vo	mV	—	—	3	—	7
Variation of average output voltage		∠V∠	mV	—	—	—	35	8

AC Characteristic (Vcc =2.2 to 3.3V, Ta = -40°C to +85°C)

Clock Characteristics (Vcc = 2.2 to 3.3V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Clock operation frequency	fcp	kHz	VCC = 2.2 to 3.3 V	100	-	600	
R-C oscillation clock	fOSC	kHz	Rf = 130Ωk, Vcc = 3.0V	352	440	528	9

80-system Bus Interface Timing Characteristics (1)

80-system 18/16/9-bit, 80-system 8-bit (TRI = 0)
Normal Write mod e(HWM1-0 = 00) (Vcc = 2.2V to 3.3V during operation)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	250	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	25	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time (RS to CS*,WR*, RD*)		t_{AS}	ns	Figure 1	15	—	—
Address hold time		t_{AH}	ns	Figure 1	15	—	—
VLD setup time		t_{VS}	ns	Figure 1	25	—	—
VLD hold time		t_{VH}	ns	Figure 1	10	—	—
Write data set up time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{H}	ns	Figure 1	10	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

High-speed Write mode (HWM1-0 = 11) (Vcc = 2.2V to 3.3V during operation)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	250	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	25	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	35	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time (RS to CS*,WR*, RD*)		t_{AS}	ns	Figure 1	15	—	—
Address hold time		t_{AH}	ns	Figure 1	15	—	—
VLD setup time		t_{VS}	ns	Figure 1	20	—	—
VLD hold time		t_{VH}	ns	Figure 1	10	—	—
Write data set up time		t_{DSW}	ns	Figure 1	20	—	—
Write data hold time		t_{H}	ns	Figure 1	10	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

80-system Bus Interface Timing Characteristics (2)

80-system 8-bit, (TRI = 1)
Normal Write mode (HWM1-0 = 00) (Vcc = 2.2V to 3.3V during operation)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	250	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	25	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time (RS to CS*,WR*, RD*)		t_{AS}	ns	Figure 1	20	—	—
Address hold time		t_{AH}	ns	Figure 1	20	—	—
VLD setup time		t_{VS}	ns	Figure 1	25	—	—
VLD hold time		t_{VH}	ns	Figure 1	10	—	—
Write data set up time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{H}	ns	Figure 1	10	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

High-speed Write mode (HWM1-0 = 11) (Vcc = 2.2V to 3.3V during operation)

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	90	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	35	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	45	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time (RS to CS*,WR*, RD*)		t_{AS}	ns	Figure 1	20	—	—
Address hold time		t_{AH}	ns	Figure 1	20	—	—
VLD setup time		t_{VS}	ns	Figure 1	20	—	—
VLD hold time		t_{VH}	ns	Figure 1	10	—	—
Write data set up time		t_{DSW}	ns	Figure 1	35	—	—
Write data hold time		t_{H}	ns	Figure 1	20	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

Clock Synchronized Serial Interface Timing Characteristics

Vcc = 2.2V to 3.3V

Item		Symbol	Unit	Test Condition	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	μs	Figure 2	0.1	—	20
	Read (transmitted)	t_{SCYC}	μs	Figure 2	0.35	—	20
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 2	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 2	150	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 2	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 2	150	—	—
Serial clock rise/fall time		t_{scr}, t_{scf}	ns	Figure 2	—	—	20
Chip select set up time		t_{CSU}	ns	Figure 2	20	—	—
Chip select hold time		t_{CH}	ns	Figure 2	60	—	—
Serial input data set up time		t_{SISU}	ns	Figure 2	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 2	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure 2	—	—	130
Serial output data hold time		t_{SOH}	ns	Figure 2	5	—	—

Reset Timing Characteristics (Vcc = 2.2 to 3.3V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max
Reset low-level width	tRES	ms	Figure 3	1	—	—
Reset rising time	trRES	μs	Figure 3	—	—	10

RGB interface timing characteristic

18/16 bit RGB interface (HWM1-0 =11), Vcc = 2.2V to 3.13V

Item	Symbol	Unit	Test Condition	min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 4	10ns	—	1
ENABLE Set up time	tENS	ns	Figure 4	25	—	—
ENABLE Hold time	tENH	ns	Figure 4	40	—	—
VLD Set up time	tVLS	ns	Figure 4	25	—	—
VLD Hold time	tVLH	ns	Figure 4	40	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 4	40	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 4	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 4	100	—	—
Data Set up time	tPDS	ns	Figure 4	25	—	—
Data Hole time	tPDH	ns	Figure 4	40	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 4	—	—	25

6 bit RGB interface (HWM1-0 = 11), Vcc = 2.2V to 3.3 V

Item	Symbol	Unit	Test Condition	Min.	typ.	max.
VSYNC/HSYNC Set up time	tSYNCS	clock	Figure 4	10ns	—	1
ENABLE Set up time	tENS	ns	Figure 4	20	—	—
ENABLE Hold time	tENH	ns	Figure 4	23	—	—
VLD Set up time	tVLS	ns	Figure 4	20	—	—
VLD Hold time	tVLH	ns	Figure 4	23	—	—
DOTCLK “Low” Level pulse width	PWDL	ns	Figure 4	25	—	—
DOTCLK “High” Level pulse width	PWDH	ns	Figure 4	25	—	—
DOTCLK cycle time	tCYCD	ns	Figure 4	55	—	—
Data Set up time	tPDS	ns	Figure 4	20	—	—
Data Hole time	tPDH	ns	Figure 4	23	—	—
DOTCLK, VSYNC, HSYNC rising and falling time	trgbr, trgbf	ns	Figure 4	—	—	25

LCD driver output characteristic

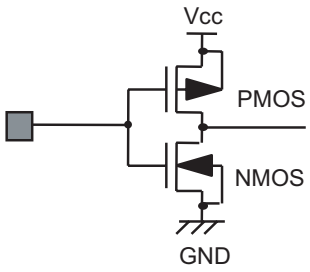
Item	Symbol	Unit	Test Condition	Min.	Typ.	Max	Note
Delay time of output driver	tdd	µs	Vcc = 3V, VLCD = 5.5V, VDH = 5.0V R-C Oscillation; f_{OSC} = 370kHz(320 line) Ta = 25 °C, REV = "0", SAP = "001" VRP14-00 = "0", PKP52-00 = "0", PRP12-00 = "0" VRN14-00 = "0" PKN52-00 = "0", PRN12-00 = "0" All pins change at the same time from same grayscale. The time till output level reaches ±35mV when VCOM polarity changes. Load resistance R = 10kΩ, Load capacity C = 20pF	—	30	—	(10)

Electrical Characteristics notes

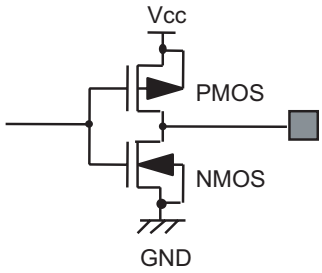
1. For bare die and wafer products, specified up to 85°C.

2. The following three circuits are I pin, i/O pin configuration

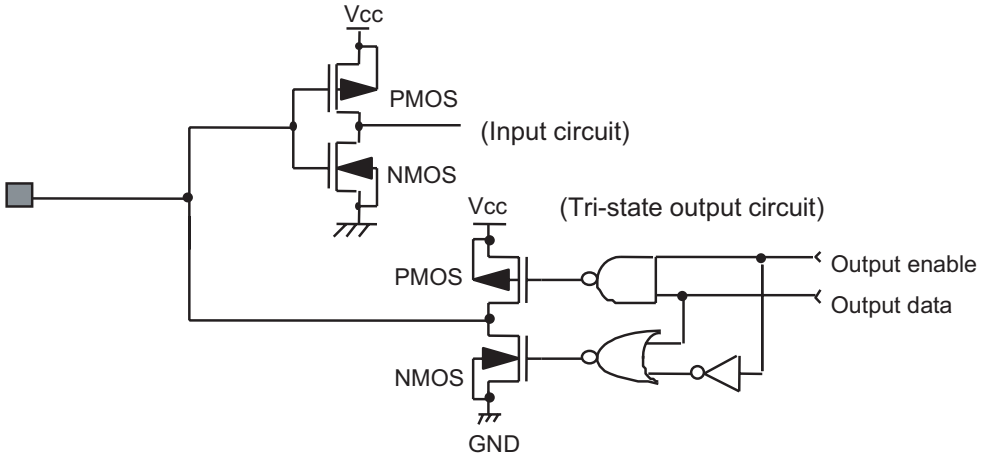
Pins: RESET*, CS*, WR*/SCL, RD, RS, VLD, IM2-1, IM0/ID, TEST, VDDTEST, VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0



Pins: OSC2-3, RESET01, RESET02, FLM, M, DISPTMG, CLA, CLB, CLC, SFTCLK1-2, GCL, GDA, GCS*, EQ, DCCLK



Pins: DB17 -DB2, DB1/SD0, DB0/SD1

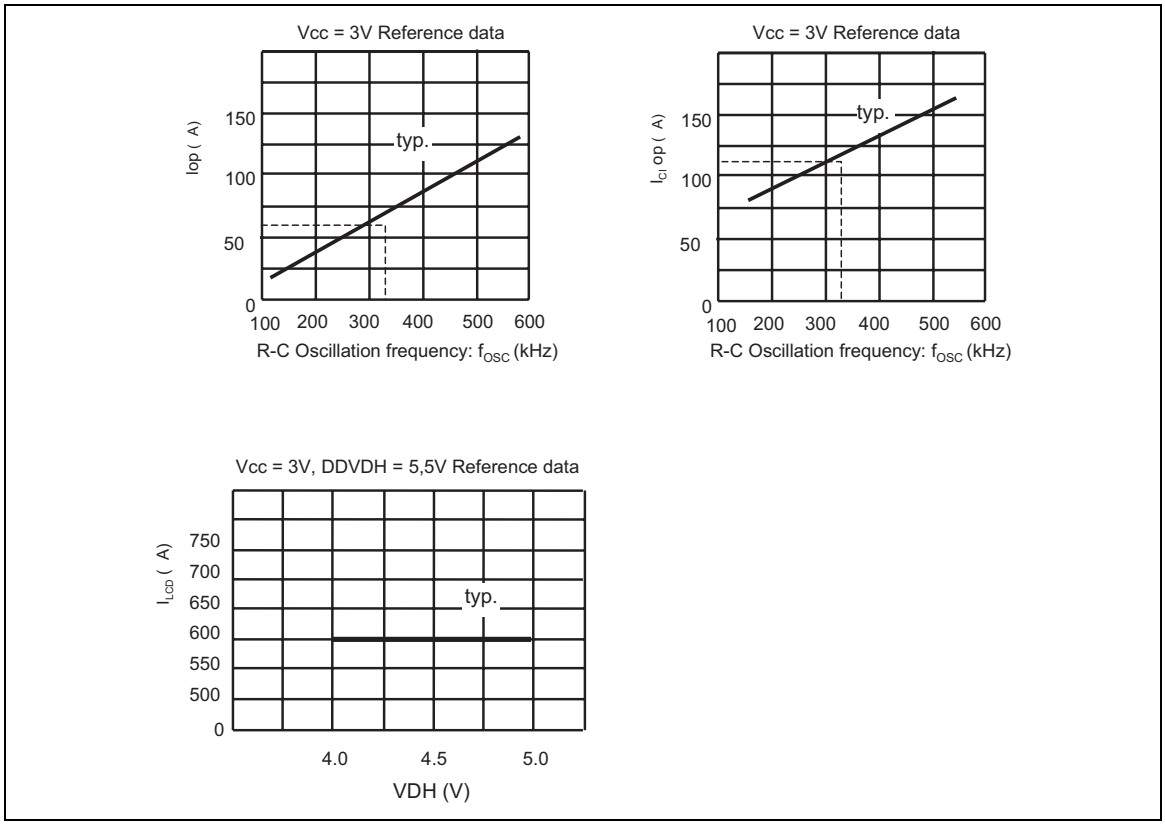


3. The TEST and VDDTEST pin must be grounded and the IM2/1 and IM0/ID pins must be grounded or connected to Vcc.

4. This excludes the current flowing through output drive MOSs.

5. This excludes the current flowing through the input/output units. The input level must be fixed high or low because through current increases if the CMOS input is left floating. Even if the CS pin in low or high when an access with the interface pin is not performed, current consumption does not change.

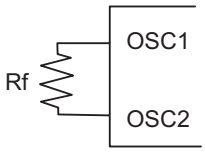
6. The following shows the relationship between the operation frequency (fosc) and current consumption (Icc).



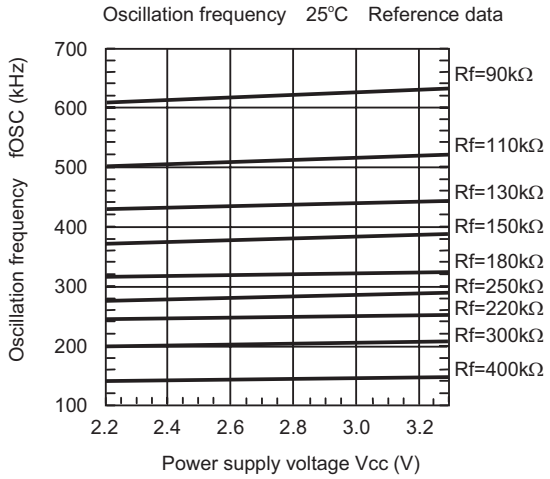
7. Indicates the output voltage difference between the pins next to in the same display. Output voltage deviation is the reverence value.

8. Fluctuation of average output voltage is the deviation of average output voltage between chips. Average output voltage is the average voltage of all pins in one chip.

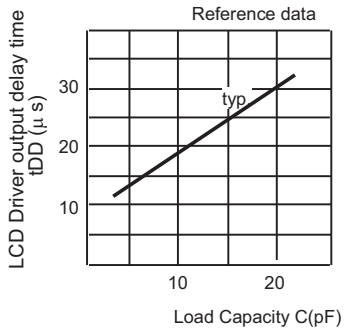
9. Applies to the internal oscillator operations using external oscillation resistor Rf.



Since the oscillation frequency varies depending on the OSC1 and OSC2 pin capacitance, the wiring length to these pins should be minimized.



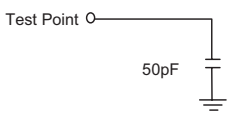
10. Supplies to the internal oscillator operations using external oscillation resistor Rf.



Vcc = 3V, VLCD = 5.5V, VDH = 5.0V, RC Oscillation, fosc = 370kHz (320lines)
Ta = 25ºC, REV = "0", SAP = "001", PKP52-00 = "0", PRP12-00 = "0",
VRP14-00 = "0", PKN52-00 = "0", PRN12-00 = "0", VRN14-00 = "0",
All pins change at the same time from the same grayscale. The time till output level reaches: 35+/-mV when VCOM polarity changes Load resistance R = 10kΩ/1pin

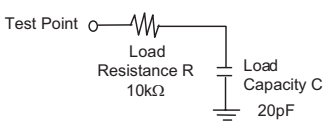
AC characteristic measuring load circuit

Data bus: DB17-DB0, PD17-0

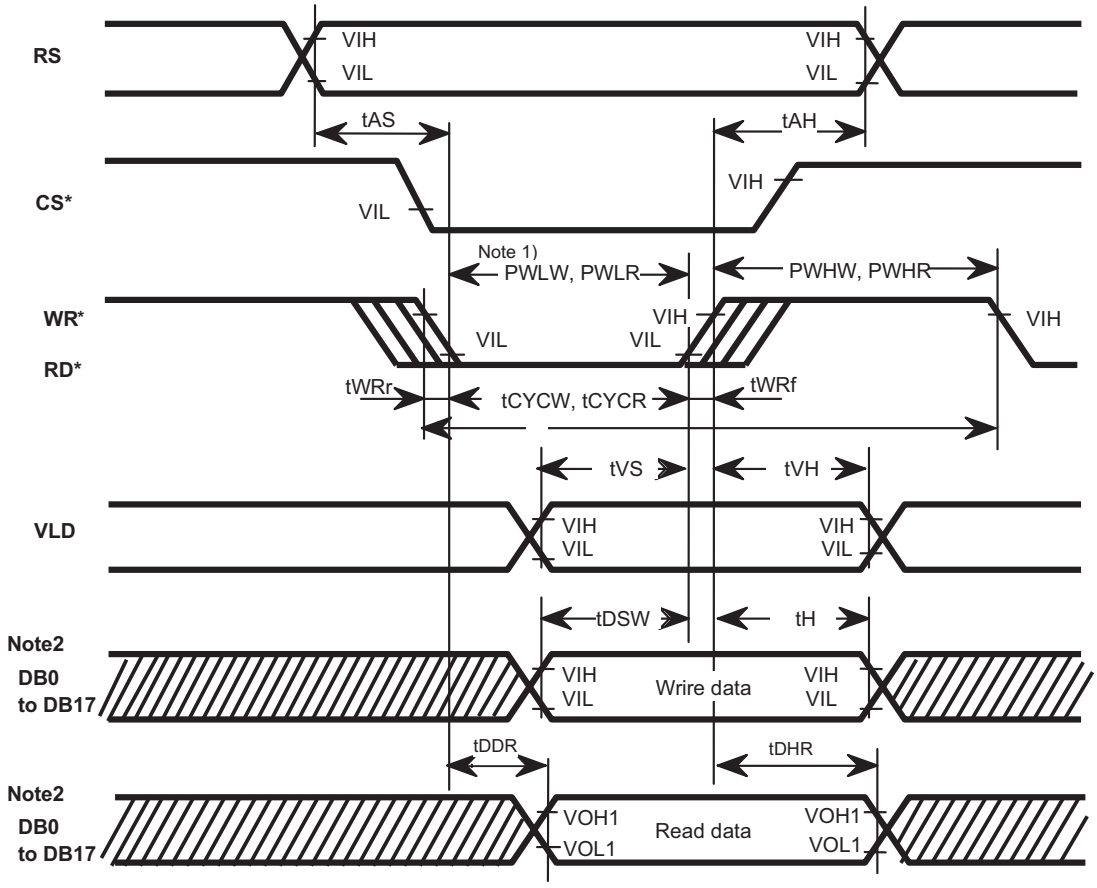


LCD driver output characteristic measuring load circuit

LCD output: S1- S256



80-system Bus Operation



Note1: Unused DB pins while bus interface must be fixed to “Vcc” or “GND” level.

Figure 1

Clock Synchronized Serial Interface Operation

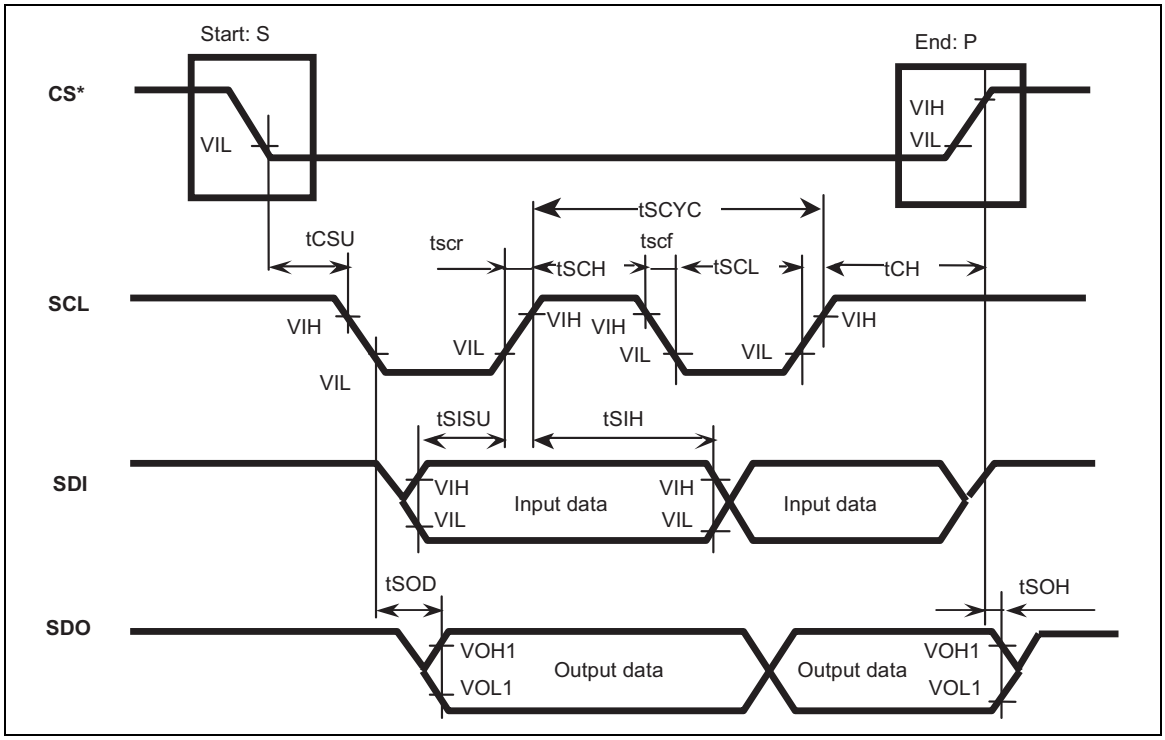


Figure 2

Reset Operation

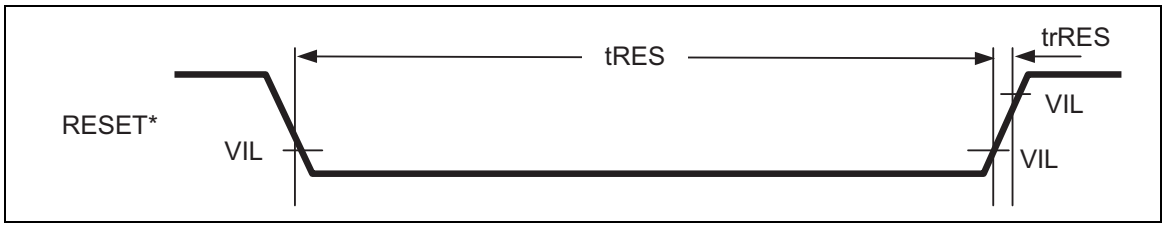


Figure 3

RGB I/F Operation

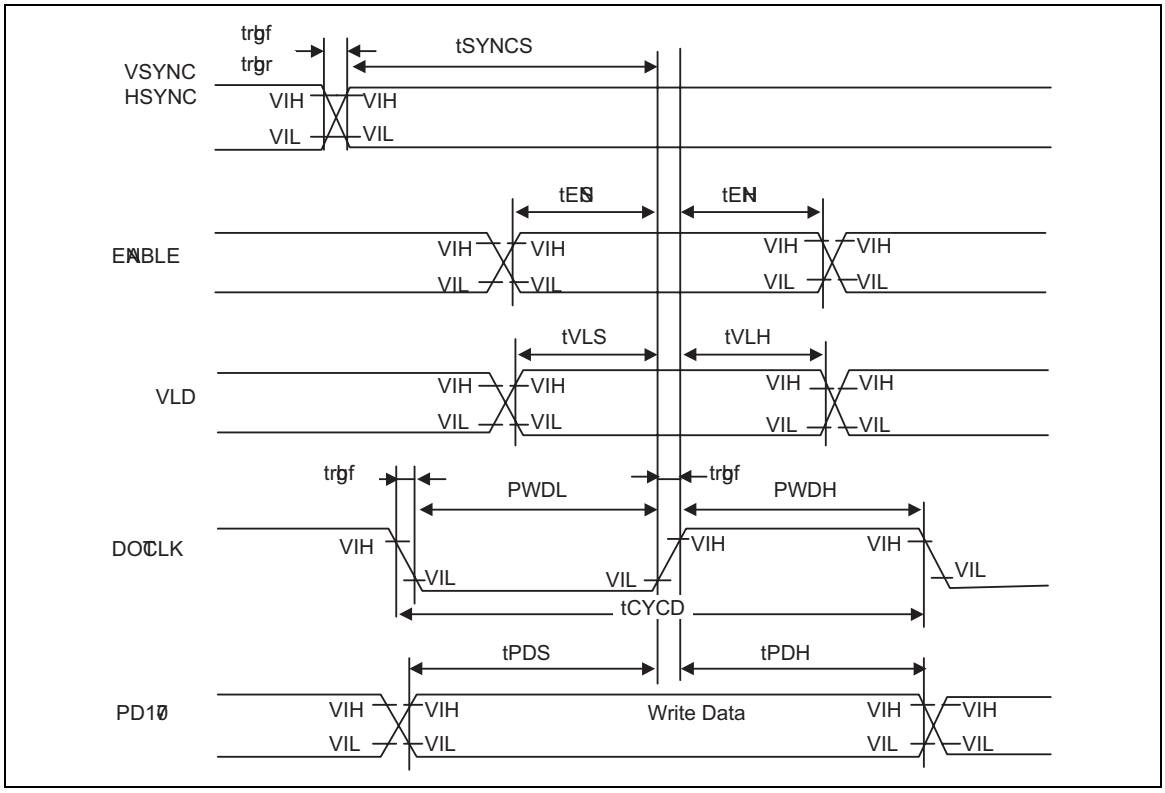


Figure 4

LCD Driver Output Character

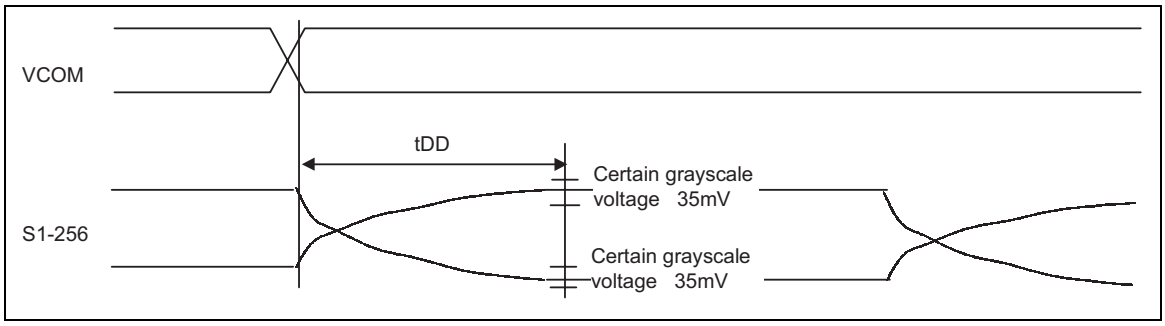


Figure 5

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Revision Record

Rev	Date	Page	Contents
0.0	2002.6.21		First edition
0.1	2002.9.27	All page	Change the number of source channel from “240” to “256”
		2	Capacity of internal RAM from “172,800” to “184,320”.
		3	Add “RESET01” and “RESET02” pins to Figure 1.
			Change “VDD” to “VDD1” and “VDDOUT” to “VDD2” in Figure 1.
			Change capacity of Graphic RAM form “172,800” to “184,320” in Figure 1.
			Delete “PMON” in Figure 1.
		4	Add items to the table in VLD Functions.
		5	Add a new function explanation sentence to the ENABLE.
			Add items to the table in ENABLE Functions.
		6	Change function explanation sentence of VSYNC.
			Add a table in VSYNC Functions.
			Change function explanation sentence of HSYNC.
			Add a table in HSYNC Functions.
			Change function explanation sentence of DOTCLK.
			Add a table in DTCLK Functions.
			Change “FLM” to “FLM1,2”.
			Change “SFTCLK1” to “SFTCLK11, SFTCLK12”.
			Change “SFTCLK2” to “SFTCLK21, SFTCLK22”.
			Change “CLA” to “CLA1, CLA2”.
			Change “CLB” to “CLB1, CLB2”.
			Change “CLC” to “CLC1, CLC2”.
			Change “DISPTMG ”to “DISPTMG1, DISPTMG2”.
			Change “M” to “M1, M2”.
		7	Change “EQ” to “EQ1, EQ2”.
			Change “DCCLK” to “DCCLK1, DCCLK2”.
			Change “GCL” to “GCL1, GCL2”.
			Change “GDA” to “GDA1, GDA2.
			Change “GCS*” to “GCS*1, GCS*2”.
			Change DDVDH from “4.5V to +5.5V” to “4.0V to +5.5V”.
			Add a row of “AGND” after “Vcc, GND”.
			Change “RESET1*, RESET*2” to “RESET1*”.
			Add a row of “RESET01, RESET02” after “RESET1*”.
		8	Change “VDD” to “VDD1”.

Rev	Date	Page	Contents
0.1	2002.9.27	8	Change function explanation sentence of “VDD1”.
			Add a row of “VDD2” after “VDD1”
		9	Add a new page “HD667B768 PAD Arrangement”.
		10,11,12	Add new pages. “HD667B76 PAD Coordinate”.
		13	Add a new page “Bump Arrangement”
		14	Add rows and columns to the Table 4. (VPL)
		17	Change contents of S255 and S256 in Table 6.
		18,19,22, 23, 24	Change “Note” from “n = lower eight bit of address (239 to 0)” to “n = …(0 to 255)”.
		21	Change contents of Table 6. Ex. “000EF”H to “000FF”H
		27	Figure 31: Change pins of IB10 to 5. From “ID7, ID6, ID5, 0,0,0” to “ID10, ID9, ID8, ID7, ID6, ID5”.
		30	Figure 36: Change pins of IB15 and 14. From “0,0” to “TRI, DFM”.
			Change number in Figure 37. From “13FEFFh” to “13FFFh”
		32	Add a new page.
		36	Change a bit of DB12 from “0” to “CAD” in Figure 46.
		40	Add rows to the Table 20.
		41	Change “Number of Clock for 1 period” of Table 22. From “16” to “8.0”, “17” to “8.5”, and “18” to “9.0”.
		57	Change DCCLK operation frequency in Table 51. From “2” to “4”, “4” to “8”, “8” to “16”, and “16” to “32”.
		58	Delete Power control (3) (R102h) in rev. 0.0, and move up the numbers of Power controls. (From “4” to “3”, “5” to “4”, and “6” to “5”.)
		59	Change “E” to “F” in Table 52. (Ex. From “000EF”H” to “000FF”H”.)
		62	Add a new page.
		70	Change “R204h” to “R203h”, and “R205h” to “R204h”.
		71	Change “0” to “VRP14”, and “VRN04” to “0”.
		74	Change “EF” to “FF”in a explanation sentence of “HSA7-0/HEA7-0” and Figure 92.
		75	Change “102h”. (From “Power control (2)” to “Setting inhibited”.)
		81	Add explanation sentence of 80-system 8-bit bus interface. (“According to the setting of TRI, RAM data for one word are divided into two ot three for two time transfer or three time transfer.”)
		82	Add a new page.
		89	Change RAM write speed from “5.70MHz” to “6.08MHz.
			Change the time of RAM write from “76800” to “81920”.
		90	Change Ram write speed from “5.70MHz” to “6.08MHz”.
		102	Delete “R202” from the Index in Figure 134.
		104	Add a sentence, “Can be set by word unit”, to the explanation o f Window address of High-Speed RAM Write.
		105	Change “HSA1-0= “10, HEA1-0= “00” to “HSA7-0, HEA7-0”.

Rev	Date	Page	Contents
0.1	2002.9.27	105	Change “h13FEF” to “h13FFF” in Figure 136.
		106	Change “EF” to “FF” in Figure 137.
		107	Delete the cells of LG2-0 in Table 66.
		124	Add a new page.
		Non	Delete a page of indicating a flow of switching display mode.
		126	Revise the Figure 158.
		Non	Delete a page of Cadd mode.
		127	Change “Cst mode 1” to “Mode 1”
			Delete “(1) CAD = 0: Cst mode”
			Delete (*5).
		128	Revise Figure 159.
		129	Change “Cst mode 2” to “Mode 2”.
			Delete (1) CAD = 0: Cst mode”
			Delete (*5).
		130	Revise Figure 160.
		131	Revise the Figure 161.
		134	Revise the Figure 164.
		141	Change “241” to “321”, “242” to “322”, and “256” to “336” in Figure 171.
		146-158	Add new pages.
0.21	2002.10.17	127	Delete p127 to 130 in revision 0.1 and insert a new p127 “Example of chipset connection”. Clearly indicated the Note “Vcc and Vci” and “AGND and GND” must be connected on FPC”.
0.3	2002.11.21	all	Correct “HD667P10” to “667P20”
		7	Functions of “RS”: Correct “Low: Index/status” to “Low :Index”.
		8	Functions of “WR*/SCL”: Correct “Data is written on …” to “Data is read…”.
		11	Functions of “V0p, V63P: Correct “(SAP2-0= “001”, “010”, “001”…” to “(SAPO2-0 = “001”, “010”, “011”…)”.
			Delete the row of “VDDOUT”.
		18	Delete “conventional” from the description of External Display Interface (RGB-I/F, VSTNC-I/F).
		21	Correct the title of Figure 10 from “80-system 8-bit interface/SPI” to “80-system 8-bit interface (1)”.
		25	Correct the title of Figure 20 from “80-system 8-bit interface/SPI” to “80-system 8-bit interface (1)”.
		29	Correct the title of Figure 30 from “80-System 8-Bit Interface (SPI two transfers/pixel)” to “80-System 8-Bit Interface/ SPI (two transfers/pixel)”.
		33	Description of “HWM1-0”: Correct ”When HWM=1…” to “When HWM=11…”.

Rev	Date	Page	Contents
0.3	2002.11.21	33	Description of “AM”: Correct the second sentence. “the data is continuously written in parallel” to “the data is continuously written horizontally”.
		35	Add Figure 41.
		39	Correct “HD66772” to “HD66776” in the description of “IDX2-0”.
			Correct Figure 46.
		43	Formula for the frame frequency: Correct “Clock cycles per raster-row” from “RTN bit” to “RTNI bit”.
		43	Table 22: Correct “Number of Clock for 1 period” as below. Error Correct 8.0 clock 16 clock 8.5 clock 17 clock 9.0 clock 18 clock 127.0 clock 254 clock 127.5 clock 255 clock
		58	Correct Table 48.
		59	Delete “gate driver” from the description of “SLP”.
			Change ”gate driver” to “power supply IC” in the description of “STB”.
		61	Add “Power Control 6 (105h)” in title and in Figure 67.
			Add the description of “VGH4-0” and “VGL4-0”.
			Add “VREG2OUT” in the description of “VRL2”.
			Correct the description of “PON ”from “Operation start bit for the step-up 3 circuit” to “Set operation/stop of VLOUT3.”.
			Add “VGH4-0” and “VGL4-0” in the Note.
		78	Correct Table 57 Instruction list.
		79	Delete “gate driver” from the description of “Reset Function”.
		97	Delete sentences from the description of “VLD and ENABLE signal”. (Deleted sentences: “When ENABLE is active, the address is not updated. When VLD is active and ENABLE is active, the address is updated. ENABLE must be set to “L”.)
		98	Correct “VSYNC” to “RGB” in the description on Note in Figure 121.
		99	Correct “clock” to “pixel” in Note1, and “VSYNC” to “RGB” in Note 3.
		101	Correct “MIF1-0 = pins to “01” to “RIM1-0 = “00”” in the description of 18-bit RGB interface.
		102	Add “6-bit RGB interface” to the description of “Usage on external display interface d)”.
			Correct “PD17-0” to “PD17-12” in the description of “Usage on external display interface d).
		106	Correct the waveform of Figure 134. (Upside down)
		107	Correct the waveform of Figure 135. (Upside down)
		109	Correct “(HS71 to 0,)” to “(HAS 7 to 0) in the description of “High-Speed RAM Write in the Window in the Waveform Address.

Rev	Date	Page	Contents
0.3	2002.11.21	109	Correct “AD = h00810” in the flow to “AD = h00812” in the flow.
		113	Correct “WM17-0 = “007FF”H” to “WM17-0 = “00FFF” in Figure 140.
		114	Correct “WM17-0 = “007FF”H” to “WM17-0 = “00FFF” in Figure 141.
		125	Correct “262,114” to “262,144” in Table 77.
		135	Correct “t1:20ns” to “t1:45ns” and “t2: 20ms” to t2: 25ns” in Figure164.
		141	Delete “on the master side” from Note in Figure 170.
		145	Change “(R14) to (R402, R403)” and “(R15)” to “(R404, R405)” in the description of “Restrictions on 1st/2nd Screen Driving Position register Settings”.
			Change “In all other display area refers to the output level based on the PT setting. (non-display)” to “RAM data in other areas are not displayed.”
			Correct “SE27” to “SE28”, “SS27” to “SS28”, “SE17” to “SE18” and “SS17” to “SS18” in Table 80.
		149,150	Correct numbers in Min of Table 84, 85,86, and 87.
		153	Correct numbers in Min of Table 93.
		154	Correct “Pins: DB15-DB2…” to “Pins: DB17-DB2…” in Figure 176.
		155	Correct Note 4, 5, 6, 7, and 8.
		158	Add “trRES” to Figure 186.
		159	Correct “S1-528” to “S1 to 256” in Figure 188.
1.01	2003.3.5	5	Correct power supply voltage. From “Vcc = 1.7 to 3.3V” to “Vcc = 2.2 to 3.3V”. From “DDVDH = 4.0 to 5.5V” to “DDVDH = “4.0 to 5.9V”.
		6	Correct Block diagram
		10	Correct Function of DDVDH. From “4.0 V to +5.5V” to “4.0V to 5.9V”
			Correct Function of VDH. From HD667P20” to “HD667P21”.
			Correct Function of Vcc, GND. From “+1.7V to +3.3V” to “2.2V to +3.3V”.
			Correct Function of DUMMY pin.
		17	Add a new page. “Pin connecting resistance recommended value”
		18	Correct the first sentence of System interface explanation. From “The HD66776 has four high-speed,,,,” to “ The HD66776 has five high-speed,,,,,”
		39	Correct explanation of FP3-0/BP3-0.
			Add “Instruction for setting FP.BP”
		40	Correct tabel”HD667P20 Instruction chart”
		47	Correct “DIVE1-0”.
		64	Add “LRL3”. Correct “VCOMG” , “VDV4-0”, and “VRL2”.
		81	Add “VRL3(0)” to the Instruction chart.
		138	Correct “Power supply On” setting flow.
		141	Correct “Deep stand-by” setting flow.
		161-163	Correct “Electrical characteristic”.

Rev	Date	Page	Contents
1.10	2003.7.15	43	Delete “Dk1” from the table of HD667P20 instruction
		66	Correct description of VRL3-0 bits.
1.11	200.10.2	33	Error correction. Driver Output Control register