

HD66779

366-channel Source Driver
for 262,144-color Displays (64 grayscale)
for Amorphous Silicon,
Low-temperature Poly-silicon TFT Panels

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Description

The HD66779 is a channel source driver LSI compliant to 366-channel graphics display on TFT LCD in 262,144 colors. With an internal timing controller, the HD66779 can adjust LCD signals to an optimum timing.

The HD66779 incorporates 18-bit RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD 17-0) for moving picture display. As a system interface with microcomputer, the HD66779 adopts a serial interface which enables high quality display and low power consumption through instruction settings.

The HD66779 enables precise management of power by software, which makes this LSI the best solution for medium or small-sized portable products such as digital cellular phones or PDA supporting WWW browser, where long battery life is major concern.

Features

- 366-channel output built-in liquid-crystal display driver circuit
- 6-bit (grayscale data) x RGB data
- 18-bit built-in RGB Interface for moving picture display: VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0
- multicolor display: 262,144 colors simultaneously available
- Built-in timing controller: adjust LCD signals to an optimized timing
- 10 reference power supply voltage pins enables optimum γ compensation according to liquid crystal characteristics
- System interface: Serial Peripheral Interface (SPI)
- Border display: 6-channel border display by mode setting
- Cascade connection
- Reversible source-driver shift direction
- Built-in level shift circuit for LCD signals
- Built-in Vcom generating circuit
- Raster-row inversion drive
- High-speed operation: 10MHz Max.
- Power supply voltage range

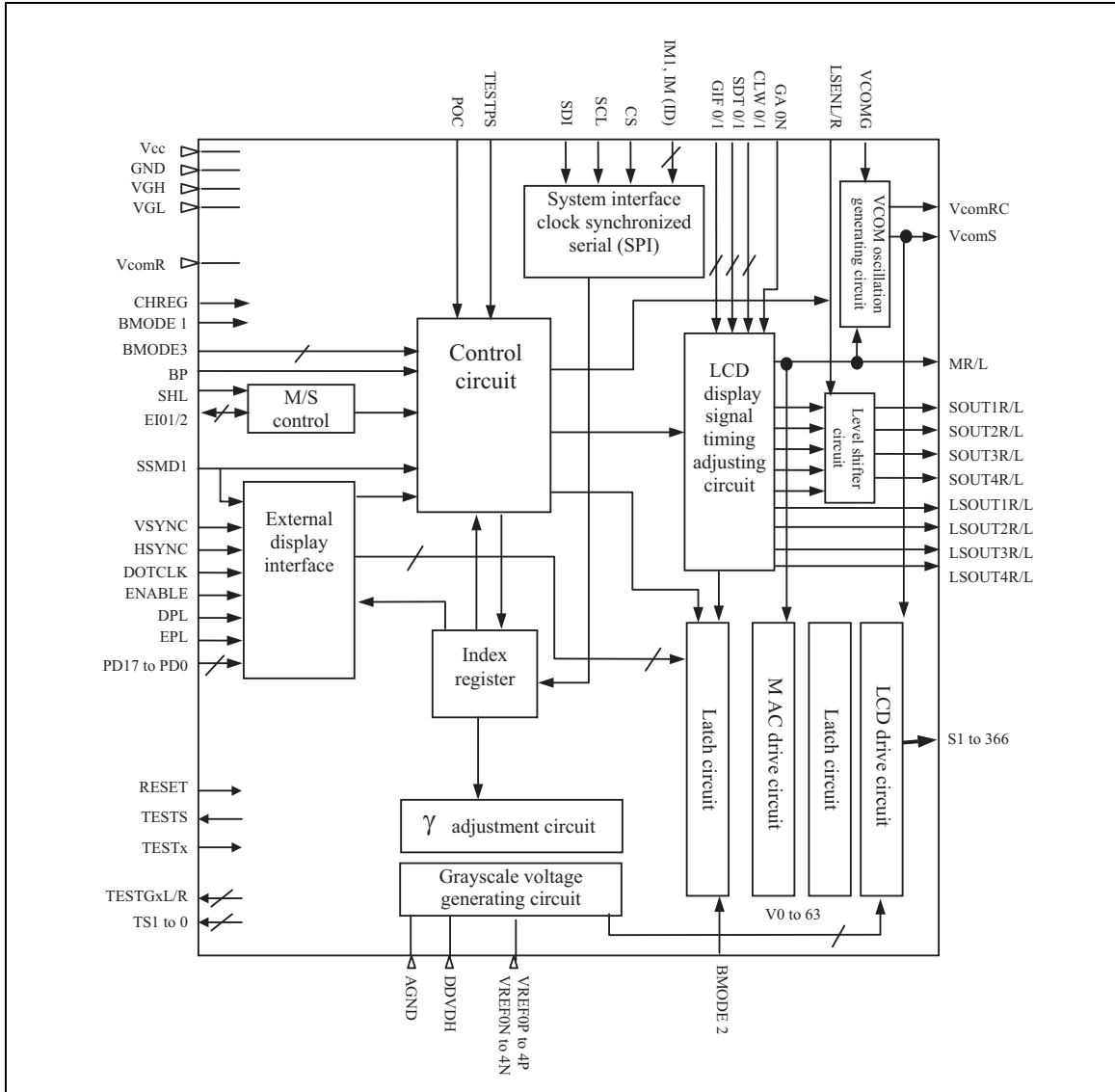
Input voltage level

- Logic power supply voltage: $V_{cc} = 2.5V \sim 3.6V$
- Source driver power supply voltage: $DDVDH = 3.5V \sim 5.5V$
- Gate driver power supply voltage: $VGH - VGL = 16V \sim 35V$
 $VGH - AGND = 8V \sim 20V$
 $VGL - AGND = -15V \sim -8V$

Output voltage level

- Output for LCD display panel: $SOUT1-4R/L = VGL \sim VGH$
 $LSOUT1-4R/L, M = GND \sim V_{cc}$
- Source output $S1$ to $S366 = AGND + 0.3 \sim DDVDH - 0.3$
- VCOMS output voltage $VCOMS = AGND \sim DDVDH$

Block Diagram

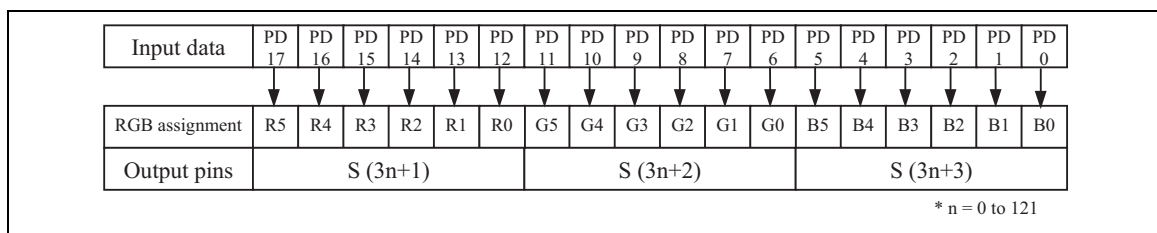


Block Function

(1) External Display Interface (RGB -I/F)

The HD66779 incorporates RGB-I/F as an external interface for moving picture display. In the RGB-I/F mode, the HD66779 operates in synchronization with externally supplied signals (VSYNC, HSYNC, and DOTCLK), and takes in data according to data enable signal (ENABLE). See “RGB interface timing” for details.

The correspondence between input and output data is as follows.



(2) Control circuit

Generate internal control signal from each signal.

(3) Grayscale Voltage Generation Circuit

Generates positive-polarity 64 grayscales and negative-polarity 64 grayscales by dividing external input voltage with resistors to enable display in 262,144 colors. See the “Grayscale Amplifier Configuration” for details.

(4) Timing Generator

Generate timing signals for LCD display operation.

(5) LCD Driver Circuit

The LCD driver circuit comprises a 366-source-output (S1-S366) driver. Line-latch display pattern data and output drive waveform. The shift direction of source output is changeable, i.e. (S1, S2, S3) to (S364, S365, S366) or (S364, S365, S366) to (S1, S2, S3), depending on the assembly.

(6) VCOM oscillation generator circuit

Generate oscillation signal VcomS to further generate Vcom, which is supplied to the TFT common electrode. Alternate at amplitude of either VcomR or GND level depending on the AC frequency signal.

(7) Level shifter circuit

Change operation voltage level from that of logic circuit “Vcc to GND” to that of gate drive circuit “VGH to VGL”.

(8) System interface clock synchronized serial circuit

Interfacing with a microcomputer enables register setting for each mode setting.

Pin function

Signals	Number of pins	I/O	Connected to	Function
DDVDH	1	I	Power supply	Power supply for the source driver. DDVDH = +3.5 ~ +5.5V. Make sure $V_{GH} \geq DDVDH \geq V_{CC}$.
AGND	1	I	Power supply	Grand for the source driver. AGND = 0V.
Vcc	1	I	Power supply	Power supply for the logic. Vcc = +2.5V ~ +3.6V Make sure $V_{GH} \geq DDVDH \geq V_{CC}$.
GND	1	I	Power supply	Grand for the logic. GND = 0V.
VGH	1	I	Power supply	Power supply for a level shifter. VGH = +8.0V ~ +20V Make sure $V_{GH} \geq DDVDH \geq V_{CC}$.
VGL	1	I	Power supply	Power supply for a level shifter. VGL = -15V ~ - 8.0V
VcomR	1	I	Power supply	Input high level of VcomS
VcomRC	1	O	Stabilizing capacitor	Output high level of VcomS
VcomS	1	O	Capacitor	Amplitude signal for alternating operation. Serve as a power supply for the electrode pair (common) of TFT display by coupling with an external circuit.
RESET	1	I	MPU or external CR circuit	Reset pins. Initialized while "Low". Power-on reset required after turning on the power supply.
VREF0P-4P VREF0N-4N	10	I	Power supply	Power supply for γ compensation. Must observe the following relationships when supplying voltage. <ul style="list-style-type: none"> · $DDVDH-0.3V \geq VREF0P > VREF1P > VREF2P > VREF3P > VREF4P \geq AGND+0.3V$ · $DDVDH-0.3V \geq VREF0N > VREF1N > VREF2N > VREF3N > VREF4N \geq AGND +0.3V$ · $DDVDH-1.0V \geq VREF1P, VREF1N$ $VREF3P, VREF3N \geq GND + 1.0V$
TEST1, 5-15 TESTM2 TESTSM2	14	I	GND	Test pins. Must be fixed to GND level.
VTES, VTEST, COMP, TS1-0 COMM	6	O	Open	Test pins. Must be disconnected.
VCOMMH, VCOMHC, VEQ, VCOMC	4	O	Open	Test pins. Must be disconnected.

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Signals	Number of pins	I/O	Connected to	Function						
TESTG1-3R TESTG1-3L	6	O	Open	Test pins. Must be disconnected.						
TESTS	1	O	Open	Test pin. Must be disconnected.						
TESTPS TEST4	2	I	Vcc	Test pin. Must be fixed to the Vcc level.						
S1 ~ S366	366	O	LCD	Output voltage applied to liquid crystal. The shift direction of source output is changeable with SHL pin. SHL = "High": (S1, S2, S3) to (S364, S365, S366) SHL = "Low": (S364, S365, S366) to (S1, S2, S3)						
BMODE1	1	I	GND or Vcc	Select border mode. BMODE1 = "High": border display (360ch display + 6-ch border) BMODE1 = "Low": No border display (360ch) Border display lasts 320H.						
BMODE2	1	I	GND or Vcc	Select pins used for the border mode. BMODE2 = "High": Right side BMODE2 = "Low": Left side						
BMODE3	1	I	GND or Vcc	Select the border color while using DE transfer mode. With normally white display, BMODE3 = "High": BLACK BMODE3 = "Low": WHITE While using DE transfer mode, 6-channel (2RGB) border color is made on the left/right sides only.						
POC	1	I	MPU or Vcc	Power control signal. POC = "High": Normal mode POC = "Low": Power control mode When POC = "L", Non-lit display is shown (white display in normally white mode). For details, see "Power Control Mode". The initialized value for the border is "1" for all.						
SHL	1	I	GND or Vcc	Control the shift direction of display data. SHL = "High": (S364,S365,S366) to (S1,S2,S3) SHL = "Low": (S1,S2,S3) to (S364, S365, S366)						
VCOMG	1	I	GND or Vcc	Vcom generator enable signal <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VCOMG</th> <th>Vcom output</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>Vcom generating</td> </tr> <tr> <td>L</td> <td>GND</td> </tr> </tbody> </table>	VCOMG	Vcom output	H	Vcom generating	L	GND
VCOMG	Vcom output									
H	Vcom generating									
L	GND									
CHREG	1	I	GND or Vcc	Switch between the pin setting and the register setting. CHREG = "High": Register setting is valid. All pin settings are made invalid. CHREG = "Low": The settings for pins, POC, POS, BP,GAON, GIF1-0, CLW1-0, SDT1-0 are valid.						

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Signals	Number of pins	I/O	Connected to	Function															
VSYNC	1	I	MPU	Frame synchronizing signal. "Low" active signal.															
HSYNC	1	I	MPU	Line synchronizing signal. "Low" active signal.															
DOTCLK	1	I	MPU	Dot clock signal. The timing for reading data is selected with DPL pin.															
PD17 ~ PD0	18	I	MPU	Input display data of 6-bit (grayscale) x 3 pixels. As data is transferred with these pins, unused pins must be fixed to either "Vcc" or "GND" level. <table border="1"> <thead> <tr> <th>PD17 to PD12</th> <th>PD11 to PD6</th> <th>PD5 to PD0</th> </tr> </thead> <tbody> <tr> <td>MSB.....LSB</td> <td>MSB.....LSB</td> <td>MSB.....LSB</td> </tr> <tr> <td>S (3n+1)</td> <td>S (3n+2)</td> <td>Sn (3n+3)</td> </tr> </tbody> </table> <p style="text-align: right;">* n = 0 to 121</p>	PD17 to PD12	PD11 to PD6	PD5 to PD0	MSB.....LSB	MSB.....LSB	MSB.....LSB	S (3n+1)	S (3n+2)	Sn (3n+3)						
PD17 to PD12	PD11 to PD6	PD5 to PD0																	
MSB.....LSB	MSB.....LSB	MSB.....LSB																	
S (3n+1)	S (3n+2)	Sn (3n+3)																	
ENABLE (DE)	1	I	MPU	Data enable signal. <table border="1"> <thead> <tr> <th>EPL</th> <th>ENABLE</th> <th>Data write</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Valid</td> </tr> <tr> <td>L</td> <td>H</td> <td>Invalid</td> </tr> <tr> <td>H</td> <td>L</td> <td>Invalid</td> </tr> <tr> <td>H</td> <td>H</td> <td>Valid</td> </tr> </tbody> </table>	EPL	ENABLE	Data write	L	L	Valid	L	H	Invalid	H	L	Invalid	H	H	Valid
EPL	ENABLE	Data write																	
L	L	Valid																	
L	H	Invalid																	
H	L	Invalid																	
H	H	Valid																	
EI01/2	2	I/O	HD66779	Start pulse signal. SHL signal controls the switch between input and output. When the signal is used as output, output the H pulse and start up the next raster-row driver. <table border="1"> <thead> <tr> <th>SHL</th> <th>EI01</th> <th>EI02</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>Input</td> <td>Output</td> </tr> <tr> <td>H</td> <td>Output</td> <td>Input</td> </tr> </tbody> </table> <p>When using EI0/2 as input, use as start pulse input or fix to Vcc level.</p>	SHL	EI01	EI02	L	Input	Output	H	Output	Input						
SHL	EI01	EI02																	
L	Input	Output																	
H	Output	Input																	
DPL	1	I	GND or Vcc	Set the polarity of DOTCLK pin while receiving data (PD17 to 0). DPL = "Low": Read data at DOTCLK falling edge. DPL = "High": Read data at DOTCLK rising edge.															
EPL	1	I	GND or Vcc	Set the polarity of ENABLE pin while receiving data (PD17 to 0). EPL = "L": When ENABLE = "L", data write is valid. When ENABLE = "H", data write is invalid. EPL = "H": When ENABLE = "L", data write is invalid. When ENABLE = "H", data write is valid.															

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Signals	Number of pins	I/O	Connected to	Function																								
BP	1	I	GND or Vcc	<p>Set a back porch during vertical period.</p> <p>BL = "L": Back porch = 4 Receive data (PD17 to 0) after 4H after VSYNC assertion</p> <p>BL = "H": Back porch = 8 Receive data (PD17 to 0) after 8H after VSYNC assertion</p> <p>* In the DE transfer mode (SSMD1 = "H"), BP setting is made invalid.</p>																								
CLW0/1	2	I	GND or Vcc	<p>Set the delay amount of the output signal from SOUT2/ SOUT3.</p> <table border="1"> <thead> <tr> <th colspan="4">Delay amount</th> </tr> <tr> <th>CLW1</th> <th>CLW0</th> <th>Delay time</th> <th>5MHz (e.g.)</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>0μS</td> <td>0 clock</td> </tr> <tr> <td>L</td> <td>H</td> <td>2.0μS</td> <td>10clocks</td> </tr> <tr> <td>H</td> <td>L</td> <td>4.0μS</td> <td>20 clocks</td> </tr> <tr> <td>H</td> <td>H</td> <td>6.0μS</td> <td>30 clocks</td> </tr> </tbody> </table> <p>* The delay time changes depending on the frequency of DOTCLK.</p>	Delay amount				CLW1	CLW0	Delay time	5MHz (e.g.)	L	L	0 μ S	0 clock	L	H	2.0 μ S	10clocks	H	L	4.0 μ S	20 clocks	H	H	6.0 μ S	30 clocks
Delay amount																												
CLW1	CLW0	Delay time	5MHz (e.g.)																									
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H	L	4.0 μ S	20 clocks																									
H	H	6.0 μ S	30 clocks																									
SDT0/1	2	I	GND or Vcc	<p>Set the delay amount of source output.</p> <table border="1"> <thead> <tr> <th colspan="4">Delay amount</th> </tr> <tr> <th>SDT1</th> <th>SDT0</th> <th>Delay time</th> <th>5MHz (e.g.)</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>2.0μS</td> <td>10 clocks</td> </tr> <tr> <td>L</td> <td>H</td> <td>3.0μS</td> <td>15 clocks</td> </tr> <tr> <td>H</td> <td>L</td> <td>4.0μS</td> <td>20 clocks</td> </tr> <tr> <td>H</td> <td>H</td> <td>5.0μS</td> <td>25 clocks</td> </tr> </tbody> </table> <p>* The delay time changes depending on the frequency of DOTCLK.</p>	Delay amount				SDT1	SDT0	Delay time	5MHz (e.g.)	L	L	2.0 μ S	10 clocks	L	H	3.0 μ S	15 clocks	H	L	4.0 μ S	20 clocks	H	H	5.0 μ S	25 clocks
Delay amount																												
SDT1	SDT0	Delay time	5MHz (e.g.)																									
L	L	2.0 μ S	10 clocks																									
L	H	3.0 μ S	15 clocks																									
H	L	4.0 μ S	20 clocks																									
H	H	5.0 μ S	25 clocks																									
ML MR	2	O	Power supply or open	<p>AC cycle clock signal. (Output logic level)</p> <p>ML and MR output a same signal. Due to chip layout, ML and MR are arranged on the left and right sides respectively. Use either one of them and left the other open.</p>																								
SOUT1L SOUT1R	2	O	Gate circuit	<p>Frame pulse signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL).</p> <p>SOUT1L and SOUT1R output a same signal. Due to chip layout, SOUT1L and SOUT1R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.</p>																								

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Signals	Number of pins	I/O	Connected to	Function																									
SOUT2R SOUT2L	2	O	Gate circuit	<p>Line cycle clock signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL).</p> <p>The line cycle mode is changeable by the combination of gate interface output select signal pins (GIF0, GIF1).</p> <p>SOUT2L and SOUT2R output a same signal. Due to chip layout, SOUT2L and SOUT2R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.</p>																									
SOUT3R SOUT3L	2	O	Gate circuit	<p>Signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL).</p> <p>The switch between line cycle mode and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1).</p> <p>SOUT3L and SOUT3R output a same signal. Due to chip layout, SOUT3L and SOUT3R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.</p>																									
SOUT4R SOUT4L	2	O	Gate circuit	<p>Signal for LCD display. (Level shifter output with operational voltage amplitude VGH-VGL).</p> <p>The switch between gate off control signal and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1).</p> <p>SOUT4L and SOUT4R output a same signal. Due to chip layout, SOUT4L and SOUT4R are arranged on the left and right sides respectively. Use either one of them and left the other open. The LSEL/LSER pin function enables to halt output from either one or both.</p>																									
LSENR	1	I	GND or Vcc	<p>Level shifter enable signal.</p> <p>LSENR = "H": SOUT1/2/3/4R = level shifter output</p> <p>LSENR = "L": SOUT1/2/3/4/R = "VGL" output</p>																									
LSENL	1	I	GND or Vcc	<p>Level shifter enable signal.</p> <p>LSENL = "H": SOUT1/2/3/4L = Level shifter output</p> <p>LSENL = "L": SOUT1/2/3/4L = "VGL" output</p>																									
GIF0/1	2	I	MPU or Vcc or GND	<p>Select display signal.</p> <table border="1"> <thead> <tr> <th>GIF1</th> <th>GIF0</th> <th>L/SOUT2</th> <th>L/SOUT3</th> <th>L/SOUT4</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>Line cycle clock 1</td> <td>Line cycle clock 2</td> <td>open</td> </tr> <tr> <td>L</td> <td>H</td> <td>Line cycle clock 1</td> <td>Line cycle clock 2</td> <td>Gate off signal</td> </tr> <tr> <td>H</td> <td>L</td> <td>Line cycle clock 1</td> <td>Line cycle clock 2</td> <td>Gate all on</td> </tr> <tr> <td>H</td> <td>H</td> <td>Line cycle clock 3</td> <td>Gate all on</td> <td>Gate off signal</td> </tr> </tbody> </table>	GIF1	GIF0	L/SOUT2	L/SOUT3	L/SOUT4	L	L	Line cycle clock 1	Line cycle clock 2	open	L	H	Line cycle clock 1	Line cycle clock 2	Gate off signal	H	L	Line cycle clock 1	Line cycle clock 2	Gate all on	H	H	Line cycle clock 3	Gate all on	Gate off signal
GIF1	GIF0	L/SOUT2	L/SOUT3	L/SOUT4																									
L	L	Line cycle clock 1	Line cycle clock 2	open																									
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H	H	Line cycle clock 3	Gate all on	Gate off signal																									

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Signals	Number of pins	I/O	Connected to	Function												
LSOUT1R LSOUT1L	2	O	Gate circuit	Frame pulse signal for LCD display. (Output logic level) LSOU1L and LSOUT1R output a same signal. Due to chip layout, LSOUT1L and LSOUT1R are arranged on the left and right sides respectively. Use either one of them and left the other open.												
LSTOU2R LSOUT2L	2	O	Gate circuit	Line cycle clock signal for LCD display. (Output logic level) The line cycle mode is changeable by the combination of gate interface output select signal pins (GIF0, GIF1). LSOUT2L and LSOUT2R output a same signal. Due to chip layout, LSOUT2L and LSOUT2R are arranged on the left and right sides respectively. Use either one of them and left the other open.												
LSOUT3R LSOUT3L	2	O	Gate circuit	Signal for LCD display. (Output logic level). The switch between line cycle mode and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). SOUT3L and SOUT3R output a same signal. Due to chip layout, SOUT3L and SOUT3R are arranged on the left and right sides respectively. Use either one of them and left the other open.												
LSOUT4R LSOUT4L	2	O	Gate circuit	Signal for LCD display. (Output logic level). The switch between gate off control signal and Gate-all-on control signal is made by the combination of gate interface output select signal pins (GIF0, GIF1). LSOUT4L and LSOUT4R output a same signal. Due to chip layout, LSOUT4L and LSOUT4R are arranged on the left and right sides respectively. Use either one of them and left the other open.												
GAON	1	I	MPU or GND	Gate-all-on signal. GAON = "1": Gate output signal "H" GAON = "0": Gate output signal "L" Output form SOUT3/4 and LSOUT3/4.												
DUMMY1-12	12	O	-	Test pins. Must be disconnected.												
IM1, IM0(ID)	2	I	GND or Vcc	Select interfacing mode with MPU. <table border="1"> <thead> <tr> <th>IM1</th> <th>IM0/ID</th> <th>MPU interfacing mode</th> <th>Pins</th> </tr> </thead> <tbody> <tr> <td>GND</td> <td>ID</td> <td>Serial Peripheral Interface (SPI)</td> <td>SDI/SCL</td> </tr> <tr> <td>Vcc</td> <td>*</td> <td>Border color setting (DE transfer mode)</td> <td>BMODE3</td> </tr> </tbody> </table> Use IM0 pin to make a device code ID setting. RGB I/F mode: Use IM1 = GND. DE transfer mode: Use IM1 = Vcc.	IM1	IM0/ID	MPU interfacing mode	Pins	GND	ID	Serial Peripheral Interface (SPI)	SDI/SCL	Vcc	*	Border color setting (DE transfer mode)	BMODE3
IM1	IM0/ID	MPU interfacing mode	Pins													
GND	ID	Serial Peripheral Interface (SPI)	SDI/SCL													
Vcc	*	Border color setting (DE transfer mode)	BMODE3													

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Signals	Number of pins	I/O	Connected to	Function
CS	1	I	MPU	Chip selection signal for Serial Peripheral Interface (SPI). “Low”: Select (accessible) “High”: (inaccessible) When not used, fix to the “Vcc” level.
SCL	1	I	MPU	Synchronizing clock signal for Serial Peripheral Interface (SPI). When not used, fix to the “Vcc” level.
SDI	1	I	MPU	Serial data input pin (SDI) for Serial Peripheral Interface (SPI). When not used, fix it to the “Vcc” level.
SSMD1	1	I	MPU or GND	Specify the transfer mode. SSMD1 = “H”: DE transfer mode (Serial Peripheral Interface (SPI) is not available) SSMD1 = “L”: RGB I/F mode (Serial Peripheral Interface (SPI) is available.)

PAD Coordinate

Input, Short side

No.	pad name	X	Y	No.	pad name	X	Y
1	DUMMY1	-7355.0	304.5	101	AGND	-31	-594.9
2	DUMMY2	-7355.0	217.5	102	AGND	54.6	-594.9
3	DUMMY3	-7355.0	130.5	103	DDVDH	202.7	-594.9
4	DUMMY4	-7355.0	43.5	104	DDVDH	287.8	-594.9
5	DUMMY5	-7355.0	-43.5	105	DDVDH	373.4	-594.9
6	DUMMY6	-7355.0	-130.5	106	DDVDH	459	-594.9
7	DUMMY7	-7355.0	-217.5	107	DDVDH	544.6	-594.9
8	SOUT1L	-7006.5	-594.9	108	DDVDH	630.2	-594.9
9	SOUT1L	-6920.0	-594.9	109	VGH	741.5	-594.9
10	SOUT2L	-6833.5	-594.9	110	VGH	828.3	-594.9
11	SOUT2L	-6747.0	-594.9	111	VGH	915.5	-594.9
12	SOUT3L	-6664.1	-594.9	112	VGH	1002.5	-594.9
13	SOUT3L	-6578.5	-594.9	113	VGH	1089.5	-594.9
14	SOUT4L	-6492.0	-594.9	114	VGH	1176.5	-594.9
15	SOUT4L	-6407.3	-594.9	115	VREF0P	1287.7	-594.9
16	VCCDUM1	-6278.3	-594.9	116	VREF1P	1373.3	-594.9
17	IE01	-6160.0	-594.9	117	VREF2P	1458.9	-594.9
18	LSOUT1L	-6101.8	-466.1	118	VREF3P	1544.5	-594.9
19	LSOUT1L	-6043	-594.9	119	VREF4P	1630.1	-594.9
20	LSOUT3L	-5984.2	-466.1	120	VREF0N	1715.7	-594.9
21	LSOUT4L	-5925.4	-594.9	121	VREF1N	1801.4	-594.9
22	ML	-5866.6	-466.1	122	VREF2N	1887	-594.9
23	TESTG1L	-5807.8	-594.9	123	VREF3N	1972.6	-594.9
24	TESTG2L	-5749	-466.1	124	VREF4N	2058.2	-594.9
25	TESTG3L	-5690.1	-594.9	125	VTEST	2143.8	-594.9
26	RESET	-5631.3	-466.1	126	TEST	2229.4	-594.9
27	IM1	-5572.5	-594.9	127	COMP	2315.2	-594.9
28	IM0	-5513.7	-466.1	128	ISO	2401	-594.9
29	BMODE1	-5454.0	-594.9	129	TS1	2527.4	-594.9
30	BMODE2	-5396.1	-466.1	130	COMM	2613	-594.9
31	BMODE3	-5337.3	-594.9	131	VCOMRC	2700.8	-594.9
32	SIL	-5278.5	-466.1	132	VCOMRC	2824.4	-594.9
33	DPL	-5219.7	-594.9	133	VCOMRC	2911	-594.9
34	EPL	-5160.8	-466.1	134	VCOMS	2996.6	-594.9
35	BPI	-5102	-594.9	135	VCOMS	3082.2	-594.9
36	TEST4	-5043.2	-466.1	136	VCOMS	3167.8	-594.9
37	TEST1	-4984.4	-594.9	137	VCOMR	3294.6	-594.9
38	LSENL	-4925.6	-466.1	138	VCOMMH	3380.2	-594.9
39	LSENR	-4866.8	-594.9	139	VCOMHC	3507	-594.9
40	CHREG	-4808	-466.1	140	VCOMHC	3592.6	-594.9
41	TEST5	-4749.2	-594.9	141	VCOMHC	3678.2	-594.9
42	SSMD1	-4690.3	-466.1	142	VEG	3763.8	-594.9
43	TESTSM2	-4631.5	-594.9	143	VEG	3849.4	-594.9
44	GNDUM1	-4513.0	-594.9	144	VCOMC	4037.2	-594.9
45	TESTM2	-4396.3	-594.9	145	VCOMC	4122.8	-594.9
46	TESTP8	-4337.5	-466.1	146	VCOMC	4208.4	-594.9
47	POC	-4278.7	-594.9	147	VCCDUM3	4348.8	-594.9
48	GAON	-4219.8	-466.1	148	CLW0	4466.5	-594.9
49	GNDUM2	-4102.2	-594.9	149	CLW1	4525.3	-466.1
50	VCCDUM2	-3984.6	-594.9	150	SD10	4584.1	-594.9
51	TEST8	-3867	-594.9	151	SD11	4642.9	-466.1
52	CS	-3808.2	-466.1	152	TEST6	4701.7	-594.9
53	SCL	-3749.4	-594.9	153	TEST7	4760.5	-466.1
54	SD1	-3690.5	-466.1	154	TEST8	4819.3	-594.9
55	GNDUM3	-3572.0	-594.9	155	TEST9	4878.1	-466.1
56	PD0	-3455.3	-594.9	156	TEST10	4937	-594.9
57	PD1	-3396.5	-466.1	157	TEST11	4995.8	-466.1
58	PD2	-3337.7	-594.9	158	TEST12	5054.6	-594.9
59	PD3	-3278.9	-466.1	159	TEST13	5113.4	-466.1
60	PD4	-3220	-594.9	160	TEST14	5172.2	-594.9
61	PD5	-3161.2	-466.1	161	TEST15	5231	-466.1
62	PD6	-3102.4	-594.9	162	VCOMG	5289.8	-594.9
63	PD7	-3043.6	-466.1	163	GIF0	5348.6	-466.1
64	PD8	-2984.8	-594.9	164	GIF1	5407.5	-594.9
65	PD9	-2926	-466.1	165	GNDUM5	5525.1	-594.9
66	PD10	-2867.2	-594.9	166	RESET	5642.7	-594.9
67	PD11	-2808.4	-466.1	167	TESTGR	5701.5	-466.1
68	PD12	-2749.5	-594.9	168	TESTGR	5760.3	-594.9
69	PD13	-2690.7	-466.1	169	TESTGR	5819.1	-466.1
70	PD14	-2631.9	-594.9	170	MR	5878	-594.9
71	PD15	-2573.1	-466.1	171	LSOUT4R	5936.8	-466.1
72	PD16	-2514.3	-594.9	172	SOUTR	5995.6	-594.9
73	PD17	-2455.5	-466.1	173	LSOUT2R	6054.4	-466.1
74	ENABLE	-2396.7	-594.9	174	LSOUT1R	6113.2	-594.9
75	B5V5NC	-2337.9	-466.1	175	ER2	6172	-466.1
76	B5V5NC	-2279.1	-594.9	176	VCCDUM4	6290.6	-594.9
77	DOTCLK	-2220.2	-466.1	177	SOUT4R	6407.3	-594.9
78	GNDUM4	-2102.6	-594.9	178	SOUT4R	6492.9	-594.9
79	VCC	-2001.2	-594.9	179	SOUT3R	6578.5	-594.9
80	VCC	-1914.2	-594.9	180	SOUT3R	6664.1	-594.9
81	VCC	-1827.2	-594.9	181	SOUT2R	6749.7	-594.9
82	VCC	-1740.2	-594.9	182	SOUT2R	6835.3	-594.9
83	VCC	-1653.2	-594.9	183	SOUT1R	6920.9	-594.9
84	VCC	-1566.2	-594.9	184	SOUT1R	7006.5	-594.9
85	GND	-1452	-594.9	185	DUMMY14	7355.9	-217.5
86	GND	-1366.8	-594.9	186	DUMMY13	7355.9	-130.5
87	GND	-1280.8	-594.9	187	DUMMY12	7355.9	-43.5
88	GND	-1195.2	-594.9	188	DUMMY11	7355.9	43.5
89	GND	-1109.6	-594.9	189	DUMMY10	7355.9	130.5
90	GND	-1024	-594.9	190	DUMMY9	7355.9	217.5
91	VGL	-912.7	-594.9	191	DUMMY8	7355.9	304.5
92	VGL	-827.1	-594.9				
93	VGL	-741.5	-594.9				
94	VGL	-655.9	-594.9				
95	VGL	-570.3	-594.9				
96	VGL	-484.7	-594.9				
97	AGND	-373.1	-594.9				
98	AGND	-287.5	-594.9				
99	AGND	-202	-594.9				
100	AGND	-116.6	-594.9				

Instruction

The HD66779 incorporates interface with microcomputer, which enables instruction setting to realize high-quality display and low power consumption. With regard to settings and timing of interface, see “Serial Peripheral Interface (SPI) Function”.

The instruction setting can not be made in DE transfer mode.

Index: IR

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	0	0	0	0	0	0	0	ID2	ID1	ID0
Initialized value	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

Specifies an index register to be accessed. Do not try to access to the register to which instruction is not assigned.

Power save, Color control: R01h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	POC	1	0	0	0	0	0	0	0	0
Initialized value	-	-	-	-	-	-	0	-	-	-	-	-	-	-	-	-

POC: Power control function.

POC = “1”: Normal operation mode. Both input/output interfaces are operable.

POC = “0”: Power control mode. White display is shown for the entire screen.

Note 1) When “CHREG” = “H”, “POC” of instruction register R01 become valid.

Note 2) See “Power Control Function” for details.

Note 3) The setting becomes effective in the next VSYNC assert timing.

Border color control (1): R02h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	0	0	0	0	BCO L17	BCO L16	BCO L15	BCO L14	BCO L13	BCO L12
Initialized value	-	-	-	-	-	-	-	-	-	-	1	1	1	1	1	1

Border color control (2): R03h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	BCO L11	BCO L10	BCO L9	BCO L8	BCO L7	BCO L6	0	0	BCO L5	BCO L4	BCO L3	BCO L2	BCO L1	BCO L0
Initialized value	-	-	1	1	1	1	1	1	-	-	1	1	1	1	1	1

BCOL17-0: Set value for the border color.

The assignment of the value to each register is as follows.

BCOL17-12: S (3n+1)

BCOL11-6: S (3n+2)

BCOL5-0: S (3n+3)

Note 1) The border pin assignment changes according to the setting for the border color control.

BMODE2 = "H": n = 0 to 1

BMODE2 = "L": n = 120 to 121

Note 2) Vertical border area is made by 2 raster-rows each at the top and bottom of the screen.

Note 3) Horizontal border area is made by 6 channels (two RGBs) each at the left and right sides of the screen.

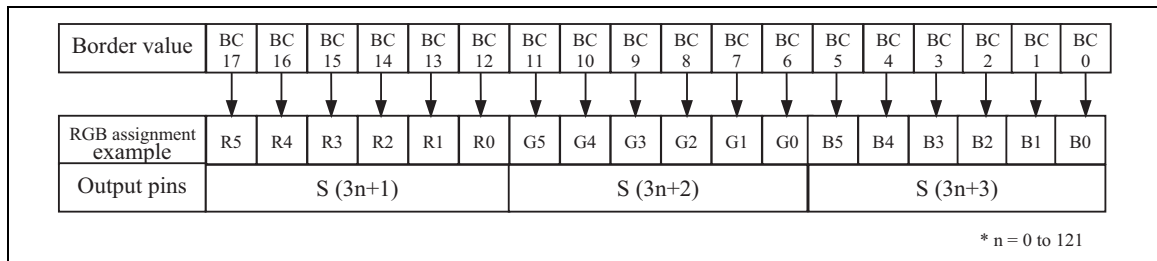
Note 4) The settings for the border control must be made during non-display period.

Note 5) The setting becomes effective from the next VSYNC assert timing.

Note 6) The setting is invalid while the border function is not used.

Note 7) The border color control function is valid only in RGBI/F mode.

The set values are assigned as follows.



LCD driving waveform control, Source output control: R04h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	0	0	0	NW1	NW0	0	0	0	0	RB3	RB2	RB1	RB0
Initialized value	-	-	-	-	-	-	0	1	-	-	-	-	1	0	0	0

NW2-0: Selects AC timing.

NW1	NW0	Alternating timing
0	0	Frame inversion
0	1	Inversion by line
1	0	Inversion by 2 lines
1	1	Setting disabled

Note 1) For details, see “LCD AC drive”.

Note 2) The setting becomes effective from the next VSYNC assert timing.

BP3-0: Set the blank period (back porch) in the following figure. BP3-0 set the number of raster-rows for the back porch. The number of raster-rows for the back porch should be:

$$14 \text{ raster-rows} \geq \text{the number of raster-rows for the back porch} - \text{the number of raster-rows for the border} \geq 2 \text{ raster-rows}$$

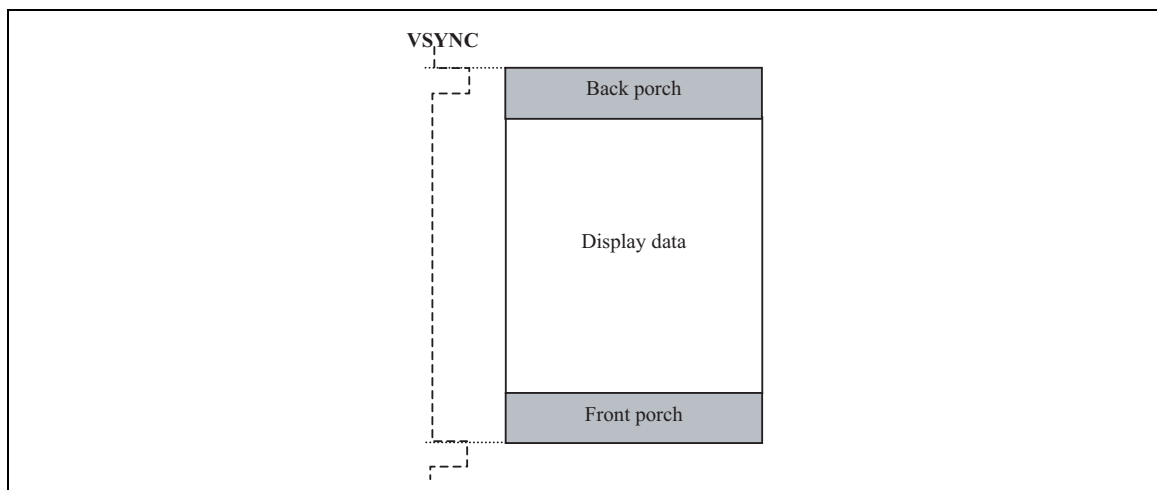
Note 1) When “CHREG” = “H”, instruction registers “BP3”, “BP2”, “BP1”, “BP0” become valid.

When “CHREG” = “L”, “BP” pin function becomes valid.

(“BP”= 0: back porch 4 lines, “BP”=1: back porch 8 lines)

Note 2) A front porch lasts from the end of the display pixel transfer to the next VSYNC assert.

Note 3) The setting becomes effective from the next assert timing.



HD66779

BP3	BP2	BP1	BP0	Back porch line
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	Two lines
0	0	1	1	Three lines
0	1	0	0	Four lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled

Gate Non Overlap Control, Border Color Control: R05h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	0	DTE	0	0	NO1	NO0	0	0	0	0	0	0	0	GAO N
Initialized value	-	-	-	1	-	-	0	0	-	-	-	-	-	-	-	0

DTE : Output gate off signal.

“DTE” = “0”: Fix to GND.

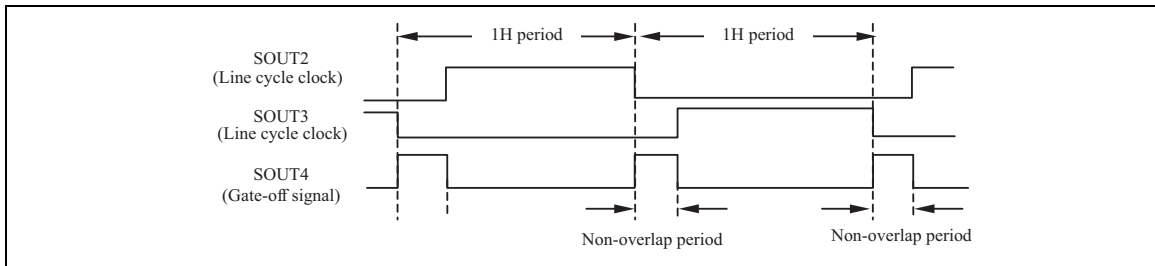
“DTE” = “1”: Output gate off signal.

The setting becomes effective from the next VSYNC assert timing.

NO1-0: Set the non-overlap period of gate off signal.

NO1	NO0	Amount of non-overlap	
		Delay time	5MHz (e.g.)
0	0	0 μ s	0 clock
0	1	4.0 μ s	20 clocks
1	0	6.0 μ s	30 clocks
1	1	8.0 μ s	40 clocks

Note) The delay time changes according to the DOTCLK frequency.



Note) When the setting is made with pins, the non-overlap amount of gate off signal equals to that set with CLW1-0.

GAON: Output gate-all-on signal.

GAON = "0": Gate output signal L/SOUT4 = "0"

GAON = "1": Gate output signal L/SOUT4 = "1"

Note 1) When "CHREG" = "H", "GAON" of instruction register R05 becomes valid.

Note 2) With regard to the selection of output pin, see "LCD display signal control".

Note 3) The setting becomes effective from the next VSYNC assert timing.

Display Signal Select Control, Flame Control 1: R06h

	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
Instruction	0	0	DSC 1	DSC 0	0	0	GIF1	GIF0	FHN	0	FTH 1	FTH 0	0	0	FWH 1	FWH 0
Initialized value	-	-	0	1	-	-	0	0	1	-	1	0	-	-	1	1

DSC1-0: Controls start/halt of LCD signals.

DSC1	DSC0	Selective signal for LCD display
0	0	Halt LCD display signal
0	1	SOUT1/2/3/4
1	0	LSOUT 1/2/3/4
1	1	L/SOUT1/2/3/4

Note 1) SOUT1/2/3/4 is a level shifter output (voltage between VGH and VGL), and LSOUT1/2/3/4 is a logic output (voltage between Vcc and GND).

Note 2) The setting becomes effective from the next VSYNC assert timing.

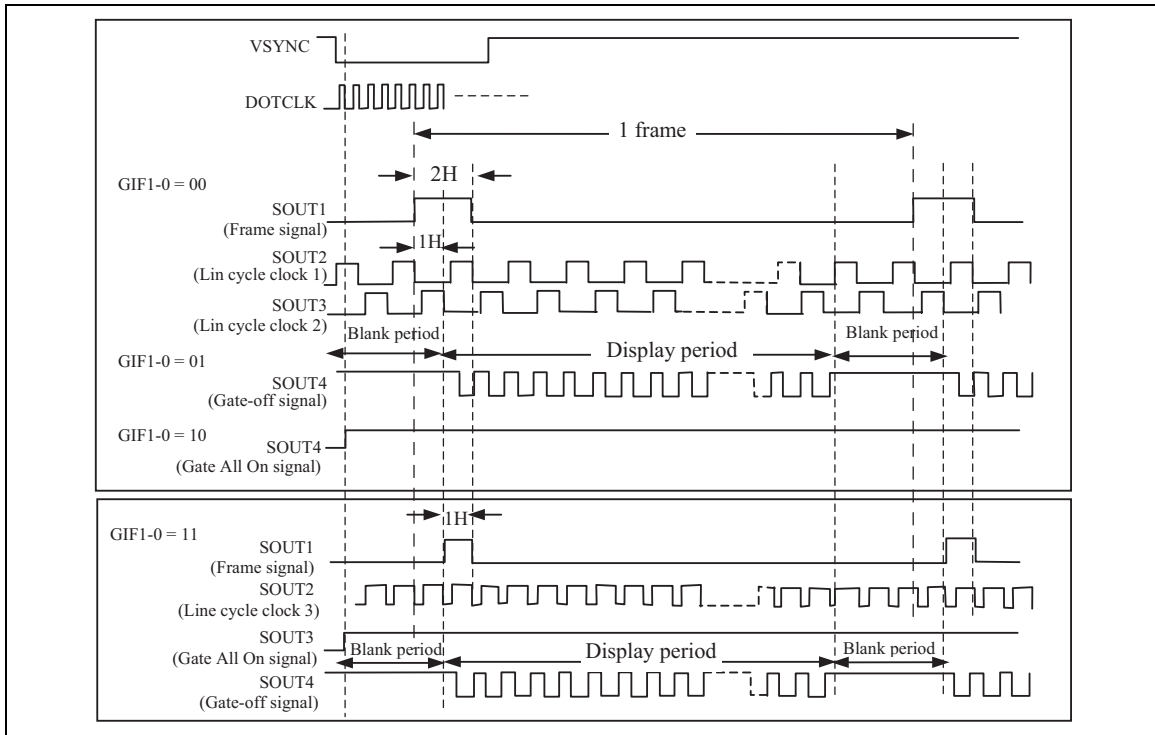
GIF1-0: Select the function of LCD display signal.

GIF1	GIF0	L/SOUT2	L/SOUT3	L/SOUT4
0	0	Line frequency clock 1	Line frequency clock 2	Disconnect pins
0	1	Line frequency clock 1	Line frequency clock 2	Gete off signal
1	0	Line frequency clock 1	Line frequency clock 2	Gate All On
1	1	Line frequency clock 3	Gate All On	Gate off signal

Note 1) When "CHREG" = "H", "GIF1" and "GIF0" of instruction registers R06 become effective.

Note 2) The setting becomes effective from the next VSYNC assert timing.

Note 3) When "GIF1-0" = 11, "FHN" = "0"(1H assert).



GIF1-0: timing chart

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FHN: Set the assert period of SOUT1 signal (frame timing signal) during horizontal period.

FHN = "0": the assert available for 1H period.

FHN = "1": the assert available for 2H period.

The setting becomes effective from the next VSYNC assert timing. The assert period is 2H in DE transfer mode (1H, when GIF1-0 = "11").

FTI1-0: Set the assert timing of SOUT1 signal (frame timing signal) during horizontal period.

FTI1	FTI0	Assert timing	
		Delay time	5MHz (e.g.)
0	0	0 μ s	0 clock
0	1	1.5 μ s	7.5 clocks
1	0	3.5 μ s	17.5 clocks
1	1	7.5 μ s	37.5 clocks

Note) The delay time cahges according to the DOTCLK frequency.

The setting becomes effective from the next VSYNC assert timing.

FWI1-0: Set the pulse width of SOUT1 signal (frame timing signal) during "High".

FWI1	FWI0	"High" period	
		Delay time	5MHz (Ex.)
0	0	2 μ s	10 clocks
0	1	8 μ s	40 clocks
1	0	16 μ s	80 clocks
1	1	Until the end of 1H period	—

The setting becomes effective from the next VSYNC assert timing.

Instruction List

		bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
	index	0	0	0	0	0	0	0	0	0	0	0	0	0	ID2	ID1	ID0
R01h	Power control Color control	0	0	0	0	0	0	*POC 0	1	0	0	0	0	0	0	0	0
R02h	Border color control (1)	0	0	0	0	0	0	0	0	0	0	BCOL17 1	BCOL16 1	BCOL15 1	BCOL14 1	BCOL13 1	BCOL12 1
R03h	Border color control (2)	0	0	BCOL11 1	BCOL10 1	BCOL9 1	BCOL8 1	BCOL7 1	BCOL6 1	0	0	BCOL5 1	BCOL4 1	BCOL3 1	BCOL2 1	BCOL1 1	BCOL0 1
R04h	LCD drive AC control, Display control	0	0	0	0	0	0	NW1 0	NW0 1	0	0	0	0	*BP3 1	*BP2 0	*BP1 0	*BP0 0
R05h	Gate output non-overlap control, All gate ON control	0	0	0	DTE 1	0	0	NO1 0	NO0 1	0	0	0	0	0	0	0	*GAON 0
R06h	Signal select control for LCD display, FLM control	0	0	DSC1 0	DSC0 1	0	0	*GIF1 0	*GIF0 0	FHN 1	0	FTI1 1	FTI0 0	0	0	FWI1 1	FWI0 1

Note 1) The initialized value is shown at the bottom of each instruction bit cell.

Note 2) Do not try to access to the register where instruction setting is disabled.

Note 3) The setting in the instruction bit with "*" conflicts with the pin setting. When the pin "CHREG" is set to "H", the setting of the instruction bit takes precedence over the pin setting.

Note 4) In the DE transfer mode, the setting of the bit without "*" is not changeable and initialized value is retained.

Reset Function

The HD66779 is internally initialized with the input of RESET. During reset period, the internal state of the HD66779 is busy and no external access is accepted. With the reset input to the HD66779, the settings for the gate-driver/power supply IC are not automatically initialized and separate resetting is required for the gate-driver/power supply IC. The reset input period must be held for 1 ms at least. Do not transfer initialized instruction sets or data during the power-on reset when power is turned on.

1. Initial state of instruction set : See description for each instruction

2. Initial level of output pin :

LCD display output:	SOUT1-4R/L	Output "VGL" level.
	LSOUT1-4R/L	Output "GND" level.
AC drive amplitude signal	VCOMS	Output "GND" level.

LCD Signal Output Timing Control Function

Adjust output timing of LCD display signal with external pins.

CLW0/1: Set output position of line cycle clock for display.

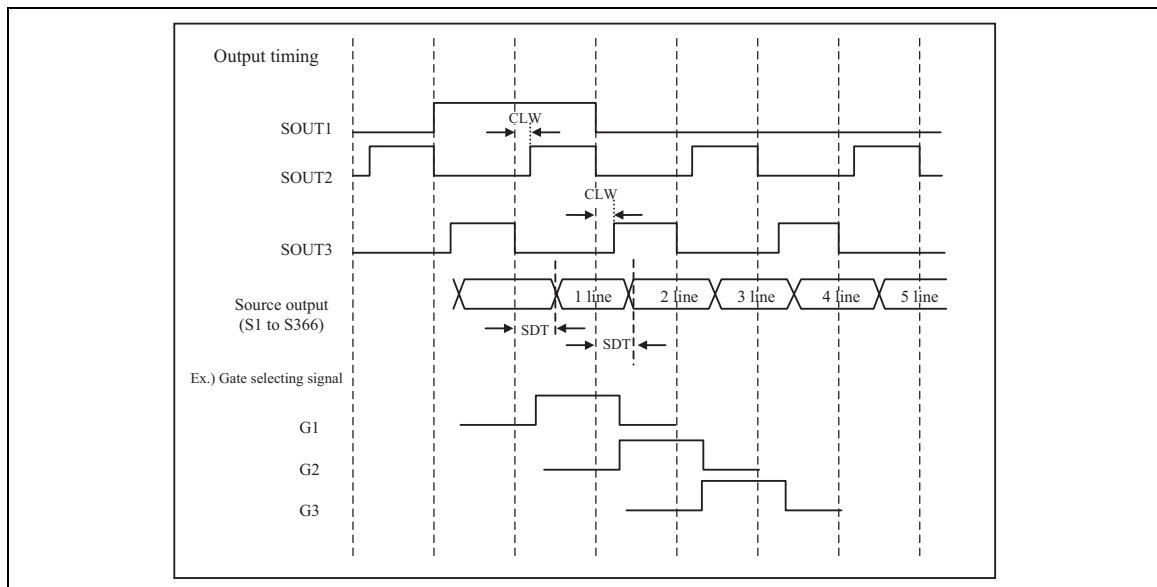
CLW1	CLW0	Delay amount	
		Delay time	5MHz (e.g.)
L	L	0 μ S	0 clock
L	H	2.0 μ S	10 clocks
H	L	4.0 μ S	20 clocks
H	H	6.0 μ S	30 clocks

Note) The delay time changes according to the DOTCLK frequency.

SDT0/1: Set output position of source output.

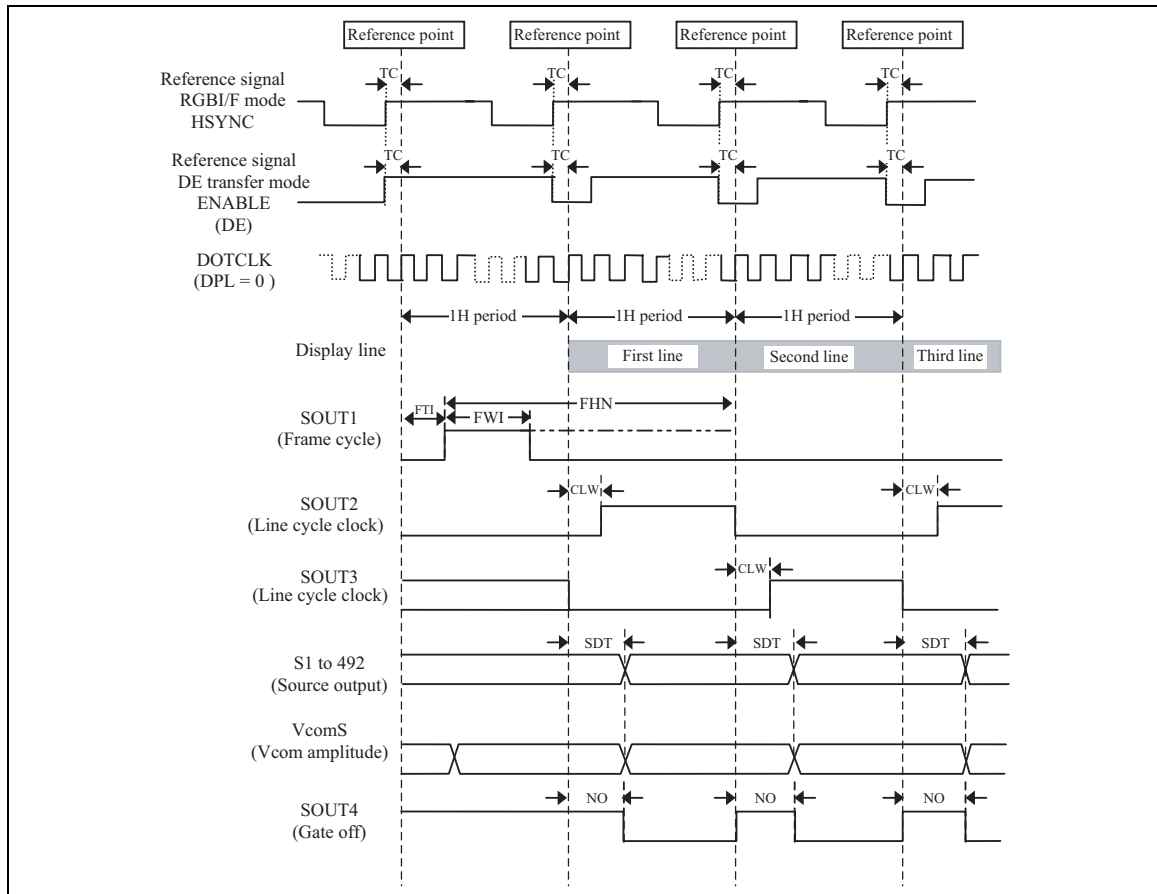
SDT1	SDT0	Delay amount	
		Delay time	5MHz (e.g.)
L	L	2 μ S	10 clocks
L	H	3.0 μ S	15 clocks
H	L	4.0 μ S	20 clocks
H	H	5.0 μ S	25 clocks

Note) The delay time changes according to the DOTCLK frequency.



LCD Signal Timing Control Function

The timing chart of control signals is illustrated as follows.



Note 1) There are some constraints when the pin setting is effective.

- L/SOUT1 (Frame) signal is $FHN = "1"$ (2H assert)
- When $FT11-0 = "10"$ (DE transfer mode: $FT11-0 = "00"$), $FW11-0 = "11"$.
- The non-overlap amount of L/SOUT4 (gate-off signal) equals to that set by $CLW1-0$.

Note 2) There are some constraints when $GIF1-0 = "11"$.

- $FHN = "0"$ (1H assert) irrespective of the pin setting and SPI setting ($FHN = "1"$).
- When the pin setting is effective, $FT11-0 = "00"$, $FW11-0 = "11"$.

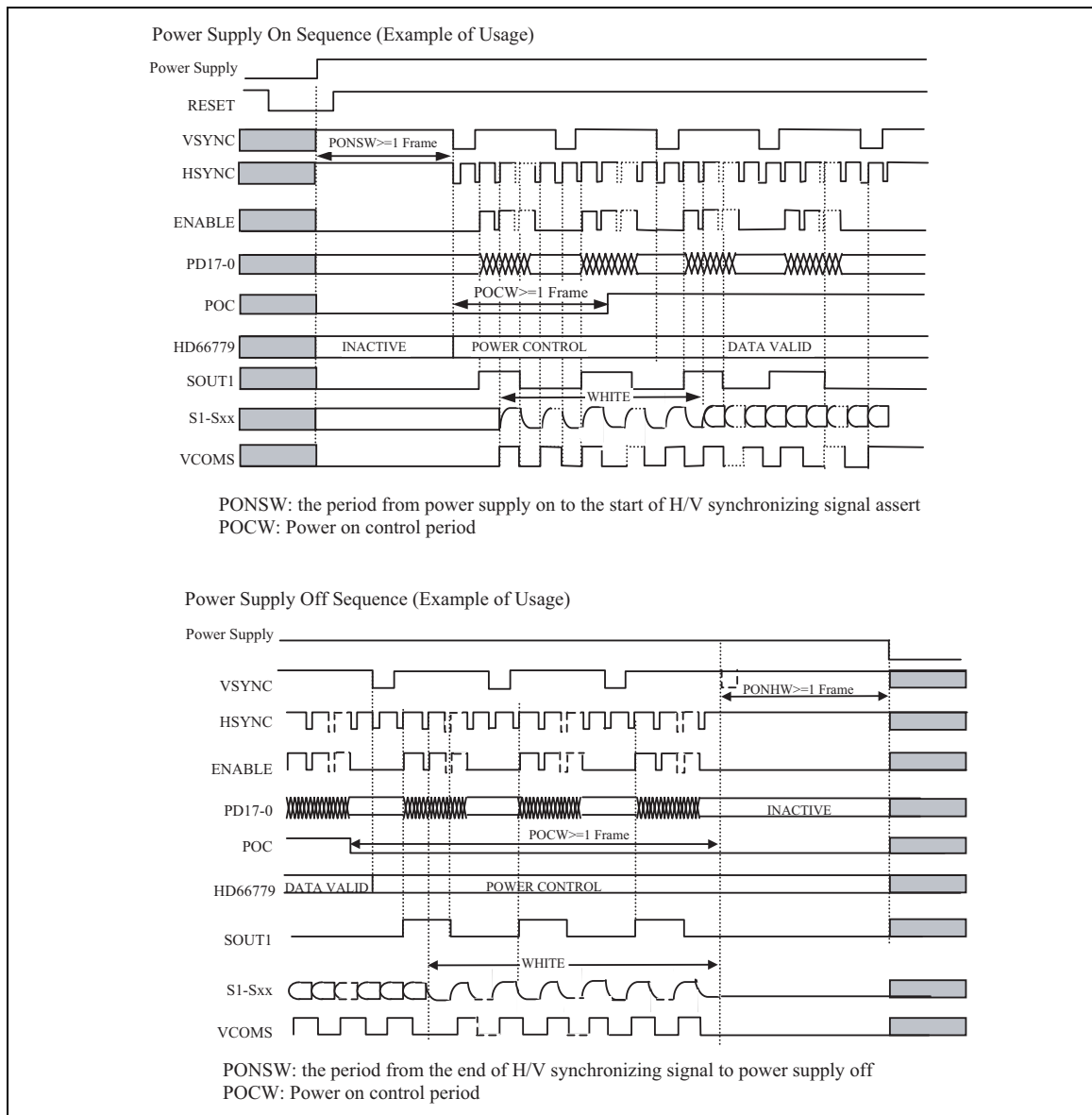
Power Control Function

Power control function (POC)

When POC = "L", a white display is shown.

Note 1) The panel display signal (SOUT*) is output normally.

Note 2) The set value of POC changes with VSYNC and the source output becomes effective from the next timing.



POC / VCOMG / LSENRL output control

The relationship among these signals is as follows.

Source output (Sn) and Vcom output (VCOMS) control by POC

Input	Output		
POC	Operation mode	Source output (Sn)	Vcom output
0	Power control mode	WHITE	VCOMS
1	Normal operation mode	Input data or Border data	VCOMS

Panel display signal (SOUT*/LSOUT*) control by LSEN/LSENRL

Input		Output			
		VGH-VGL		Vcc-GND	
LSEN	LSENRL	SOUT1/2/3/4L	SOUT1/2/3/4R	LSOUT1/2/3/4L	LSOUT1/2/3/4R
0	0	VGL	VGL	Vcc - GND	Vcc - GND
0	1	VGL	VGH - VGL		
1	0	VGH - VGL	VGL		
1	1	VGH - VGL	VGH - VGL		

VCOM (VCOMS) control by VCOMG

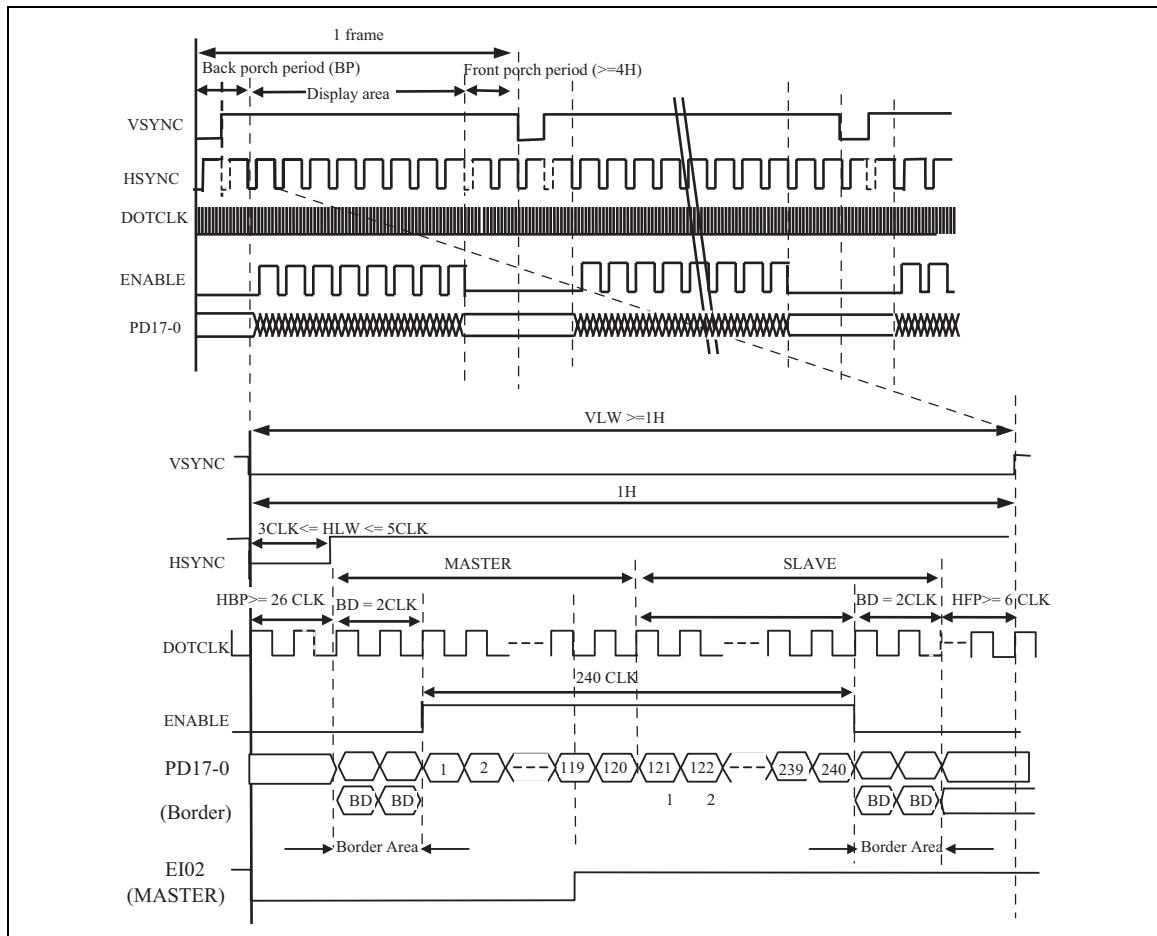
Input	Output
VCOMG	VCOMS
0	GND
1	VCOMS

Interface

RGB interface timing 1 (366ch x 2 / With Border)

The timing chart of RGB interface signal is as follows.

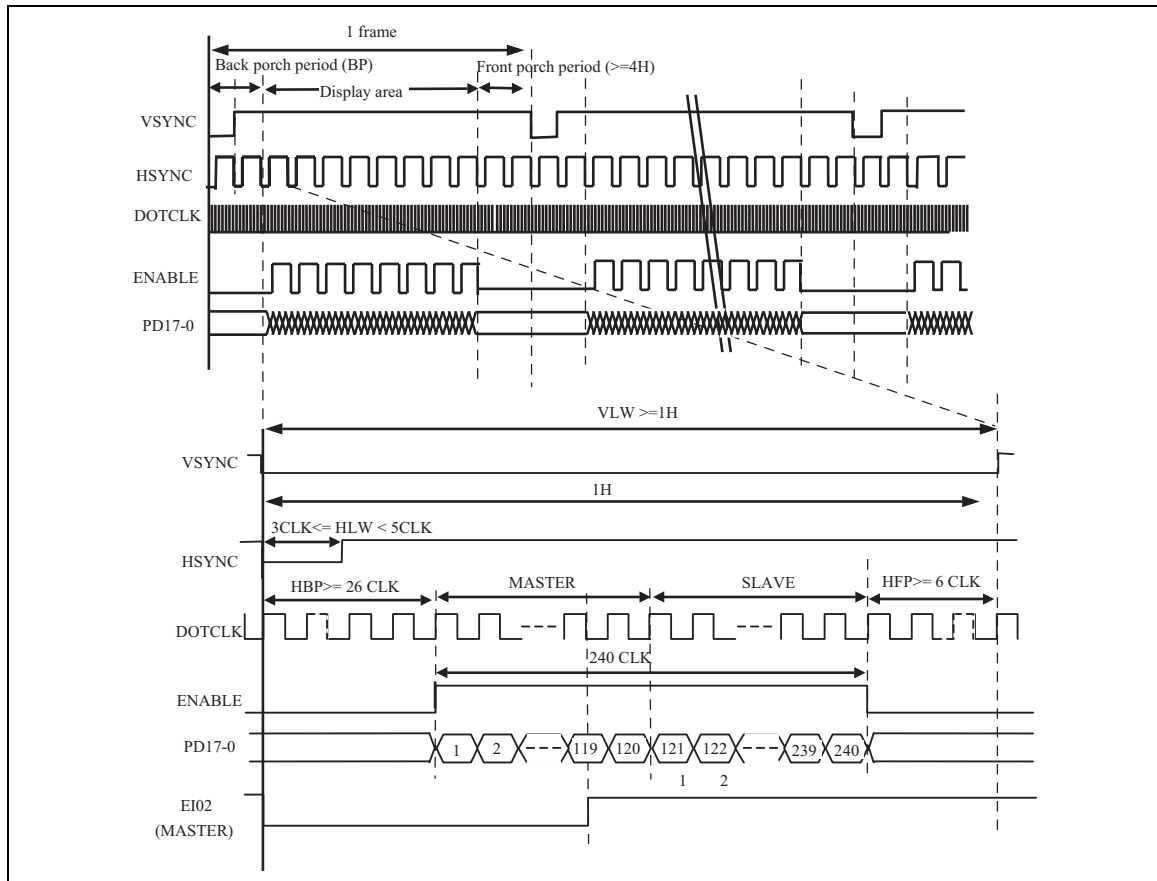
The value for the border is the one received through SPI.



VLW: VSYNC "Low" period
 HLW: HSYNC "Low" period
 HBP: Horizontal period back porch
 HFP: Horizontal period front porch
 BD: Border Area

RGB interface timing 2 (360ch x 2 / Without Border)

The timing chart of signals in RGB interface is as follows.

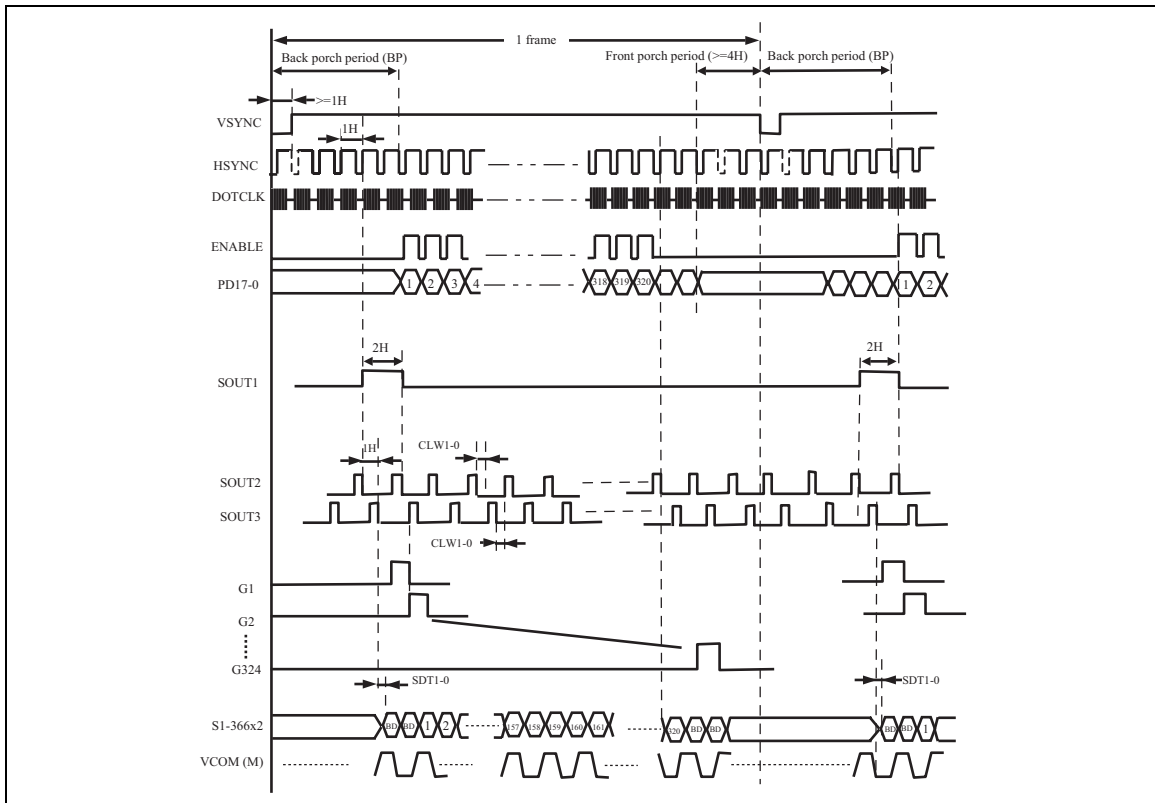


VLW: VSYNC "Low" period
 HLW: HSYNC "Low" period
 HBP: Horizontal period back porch
 HFP: Horizontal period front porch

LCD panel interface timing 1 (366ch x 2 / With Border)

The timing chart of RGB interface signal is as follows.

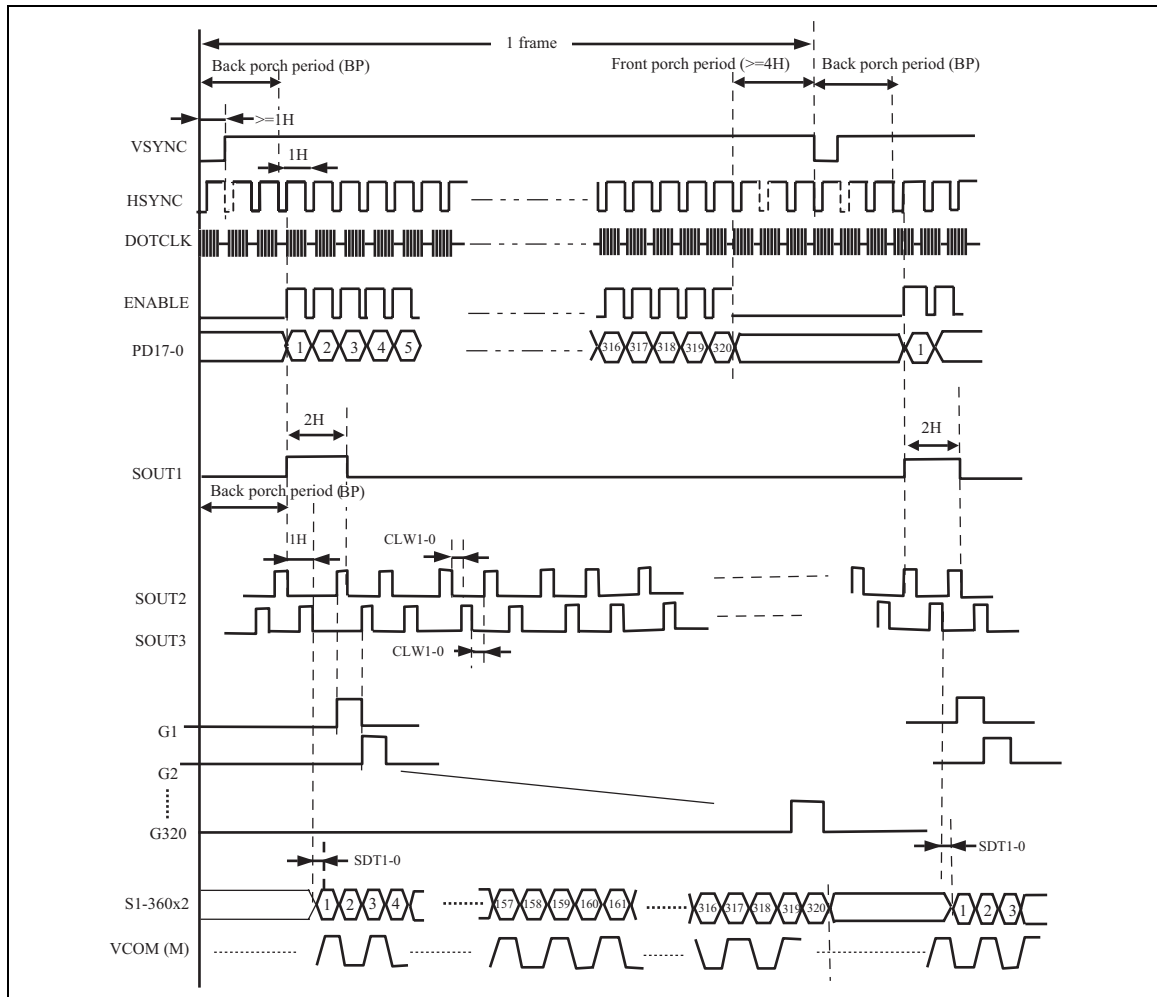
The value for the border is the one received through SPI.



Note) See "LCD Signal Timing Control Function" for details of setting the timing.

LCD panel interface timing 2 (366ch x 2 / Without Border)

The timing chart of RGB interface signal and LCD panel signal is as follows.

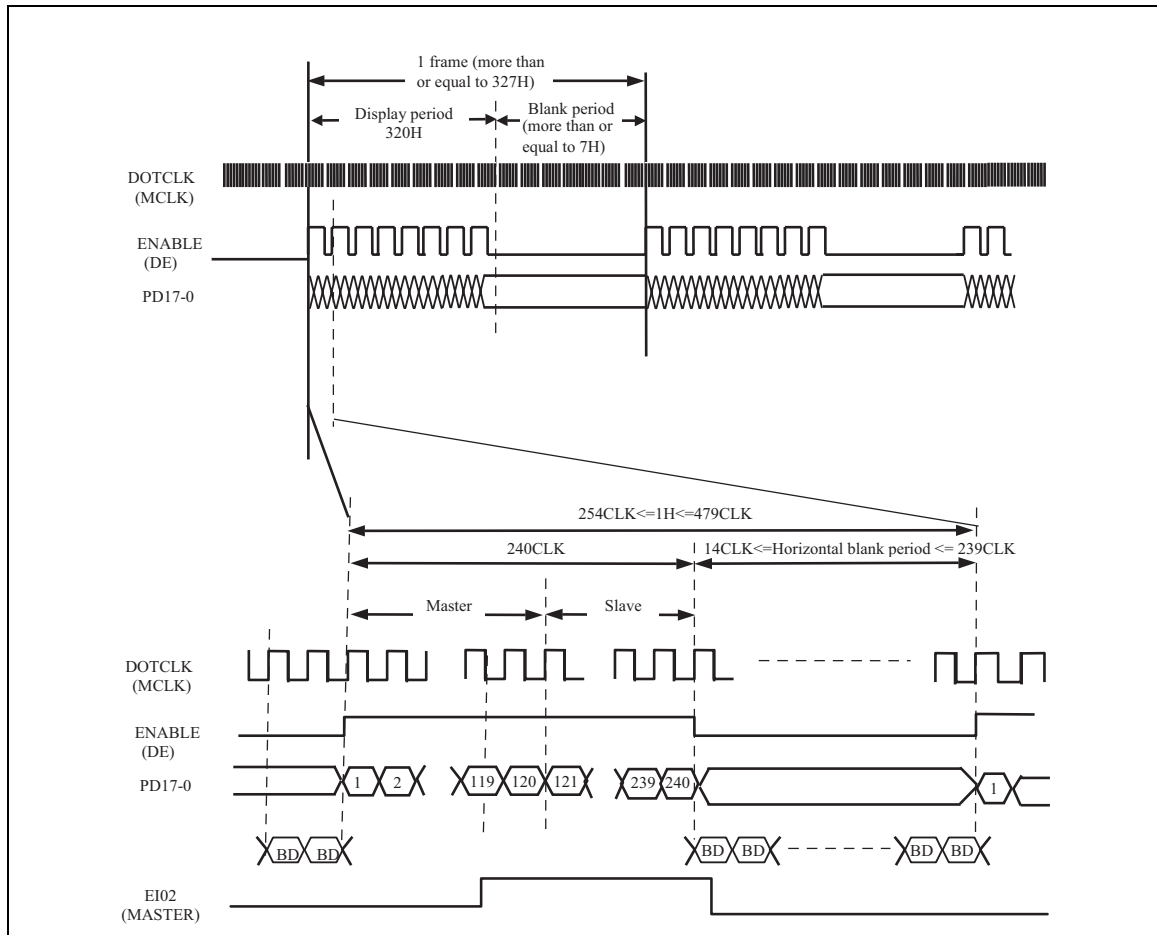


Note) See "LCD Signal Timing Control Function" for details of setting the timing.

DE transfer mode 1 (366ch x 2 / With Border)

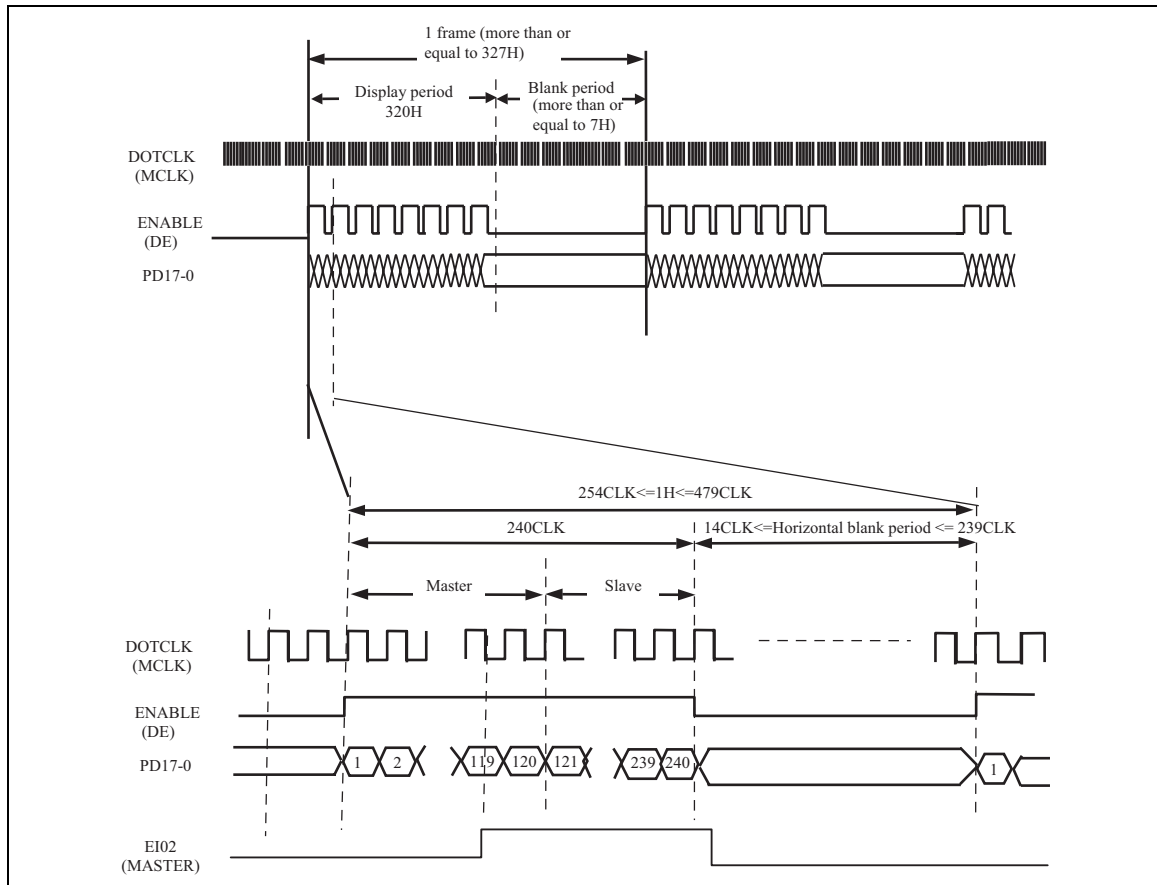
The timing chart of DE transfer mode signal is as follows.

The border color in DE transfer mode is either black or white to be switched with BMODE3 pin.



DE transfer mode 2 (366ch x 2 / Without Border)

The timing chart of DE transfer mode signal is as follows.

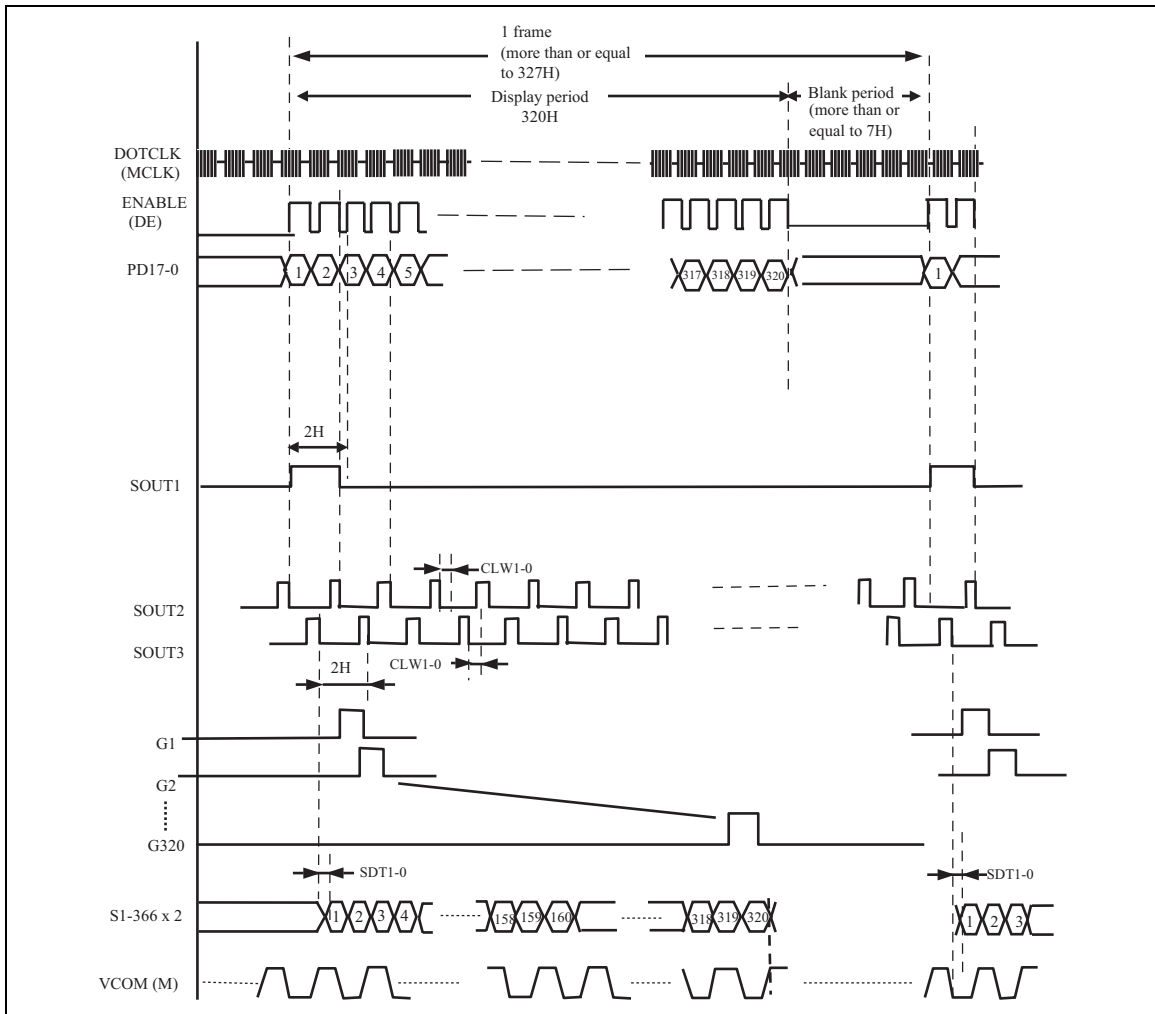


LCD panel interface timing while DE transfer mode 1 (With Border)

The relationship between the DE transfer mode signal and the LCD panel signal is as follows.

Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.

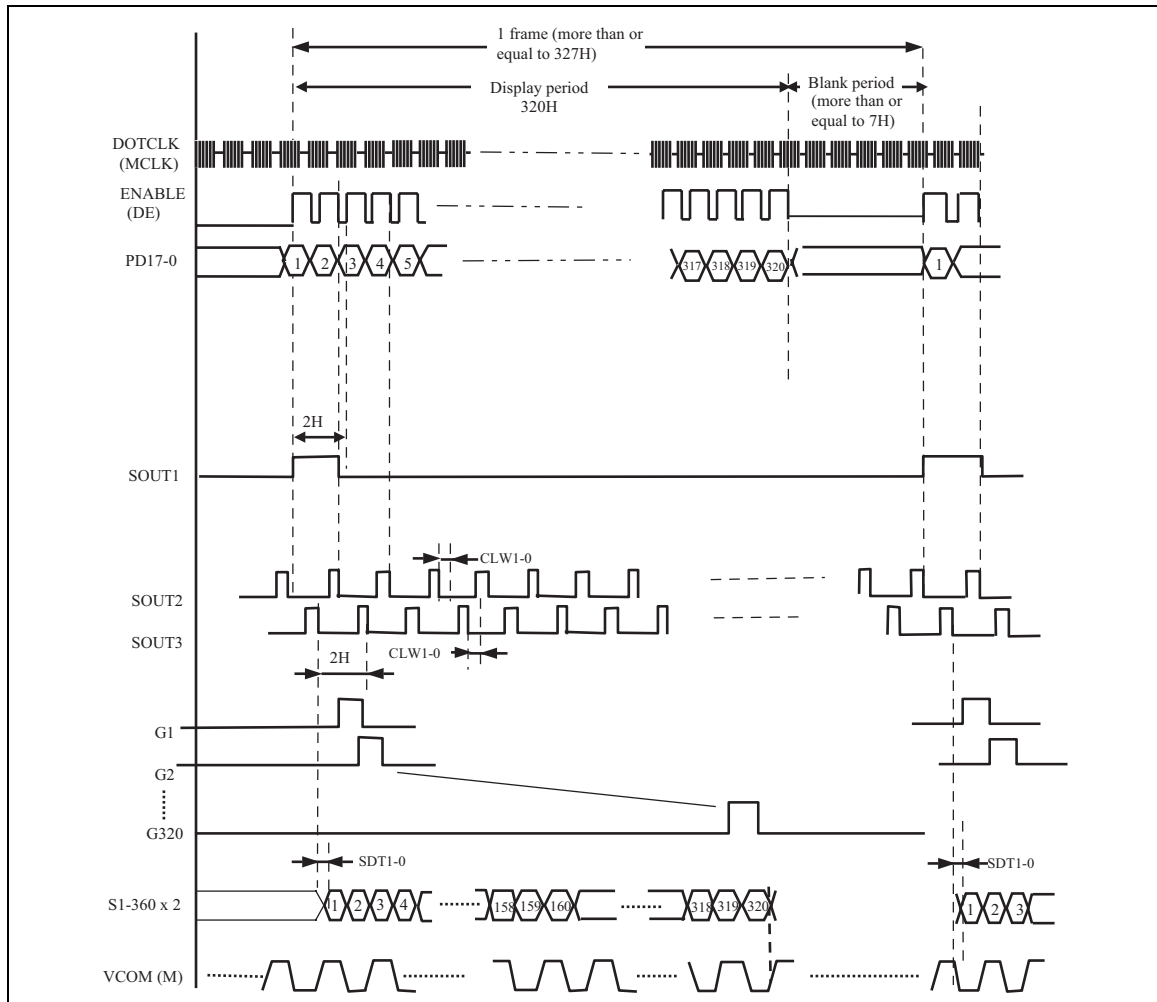
Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.



Note) See "LCD Signal Timing Control Function" for details of setting the timing.

LCD panel interface timing while DE transfer mode 2 (Without Border)

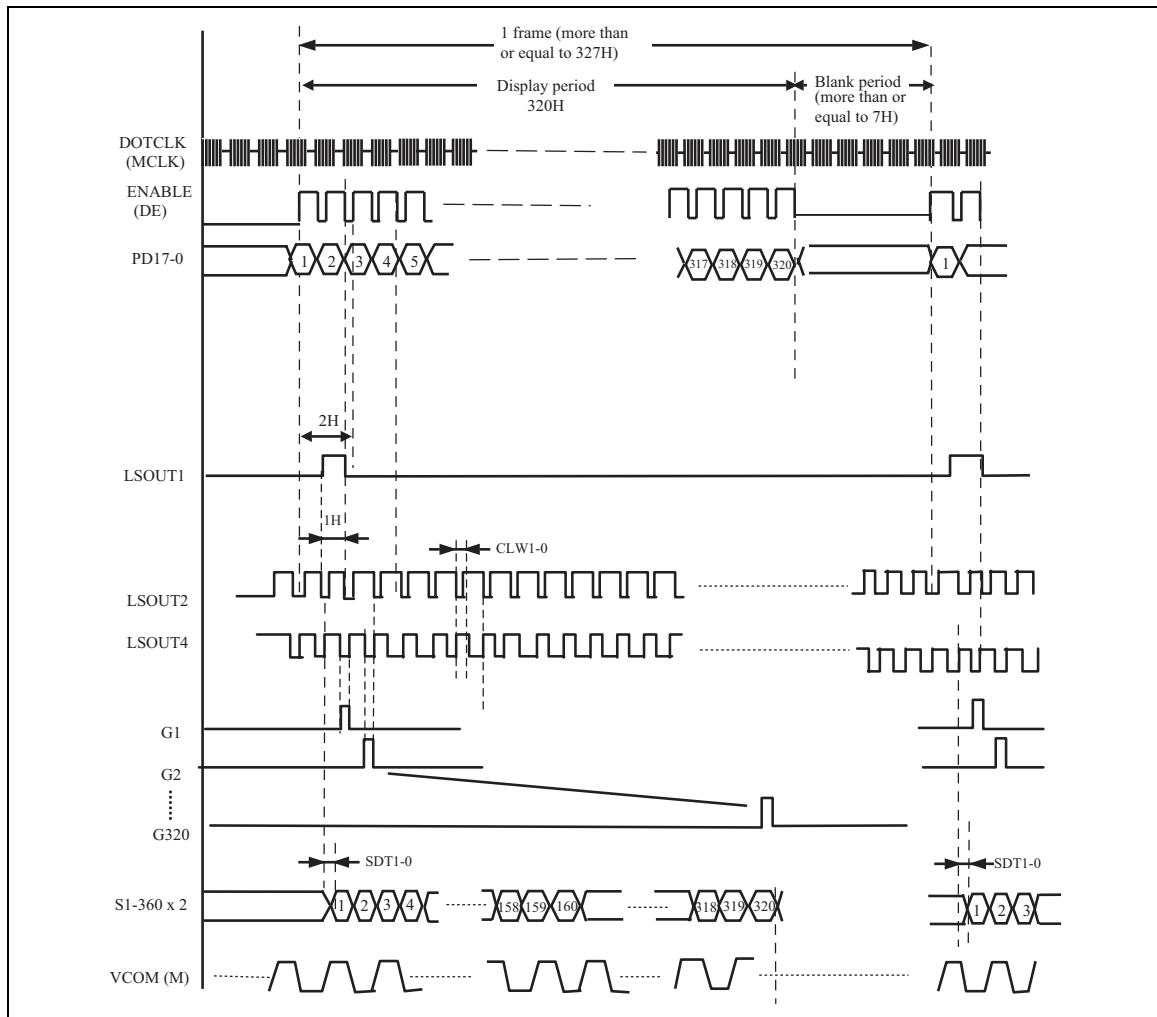
The relationship between the DE transfer mode signal and the LCD panel signal is as follows.



Note) See "LCD Signal Timing Control Function" for details of setting the timing.

LCD panel interface timing while DE transfer mode 3

The relationship between the DE transfer mode signal, gate driver outputs and the LCD panel signal is as follows.



Note) See "LCD Signal Timing Control Function" for details of setting the timing.

Serial Peripheral Interface (SPI) Function

(Only available with RGB I/F)

Serial Peripheral Interface (SPI) transfer is made by setting IM1/ pin to the GND level. The interfacing is executed through chip select line (CS*), serial transfer clock line (SCL), and serial input data (SDI). The HD66779 initiates serial data transfer by recognizing the falling edge of CS* input as a start and then start the transfer of the start byte. The condition for the end of data transfer is that the HD66779 recognizes the rising edge of CS* input as an end of transfer.

The HD66779 is selected when the 6-bit chip address in the start byte from the transmission side and the 6-bit device identification code assigned to the HD66779 are compared and matches with each other. The HD66779, when selected, receives data from the subsequent data string. The least significant bit of the identification code can be specified with ID pin. The upper five bits of the device ID code must be 01110. The 7th bit of the start byte is assigned to the selection of HD66779's register (RS) and when this bit is set to 0, index register write is executed and when this bit is set to 1, instruction write is executed. Accordingly, two chip addresses must be assigned to one HD66779.

After receiving the start byte, the HD66779 receives and transfers data by byte. The transfer data format is MSB first. The instruction of the HD66779 comprise 16 bits. The instruction is executed internally after 2-byte (D15-0) transfer with MSB first.

Start byte format

Example of transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Start	Device ID code						RS	0
		0	1	1	1	0	ID		

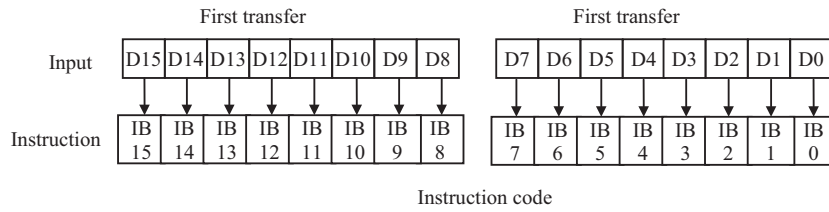
Note) ID bit is selected with IM0/ID pins.

RS bit function

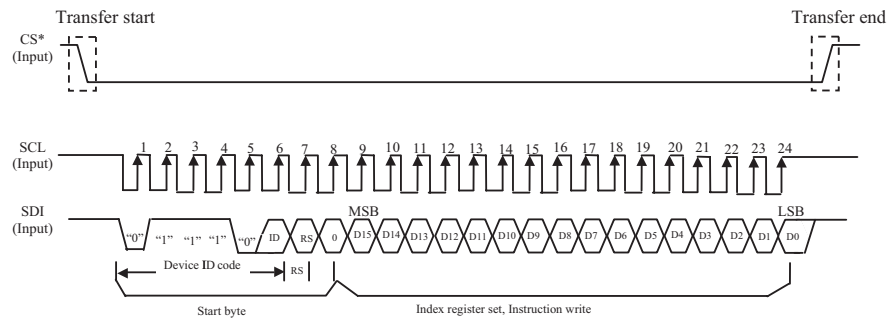
RS	Function
0	Set Index register
1	Instruction write

Data format for Serial Peripheral Interface (SPI)

Instruction



Clock synchronized serial transfer (Basic Transfer)



Settings for Data Shift Direction/Boder mode

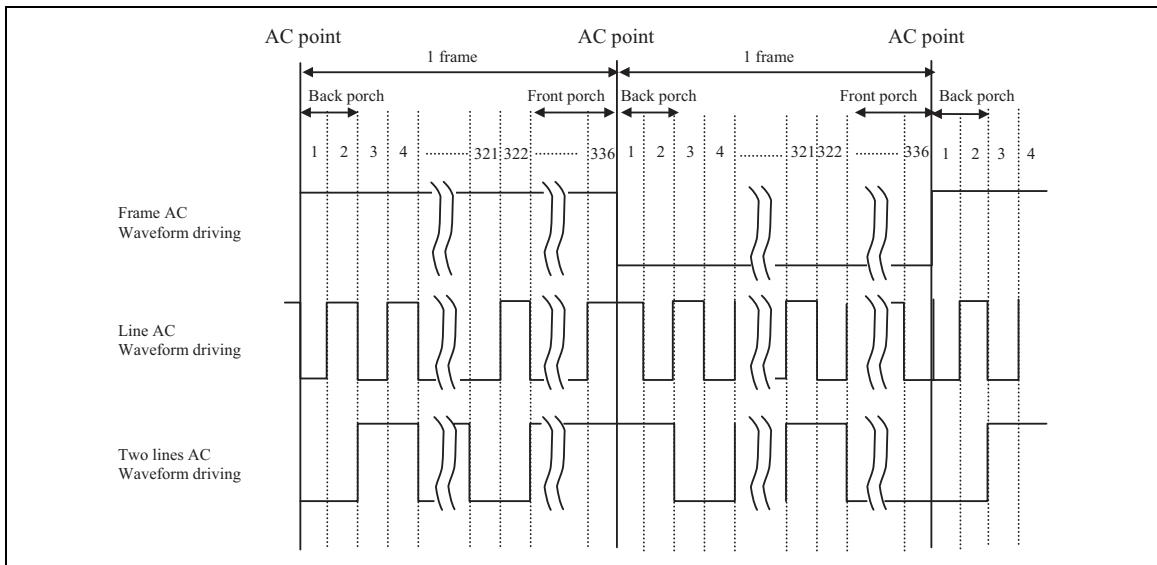
The data shift direction is changeable by setting according to the panel size and the assembly.

The border color control is only on the 6 channels (2RGBs) each at the left and right sides in DE transfer mode. See page 53, "System Configuration Example 4".

BMODE I	SHL	Panel Configuration Example (without border)	Make settings for Data shift direction & Border mode only with pin settings
L	L	<p>TFT Panel 720ch (240RGB)</p> <p>S1 → S360 Chip Top</p>	Possible
L	H	<p>TFT Panel 720ch (240RGB)</p> <p>S7 ← S366 Chip Top</p>	Possible
BMODE I	SHL	Panel Configuration Example (with border)	Make settings for Data shift direction & Border mode only with pin settings
H	L	<p>6ch (2RGB)</p> <p>2line</p> <p>TFT Panel 720ch (240RGB)</p> <p>2line</p> <p>S1 → S7 → S366 Chip Top</p> <p>S1 → S360 → S366 Chip Top</p> <p>BMODE2="L" BMODE2="H"</p>	Impossible
H	H	<p>6ch (2RGB)</p> <p>2line</p> <p>TFT Panel 720ch (240RGB)</p> <p>2line</p> <p>S1 ← S7 ← S366 Chip Top</p> <p>S1 ← S360 ← S366 Chip Top</p> <p>BMODE2="L" BMODE2="H"</p>	Impossible

LCD AC Drive

The HD66779 supports n-raster-row inversion AC drive to alternate signals by arbitrary n raster-rows, where “n” is from 1 to 2, in addition to LCD inversion drive by frame. When deciding the number of “n”, by which alternation occurs, with NW bit, check the quality of display on the actual LCD panel. If the number of raster rows for alternation is set small, the LCD alternation frequency becomes high and the charged/discharged current will increase on the LCD cell.



LCD Display Signal Control

The HD66779 allows selection of an optimum LCD display signal for the configuration of a system. See “Display Signal Select Control” in the “Instruction” section, with regard to the timing of signal.

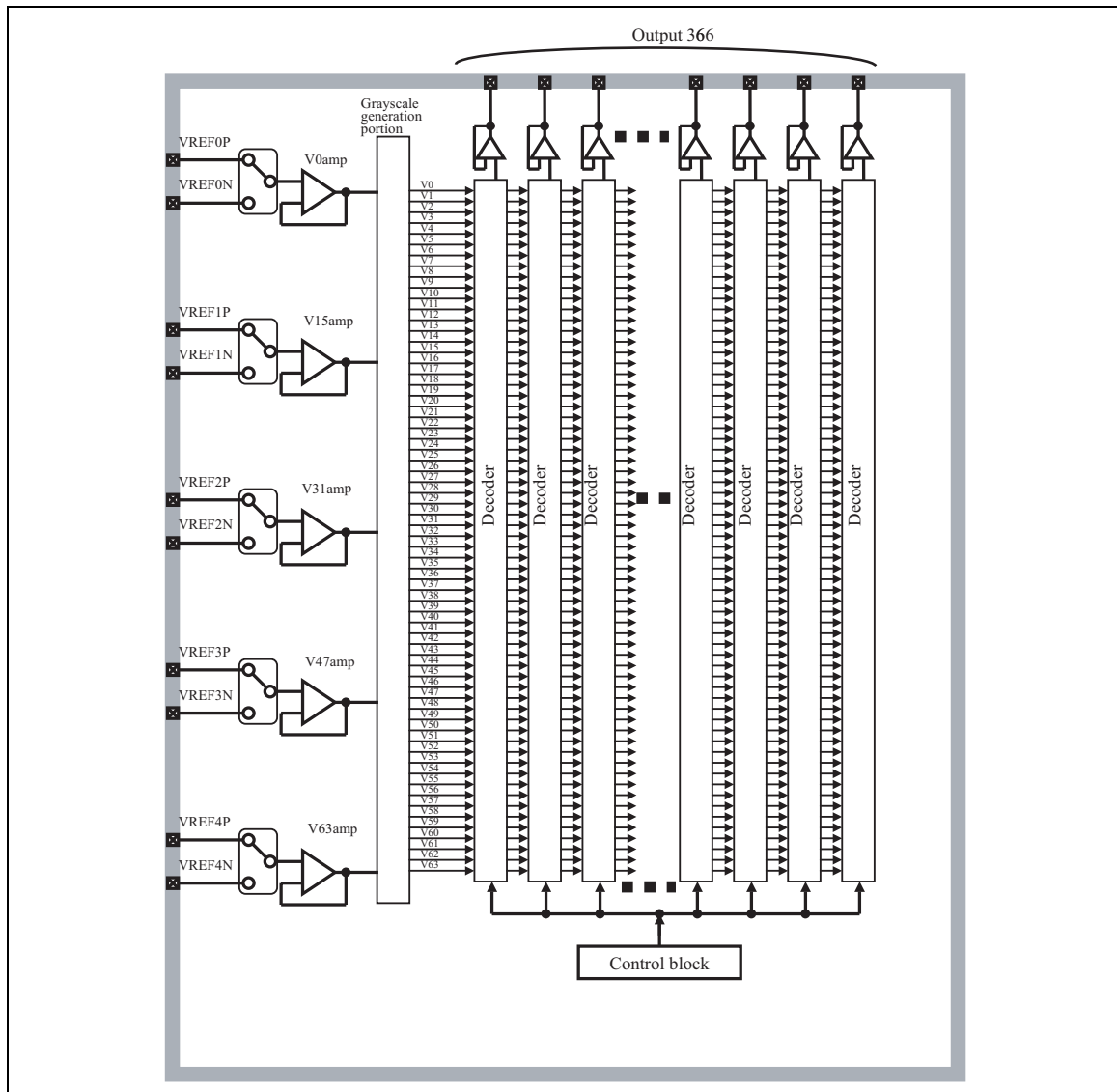
Register setting

DSC1	DSC0	GIF1	GIF0	Level shifter voltage output (VGH-VGL)			Logic voltage output (Vcc-GND)		
				SOUT2	SOUT3	SOUT4	LSOUT2	LSOUT3	LSOUT4
0	0	0	0	—	—	—	—	—	—
		0	1	—	—	—	—	—	—
		1	0	—	—	—	—	—	—
		1	1	—	—	—	—	—	—
0	1	0	0	Line cycle clock 1	Line cycle clock 2	—	—	—	—
		0	1	Line cycle clock 1	Line cycle clock 2	Gate off signal	—	—	—
		1	0	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal	—	—	—
		1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal	—	—	—
1	0	0	0	—	—	—	Line cycle clock 1	Line cycle clock 2	—
		0	1	—	—	—	Line cycle clock 1	Line cycle clock 2	Gate off signal
		1	0	—	—	—	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal
		1	1	—	—	—	Line cycle clock 3	Gate all ON signal	Gate off signal
1	1	0	0	Line cycle clock 1	Line cycle clock 2	—	Line cycle clock 1	Line cycle clock 2	—
		0	1	Line cycle clock 1	Line cycle clock 2	Gate off signal	Line cycle clock 1	Line cycle clock 2	Gate off signal
		1	0	Line cycle clock 1	Line cycle clock 2	Gate all ON signal	Line cycle clock 1	Line cycle clock 2	Gate-all-on signal
		1	1	Line cycle clock 3	Gate-all-on signal	Gate off signal	Line cycle clock 3	Gate-all-on signal	Gate off signal

Note) Leave open for “—”.

Grayscale Amplifier Configuration

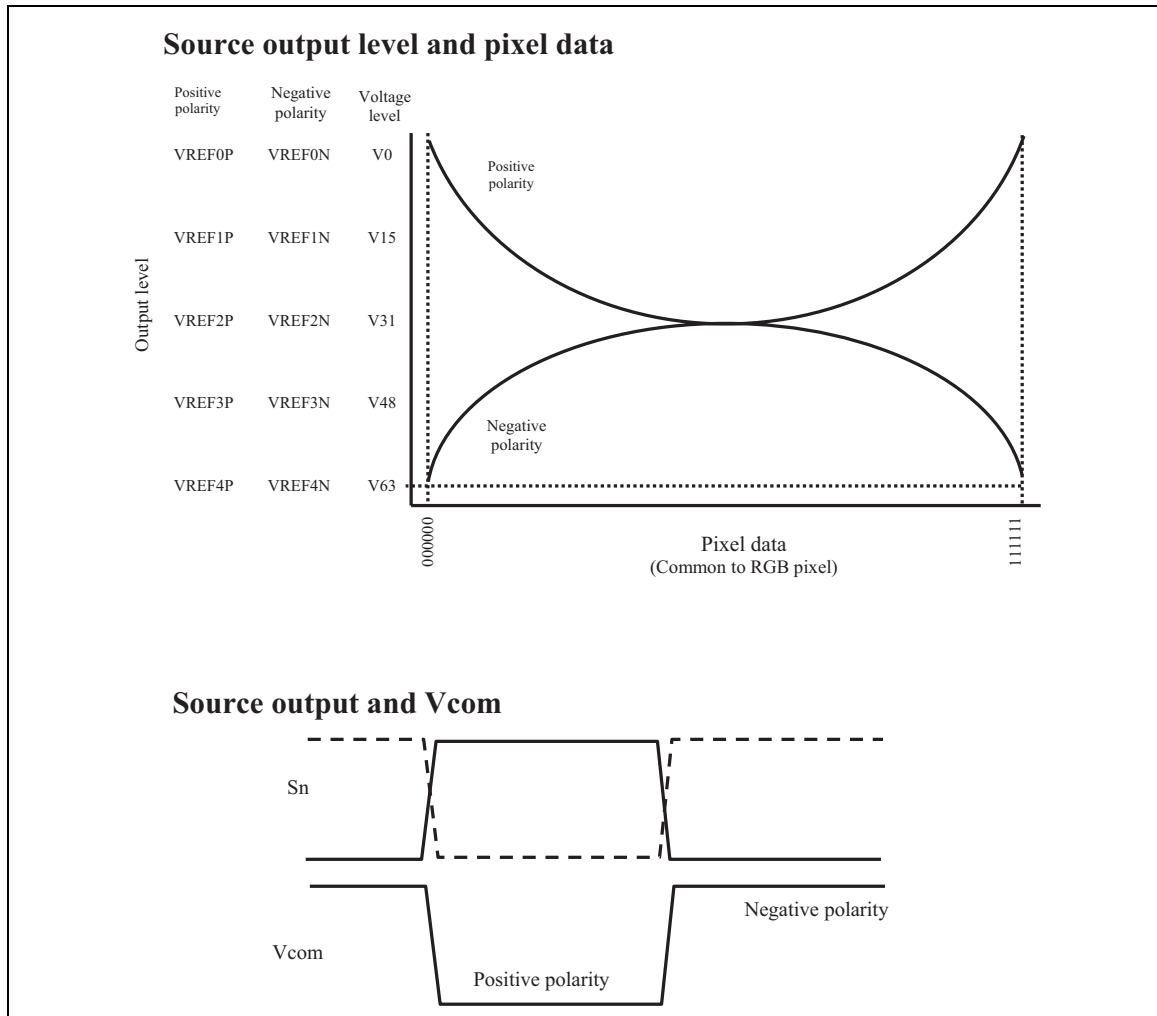
The following figure illustrates the configuration of a grayscale amplifier. The input power into VREF0P ~ VREF4P, VREF0N ~ VREF4N is divided internally with internal resistor of HD66779 to generate voltages from V0 to V63.



Note) Electric potential must be supplied externally to all VREF0P~VREF4P, VREF0N~VREF4N.

The Relationship between Input Data and Output Level

The following figure shows the relationship between the pixel data and the source output level.



Voltage calculation formula (positive polarity)

Grayscale voltage	Formula
V0	VREF0P
V1	$V15+(V0-V15)*(134/154)$
V2	$V15+(V0-V15)*(124/154)$
V3	$V15+(V0-V15)*(114/154)$
V4	$V15+(V0-V15)*(104/154)$
V5	$V15+(V0-V15)*(94/154)$
V6	$V15+(V0-V15)*(84/154)$
V7	$V15+(V0-V15)*(74/154)$
V8	$V15+(V0-V15)*(64/154)$
V9	$V15+(V0-V15)*(54/154)$
V10	$V15+(V0-V15)*(44/154)$
V11	$V15+(V0-V15)*(34/154)$
V12	$V15+(V0-V15)*(25/154)$
V13	$V15+(V0-V15)*(16/154)$
V14	$V15+(V0-V15)*(8/154)$
V15	VREP1P
V16	$V31+(V15-V31)*(77/84)$
V17	$V31+(V15-V31)*(70/84)$
V18	$V31+(V15-V31)*(63/84)$
V19	$V31+(V15-V31)*(57/84)$
V20	$V31+(V15-V31)*(51/84)$
V21	$V31+(V15-V31)*(45/84)$
V22	$V31+(V15-V31)*(39/84)$
V23	$V31+(V15-V31)*(34/84)$
V24	$V31+(V15-V31)*(29/84)$
V25	$V31+(V15-V31)*(24/84)$
V26	$V31+(V15-V31)*(20/84)$
V27	$V31+(V15-V31)*(16/84)$
V28	$V31+(V15-V31)*(12/84)$
V29	$V31+(V15-V31)*(8/84)$
V30	$V31+(V15-V31)*(4/84)$
V31	VREF2P
V32	$V48+(V31-V48)*(55/59)$
V33	$V48+(V31-V48)*(51/59)$
V34	$V48+(V31-V48)*(47/59)$
V35	$V48+(V31-V48)*(44/59)$
V36	$V48+(V31-V48)*(41/59)$
V37	$V48+(V31-V48)*(38/59)$
V38	$V48+(V31-V48)*(35/59)$
V39	$V48+(V31-V48)*(32/59)$
V40	$V48+(V31-V48)*(29/59)$
V41	$V48+(V31-V48)*(26/59)$
V42	$V48+(V31-V48)*(23/59)$
V43	$V48+(V31-V48)*(20/59)$
V44	$V48+(V31-V48)*(16/59)$
V45	$V48+(V31-V48)*(12/59)$
V46	$V48+(V31-V48)*(8/59)$
V47	$V48+(V31-V48)*(4/59)$
V48	VREF3P
V49	$V63+(V48-V63)*(85/89)$
V50	$V63+(V48-V63)*(81/89)$
V51	$V63+(V48-V63)*(77/89)$
V52	$V63+(V48-V63)*(73/89)$
V53	$V63+(V48-V63)*(69/89)$
V54	$V63+(V48-V63)*(64/89)$
V55	$V63+(V48-V63)*(59/89)$
V56	$V63+(V48-V63)*(54/89)$
V57	$V63+(V48-V63)*(48/89)$
V58	$V63+(V48-V63)*(42/89)$
V59	$V63+(V48-V63)*(35/89)$
V60	$V63+(V48-V63)*(28/89)$
V61	$V63+(V48-V63)*(21/89)$
V62	$V63+(V48-V63)*(14/89)$
V63	VREF4P

Note: the following relationship must be observed.

DDVDH-0.3V>=VREF0P>VREF1P>VREF2P>VREF3P>VREF4P>=GND-0.3V
 DDVDH-0.3V>=VREF0N>VREF1N>VREF2N>VREF3N>VREF4N>=GND+0.3V
 DDVDH-1.0V>=VREF1P, VREF1N
 VREF3P, VREF3N>=GND+1.0V
 $V_n - V_{n-1} > 20\text{mV} (n=0-62)$

Voltage calculation formula (Negative polarity)

Grayscale voltage	Formula
V0	VREF0N
V1	$V15+(V0-V15) * (75/89)$
V2	$V15+(V0-V15) * (68/89)$
V3	$V15+(V0-V15) * (61/89)$
V4	$V15+(V0-V15) * (54/89)$
V5	$V15+(V0-V15) * (47/89)$
V6	$V15+(V0-V15) * (41/89)$
V7	$V15+(V0-V15) * (35/89)$
V8	$V15+(V0-V15) * (30/89)$
V9	$V15+(V0-V15) * (25/89)$
V10	$V15+(V0-V15) * (20/89)$
V11	$V15+(V0-V15) * (16/89)$
V12	$V15+(V0-V15) * (12/89)$
V13	$V15+(V0-V15) * (8/89)$
V14	$V15+(V0-V15) * (4/89)$
V15	VREF1N
V16	$V32+(V15-V32) * (55/59)$
V17	$V32+(V15-V32) * (51/59)$
V18	$V32+(V15-V32) * (47/59)$
V19	$V32+(V15-V32) * (43/59)$
V20	$V32+(V15-V32) * (39/59)$
V21	$V32+(V15-V32) * (36/59)$
V22	$V32+(V15-V32) * (33/59)$
V23	$V32+(V15-V32) * (30/59)$
V24	$V32+(V15-V32) * (27/59)$
V25	$V32+(V15-V32) * (24/59)$
V26	$V32+(V15-V32) * (21/59)$
V27	$V32+(V15-V32) * (18/59)$
V28	$V32+(V15-V32) * (15/59)$
V29	$V32+(V15-V32) * (12/59)$
V30	$V32+(V15-V32) * (8/59)$
V31	$V32+(V15-V32) * (4/59)$
V32	VREF2N
V33	$V48+(V32-V48) * (80/84)$
V34	$V48+(V32-V48) * (76/84)$
V35	$V48+(V32-V48) * (72/84)$
V36	$V48+(V32-V48) * (68/84)$
V37	$V48+(V32-V48) * (64/84)$
V38	$V48+(V32-V48) * (60/84)$
V39	$V48+(V32-V48) * (55/84)$
V40	$V48+(V32-V48) * (50/84)$
V41	$V48+(V32-V48) * (45/84)$
V42	$V48+(V32-V48) * (39/84)$
V43	$V48+(V32-V48) * (33/84)$
V44	$V48+(V32-V48) * (27/84)$
V45	$V48+(V32-V48) * (21/84)$
V46	$V48+(V32-V48) * (14/84)$
V47	$V48+(V32-V48) * (7/84)$
V48	VREF3N
V49	$V63+(V48-V63) * (146/154)$
V50	$V63+(V48-V63) * (138/154)$
V51	$V63+(V48-V63) * (129/154)$
V52	$V63+(V48-V63) * (120/154)$
V53	$V63+(V48-V63) * (110/154)$
V54	$V63+(V48-V63) * (100/154)$
V55	$V63+(V48-V63) * (90/154)$
V56	$V63+(V48-V63) * (80/154)$
V57	$V63+(V48-V63) * (70/154)$
V58	$V63+(V48-V63) * (60/154)$
V59	$V63+(V48-V63) * (50/154)$
V60	$V63+(V48-V63) * (40/154)$
V61	$V63+(V48-V63) * (30/154)$
V62	$V63+(V48-V63) * (20/154)$
V63	VREF4N

Note: the following relationship must be observed.

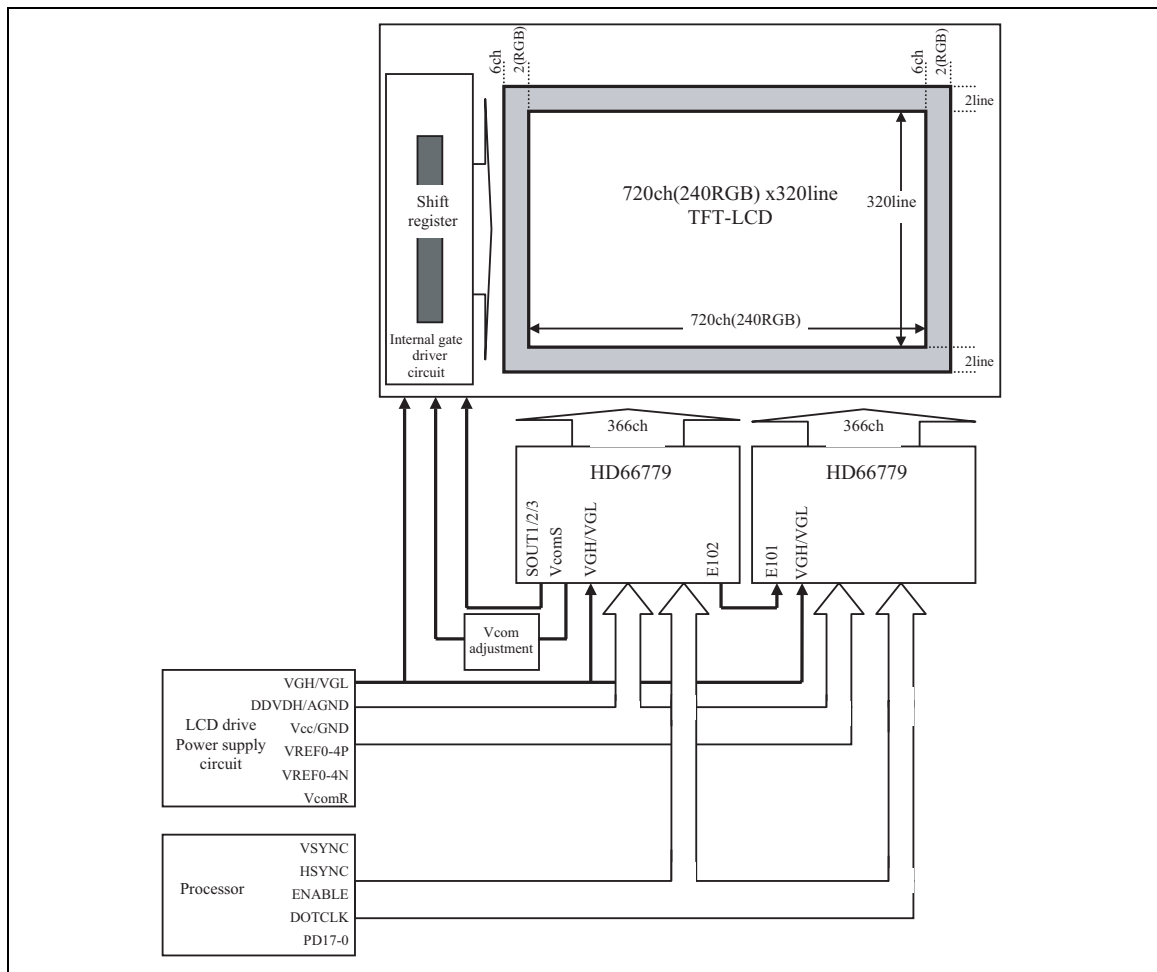
DDVDH-0.3V>=VREF0P>VREF1P>VREF2P>VREF3P>VREF4P>=GND- 0.3V
 DDVDH-0.3V>=VREF0N>VREF1N>VREF2N>VREF3N>VREF4N>=GND- 0.3V
 DDVDH-1.0V>=VREF1P, VREF1N
 VREF3P, VREF3N>=GND-1. 0V
 $V_n - V_{n+1} > 20mV (n=0-62)$

System Configuration Examples

System Configuration Example 1

240(horizontal) x 320(vertical) pixels only with pin settings, No SPI

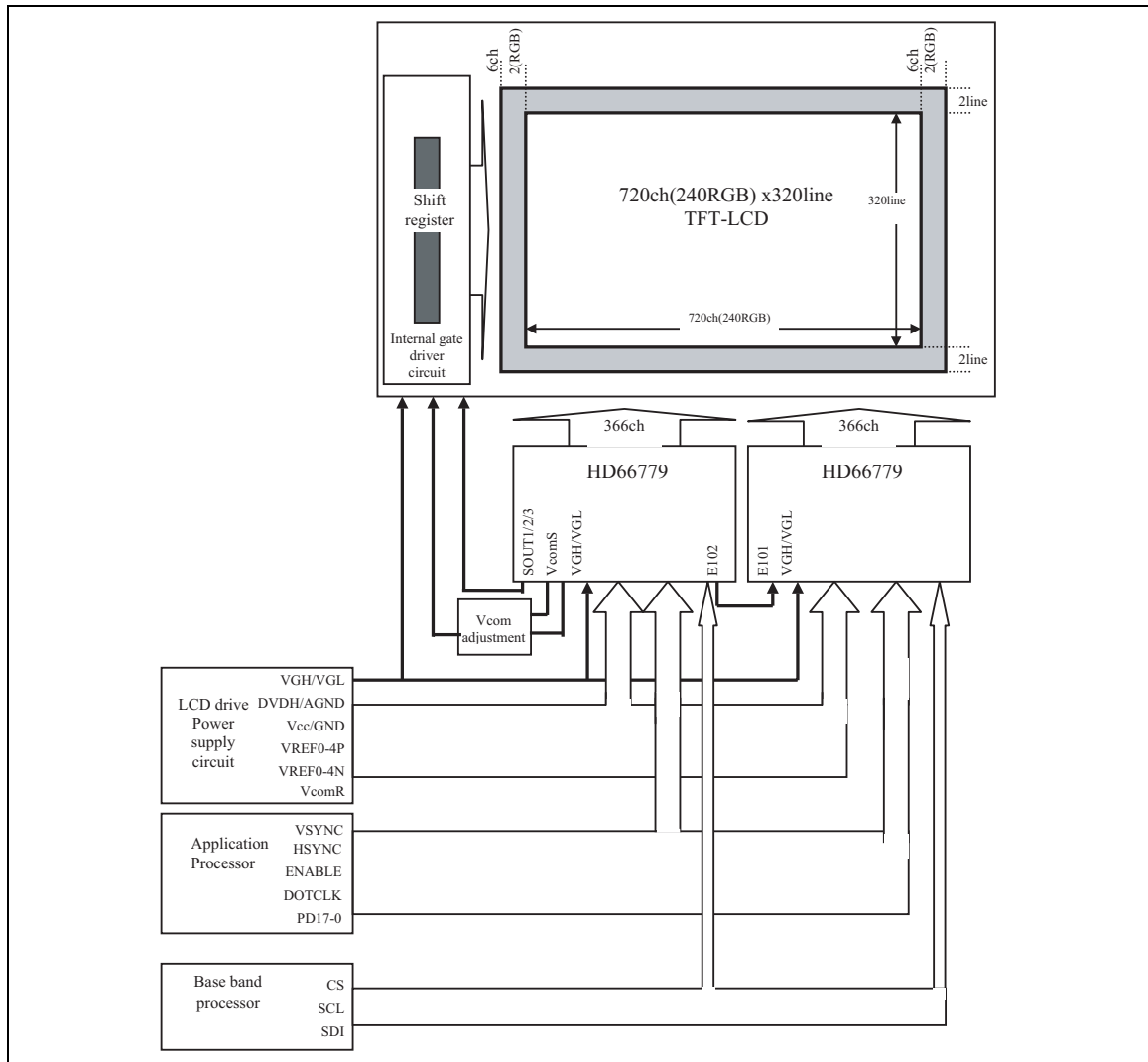
The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.



System Configuration Example 2

240(horizontal) x 320(vertical) pixels with SPI

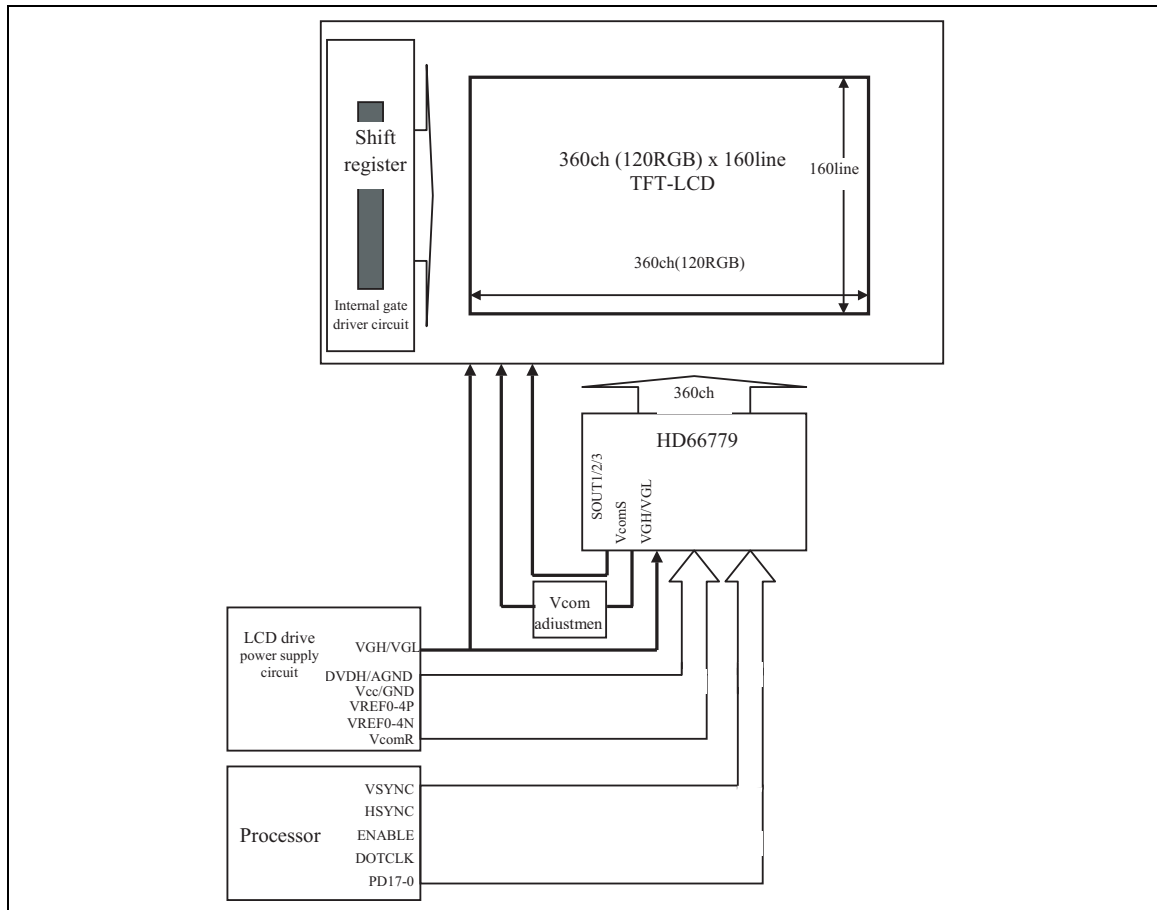
The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.



System Configuration Example 3

120(horizontal) x 160(vertical) pixels only with pin settings, No SPI

The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.



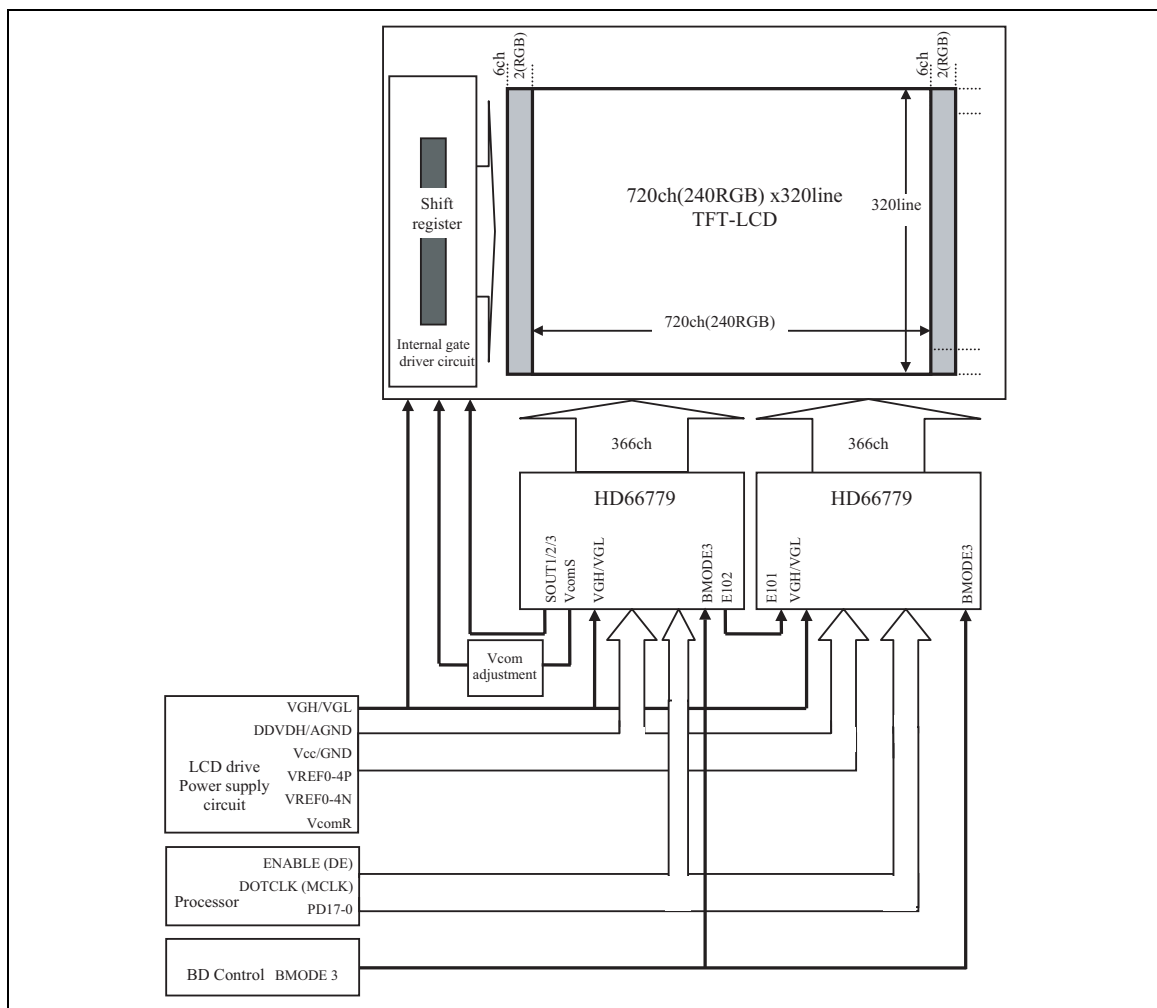
System Configuration Example 4

120(horizontal) x 160(vertical) pixels only with pin settings, DE transfer mode

The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.

Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.

Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.



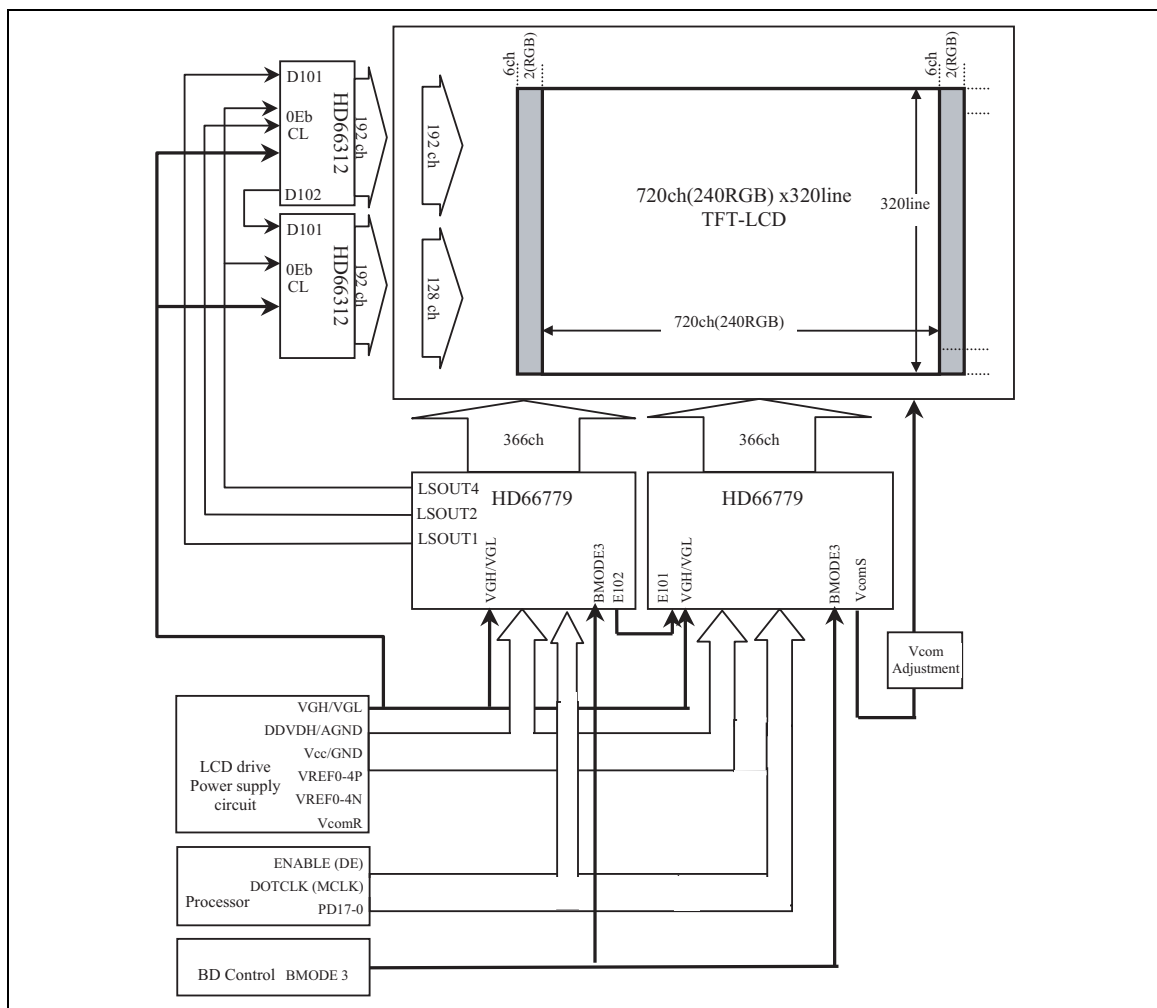
System Configuration Example 5

240(horizontal) x 320(vertical) pixels only with pin settings, DE transfer mode

The following figure illustrates an example of adopting HD66779 for TFT-LCD panel with an incorporated gate driver.

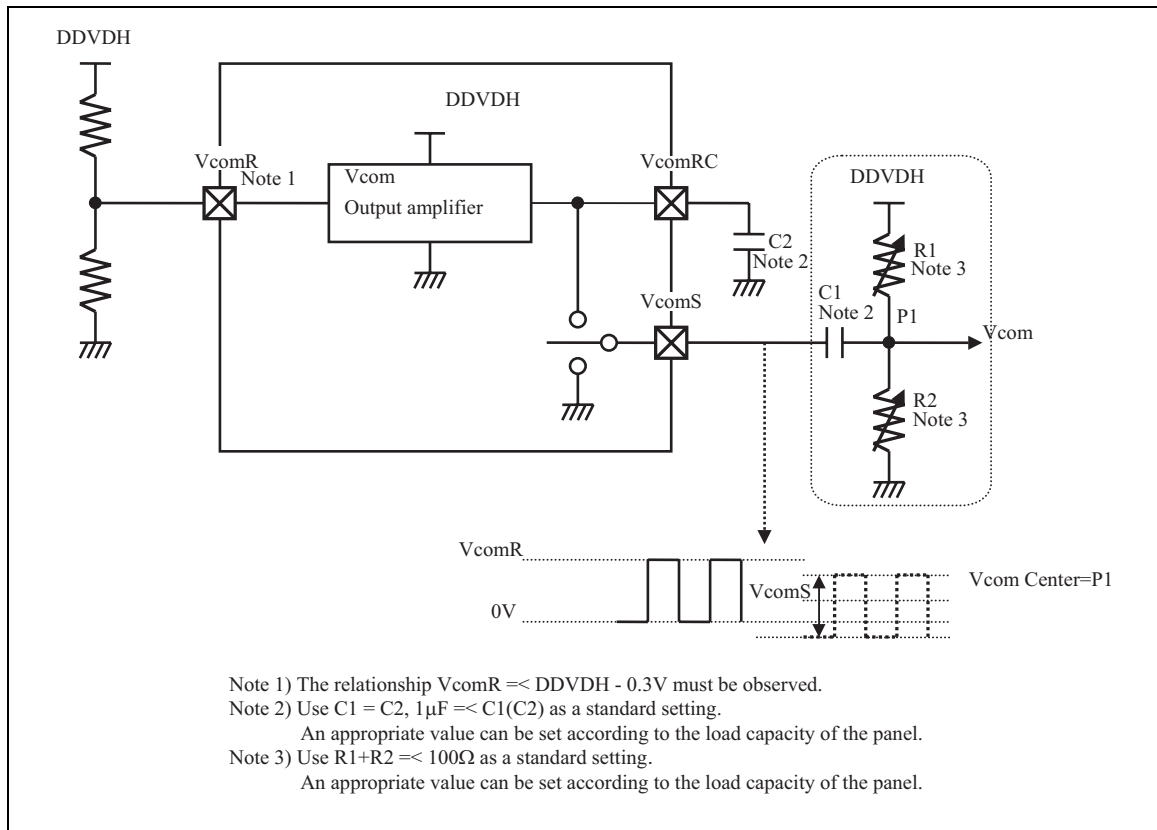
Note 1) The border color control while using DE transfer mode is on the 6 channels each at left and right side.

Note 2) The border color in DE transfer mode is only black and white to be switched with BMODE3 pin.



Vcom Generation

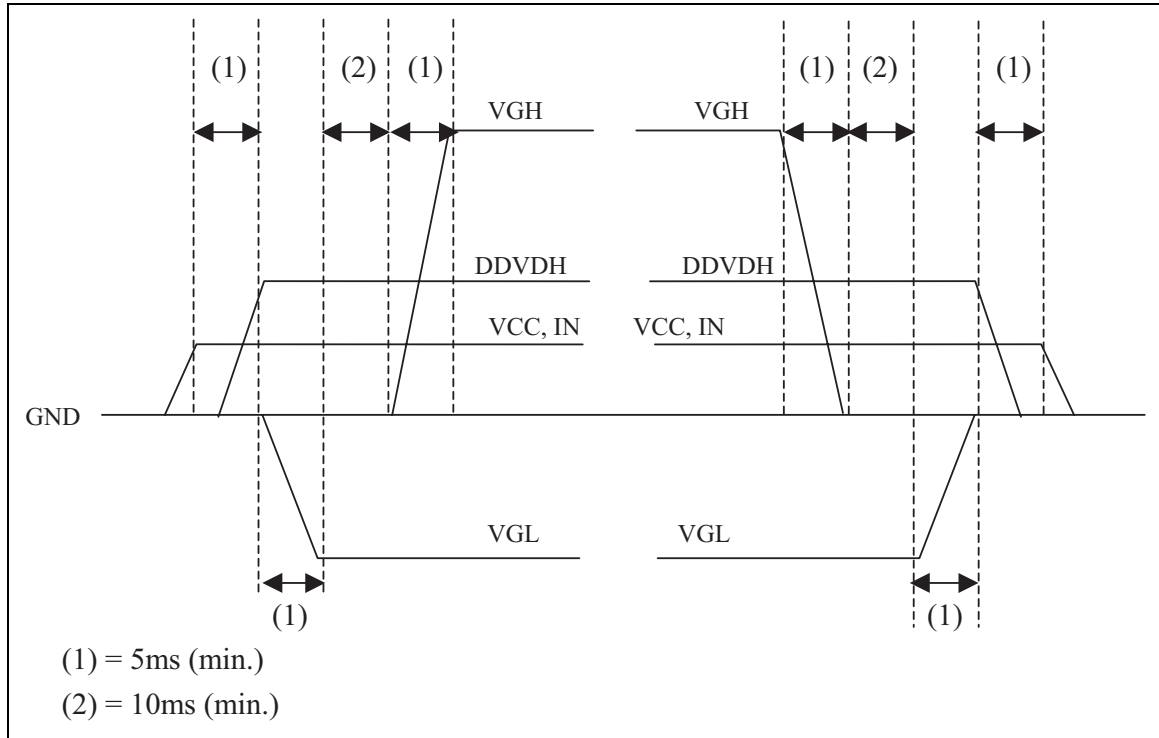
Vcom is generated from VcomR, a reference voltage of Vcom, by coupling method with an external circuit, which is supplied with the TFT display common electrode.



The external capacitor “C1” must be lowered to GND when VcomS is halted.

Voltage Application and insulation sequence

The voltage application/insulation sequence illustrated as follows must be observed.



Absolute Maximum Ratings

Items	Symbol	Unit	Rated value	Notes
Power supply voltage (1)	Vcc	V	- 0.3 ~ +4.3	(1), (2)
Power supply voltage (2)	DDVDH-GND	V	- 0.3 ~ + 6.0	(1), (3)
Power supply voltage (3)	VGH-AGND	V	- 0.3 ~ + 22.0	(1), (4)
Power supply voltage (4)	AGND-VGL	V	- 0.3 ~ + 16.5	(1), (5)
Input voltage	Vt	V	- 0.3 ~ Vcc + 0.3	(1)
Operational temperature	Topr	°C	- 40 ~ +85	(1), (6)
Storage temperature	Tstg	°C	- 55 ~ +110	(1)

Note1: If the LSI is used above these absolute maximum ratings, it may be permanently damaged. Using the LSI within the limit of electrical characteristics is strongly recommended during normal operation.

The use of LSI under a condition above the limit may lead to malfunction and loss of credibility of LSI.

Note2: Vcc (High) \geq GND (Low) must be observed.

Note3: DDVDH (High) \geq GND (Low) must be observed.

Note4: VGH (High) \geq AGND (Low) must be observed.

Note5: AGND (High) \geq VGL (Low) must be observed.

Note6: The DC/AC characteristics of die and wafer products is guaranteed at 85 °C.

Electrical characteristics

DC characteristics

V_{cc} = 2.5V ~ 3.6V, Ta = -40°C ~ +85°C: See Note 1

Items	Symbol	Unit	Measurement Condition	min.	typ.	max.	Notes	
Input "High" level voltage	V _{IH}	V	V _{cc} = 2.5V ~ 3.6V	0.7V _{cc}		V _{cc}	(2),(3)	
Input "Low" level voltage	V _{IL}	V	V _{cc} = 2.5V ~ 3.6V	-0.3		0.15V _{cc}	(2),(3)	
Output "High" level voltage	V _{OH}	V	I _{OH} = -0.1mA	0.7V _{cc}			(2)	
Output "Low" level voltage	V _{OL}	V	I _{OL} = 0.1mA			0.15V _{cc}	(2)	
input/output leak current	I _{Li}	μA	V _{in} = 0 ~ V _{cc}	-5		5	(4)	
Current Consumption (V _{cc} ~ GND)	Normal operation mode	I _{OP}	mA	V _{cc} = 3V, DDVDH = 5H, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25°C		1.1	1.35	(5)
	Static state	I _{ST}	μA	V _{cc} = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25°C		5	10	(5)
LCD power supply voltage (DDVDH ~ AGND)	DDVDH – AGND	I _{DDP}	mA	V _{cc} = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25°C		1.7	1.9	(5)
	AGND – VGL	I _{VLP}	μA	V _{cc} = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45μS, 366ch Ta = 25°C		80	110	(5)

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Items		Symbol	Unit	Measurement Condition	min.	typ.	max.	Notes
LCD power supply voltage (DDVDH ~ AGND)	VGH - AGND	I_{VHP}	μA	Vcc = 3V, DDVDH = 5V, VGH = 12V, VGL = -8V, DOTCLK = 8MHz, 1H period = 45 μ S, 366ch Ta = 25°C		80	110	(5)
Output voltage difference		ΔV_o	mV			+/-15	+/-25	(7)
Average output voltage fluctuation		ΔV_{Δ}	mV			+/-15		(8)

Serial Peripheral Interface Timing Characteristics

V_{CC} = 2.5 ~ 3.6 V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	t _{SCYC}	μs	Figure 1	0.2	—	40
Serial clock "High"-level pulse width	t _{SCH}	ns	Figure 1	80	—	—
Serial clock "Low"-level pulse width	t _{SCL}	ns	Figure 1	80	—	—
Serial clock rise/fall time	t _{scr} , t _{scf}	ns	Figure 1	—	—	40
Chip select set up time	t _{CSU}	ns	Figure 1	40	—	—
Chip select hold time	t _{CH}	ns	Figure 1	120	—	—
Serial input data set up time	t _{SISU}	ns	Figure 1	60	—	—
Serial input data hold time	t _{SIH}	ns	Figure 1	60	—	—

Reset Timing Characteristics

V_{CC} = 2.5 to 3.6 V

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset "Low"-level width	t _{RES}	ms	Figure 2	1	—	—
Reset rise time	t _{rRES}	μs	Figure 2	—	—	10

RGB interface timing characteristics

RGB interface, V_{CC} = 2.5V ~ 3.6V

Item	Symbol	Unit	Timing diagram	min.	typ.	max.
VSYNC/HSYNC Set up time	t _{SYNCS}	ns	Figure 3	20	—	—
ENABLE Set up time	t _{ENS}	ns	Figure 3	30	—	—
ENABLE Hold time	t _{ENH}	ns	Figure 3	30	—	—
DOTCLK "Low"-level pulse width	PWDL	ns	Figure 3	40	—	—
DOTCLK "High"-level pulse width	PWDH	ns	Figure 3	40	—	—
DOTCLK cycle time	t _{CYCD}	ns	Figure 3	100	—	—
Data Set up time	t _{PDS}	ns	Figure 3	30	—	—
Data Hole time	t _{PDH}	ns	Figure 3	30	—	—
DOTCLK, VSYNC, HSYNC rise/fall time	trgbr, trgbf	ns	Figure 3	—	—	25

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Switching characteristics

RGB interface, Vcc = 2.5V to 3.6 V

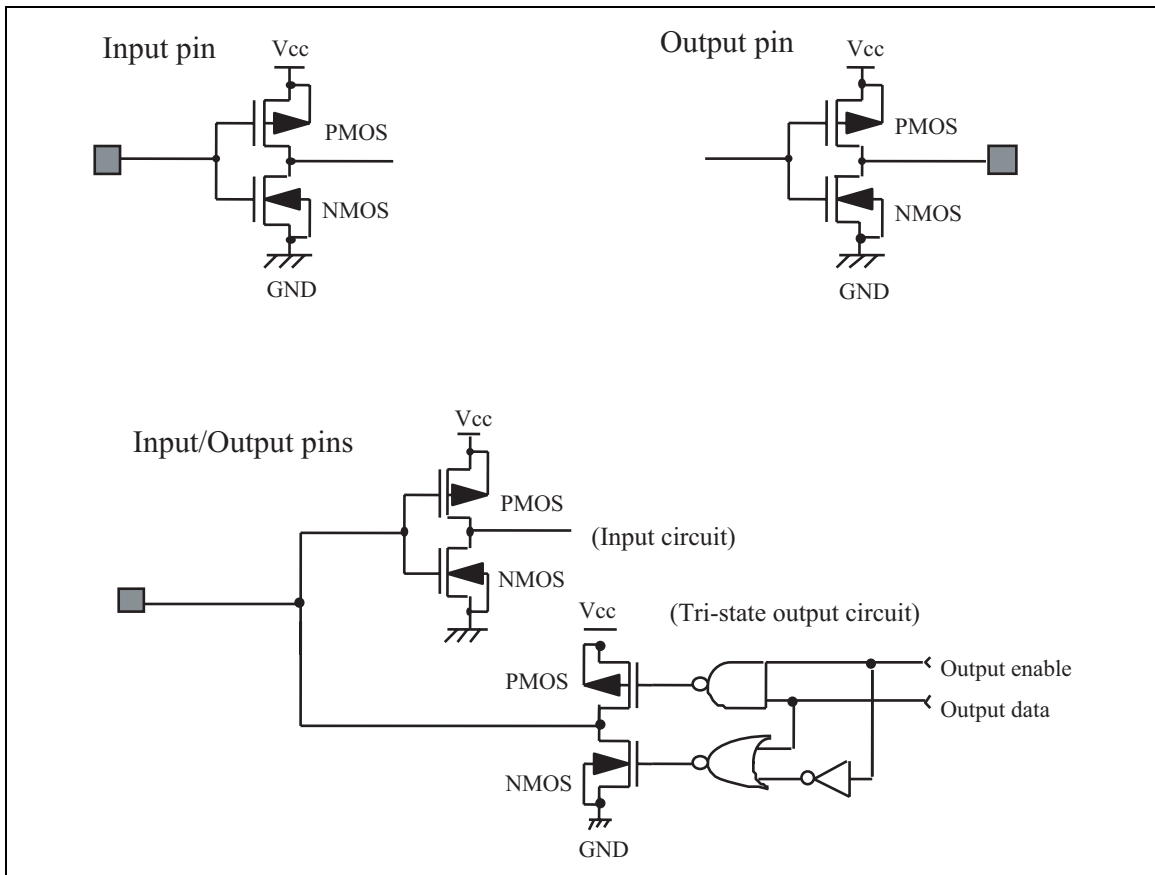
Item	Symbol	Unit	Timing diagram	min.	typ.	max.
Start pulse set up time	tSWS	ns	Figure 4	20	—	—
Start pulse delay time	tSWO	ns	Figure 4	—	—	80

LCD driver output characteristics

Item	Symbol	Unit	Test Condition	min.	typ.	max.	Note
Driver output delay time	tDD	μ s	Vcc = 3V, DDVDH = 5V, VGH = 8V, VGL = 0V, Ta = 25°C, DOTCLK = 8MHz, All pins undergo a same change from same grayscale level Time required to reach +/- 25 mV during VCOMS polarity change Load resistance R = 10k Ω , Load capacity 50pF	—	20	35	(10)

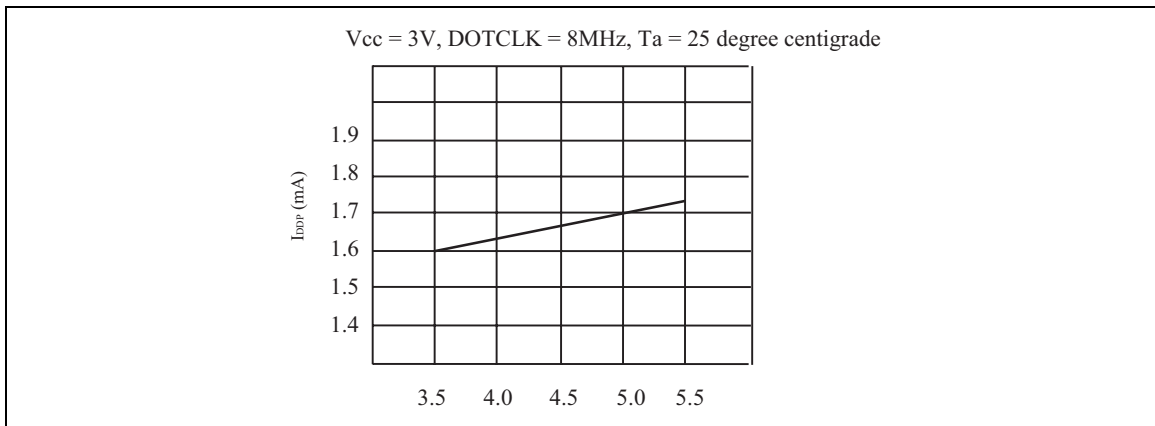
Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.
2. The following figures illustrate the configurations of I pin, I/O pin, and O pin.

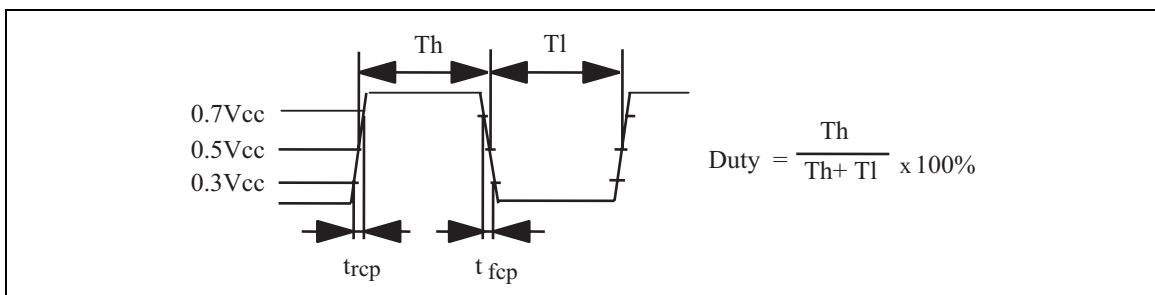


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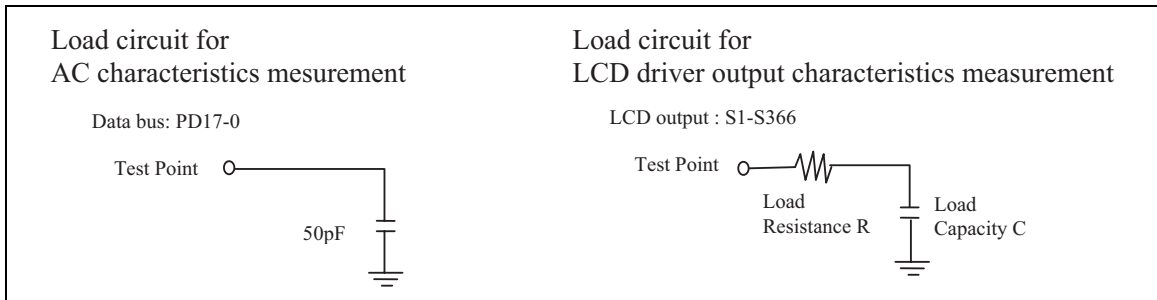
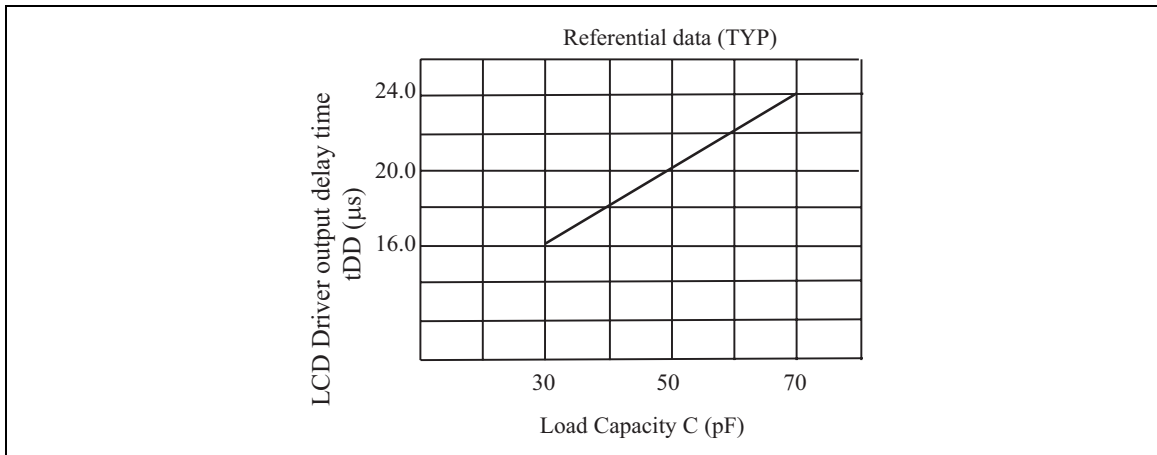
3. TEST, IM1, IM0/ID pins must be grounded or connected to Vcc.
4. This excludes the current through output drive MOS.
5. This excludes the current through the input/output units. The input level must be fixed to a certain level because penetrating current increases in the input circuit when CMOS input level takes a middle level. The current consumption is unchanged irrespective of “High” or “Low” of CS*pin while the HD66779 is not accessed through interface pins.
6. The relationship between operational condition and current consumption is as follows.



7. The output voltage difference is the difference in the neighboring output voltages for a same display (within a chip). The output voltage difference in offset cancel operation is within +/- 10mV.
8. The average output voltage fluctuation is the difference in the average output voltages among different chips. The average output voltage is an average voltage within a chip for a same display. This value is just for a referential purpose.
9. This applies to the case when clocks are supplied externally.



10. The LCD driver output delay time depends on the load on the LCD panel. Check the quality of display on the actual LCD panel before making settings for the frame frequency and one-line cycle.



Timing diagram

Serial Peripheral Interface Operation

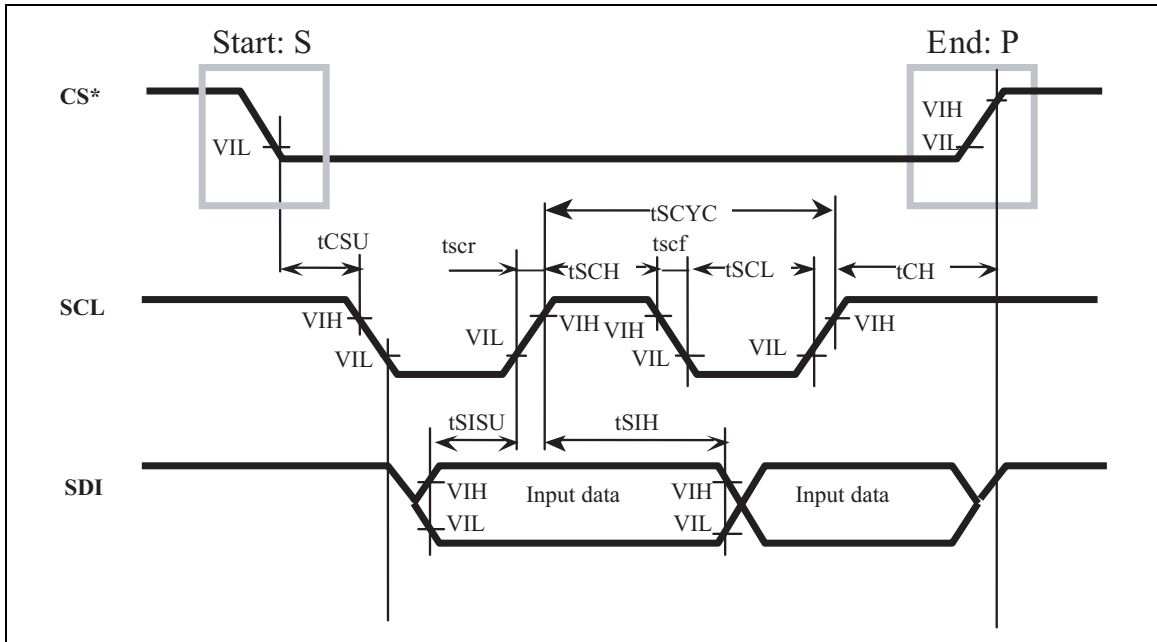


Figure 1

Reset Operation

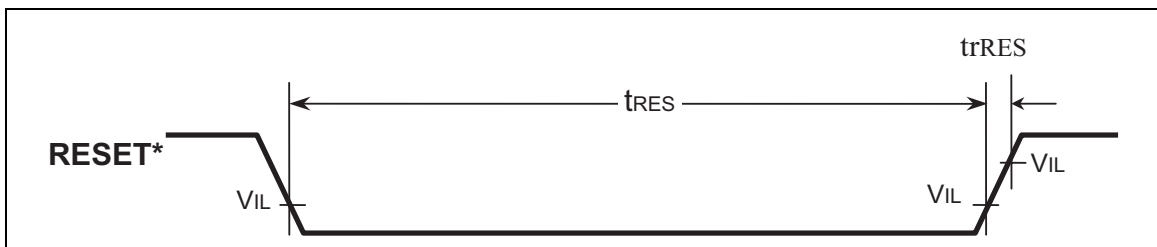


Figure 2

Interfacing Operation

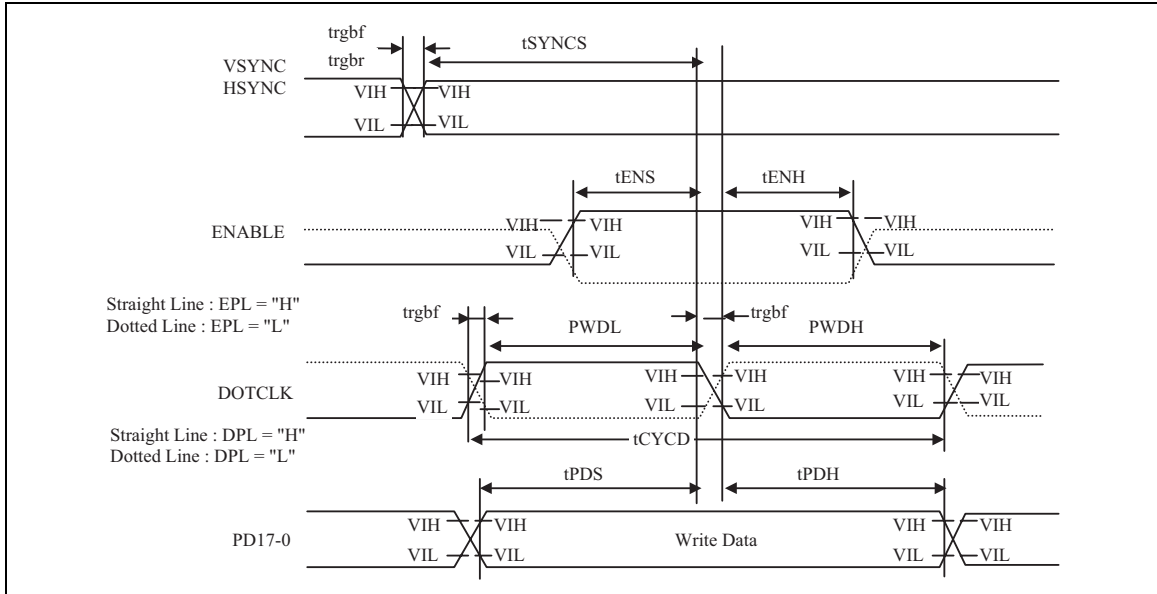


Figure 3

Switching Operation

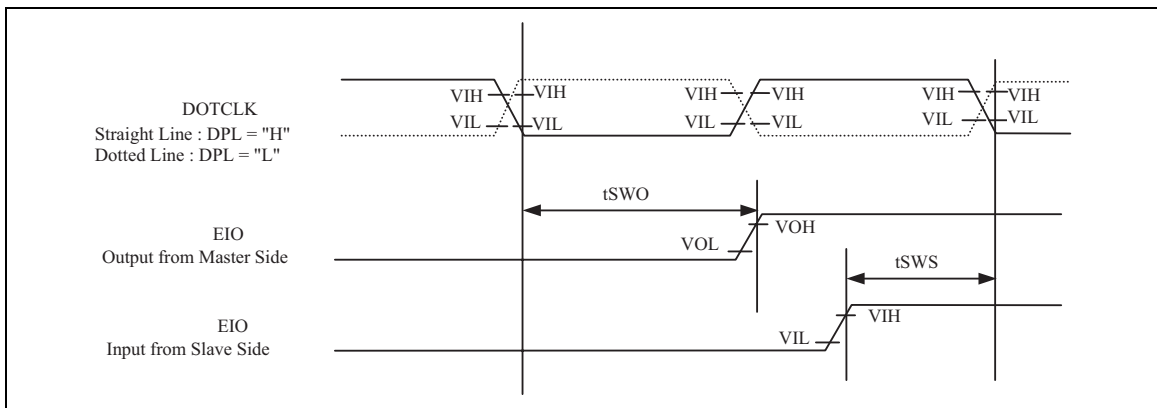


Figure 4

LCD Driver Output Characteristics

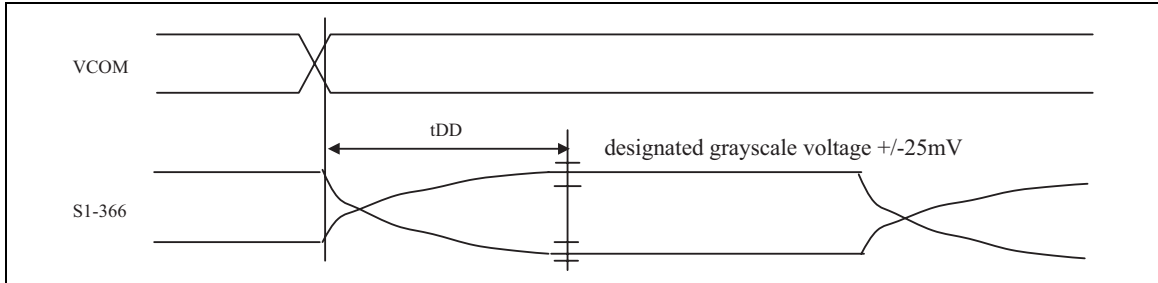


Figure 5

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Revision Record

Rev.	Date	Page	Contents of Modification	Approved by
0.2	2002.10.25		First issue	
0.3	2002.12.13	4	Figure 1: Change "POS" to "TESTPS"	
		5	Change the explanation for (1) External Display Interface.	
		6	Add "TESTPS" to Table 1.	
		7	Add "When using border display, display period is 320H." to Function of BMODE1.	
			Delete "POS" from Table 1.	
		8	Change Function of DOTCLK.	
			Add "(DE)" to the Signal name "ENABLE".	
			Add "When using DE transfer mode (SSMD1 = "H"), BP setting is invalid." to Function of BP.	
		10	Change Function of GAON.	
		12	Revise PAD arrangement figure to Rev.0.1.	
		13	Revise Pad coordinate (Input) to Rev. 0.1.	
		15	Delete "POS" from Figure 5.	
			Delete the explanation of "POS".	
		17	Change "14 lines \geq BP \geq 2 lines" in the explanation of BP3-0 to "14 lines \geq Number of back porch lines minus number of border lines".	
		19	Change the waveform of SOUT4 upside down in Figure 12.	
			Change the note added to Figure 12.	
		20	Add a note "" to the explanation of FHN.	
		21	Delete "*POS" and "0" in bit 9 of R01h, and add "1" instead of "POS".	
		22	Delete "Source output: S1 - S366 Output "GND" level" from 2. Initial level of output pin.	
		24	Change Figure 16 and its note.	
		25	Delete the explanation of "Power save function (POS)".	
			Change Figure 18.	
		26	Delete Table 13 and add new Table 13, 14, and 15.	
		29	Add "For the detail setting of timing, refer to "Signal timing control function for LCD display" to Figure 21.	
		30	Add the same note added to Figure 21 to Figure 22.	
		33	Add the same note added to Figure 21 to Figure 25.	
		34	Add the same note added to Figure 21 to Figure 26.	
		35	Add the same note added to Figure 21 to Figure 27.	
		40	Delete Table 17(old) Wire setting.	
		40	Correct Table 18.	

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Rev.	Date	Page	Contents of Modification	Approved by
0.3	2002.12.13	51 53 54 55 57 60	Correct "VCC" to "VCC, IN" in Figure 44. Change Table 22. (T.B.D → Decided) Change Table 23 and 24. (T.B.D → Decided) Change Table 24, 25, and 26. (T.B.D → Decided) Correct "+/- 2m" to "+/- 10m" in note 7. Change Figure 56 and 57.	
1.0	2002.6.13	9 5, 14, 19, 26, 32~35, 54, 57 58, 60, 61, 63, 64, 67	Error Correction. Change "GND" to "Vcc" to which TEST4 is connected. Change "TEST1, 4-15" to "TEST1, 5-15" and number of pins from "15" to "14". Addition to function column. "Make sure $V_{GH} \geq DDVDH \geq V_{CC}$ " Error Corrections Addition of measurement to the electrical characteristics tables where marked with "TBD".	