HD66789R

528-channel One-chip Driver with 262,144-color Display RAM, Power Supply and Gate Circuits for TFT Panels

REJxxxxxxx-xxxx
Rev.1.01
24 December 2003

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Description

The HD66789R is a TFT liquid crystal display driver compliant to 262,144 colors with RAM for graphics display of 176 RGB x 240 dots at maximum, a 528-channel source driver, a gate driver and a power supply circuit, all incorporated in one chip to provide a single-chip solution to drive a TFT panel.

The HD66789R supports 8/9/16/18-bit high-speed bus interfaces and a high-speed RAM write function, enabling efficient data transfers and high-speed rewrite of RAM graphics data. In addition, the HD66789R incorporates an RGB interface (VSYNC, HSYNC, DOTCLK, ENABLE, and PD17-0), and a VSYNC interface (system interface + VSYNC) to display moving pictures. In combination with a window address function, the RGB, VSYNC interfaces facilitate moving picture display in an arbitrary position, and allow for simultaneous display of a moving picture and the internal RAM data to realize the moving picture display operation not constrained by the still picture display. This means data transfer required for moving picture display is minimized, contributing to the reduction of power consumption by the entire system.

The HD66789R is compliant to the low voltage operation up to 1.65V for power supply to the I/O interface, and incorporates a voltage follower circuit. The HD66789R also supports an 8-color display mode and a standby function to allow precise power control by software. These features make the HD66789R the ideal solution for medium or small-size portable products that require a long battery life, such as digital cellular phones, small/medium PDAs supporting WWW browsers.

Features

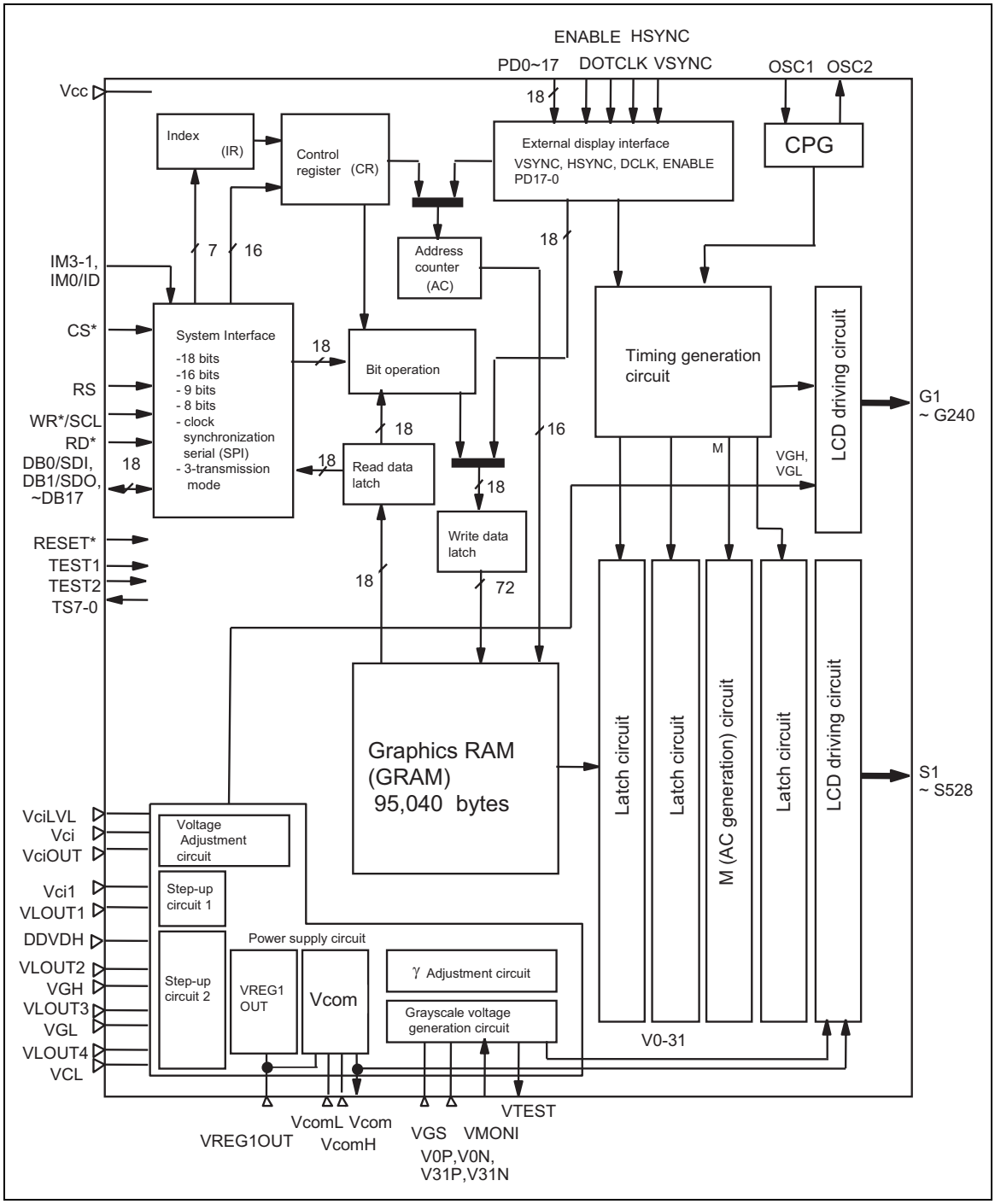
- Liquid crystal controller/driver for 262,144 TFT-color 176RGB x 240-dot graphics display
- Single chip solution to drive a TFT display panel
- System interface
  - 8-/9-/16-/18-bit high-speed bus interfaces
  - Serial Peripheral Interface (SPI)
  - 8-bit transfer x 3 times (262k/65k color modes)
- Interface for moving picture display
  - 6-/16-/18-bit RGB interfaces (VSYNC, HSYNC, DOTCLK, ENABLE, PD17-0)
  - VSYNC interface (System interface + VSYNC)
- Window address function to write data to a rectangular area of RAM specified by window addresses
  - Facilitates moving picture display in an arbitrary area through a moving picture display interface
  - Reduces data transfers by transferring only data relevant to a moving picture area
  - Enables simultaneous display of a moving picture and the contents of the internal RAM
- Bit operation functions for graphics processing
  - Bit-unit write data mask function
  - Pixel-unit logical operation and conditional rewrite function
- Various functions to control color display
  - Simultaneous availability of 262,144 colors with γ-correction function
  - Line-unit vertical scrolling
- Low-power architecture
  - Features for low voltage operation
    - Vcc = 2.4 ~ 3.3 V (internal logic power supply)
    - IOVcc = 1.65 ~ 3.3 V (interface I/O power supply)
    - Vci = 2.5 ~ 3.3 V (analog power supply)
  - Low-voltage drive: DDVDH = 4.5 ~ 5.5 V
  - Power-saving functions (standby mode etc.)
  - Partial liquid crystal drive to display two screens at arbitrary positions
  - Voltage follower circuit for a liquid crystal drive power supply to prevent direct current of bleeder resistors
- Circuits to step-up liquid crystal drive voltage up to 6 times (x6)
- 95,040-byte internal RAM
- Incorporated liquid crystal display driver with 528 source outputs / 240 gate outputs
- n-line inversion alternating drive, i.e. to invert polarity at an interval of the number of lines set arbitrarily
- Reset function for the Internal oscillator and hardware
- Reversible shift direction of source outputs
- For Cst only

Liquid crystal power supply specification

Table 1 HD66789R liquid crystal power supply specification

No.	Item		HD66789R
1	TFT data lines		528 pins (176 x RGB)
2	TFT gate lines		240 pins
3	TFT display capacitor structure		Cst structure
4	Liquid crystal drive output	S1~S528	V0 ~ V31 grayscales
		G1~G240	VGH-VHL
		Vcom1, 2	VcomH-VcomL: amplitude = electronic volumes VcomH=VcomR: Adjusted by an external resistor
5	Input voltage	IOVcc	1.65 ~ 3.30V
		Vcc	2.40 ~ 3.30V
		Vci	2.50 ~ 3.30V
6	Internal step-up circuits	VLOUT1 (DDVDH)	Vci1 x 2
		VLOUT2 (VGH)	Vci1 x 4, x 5, x 6
		VLOUT3 (VGL)	Vci1 x -3, x -4, x -5
		VLOUT4 (VCL)	Vci1 x -1

Block Diagram



Pin Functions

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>IM3~1, IM0/ID</td><td>4</td><td>I</td><td>GND/ IOVcc</td><td>Selects an interfacing mode with MPU.
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU-Interface Mode</th><th>DB Pin</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>80-system 16-bit interface</td><td>DB17~10, DB8~1</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>1</td><td>80-system 8-bit interface</td><td>DB17 ~10</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>ID</td><td>Serial Peripheral Interface (SPI)</td><td>DB1-0</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>*</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>0</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>Setting disabled</td><td>_</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>80-system 18-bit interface</td><td>DB17~0</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>1</td><td>80-system 9-bit interface</td><td>DB17~9</td></tr>
<tr><td>1</td><td>1</td><td>*</td><td>*</td><td>Setting disabled</td><td>_</td></tr>
</table>
In SPI mode, IM0/ID pin is used for setting an ID for the device code.</td></tr>
<tr><td>CS*</td><td>1</td><td>I</td><td>MPU</td><td>A chip (the HD66789R) selecting signal. Fix to the GND level when not used.
Low: the HD66789R is selected and accessible
High: the HD66789R is not selected and not accessible</td></tr>
<tr><td>VLD</td><td>1</td><td>I</td><td>MPU</td><td>Fix to GND.</td></tr>
<tr><td>RS</td><td>1</td><td>I</td><td>MPU</td><td>A register selecting signal. Fix to the IOVcc level or the GND level in SPI mode.
Low: selects an Index or status register
High: selects a control register</td></tr>
<tr><td>WR*/SCL</td><td>1</td><td>I</td><td>MPU</td><td>In 80-system bus interface mode, serves as a write strobe signal. Write data at the “Low” level. In SPI mode, serves as a clock synchronizing signal.</td></tr>
<tr><td>RD*</td><td>1</td><td>I</td><td>MPU</td><td>In 80-system bus interface mode, serves as a read-strobe signal. Read data at the “Low” level. In SPI mode, fix to either the GND level or the IOVcc level.</td></tr>
<tr><td>DB0/SDI</td><td>1</td><td>I/O</td><td>MPU</td><td>An 18-bit parallel bi-directional data bus in 80-system interface mode. Fix the unused pins to either the GND level or the IOVcc level.
8-bit bus: use DB8-DB1
9-bit bus: use DB8-DB0
16-bit bus: use DB17-DB10 and DB8-DB1
18-bit bus: use DB17-DB0
In SPI mode, serves as a serial data input (SDI) pin to take in data on the rising edge of the SCL signal.</td></tr>
</table>

<table>
<tr><th>Signals</th><th>Number of Pins</th><th>I/O</th><th>Connected to</th><th>Functions</th></tr>
<tr><td>DB1/SDO</td><td>1</td><td>I/O</td><td>MPU</td><td>An 18-bit parallel bi-directional data bus in 80-system interface mode. Fix the unused pins to either the GND level or the IOVcc level.
8-bit bus: use DB8-DB1
9-bit bus: use DB8-DB0
16-bit bus: use DB17-DB10 and DB8-DB1
18-bit bus: use DB17-DB0
In SPI mode, serves as a serial data output (SDO) pin to output data on the falling edge of the SCL signal.</td></tr>
<tr><td>DB2~17</td><td>16</td><td>I/O</td><td>MPU</td><td>An 18-bit parallel bi-directional data bus in 80-system interface mode. Fix the unused pins to either the GND level or the IOVcc level.
8-bit bus: use DB8-DB1
9-bit bus: use DB8-DB0
16-bit bus: use DB17-DB10 and DB8-DB1
18-bit bus: use DB17-DB0</td></tr>
<tr><td>ENABLE</td><td>1</td><td>I</td><td>MPU</td><td>A data ENEABLE signal in RGB I/F mode. Fix the unused pins to either the GND level or the IOVcc level.
Low: Selected (access enabled)
High: Not selected (access disabled)
The polarity of the ENABLE signal is inverted by the EPL bit.
<table>
<tr><th>EPL</th><th>ENABLE</th><th>RAM write</th><th>RAM address</th></tr>
<tr><td>0</td><td>0</td><td>Enabled</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Disabled</td><td>Retained</td></tr>
<tr><td>1</td><td>0</td><td>Enabled</td><td>Retained</td></tr>
<tr><td>1</td><td>1</td><td>Disabled</td><td>Updated</td></tr>
</table></td></tr>
<tr><td>VSYNC</td><td>1</td><td>I</td><td>MPU</td><td>A frame synchronizing signal. Fix to the IOVcc level when not used.
If VSPL=0: Active low.
If VSPL=1: Active high</td></tr>
<tr><td>HSYNC</td><td>1</td><td>I</td><td>MPU</td><td>A line synchronizing signal. Fix to the IOVcc level when not used.
If HSPL=0: Active low.
If HSPL=1: Active high</td></tr>
<tr><td>DOTCLK</td><td>1</td><td>I</td><td>MPU</td><td>A dot clock signal. Fix to the IOVcc level when not used.
If DPL=0: Data are input on the rising edge of DOTCLK.
If DPL=1: Data are input on the falling edge of DOTCLK.</td></tr>
<tr><td>PD0~17</td><td>18</td><td>I</td><td>MPU</td><td>An 18-bit RGB data bus in 80-system interface mode. Fix the unused pins to either the GND level or the IOVcc level.
6-bit bus: use PD17-PD12
16-bit bus: use PD17-PD13 and PD11-PD1
18-bit bus: use PD17-PD0</td></tr>
<tr><td>RESET*</td><td>1</td><td>I</td><td>MPU or reset circuit</td><td>A reset pin. Initializes the HD66789R at the “Low” level.
A power-on reset is required after turning on the power supply.</td></tr>
</table>

Signals	Number of Pins	I/O	Connected to	Functions
S1~S528	528	O	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, if SS = 0, data in the RAM address "0000" is output from S1. If SS = 1, the same data in the RAM address "0000" is output from S528. S1, S4, S7, ... display red (R), S2, S5, S8, ... display green (G), and S3, S6, S9, ... display blue (B) (SS = 0).
G1~G240	240	O	LCD	Output signals from gate lines. VGH: the level to select the gate lines VGL: the level not to select the gate lines
Vcom1, Vcom2	2	O	TFT common electrode	A power supply for the TFT common electrode. Outputs alternating voltage levels of VcomH and VcomL. Outputs the same voltage level as VcomL when not alternating Vcom levels. The alternating cycle is determined by the M signal. Connect to the TFT common electrode.
VcomH	1	O	Stabilizing capacitor	The Vcom High level when Vcom alternating drive is executed. Connect to a stabilizing capacitor.
VcomL	1	O	Stabilizing capacitor or open	The Vcom level when Vcom alternating drive is not executed. The Vcom "Low" level when Vcom alternating drive is executed. The voltage level is adjusted by the internal register. Connect to a stabilizing capacitor. When the VCOMG bit is set to "0", the VcomL output is halted. In this case, capacitor connection is not required.
VcomR	1	I	Variable resistor or open	A VcomH reference voltage. When adjusting VcomH externally, set registers to halt the VcomH internal adjusting circuit and place a variable resistor between VREG1OUT and GND. Otherwise, leave this pin open and adjust VcomH by setting the internal register of the HD66789R.
C11+, C11-	2	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 1. When not using the step-up circuit 1, disconnect them.
C12+, C12- C21+, C21- C22+, C22-	6	I/O	Step-up capacitor	Pins to connect capacitors for the step-up circuit 2. Connect capacitors as required according to the step-up rate. When not using the step-up circuit 2, disconnect them.
OSC1, OSC2	2	I/O	Oscillation resistor	Pins to connect an external resistor for RC oscillation.
FLM	1	O	MPU or open	A frame head pulse (amplitude: IOVcc-GND). Use when writing data to RAM in synchronization with FLM. When FLM is not used, disconnect it.
Vci	1	I	Power supply	A power supply for the analog circuits. Connect to an external power supply of 2.5~3.3V.
VciLVL	1	I	Power supply	Generates a reference voltage (VciOUT, REGP) from the VciLVL level according to the ratio determined by the VC2-0 bits. Connect to Vci on the FPC.
REGP	1	I/O	Test pin	A test pin for VREG1OUT. Disconnect it.
VciOUT	1	O	Stabilizing capacitor, Vci1	An internal reference voltage. The amplitude between Vci and GND is determined by the VC2-0 bits.

Signals	Number of Pins	I/O	Connected to	Functions
Vci1	1	I	VciOUT	A reference voltage for the step-up circuit 1. Connect to an external power supply of 2.75V or less when not using an internal reference voltage.
VLOUT1	1	O	Stabilizing capacitor, DDVDH	An output from the step-up circuit 1, of twice the Vci1 level. Connect to a stabilizing capacitor between GND and VLOUT1. Place a schottkey barrier diode (see “configuration of the power supply” p.128). VLOUT1 = 4.0~5.5V
DDVDH	1	I	VLOUT1	A power supply for the source driver outputs. A reference voltage for the step-up circuit 2.
VLOUT2	1	O	Stabilizing capacitor, VGH	An output from the step-up circuit 2, of 4 ~ 6 times the Vci1 level. The step-up rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between GND and VLOUT2. Place a schottkey barrier diode between Vci and VLOUT2. Place a schottkey barrier diode (see “configuration of the power supply” p.128). VLOUT2 = max 16.5V
VGH	1	I	VLOUT2	A power supply for the TFT LCD’s gate driver. Connect to VLOUT2.
VLOUT3	1	O	Stabilizing capacitor, VGL	An output from the step-up circuit 2, of -3 ~ -5 times the Vci1 level. The step-down rate is determined with BT2-0 bits. Connect to a stabilizing capacitor between GND and VLOUT3. Place a schottkey barrier diode between Vci and VLOUT2. Place a schottkey barrier diode (see “configuration of the power supply” p.128). VLOUT3 = min -16.5V
VGL	1	I	VLOUT3	A power supply for the TFT LCD’s gate driver. Connect to VLOUT3.
VLOUT4	1	O	Stabilizing capacitor, VCL	An output from the step-up circuit 2, of –1 time the Vci1 level. Connect to a stabilizing capacitor. VLOUT4 = 0 ~ -3.3V
VCL	1	I	VLOUT4	A power supply for the VcomL level. Connect to VLOUT4.
VREG1OUT	1	I/O	Stabilizing capacitor or power supply	A reference voltage of DDVDH-GND, which is generated from an internally generated reference voltage of Vci-GND. The ste-up rate is determined with the VRH bits. VREG1OUT serves as (1) a source driver grayscale reference voltage VDH, (2) a VcomH level reference voltage, and (3) a Vcom amplitude reference voltage. Connect to a stabilizing capacitor. VREG1OUT = 3.0 ~ (DDVDH – 0.5)V
Vcc	1	-	Power supply	A power supply for the internal logic. Vcc = 2.4 ~ 3.3V
IOVcc	1	-	Power supply	A power supply for the interface pins. IOVcc = 1.65 ~ 3.3V. Provide the supply voltage IOVcc simultaneously with the internal logic voltage Vcc. When using the COG method, connect to Vcc on the FPC if IOVcc=Vcc, to prevent noise.
RVcc	1	-	Power supply	A Vcc power supply for the internal RAM. RVcc must be at the same electric potential as Vcc.
GND	1	-	Power supply	Ground for the logic side. GND = 0V
AGND	1	-	Power supply	Ground for the analog side. AGND = 0V. When using the COG method, connect to GND on the FPC to prevent noise.

Signals	Number of Pins	I/O	Connected to	Functions
RGND	1	-	Power supply	Ground for the internal RAM. RGND = 0V. When using the COG method, connect to GND on the FPC to prevent noise.
CGND	1	O	Opposing GND for external elements	Output the GND level. Used as the GND for external elements, such as diodes or capacitors.
TEST1	1	I	GND	A test pin. Make sure to fix it to the GND level.
TEST2	1	I	GND	A test pin. Make sure to fix it to the GND level.
V0P, V31P	2	I or O	Stabilizing capacitor	Outputs from the internal positive polarity operational amplifier when it is on (when SAP2-0 = “001”, “010”, “011”, “100”, and “101”). Connect to a capacitor to stabilize the amplifier.
V0N, V31N	2	I or O	Stabilizing capacitor	Outputs from the internal negative polarity operational amplifier when it is on (when SAP2-0 = “001”, “010”, “011”, “100”, and “101”). Connect to a capacitor to stabilize the amplifier
VGS	1	I	GND or external resistor	A reference level for a grayscale voltage generating circuit. Connect to an external resistor when adjusting the reference level.
VTESTS	1	I/O	Open	A test pin. Disconnect it.
TS0~TS7	8	O	Open	Test pins. Disconnect them.
TESTA1	1	I/O	Open	A test pin for VcomH. Disconnect it.
TESTA2	1	I/O	Open	A test pin for VcomL. Disconnect it.
TESTA4	1	I/O	Open	A test pin for VcomL. Disconnect it.
VMONI	1	O	Open	A test pin. Disconnect it.
IOVccDUM1~4	4	O	Input pin	Internal IOVcc level outputs. When adjacent input pins are fixed to the IOVcc level, short-circuit them.
IOGNDDUM1~7	7	O	Input pin	Internal GND level outputs. When neighboring input pins are fixed to the GND level, short-circuit them.
TESTO1~4	4	-	-	Dummy pads. Disconnect them.
DUMMY1, 2, 13	3	-	-	Dummy pads. Disconnect them.
DUMMY3-12, 14-19	16	-	-	Dummy pads. Can be connected to the wiring to the COG panel.
DUMMYR1-9	9	-	-	Dummy pads. Available for measuring the COG contact resistance. DUMMYR1 and DUMMYR2 are short-circuited within the chip. DUMMYR3, DUMMYR4 and DUMMYR5 are short-circuited within the chip. DUMMYR6, DUMMYR7, DUMMYR8, and DUMMYR9 are short-circuited within the chip.
VGLDUM1~4	4	-	-	Outputs the internal VGL level. Use as dummy gate output pins.

Patents of dummy pin which is used to fix pin to VCC or GND are pending and granted.

PATENT ISSUED: United States Patent No. 6,323,930
PATENT PENDING: Japanese Application No. 10-514484, Korean Application No. 19997002322
Taiwanese Application No.086103756, (PCT/JP96/02728(W098/12597)

PAD Arrangement

- Chip size : 22.7mm × 2.80mm
- Chip thickness : 550μm (typ.)
- PAD coordinate : PAD center
- Coordinate origin : Chip center

- Au bump size :

(1) 80μm × 80μm
Corner dummy
No.1, No220, No.284, No.937

(2) 54μm×100μm
Input :
No.2 ~ No.219

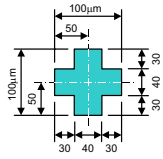
(3) 31μm×77μm
Staggered LCD output side :
No.285 ~ No.936

(4) 77μm×31μm
Staggered LCD output side :
No.221 ~ No.283
No.938 ~ No.1000

- Au bump pitch : See PAD coordinate
- Au bump height :15μm
- Numbers in the figure indicates numbers of PAD coordinate

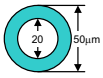
- Alignment mark

(1) Arrangement : 2 places
Coordinate (X,Y) = (-11164.7, 1110.9)
Coordinate (X,Y) = (11164.7, 1110.9)

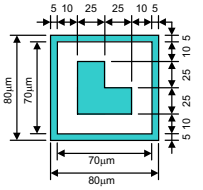


(2-a) Coordinate (X,Y) = (-11124, 1264.6)

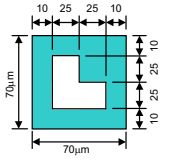
(2-b)Coordinate (X,Y) = (11124, 1264.6)

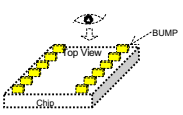


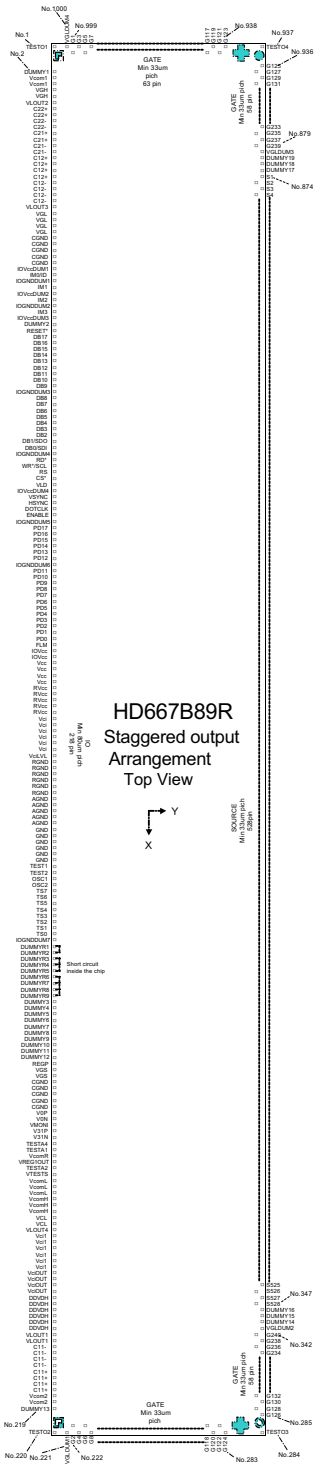
(3-a) Coordinate(X ,Y) = (-11124, -1264.6)



(3-b) Coordinate(X ,Y) = (11124, -1264.6)







PAD Coordinate

(Unit: µm)

pad No.	pad name	X	Y
1	TESTO1	-11214.0	-1264.0
2	DUMMY1	-10888.2	-1254.0
3	Vcom1	-10782.3	-1254.0
4	Vcom1	-10702.1	-1254.0
5	VGH	-10569.1	-1254.0
6	VGH	-10489.0	-1254.0
7	VLOUT2	-10387.5	-1254.0
8	C22+	-10227.4	-1254.0
9	C22+	-10147.2	-1254.0
10	C22-	-10067.1	-1254.0
11	C22-	-9986.9	-1254.0
12	C21+	-9906.8	-1254.0
13	C21+	-9826.6	-1254.0
14	C21-	-9746.5	-1254.0
15	C21-	-9666.3	-1254.0
16	C12+	-9527.9	-1254.0
17	C12+	-9447.7	-1254.0
18	C12+	-9367.6	-1254.0
19	C12+	-9287.4	-1254.0
20	C12-	-9149.0	-1254.0
21	C12-	-9068.9	-1254.0
22	C12-	-8988.7	-1254.0
23	C12-	-8908.6	-1254.0
24	VLOUT3	-8775.6	-1254.0
25	VGL	-8642.6	-1254.0
26	VGL	-8562.4	-1254.0
27	VGL	-8482.3	-1254.0
28	VGL	-8402.1	-1254.0
29	CGND	-8269.1	-1254.0
30	CGND	-8189.0	-1254.0
31	CGND	-8108.8	-1254.0
32	CGND	-8028.7	-1254.0
33	CGND	-7948.5	-1254.0
34	IOVccDUM1	-7815.5	-1254.0
35	IM0/ID	-7698.2	-1254.0
36	IOGNDDUM1	-7553.7	-1254.0
37	IM1	-7436.4	-1254.0
38	IOVccDUM2	-7291.9	-1254.0
39	IM2	-7174.6	-1254.0
40	IOGNDDUM2	-7030.1	-1254.0
41	IM3	-6912.8	-1254.0
42	IOVccDUM3	-6768.3	-1254.0
43	DUMMY2	-6635.3	-1254.0
44	RESET*	-6512.5	-1254.0
45	DB17	-6372.9	-1254.0
46	DB16	-6292.7	-1254.0
47	DB15	-6212.6	-1254.0
48	DB14	-6132.4	-1254.0
49	DB13	-6052.3	-1254.0
50	DB12	-5972.1	-1254.0
51	DB11	-5892.0	-1254.0
52	DB10	-5811.8	-1254.0
53	DB9	-5731.7	-1254.0
54	IOGNDDUM3	-5587.2	-1254.0
55	DB8	-5469.9	-1254.0
56	DB7	-5389.7	-1254.0
57	DB6	-5309.6	-1254.0
58	DB5	-5229.4	-1254.0
59	DB4	-5149.3	-1254.0
60	DB3	-5069.1	-1254.0
61	DB2	-4989.0	-1254.0
62	DB1/SDO	-4908.8	-1254.0
63	DB0/SDI	-4828.7	-1254.0
64	IOGNDDUM4	-4684.2	-1254.0
65	RD*	-4566.9	-1254.0
66	WR*/SCL	-4486.7	-1254.0
67	RS	-4406.6	-1254.0
68	CS*	-4326.4	-1254.0
69	VLD	-4246.3	-1254.0
70	IOVccDUM4	-4101.8	-1254.0
71	VSYNC	-3984.5	-1254.0
72	HSYNC	-3904.3	-1254.0
73	DOTCLK	-3824.2	-1254.0
74	ENABLE	-3744.0	-1254.0
75	IOGNDDUM5	-3599.6	-1254.0
76	PD17	-3482.2	-1254.0
77	PD16	-3402.1	-1254.0
78	PD15	-3321.9	-1254.0
79	PD14	-3241.8	-1254.0
80	PD13	-3161.6	-1254.0
81	PD12	-3081.5	-1254.0
82	IOGNDDUM6	-2937.0	-1254.0
83	PD11	-2819.7	-1254.0
84	PD10	-2739.5	-1254.0
85	PD9	-2659.4	-1254.0
86	PD8	-2579.2	-1254.0
87	PD7	-2499.1	-1254.0
88	PD6	-2418.9	-1254.0
89	PD5	-2338.8	-1254.0
90	PD4	-2258.6	-1254.0
91	PD3	-2178.5	-1254.0
92	PD2	-2098.3	-1254.0
93	PD1	-2018.2	-1254.0
94	PD0	-1938.0	-1254.0
95	FLM	-1857.9	-1254.0
96	IOVcc	-1702.6	-1254.0
97	IOVcc	-1622.4	-1254.0
98	Vcc	-1478.6	-1254.0
99	Vcc	-1398.4	-1254.0
100	Vcc	-1307.4	-1254.0
101	Vcc	-1227.3	-1254.0
102	RVcc	-1083.4	-1254.0
103	RVcc	-1003.3	-1254.0
104	Vcc	-912.3	-1254.0
105	RVcc	-832.1	-1254.0
106	RVcc	-752.0	-1254.0
107	Vci	-608.1	-1254.0
108	Vci	-528.0	-1254.0
109	Vci	-447.8	-1254.0
110	Vci	-367.7	-1254.0
111	Vci	-287.5	-1254.0
112	Vci	-207.4	-1254.0
113	VciLVL	-57.7	-1254.0
114	RGND	86.6	-1254.0
115	RGND	166.8	-1254.0
116	RGND	246.9	-1254.0
117	RGND	327.1	-1254.0
118	RGND	407.2	-1254.0
119	RGND	487.4	-1254.0
120	AGND	620.4	-1254.0
121	AGND	700.5	-1254.0
122	AGND	780.7	-1254.0
123	AGND	860.8	-1254.0
124	AGND	941.0	-1254.0
125	GND	1074.0	-1254.0
126	GND	1154.1	-1254.0
127	GND	1287.1	-1254.0
128	GND	1367.3	-1254.0
129	GND	1447.4	-1254.0
130	GND	1527.6	-1254.0
131	TEST1	1679.2	-1254.0
132	TEST2	1759.4	-1254.0
133	OSC1	1899.0	-1254.0
134	OSC2	1979.2	-1254.0
135	TS7	2118.8	-1254.0
136	TS6	2199.0	-1254.0
137	TS5	2279.1	-1254.0
138	TS4	2359.3	-1254.0
139	TS3	2439.4	-1254.0
140	TS2	2519.6	-1254.0
141	TS1	2599.7	-1254.0
142	TS0	2679.9	-1254.0
143	IOGNDDUM7	2824.3	-1254.0
144	DUMMYR1	2984.5	-1254.0
145	DUMMYR2	3064.6	-1254.0
146	DUMMYR3	3144.8	-1254.0
147	DUMMYR4	3224.9	-1254.0
148	DUMMYR5	3305.1	-1254.0
149	DUMMYR6	3385.2	-1254.0
150	DUMMYR7	3465.4	-1254.0
151	DUMMYR8	3545.5	-1254.0
152	DUMMYR9	3625.7	-1254.0
153	DUMMY3	3705.8	-1254.0
154	DUMMY4	3786.0	-1254.0
155	DUMMY5	3866.1	-1254.0
156	DUMMY6	3946.3	-1254.0
157	DUMMY7	4026.4	-1254.0
158	DUMMY8	4106.6	-1254.0
159	DUMMY9	4186.7	-1254.0
160	DUMMY10	4266.9	-1254.0
161	DUMMY11	4347.0	-1254.0
162	DUMMY12	4427.2	-1254.0
163	REGP	4571.4	-1254.0
164	VGS	4747.5	-1254.0
165	VGS	4873.3	-1254.0
166	CGND	5017.6	-1254.0
167	CGND	5097.8	-1254.0
168	CGND	5177.9	-1254.0
169	CGND	5258.1	-1254.0
170	CGND	5338.2	-1254.0
171	VOP	5482.5	-1254.0
172	V0N	5608.3	-1254.0
173	VMONI	5734.1	-1254.0
174	V31P	5860.0	-1254.0
175	V31N	5985.8	-1254.0
176	TESTA4	6135.5	-1254.0
177	TESTA1	6418.2	-1254.0
178	VcomR	6544.0	-1254.0
179	VREG1OUT	6669.9	-1254.0
180	TESTA2	6795.7	-1254.0
181	VTESTS	6921.5	-1254.0
182	VcomL	7071.2	-1254.0
183	VcomL	7249.7	-1254.0
184	VcomL	7428.2	-1254.0
185	VcomH	7572.1	-1254.0
186	VcomH	7750.6	-1254.0
187	VcomH	7929.1	-1254.0
188	VCL	8067.5	-1254.0
189	VCL	8150.3	-1254.0
190	VLOUT4	8230.4	-1254.0
191	Vci1	8368.9	-1254.0
192	Vci1	8449.0	-1254.0
193	Vci1	8529.2	-1254.0
194	Vci1	8609.3	-1254.0
195	Vci1	8689.5	-1254.0
196	Vci1	8769.6	-1254.0
197	VciOUT	8849.8	-1254.0
198	VciOUT	8929.9	-1254.0
199	VciOUT	9010.1	-1254.0
200	VciOUT	9090.2	-1254.0
201	DDVDH	9234.1	-1254.0
202	DDVDH	9314.2	-1254.0
203	DDVDH	9394.4	-1254.0
204	DDVDH	9474.5	-1254.0
205	DDVDH	9554.7	-1254.0
206	DDVDH	9634.8	-1254.0
207	VLOUT1	9778.7	-1254.0
208	VLOUT1	9858.8	-1254.0
209	C11-	10002.7	-1254.0
210	C11-	10082.8	-1254.0
211	C11-	10163.0	-1254.0
212	C11-	10243.1	-1254.0
213	C11+	10323.3	-1254.0
214	C11+	10403.4	-1254.0
215	C11+	10483.6	-1254.0
216	C11+	10563.7	-1254.0
217	Vcom2	10702.1	-1254.0
218	Vcom2	10782.3	-1254.0
219	DUMMY13	10888.2	-1254.0
220	TESTO2	11214.0	-1264.0
221	VGLDUM1	11215.5	-1118.7
222	G2	11098.5	-1050.6
223	G4	11215.5	-1017.5
224	G6	11098.5	-984.5
225	G8	11215.5	-951.4
226	G10	11098.5	-918.3
227	G12	11215.5	-885.2
228	G14	11098.5	-852.2
229	G16	11215.5	-819.1
230	G18	11098.5	-786.0
231	G20	11215.5	-752.9
232	G22	11098.5	-719.9
233	G24	11215.5	-686.8
234	G26	11098.5	-653.7
235	G28	11215.5	-620.6
236	G30	11098.5	-587.6
237	G32	11215.5	-554.5
238	G34	11098.5	-521.4
239	G36	11215.5	-488.3
240	G38	11098.5	-455.3
241	G40	11215.5	-422.2
242	G42	11098.5	-389.1
243	G44	11215.5	-356.0
244	G46	11098.5	-323.0
245	G48	11215.5	-289.9
246	G50	11098.5	-256.8
247	G52	11215.5	-223.7
248	G54	11098.5	-190.7
249	G56	11215.5	-157.6
250	G58	11098.5	-124.5
251	G60	11215.5	-91.4
252	G62	11098.5	-58.4
253	G64	11215.5	-25.3
254	G66	11098.5	7.8
255	G68	11215.5	40.9
256	G70	11098.5	73.9
257	G72	11215.5	107.0
258	G74	11098.5	140.1
259	G76	11215.5	173.2
260	G78	11098.5	206.2
261	G80	11215.5	239.3
262	G82	11098.5	272.4
263	G84	11215.5	305.5
264	G86	11098.5	338.5
265	G88	11215.5	371.6
266	G90	11098.5	404.7
267	G92	11215.5	437.8
268	G94	11098.5	470.8
269	G96	11215.5	503.9
270	G98	11098.5	537.0
271	G100	11215.5	570.1
272	G102	11098.5	603.1
273	G104	11215.5	636.2
274	G106	11098.5	669.3
275	G108	11215.5	702.4
276	G110	11098.5	735.4
277	G112	11215.5	768.5
278	G114	11098.5	801.6
279	G116	11215.5	834.7
280	G118	11098.5	867.7
281	G120	11215.5	900.8
282	G122	11098.5	933.9
283	G124	11215.5	967.0
284	TESTO3	11214.0	1264.0
285	G126	10958.4	1265.5
286	G128	10925.3	1148.5
287	G130	10892.3	1265.5
288	G132	10859.2	1148.5
289	G134	10826.1	1265.5
290	G136	10793.0	1148.5
291	G138	10760.0	1265.5
292	G140	10726.9	1148.5
293	G142	10693.8	1265.5
294	G144	10660.7	1148.5
295	G146	10627.7	1265.5
296	G148	10594.6	1148.5
297	G150	10561.5	1265.5
298	G152	10528.4	1148.5
299	G154	10495.4	1265.5
300	G156	10462.3	1148.5
301	G158	10429.2	1265.5
302	G160	10396.1	1148.5
303	G162	10363.1	1265.5
304	G164	10330.0	1148.5
305	G166	10296.9	1265.5
306	G168	10263.8	1148.5
307	G170	10230.8	1265.5
308	G172	10197.7	1148.5
309	G174	10164.6	1265.5
310	G176	10131.5	1148.5
311	G178	10098.5	1265.5
312	G180	10065.4	1148.5
313	G182	10032.3	1265.5
314	G184	9999.2	1148.5
315	G186	9966.2	1265.5
316	G188	9933.1	1148.5
317	G190	9900.0	1265.5
318	G192	9866.9	1148.5
319	G194	9833.9	1265.5
320	G196	9800.8	1148.5
321	G198	9767.7	1265.5
322	G200	9734.6	1148.5
323	G202	9701.6	1265.5
324	G204	9668.5	1148.5
325	G206	9635.4	1265.5
326	G208	9602.3	1148.5
327	G210	9569.3	1265.5
328	G212	9536.2	1148.5
329	G214	9503.1	1265.5
330	G216	9470.0	1148.5
331	G218	9437.0	1265.5
332	G220	9403.9	1148.5
333	G222	9370.8	1265.5
334	G224	9337.7	1148.5
335	G226	9304.7	1265.5
336	G228	9271.6	1148.5
337	G230	9238.5	1265.5
338	G232	9205.4	1148.5
339	G234	9172.4	1265.5
340	G236	9139.3	1148.5
341	G238	9106.2	1265.5
342	G240	9073.1	1148.5
343	VGLDUM2	9005.1	1265.5
344	DUMMY14	8937.0	1265.5
345	DUMMY15	8868.9	1265.5
346	DUMMY16	8800.8	1265.5
347	S528	8732.8	1148.5
348	S527	8699.7	1265.5
349	S526	8666.6	1148.5
350	S525	8633.5	1265.5
351	S524	8600.5	1148.5
352	S523	8567.4	1265.5
353	S522	8534.3	1148.5
354	S521	8501.2	1265.5
355	S520	8468.2	1148.5
356	S519	8435.1	1265.5
357	S518	8402.0	1148.5
358	S517	8368.9	1265.5
359	S516	8335.9	1148.5
360	S515	8302.8	1265.5
361	S514	8269.7	1148.5
362	S513	8236.6	1265.5
363	S512	8203.6	1148.5
364	S511	8170.5	1265.5
365	S510	8137.4	1148.5
366	S509	8104.3	1265.5
367	S508	8071.3	1148.5
368	S507	8038.2	1265.5
369	S506	8005.1	1148.5
370	S505	7972.0	1265.5
371	S504	7939.0	1148.5
372	S503	7905.9	1265.5
373	S502	7872.8	1148.5
374	S501	7839.7	1265.5
375	S500	7806.7	1148.5
376	S499	7773.6	1265.5
377	S498	7740.5	1148.5
378	S497	7707.4	1265.5
379	S496	7674.4	1148.5
380	S495	7641.3	1265.5
381	S494	7608.2	1148.5
382	S493	7575.1	1265.5
383	S492	7542.1	1148.5
384	S491	7509.0	1265.5
385	S490	7475.9	1148.5
386	S489	7442.8	1265.5
387	S488	7409.8	1148.5
388	S487	7376.7	1265.5
389	S486	7343.6	1148.5
390	S485	7310.5	1265.5
391	S484	7277.5	1148.5
392	S483	7244.4	1265.5
393	S482	7211.3	1148.5
394	S481	7178.2	1265.5
395	S480	7145.2	1148.5
396	S479	7112.1	1265.5
397	S478	7079.0	1148.5
398	S477	7045.9	1265.5
399	S476	7012.9	1148.5
400	S475	6979.8	1265.5
401	S474	6946.7	1148.5
402	S473	6913.6	1265.5
403	S472	6880.6	1148.5
404	S471	6847.5	1265.5
405	S470	6814.4	1148.5
406	S469	6781.3	1265.5
407	S468	6748.3	1148.5
408	S467	6715.2	1265.5
409	S466	6682.1	1148.5
410	S465	6649.0	1265.5
411	S464	6616.0	1148.5
412	S463	6582.9	1265.5
413	S462	6549.8	1148.5
414	S461	6516.7	1265.5
415	S460	6483.7	1148.5
416	S459	6450.6	1265.5
417	S458	6417.5	1148.5
418	S457	6384.4	1265.5
419	S456	6351.4	1148.5
420	S455	6318.3	1265.5
421	S454	6285.2	1148.5
422	S453	6252.1	1265.5
423	S452	6219.1	1148.5
424	S451	6186.0	1265.5
425	S450	6152.9	1148.5
426	S449	6119.8	1265.5
427	S448	6086.8	1148.5
428	S447	6053.7	1265.5
429	S446	6020.6	1148.5
430	S445	5987.5	1265.5
431	S444	5954.5	1148.5
432	S443	5921.4	1265.5
433	S442	5888.3	1148.5
434	S441	5855.2	1265.5
435	S440	5822.2	1148.5
436	S439	5789.1	1265.5
437	S438	5756.0	1148.5
438	S437	5722.9	1265.5
439	S436	5689.9	1148.5
440	S435	5656.8	1265.5
441	S434	5623.7	1148.5
442	S433	5590.6	1265.5
443	S432	5557.6	1148.5
444	S431	5524.5	1265.5
445	S430	5491.4	1148.5
446	S429	5458.3	1265.5
447	S428	5425.3	1148.5
448	S427	5392.2	1265.5
449	S426	5359.1	1148.5
450	S425	5326.0	1265.5
451	S424	5293.0	1148.5
452	S423	5259.9	1265.5
453	S422	5226.8	1148.5
454	S421	5193.7	1265.5
455	S420	5160.7	1148.5
456	S419	5127.6	1265.5
457	S418	5094.5	1148.5
458	S417	5061.4	1265.5
459	S416	5028.4	1148.5
460	S415	4995.3	1265.5
461	S414	4962.2	1148.5
462	S413	4929.1	1265.5
463	S412	4896.1	1148.5
464	S411	4863.0	1265.5
465	S410	4829.9	1148.5
466	S409	4796.8	1265.5
467	S408	4763.8	1148.5
468	S407	4730.7	1265.5
469	S406	4697.6	1148.5
470	S405	4664.5	1265.5
471	S404	4631.5	1148.5
472	S403	4598.4	1265.5
473	S402	4565.3	1148.5
474	S401	4532.2	1265.5
475	S400	4499.2	1148.5
476	S399	4466.1	1265.5
477	S398	4433.0	1148.5
478	S397	4399.9	1265.5
479	S396	4366.9	1148.5
480	S395	4333.8	1265.5
481	S394	4300.7	1148.5
482	S393	4267.6	1265.5
483	S392	4234.6	1148.5
484	S391	4201.5	1265.5
485	S390	4168.4	1148.5
486	S389	4135.3	1265.5
487	S388	4102.3	1148.5
488	S387	4069.2	1265.5
489	S386	4036.1	1148.5
490	S385	4003.0	1265.5
491	S384	3970.0	1148.5
492	S383	3936.9	1265.5
493	S382	3903.8	1148.5
494	S381	3870.7	1265.5
495	S380	3837.7	1148.5
496	S379	3804.6	1265.5
497	S378	3771.5	1148.5
498	S377	3738.4	1265.5
499	S376	3705.4	1148.5
500	S375	3672.3	1265.5
501	S374	3639.2	1148.5
502	S373	3606.1	1265.5
503	S372	3573.1	1148.5
504	S371	3540.0	1265.5
505	S370	3506.9	1148.5
506	S369	3473.8	1265.5
507	S368	3440.8	1148.5
508	S367	3407.7	1265.5
509	S366	3374.6	1148.5
510	S365	3341.5	1265.5
511	S364	3308.5	1148.5
512	S363	3275.4	1265.5
513	S362	3242.3	1148.5
514	S361	3209.2	1265.5
515	S360	3176.2	1148.5
516	S359	3143.1	1265.5
517	S358	3110.0	1148.5
518	S357	3076.9	1265.5
519	S356	3043.9	1148.5
520	S355	3010.8	1265.5

pad No.	pad name	X	Y
521	S354	2977.7	1148.5
522	S353	2944.6	1265.5
523	S352	2911.6	1148.5
524	S351	2878.5	1265.5
525	S350	2845.4	1148.5
526	S349	2812.3	1265.5
527	S348	2779.3	1148.5
528	S347	2746.2	1265.5
529	S346	2713.1	1148.5
530	S345	2680.0	1265.5
531	S344	2647.0	1148.5
532	S343	2613.9	1265.5
533	S342	2580.8	1148.5
534	S341	2547.7	1265.5
535	S340	2514.7	1148.5
536	S339	2481.6	1265.5
537	S338	2448.5	1148.5
538	S337	2415.4	1265.5
539	S336	2382.4	1148.5
540	S335	2349.3	1265.5
541	S334	2316.2	1148.5
542	S333	2283.1	1265.5
543	S332	2250.1	1148.5
544	S331	2217.0	1265.5
545	S330	2183.9	1148.5
546	S329	2150.8	1265.5
547	S328	2117.8	1148.5
548	S327	2084.7	1265.5
549	S326	2051.6	1148.5
550	S325	2018.5	1265.5
551	S324	1985.5	1148.5
552	S323	1952.4	1265.5
553	S322	1919.3	1148.5
554	S321	1886.2	1265.5
555	S320	1853.2	1148.5
556	S319	1820.1	1265.5
557	S318	1787.0	1148.5
558	S317	1753.9	1265.5
559	S316	1720.9	1148.5
560	S315	1687.8	1265.5
561	S314	1654.7	1148.5
562	S313	1621.6	1265.5
563	S312	1588.6	1148.5
564	S311	1555.5	1265.5
565	S310	1522.4	1148.5
566	S309	1489.3	1265.5
567	S308	1456.3	1148.5
568	S307	1423.2	1265.5
569	S306	1390.1	1148.5
570	S305	1357.0	1265.5
571	S304	1324.0	1148.5
572	S303	1290.9	1265.5
573	S302	1257.8	1148.5
574	S301	1224.7	1265.5
575	S300	1191.7	1148.5
576	S299	1158.6	1265.5
577	S298	1125.5	1148.5
578	S297	1092.4	1265.5
579	S296	1059.4	1148.5
580	S295	1026.3	1265.5
581	S294	993.2	1148.5
582	S293	960.1	1265.5
583	S292	927.1	1148.5
584	S291	894.0	1265.5
585	S290	860.9	1148.5
586	S289	827.8	1265.5
587	S288	794.8	1148.5
588	S287	761.7	1265.5
589	S286	728.6	1148.5
590	S285	695.5	1265.5
591	S284	662.5	1148.5
592	S283	629.4	1265.5
593	S282	596.3	1148.5
594	S281	563.2	1265.5
595	S280	530.2	1148.5
596	S279	497.1	1265.5
597	S278	464.0	1148.5
598	S277	430.9	1265.5
599	S276	397.9	1148.5
600	S275	364.8	1265.5
601	S274	331.7	1148.5
602	S273	298.6	1265.5
603	S272	265.6	1148.5
604	S271	232.5	1265.5
605	S270	199.4	1148.5
606	S269	166.3	1265.5
607	S268	133.3	1148.5
608	S267	100.2	1265.5
609	S266	67.1	1148.5
610	S265	34.0	1265.5
611	S264	-34.0	1148.5
612	S263	-67.1	1265.5
613	S262	-100.2	1148.5
614	S261	-133.3	1265.5
615	S260	-166.3	1148.5
616	S259	-199.4	1265.5
617	S258	-232.5	1148.5
618	S257	-265.6	1265.5
619	S256	-298.6	1148.5
620	S255	-331.7	1265.5
621	S254	-364.8	1148.5
622	S253	-397.9	1265.5
623	S252	-430.9	1148.5
624	S251	-464.0	1265.5
625	S250	-497.1	1148.5
626	S249	-530.2	1265.5
627	S248	-563.2	1148.5
628	S247	-596.3	1265.5
629	S246	-629.4	1148.5
630	S245	-662.5	1265.5
631	S244	-695.5	1148.5
632	S243	-728.6	1265.5
633	S242	-761.7	1148.5
634	S241	-794.8	1265.5
635	S240	-827.8	1148.5
636	S239	-860.9	1265.5
637	S238	-894.0	1148.5
638	S237	-927.1	1265.5
639	S236	-960.1	1148.5
640	S235	-993.2	1265.5
641	S234	-1026.3	1148.5
642	S233	-1059.4	1265.5
643	S232	-1092.4	1148.5
644	S231	-1125.5	1265.5
645	S230	-1158.6	1148.5
646	S229	-1191.7	1265.5
647	S228	-1224.7	1148.5
648	S227	-1257.8	1265.5
649	S226	-1290.9	1148.5
650	S225	-1324.0	1265.5

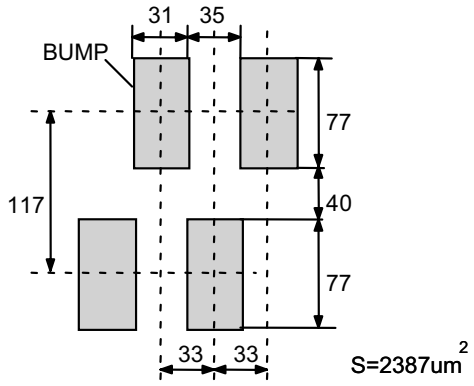
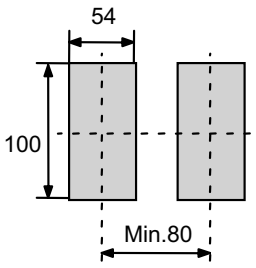
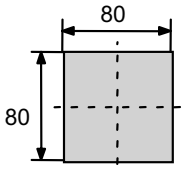
pad No.	pad name	X	Y
651	S224	-1357.0	1148.5
652	S223	-1390.1	1265.5
653	S222	-1423.2	1148.5
654	S221	-1456.3	1265.5
655	S220	-1489.3	1148.5
656	S219	-1522.4	1265.5
657	S218	-1555.5	1148.5
658	S217	-1588.6	1265.5
659	S216	-1621.6	1148.5
660	S215	-1654.7	1265.5
661	S214	-1687.8	1148.5
662	S213	-1720.9	1265.5
663	S212	-1753.9	1148.5
664	S211	-1787.0	1265.5
665	S210	-1820.1	1148.5
666	S209	-1853.2	1265.5
667	S208	-1886.2	1148.5
668	S207	-1919.3	1265.5
669	S206	-1952.4	1148.5
670	S205	-1985.5	1265.5
671	S204	-2018.5	1148.5
672	S203	-2051.6	1265.5
673	S202	-2084.7	1148.5
674	S201	-2117.8	1265.5
675	S200	-2150.8	1148.5
676	S199	-2183.9	1265.5
677	S198	-2217.0	1148.5
678	S197	-2250.1	1265.5
679	S196	-2283.1	1148.5
680	S195	-2316.2	1265.5
681	S194	-2349.3	1148.5
682	S193	-2382.4	1265.5
683	S192	-2415.4	1148.5
684	S191	-2448.5	1265.5
685	S190	-2481.6	1148.5
686	S189	-2514.7	1265.5
687	S188	-2547.7	1148.5
688	S187	-2580.8	1265.5
689	S186	-2613.9	1148.5
690	S185	-2647.0	1265.5
691	S184	-2680.0	1148.5
692	S183	-2713.1	1265.5
693	S182	-2746.2	1148.5
694	S181	-2779.3	1265.5
695	S180	-2812.3	1148.5
696	S179	-2845.4	1265.5
697	S178	-2878.5	1148.5
698	S177	-2911.6	1265.5
699	S176	-2944.6	1148.5
700	S175	-2977.7	1265.5
701	S174	-3010.8	1148.5
702	S173	-3043.9	1265.5
703	S172	-3076.9	1148.5
704	S171	-3110.0	1265.5
705	S170	-3143.1	1148.5
706	S169	-3176.2	1265.5
707	S168	-3209.2	1148.5
708	S167	-3242.3	1265.5
709	S166	-3275.4	1148.5
710	S165	-3308.5	1265.5
711	S164	-3341.5	1148.5
712	S163	-3374.6	1265.5
713	S162	-3407.7	1148.5
714	S161	-3440.8	1265.5
715	S160	-3473.8	1148.5
716	S159	-3506.9	1265.5
717	S158	-3540.0	1148.5
718	S157	-3573.1	1265.5
719	S156	-3606.1	1148.5
720	S155	-3639.2	1265.5
721	S154	-3672.3	1148.5
722	S153	-3705.4	1265.5
723	S152	-3738.4	1148.5
724	S151	-3771.5	1265.5
725	S150	-3804.6	1148.5
726	S149	-3837.7	1265.5
727	S148	-3870.7	1148.5
728	S147	-3903.8	1265.5
729	S146	-3936.9	1148.5
730	S145	-3970.0	1265.5
731	S144	-4003.0	1148.5
732	S143	-4036.1	1265.5
733	S142	-4069.2	1148.5
734	S141	-4102.3	1265.5
735	S140	-4135.3	1148.5
736	S139	-4168.4	1265.5
737	S138	-4201.5	1148.5
738	S137	-4234.6	1265.5
739	S136	-4267.6	1148.5
740	S135	-4300.7	1265.5
741	S134	-4333.8	1148.5
742	S133	-4366.9	1265.5
743	S132	-4399.9	1148.5
744	S131	-4433.0	1265.5
745	S130	-4466.1	1148.5
746	S129	-4499.2	1265.5
747	S128	-4532.2	1148.5
748	S127	-4565.3	1265.5
749	S126	-4598.4	1148.5
750	S125	-4631.5	1265.5
751	S124	-4664.5	1148.5
752	S123	-4697.6	1265.5
753	S122	-4730.7	1148.5
754	S121	-4763.8	1265.5
755	S120	-4796.8	1148.5
756	S119	-4829.9	1265.5
757	S118	-4863.0	1148.5
758	S117	-4896.1	1265.5
759	S116	-4929.1	1148.5
760	S115	-4962.2	1265.5
761	S114	-4995.3	1148.5
762	S113	-5028.4	1265.5
763	S112	-5061.4	1148.5
764	S111	-5094.5	1265.5
765	S110	-5127.6	1148.5
766	S109	-5160.7	1265.5
767	S108	-5193.7	1148.5
768	S107	-5226.8	1265.5
769	S106	-5259.9	1148.5
770	S105	-5293.0	1265.5
771	S104	-5326.0	1148.5
772	S103	-5359.1	1265.5
773	S102	-5392.2	1148.5
774	S101	-5425.3	1265.5
775	S100	-5458.3	1148.5
776	S99	-5491.4	1265.5
777	S98	-5524.5	1148.5
778	S97	-5557.6	1265.5
779	S96	-5590.6	1148.5
780	S95	-5623.7	1265.5

pad No.	pad name	X	Y
781	S94	-5656.8	1148.5
782	S93	-5689.9	1265.5
783	S92	-5722.9	1148.5
784	S91	-5756.0	1265.5
785	S90	-5789.1	1148.5
786	S89	-5822.2	1265.5
787	S88	-5855.2	1148.5
788	S87	-5888.3	1265.5
789	S86	-5921.4	1148.5
790	S85	-5954.5	1265.5
791	S84	-5987.5	1148.5
792	S83	-6020.6	1265.5
793	S82	-6053.7	1148.5
794	S81	-6086.8	1265.5
795	S80	-6119.8	1148.5
796	S79	-6152.9	1265.5
797	S78	-6186.0	1148.5
798	S77	-6219.1	1265.5
799	S76	-6252.1	1148.5
800	S75	-6285.2	1265.5
801	S74	-6318.3	1148.5
802	S73	-6351.4	1265.5
803	S72	-6384.4	1148.5
804	S71	-6417.5	1265.5
805	S70	-6450.6	1148.5
806	S69	-6483.7	1265.5
807	S68	-6516.7	1148.5
808	S67	-6549.8	1265.5
809	S66	-6582.9	1148.5
810	S65	-6616.0	1265.5
811	S64	-6649.0	1148.5
812	S63	-6682.1	1265.5
813	S62	-6715.2	1148.5
814	S61	-6748.3	1265.5
815	S60	-6781.3	1148.5
816	S59	-6814.4	1265.5
817	S58	-6847.5	1148.5
818	S57	-6880.6	1265.5
819	S56	-6913.6	1148.5
820	S55	-6946.7	1265.5
821	S54	-6979.8	1148.5
822	S53	-7012.9	1265.5
823	S52	-7045.9	1148.5
824	S51	-7079.0	1265.5
825	S50	-7112.1	1148.5
826	S49	-7145.2	1265.5
827	S48	-7178.2	1148.5
828	S47	-7211.3	1265.5
829	S46	-7244.4	1148.5
830	S45	-7277.5	1265.5
831	S44	-7310.5	1148.5
832	S43	-7343.6	1265.5
833	S42	-7376.7	1148.5
834	S41	-7409.8	1265.5
835	S40	-7442.8	1148.5
836	S39	-7475.9	1265.5
837	S38	-7509.0	1148.5
838	S37	-7542.1	1265.5
839	S36	-7575.1	1148.5
840	S35	-7608.2	1265.5
841	S34	-7641.3	1148.5
842	S33	-7674.4	1265.5
843	S32	-7707.4	1148.5
844	S31	-7740.5	1265.5
845	S30	-7773.6	1148.5
846	S29	-7806.7	1265.5
847	S28	-7839.7	1148.5
848	S27	-7872.8	1265.5
849	S26	-7905.9	1148.5
850	S25	-7939.0	1265.5
851	S24	-7972.0	1148.5
852	S23	-8005.1	1265.5
853	S22	-8038.2	1148.5
854	S21	-8071.3	1265.5
855	S20	-8104.3	1148.5
856	S19	-8137.4	1265.5
857	S18	-8170.5	1148.5
858	S17	-8203.6	1265.5
859	S16	-8236.6	1148.5
860	S15	-8269.7	1265.5
861	S14	-8302.8	1148.5
862	S13	-8335.9	1265.5
863	S12	-8368.9	1148.5
864	S11	-8402.0	1265.5
865	S10	-8435.1	1148.5
866	S9	-8468.2	1265.5
867	S8	-8501.2	1148.5
868	S7	-8534.3	1265.5
869	S6	-8567.4	1148.5
870	S5	-8600.5	1265.5
871	S4	-8633.5	1148.5
872	S3	-8666.6	1265.5
873	S2	-8699.7	1148.5
874	S1	-8732.8	1265.5
875	DUMMY17	-8800.8	1265.5
876	DUMMY18	-8868.9	1265.5
877	DUMMY19	-8937.0	1265.5
878	VGLDUM3	-9005.1	1265.5
879	G239	-9073.1	1148.5
880	G237	-9106.2	1265.5
881	G235	-9139.3	1148.5
882	G233	-9172.4	1265.5
883	G231	-9205.4	1148.5
884	G229	-9238.5	1265.5
885	G227	-9271.6	1148.5
886	G225	-9304.7	1265.5
887	G223	-9337.7	1148.5
888	G221	-9370.8	1265.5
889	G219	-9403.9	1148.5
890	G217	-9437.0	1265.5
891	G215	-9470.0	1148.5
892	G213	-9503.1	1265.5
893	G211	-9536.2	1148.5
894	G209	-9569.3	1265.5
895	G207	-9602.3	1148.5
896	G205	-9635.4	1265.5
897	G203	-9668.5	1148.5
898	G201	-9701.6	1265.5
899	G199	-9734.6	1148.5
900	G197	-9767.7	1265.5
901	G195	-9800.8	1148.5
902	G193	-9833.9	1265.5
903	G191	-9866.9	1148.5
904	G189	-9900.0	1265.5
905	G187	-9933.1	1148.5
906	G185	-9966.2	1265.5
907	G183	-9999.2	1148.5
908	G181	-10032.3	1265.5
909	G179	-10065.4	1148.5
910	G177	-10098.5	1265.5

pad No.	pad name	X	Y
911	G175	-10131.5	1148.5
912	G173	-10164.6	1265.5
913	G171	-10197.7	1148.5
914	G169	-10230.8	1265.5
915	G167	-10263.8	1148.5
916	G165	-10296.9	1265.5
917	G163	-10330.0	1148.5
918	G161	-10363.1	1265.5
919	G159	-10396.1	1148.5
920	G157	-10429.2	1265.5
921	G155	-10462.3	1148.5
922	G153	-10495.4	1265.5
923	G151	-10528.4	1148.5
924	G149	-10561.5	1265.5
925	G147	-10594.6	1148.5
926	G145	-10627.7	1265.5
927	G143	-10660.7	1148.5
928	G141	-10693.8	1265.5
929	G139	-10726.9	1148.5
930	G137	-10760.0	1265.5
931	G135	-10793.0	1148.5
932	G133	-10826.1	1265.5
933	G131	-10859.2	1148.5
934	G129	-10892.3	1265.5
935	G127	-10925.3	1148.5
936	G125	-10958.4	1265.5
937	TESTO4	-11214.0	1264.0
938	G123	-11215.5	967.0
939	G121	-11098.5	933.9
940	G119	-11215.5	900.8
941	G117	-11098.5	867.7
942	G115	-11215.5	834.7
943	G113	-11098.5	801.6
944	G111	-11215.5	768.5
945	G109	-11098.5	735.4
946	G107	-11215.5	702.4
947	G105	-11098.5	669.3
948	G103	-11215.5	636.2
949	G101	-11098.5	603.1
950	G99	-11215.5	570.1
951	G97	-11098.5	537.0
952	G95	-11215.5	503.9
953	G93	-11098.5	470.8
954	G91	-11215.5	437.8
955	G89	-11098.5	404.7
956	G87	-11215.5	371.6
957	G85	-11098.5	338.5
958	G83	-11215.5	305.5
959	G81	-11098.5	272.4
960	G79	-11215.5	239.3
961	G77	-11098.5	206.2
962	G75	-11215.5	173.2
963	G73	-11098.5	140.1
964	G71	-11215.5	107.0
965	G69	-11098.5	73.9
966	G67	-11215.5	40.9
967	G65	-11098.5	7.8
968	G63	-11215.5	-25.3
969	G61	-11098.5	-58.4
970	G59	-11215.5	-91.4
971	G57	-11098.5	-124.5
972	G55	-11215.5	-157.6
973	G53	-11098.5	-190.7
974	G51	-11215.5	-223.7
975	G49	-11098.5	-256.8
976	G47	-11215.5	-289.9
977	G45	-11098.5	-323.0
978	G43	-11215.5	-356.0
979	G41	-11098.5	-389.1
980	G39	-11215.5	-422.2
981	G37	-11098.5	-455.3
982	G35	-11215.5	-488.3
983	G33	-11098.5	-521.4
984	G31	-11215.5	-554.5
985	G29	-11098.5	-587.6
986	G27	-11215.5	-620.6
987	G25	-11098.5	-653.7
988	G23	-11215.5	-686.8
989	G21	-11098.5	-719.9
990	G19	-11215.5	-752.9
991	G17	-11098.5	-786.0
992	G15	-11215.5	-819.1
993	G13	-11098.5	-852.2
994	G11	-11215.5	-885.2
995	G9	-11098.5	-918.3
996	G7	-11215.5	-951.4
997	G5	-11098.5	-984.5
998	G3	-11215.5	-1017.5
999	G1	-11098.5	-1050.6
1000	VGLDUM4	-11215.5	-1118.7

Alignment mark	x	y
L type (positive)	-11124.0	-1264.6
L type (negative)	11124.0	-1264.6
Circle (positive)	-11124.0	1264.6
Circle (negative)	11124.0	1264.6
Cross	-11164.7	1110.9
	11164.7	1110.9

BUMP Arrangement

S1 ~ S528 G1 ~ G240	 S=2387um^2 Unit: um
I/O pins	 S=5400um^2 Unit: um
TESTO1 ~ 4	 S=6400um^2 Unit: um

Block Function

1. System Interface

The HD66789R has 2 system high-speed interfaces: an 80-system interface with18, 16, 9, and 8-bit bus, and a Serial Peripheral Interface (SPI). An interface mode is selected by setting the IM3-0 pins.

The HD66789R incorporates a 16-bit index register (IR), 18-bit write-data register (WDR) and read-data register (RDR). The IR is a register to store index information of the control registers and the GRAM. The WDR is a register to temporarily store data that are written to the control registers and the internal GRAM. The RDR is a register to temporarily store data read from GRAM. Data from the MPU to be written to the internal GRAM are once written to the WDR and then automatically written to the GRAM in the internal operation. Data are read through the RDR from the internal GRAM. This means the first read operation is a dummy read operation and the GRAM data are read out from the second read operation.

The instruction execution time other than starting oscillator is 0 clock cycle, enabling to write instructions consecutively.

Table 2 Register Selection (8/9/16/18-bit Parallel Interface)

80-system Bus			Function
WR*	RD*	RS	
0	1	0	Write an index to the IR
1	0	0	Read an internal status
0	1	1	Write to control registers or GRAM through the WDR
1	0	1	Read from GRAM through the RDR

Table 3 Register Selection (Serial Peripheral Interface)

Start bytes		
R/W	RS	Function
0	0	Write an index to the IR
1	0	Read an internal status
0	1	Write to a control register and GRAM through the WDR
1	1	Read from GRAM through the RDR

2. External Display Interface

The HD66789R incorporates the RGB and VSYNC interfaces as an external interface for displaying moving pictures. When the RGB-I/F is selected, the display operation is synchronized with externally supplied signals, VSYNC, HSYNC, and DOTCLK. The display data (PD17-0) are written in synchronization with these signals according to the ENABLE signal to prevent flicker on display while rewriting the display data.

In VSYNC-I/F mode, the display operation is synchronized with internal clocks except the frame synchronization that is synchronized with VSYNC signal. Display data are written to the internal GRAM through the system interface. In this case, there are constraints in the speed and methods of rewriting the RAM data. For details, see the "External Display Interface" section.

The HD66789R allows switching between the external display interface and the system interface through the instruction to select an optimum interface for the kind of display (still or moving picture). All display data that are written through the RGB-I/F are written to the internal GRAM so that data are transferred only when rewriting the screens. This contributes to reducing power consumption during moving picture display.

3. Bit Operations

The HD66789R supports a function to write data selectively in the unit of bits, such as a write data mask function and a logical operation and conditional rewrite function in which GRAM write data are compared with the values in the compare register. For details, see "Graphics Operation Functions".

4. Address Counter (AC)

The address counter (AC) gives an address to the GRAM. When an instruction to set a RAM address to the AC is written to the index register, the address information is sent from the index register to the AC. After writing data to GRAM, the AC is automatically updated plus or minus 1. The window address function enables to write data only in the rectangular area of GRAM specified with the window addresses.

5. Graphics RAM (GRAM)

The GRAM is graphics RAM that stores bit-pattern data of 176 x 240 dots in the unit of 18 bits per pixel. The HD66789R's RAM has a capacity of 95,040 bytes (176 x240x 18/8).

6. Grayscale Power Supply Voltage Generating Circuit

The grayscale voltage generating circuit generates a liquid crystal drive voltage according to the grayscale data set in the γ-correction register, enabling display in 262,144 colors. For details, see the "γ-Correction Register" section.

7. Timing Generator

The timing generator generates a timing signal for the operations of internal circuits such as GRAM. The timing for the display operation such as a RAM read operation and the internal operation timing such as the access from the MPU are generated in a way that the two will not interfere with each other. The FLM signal is generated internally and output from the timing generator.

8. Oscillator (OSC)

The HD66789R provides RC oscillation from the external oscillation-resistor connected between the OSC1 and OSC2 pins. An appropriate oscillation frequency for the operating voltage, the size of the display, and the frame frequency can be obtained by adjusting the value of the external resistor. Clock pulses can be supplied externally. The RC oscillation is halted during the standby mode to reduce current consumption. For details, see the "Oscillator" section.

9. LCD Driver Circuit

The LCD driver circuit of HD66789R consists of a 528-output source driver (S1~S528) and a 240-output gate driver (G1~G240). Display pattern data are latched when data of 528 bits are sent. The latched data controls the source driver and generates a drive waveform. The shift direction of 528-bit outputs from the source driver is changeable with the SS bit. The shift direction of outputs from the gate lines is changeable with the GS bit. The scan mode by the gate driver is changeable with the SM bit. Select appropriate shift direction and scan mode according to the assembling method.

10. LCD Drive Power Supply Circuit

The LCD drive power supply circuit of the HD66789R generates voltage levels V0P, V0N, V31P, V31N, VGH, VGL and Vcom, which are required for driving LCDs.

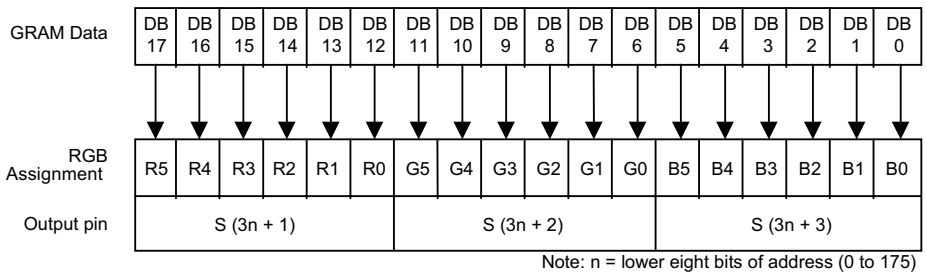
GRAM Address MAP

GRAM address and display panel position (SS =”0”)

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	PD 17 … 0			PD 17 … 0			PD 17 … 0			PD 17 … 0				PD 17 … 0			PD 17 … 0			PD 17 … 0			PD 17 … 0		
G1	G240	"0000"H			"0001"H			"0002"H			"0003"H			.....	"00AC"H			"00AD"H			"00AE"H			"00AF"H		
G2	G239	"0100"H			"0101"H			"0102"H			"0103"H			.....	"01AC"H			"01AD"H			"01AE"H			"01AF"H		
G3	G238	"0200"H			"0201"H			"0202"H			"0203"H			.....	"02AC"H			"02AD"H			"02AE"H			"02AF"H		
G4	G237	"0300"H			"0301"H			"0302"H			"0303"H			.....	"03AC"H			"03AD"H			"03AE"H			"03AF"H		
G5	G236	"0400"H			"0401"H			"0402"H			"0403"H			.....	"04AC"H			"04AD"H			"04AE"H			"04AF"H		
G6	G235	"0500"H			"0501"H			"0502"H			"0503"H			.....	"05AC"H			"05AD"H			"05AE"H			"05AF"H		
G7	G234	"0600"H			"0601"H			"0602"H			"0603"H			.....	"06AC"H			"06AD"H			"06AE"H			"06AF"H		
G8	G233	"0700"H			"0701"H			"0702"H			"0703"H			.....	"07AC"H			"07AD"H			"07AE"H			"07AF"H		
G9	G232	"0800"H			"0801"H			"0802"H			"0803"H			.....	"08AC"H			"08AD"H			"08AE"H			"08AF"H		
G10	G231	"0900"H			"0901"H			"0902"H			"0903"H			.....	"09AC"H			"09AD"H			"09AE"H			"09AF"H		
G11	G230	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0AAC"H			"0AAD"H			"0AAE"H			"0AAF"H		
G12	G229	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0BAC"H			"0BAD"H			"0BAE"H			"0BAF"H		
G13	G228	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0CAC"H			"0CAD"H			"0CAE"H			"0CAF"H		
G14	G227	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0DAC"H			"0DAD"H			"0DAE"H			"0DAF"H		
G15	G226	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0EAC"H			"0EAD"H			"0EAE"H			"0EAF"H		
G16	G225	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0FAC"H			"0FAD"H			"0FAE"H			"0FAF"H		
G17	G224	"1000"H			"1001"H			"1002"H			"1003"H			.....	"10AC"H			"10AD"H			"10AE"H			"10AF"H		
G18	G223	"1100"H			"1101"H			"1102"H			"1103"H			.....	"11AC"H			"11AD"H			"11AE"H			"11AF"H		
G19	G222	"1200"H			"1201"H			"1202"H			"1203"H			.....	"12AC"H			"12AD"H			"12AE"H			"12AF"H		
G20	G221	"1300"H			"1301"H			"1302"H			"1303"H			.....	"13AC"H			"13AD"H			"13AE"H			"13AF"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G233	G8	"0800"H			"0801"H			"0802"H			"0803"H			.....	"E8AC"H			"E8AD"H			"E8AE"H			"E8AF"H		
G234	G7	"0900"H			"0901"H			"0902"H			"0903"H			.....	"E9AC"H			"E9AD"H			"E9AE"H			"E9AF"H		
G235	G6	"EA00"H			"EA01"H			"EA02"H			"EA03"H			.....	"EAAC"H			"EAAD"H			"EAAE"H			"EAAF"H		
G236	G5	"EB00"H			"EB01"H			"EB02"H			"EB03"H			.....	"EBAC"H			"EBAD"H			"EBAE"H			"EBAF"H		
G237	G4	"EC00"H			"EC01"H			"EC02"H			"EC03"H			.....	"ECAC"H			"ECAD"H			"ECAE"H			"ECAF"H		
G238	G3	"ED00"H			"ED01"H			"ED02"H			"ED03"H			.....	"EDAC"H			"EDAD"H			"EDAE"H			"EDAF"H		
G239	G2	"EE00"H			"EE01"H			"EE02"H			"EE03"H			.....	"EEAC"H			"EEAD"H			"EEAE"H			"EEAF"H		
G240	G1	"EF00"H			"EF01"H			"EF02"H			"EF03"H			.....	"EFAC"H			"EFAD"H			"EFAE"H			"EFAF"H		

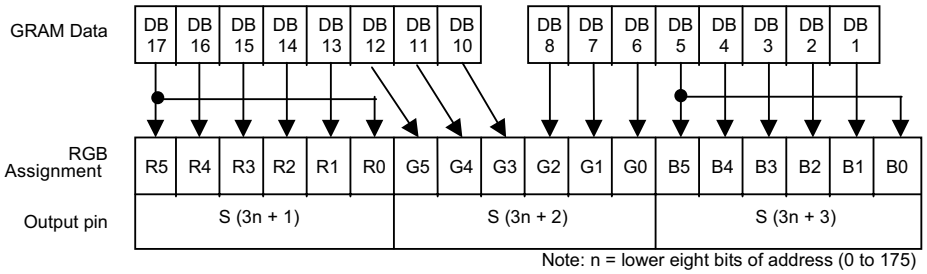
GRAM data and display data: system interface (SS = "0", BGR = "0")

80-System 18-Bit Interface



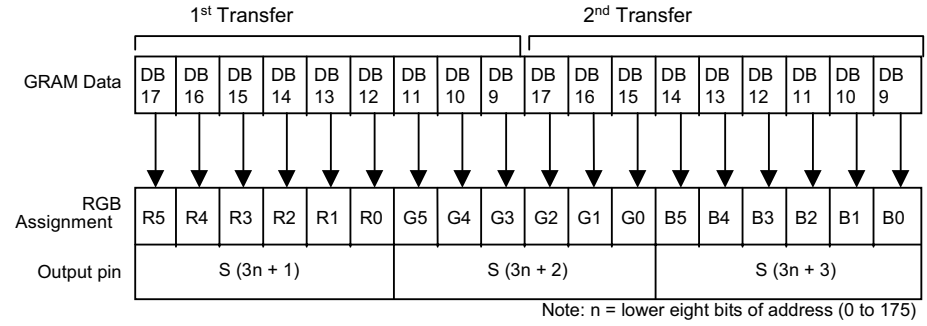
Note: n = lower eight bits of address (0 to 175)

80-System 16-Bit Interface



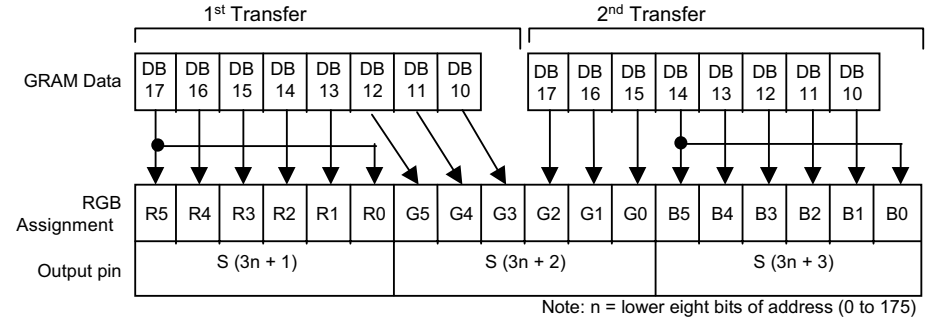
Note: n = lower eight bits of address (0 to 175)

80-System 9-Bit Interface



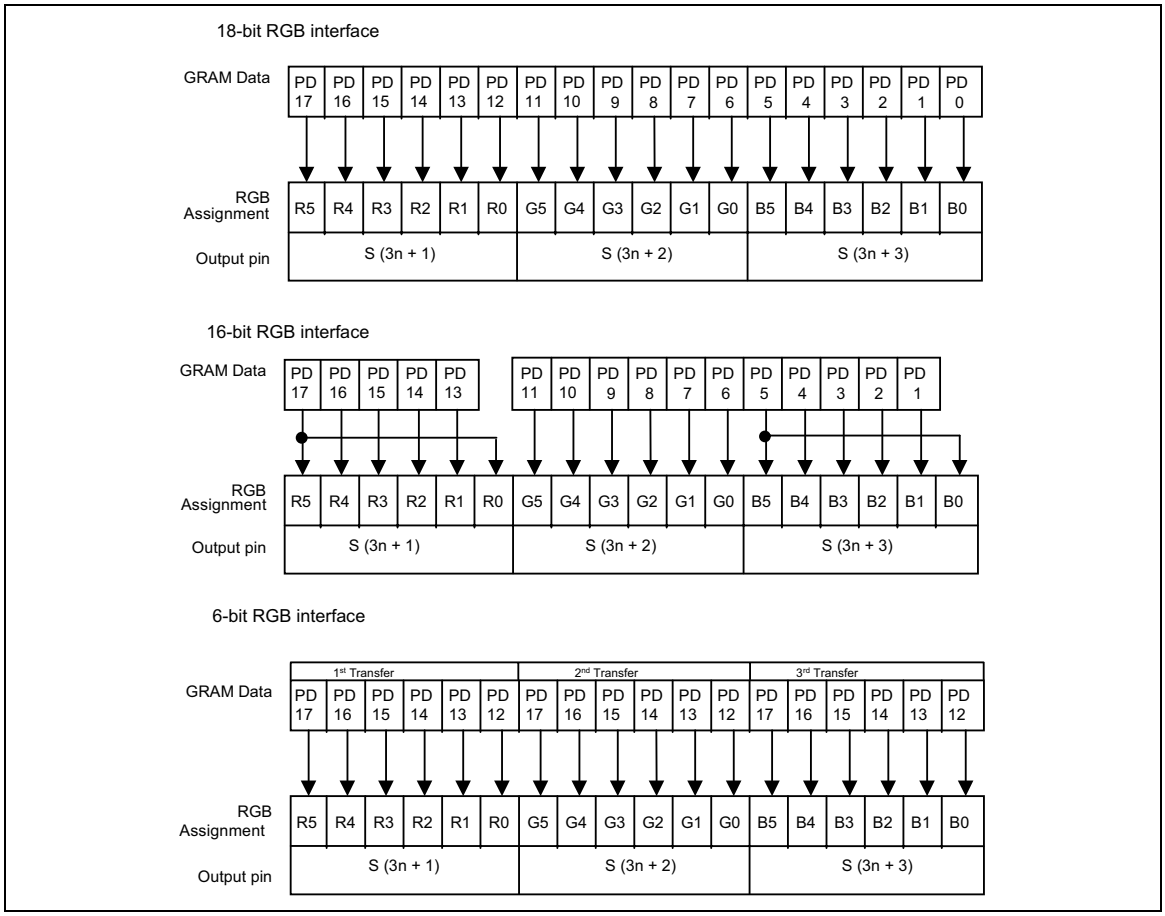
Note: n = lower eight bits of address (0 to 175)

80-System 8-Bit Interface/SPI (2 transfers/pixel)



Note: n = lower eight bits of address (0 to 175)

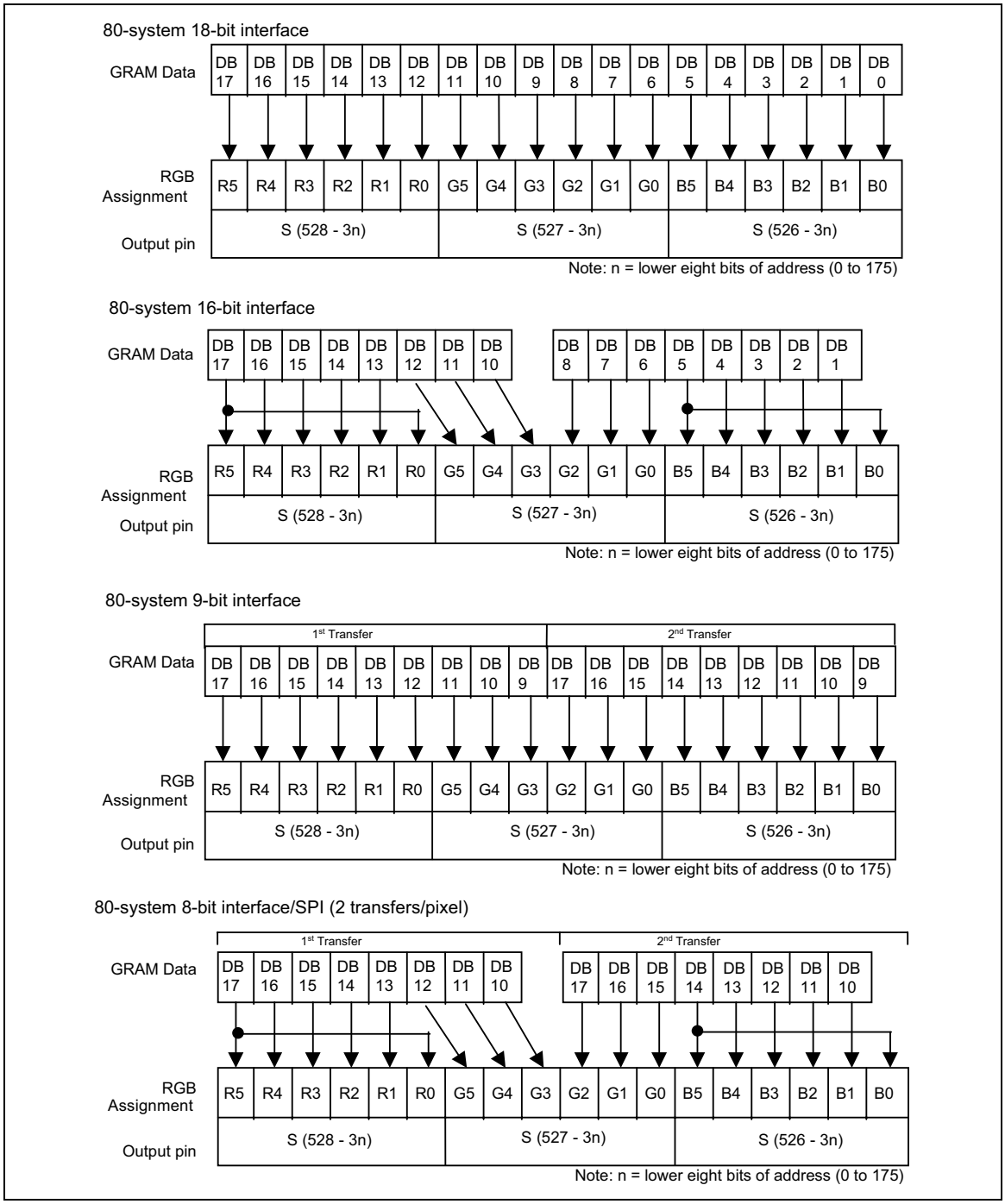
GRAM data and display data: RGB interface (SS = “0”, BGR = “0”)



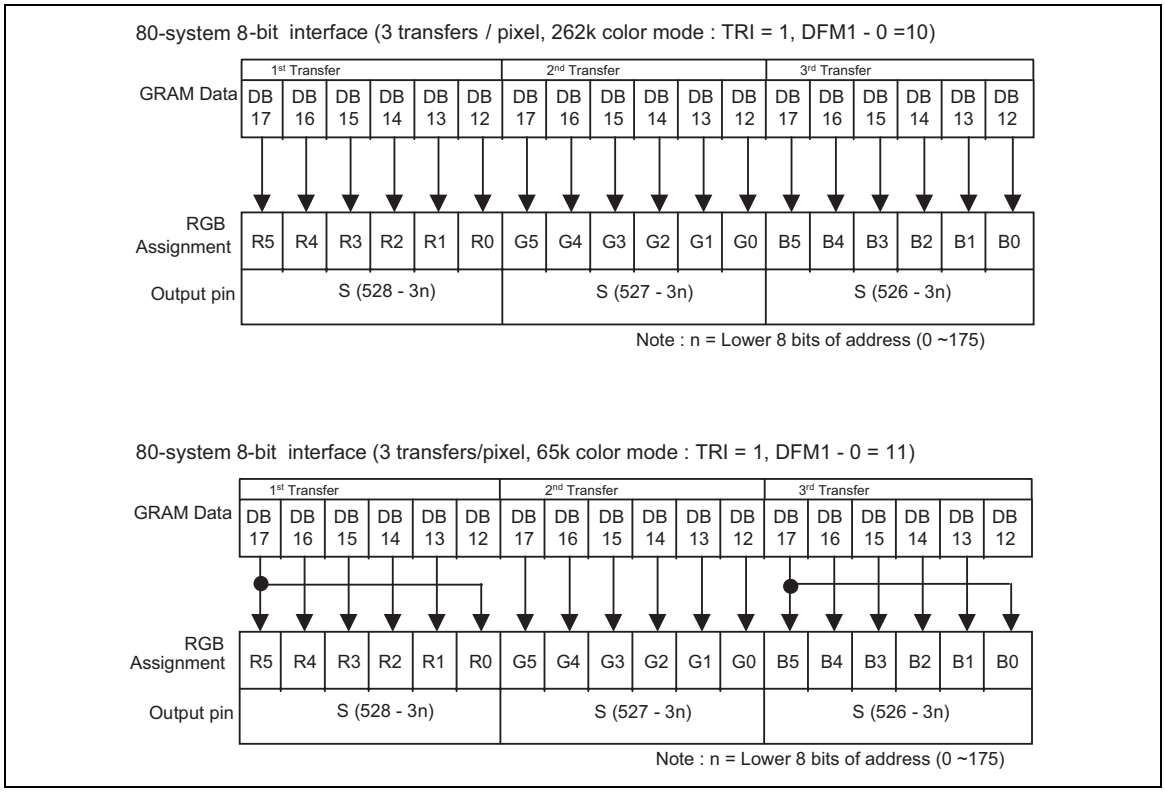
GRAM address and display panel position (SS ="1", BGR "1")

S/G pins		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S517	S518	S519	S520	S521	S522	S523	S524	S525	S526	S527	S528
GS=0	GS=1	PD 17 … 0			PD 17 … 0			PD 17 … 0			PD 17 … 0				PD 17 … 0			PD 17 … 0			PD 17 … 0			PD 17 … 0		
G1	G240	"00AF"H			"00AE"H			"00AD"H			"00AC"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G239	"01AF"H			"01AE"H			"01AD"H			"01AC"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G238	"02AF"H			"02AE"H			"02AD"H			"02AC"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G237	"03AF"H			"03AE"H			"03AD"H			"03AC"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G236	"04AF"H			"04AE"H			"04AD"H			"04AC"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G235	"05AF"H			"05AE"H			"05AD"H			"05AC"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G234	"06AF"H			"06AE"H			"06AD"H			"06AC"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G233	"07AF"H			"07AE"H			"07AD"H			"07AC"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G232	"08AF"H			"08AE"H			"08AD"H			"08AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G231	"09AF"H			"09AE"H			"09AD"H			"09AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G230	"0AAF"H			"0AAE"H			"0AAD"H			"0AAC"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G229	"0BAF"H			"0BAE"H			"0BAD"H			"0BAC"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G228	"0CAF"H			"0CAE"H			"0CAD"H			"0CAC"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G227	"0DAF"H			"0DAE"H			"0DAD"H			"0DAC"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G226	"0EAF"H			"0EAE"H			"0EAD"H			"0EAC"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G225	"0FAF"H			"0FAE"H			"0FAD"H			"0FAC"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G224	"10AF"H			"10AE"H			"10AD"H			"10AC"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G223	"11AF"H			"11AE"H			"11AD"H			"11AC"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G222	"12AF"H			"12AE"H			"12AD"H			"12AC"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G221	"13AF"H			"13AE"H			"13AD"H			"13AC"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮	⋮			⋮			⋮			⋮				⋮			⋮			⋮			⋮		
G233	G8	"E8AF"H			"E8AE"H			"E8AD"H			"E8AC"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G234	G7	"E9AF"H			"E9AE"H			"E9AD"H			"E9AC"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G235	G6	"EAAF"H			"EAAE"H			"EAAD"H			"EAAC"H			.....	"EA03"H			"EA02"H			"EA01"H			"EA00"H		
G236	G5	"EBAF"H			"EBAE"H			"EBAD"H			"EBAC"H			.....	"EB03"H			"EB02"H			"EB01"H			"EB00"H		
G237	G4	"ECAF"H			"ECAE"H			"ECAD"H			"ECAC"H			.....	"EC03"H			"EC02"H			"EC01"H			"EC00"H		
G238	G3	"EDAF"H			"EDAE"H			"EDAD"H			"EDAC"H			.....	"ED03"H			"ED02"H			"ED01"H			"ED00"H		
G239	G2	"EEAF"H			"EEAE"H			"EEAD"H			"EEAC"H			.....	"EE03"H			"EE02"H			"EE01"H			"EE00"H		
G240	G1	"EFAF"H			"EFAE"H			"EFAD"H			"EFAC"H			.....	"EF03"H			"EF02"H			"EF01"H			"EF00"H		

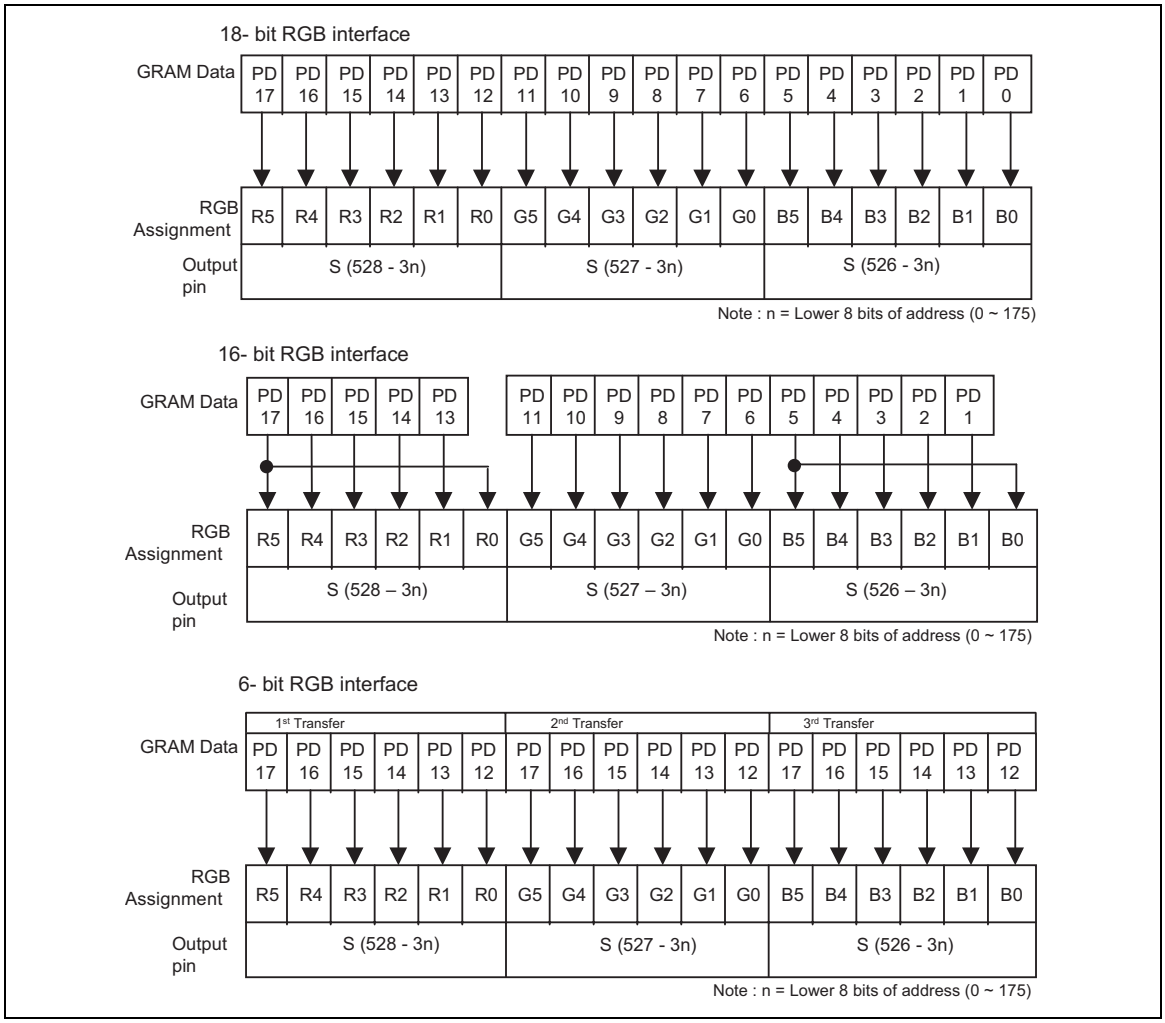
GRAM data and display data: system interface (SS = "1", BGR = "1")



GRAM data and display data: system interface (SS = "1", BGR = "1")



GRAM data and display data: RGB interface (SS = “1”, BGR = “1”)



Instructions

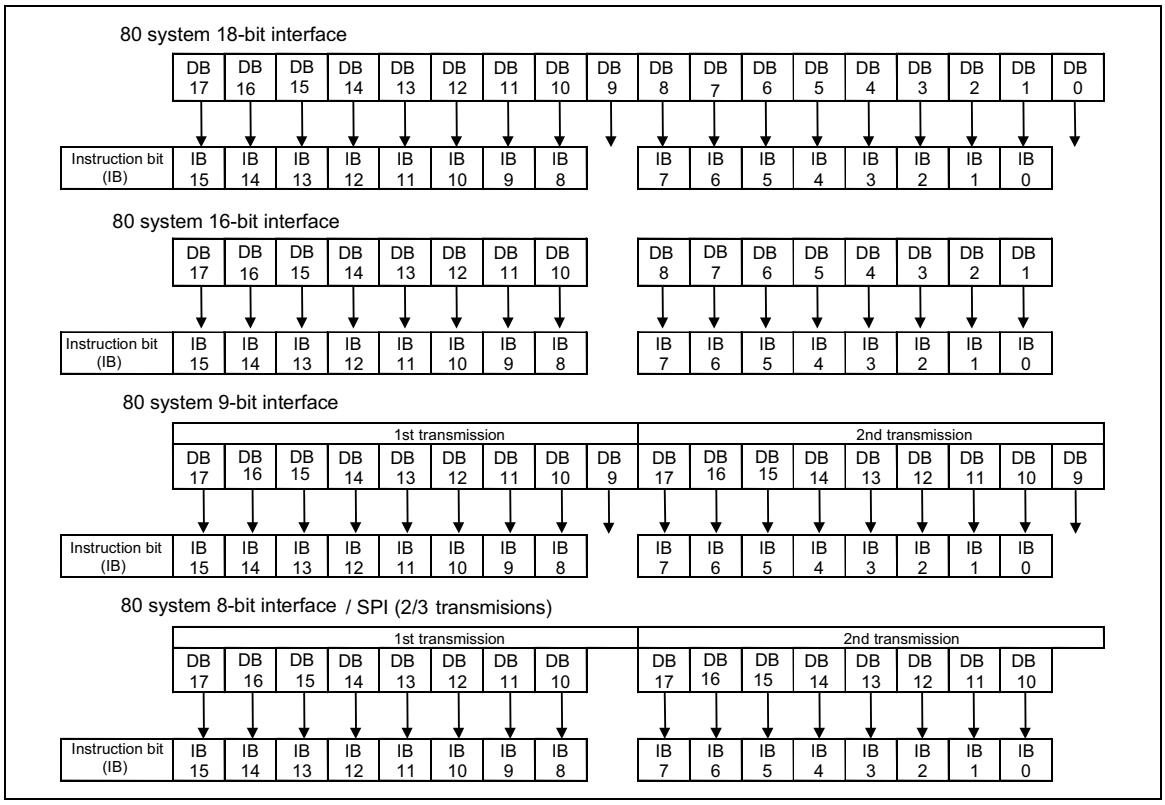
Outline

The HD66789R adapts an 18-bit bus architecture that enables high-speed interfacing with a high-performance microcomputer. The HD66789R starts internal processing of 18/16/9/8/-bit data sent externally after storing control information in the instruction register (IR) and the data register (DR). Since the internal operations of the HD66789R are determined by signals sent from the microcomputer, the register selection signal (RS), read/write signal (R/W), and internal 16-bit data bus signals (IB15 to IB0) are called instructions. Data are transferred to the internal GRAM through the 18-bit data format. The HD66789R has the following categories of instructions.

1. Specify an index
2. Read a status
3. Control display
4. Power management Control
5. Graphics data Processing
6. Set internal GRAM addresses
7. Transfer data to and from the internal GRAM
8. Internal grayscale γ-adjustment

Normally, the instruction to write data on the internal GRAM is used the most often. The internal GRAM addresses are updated automatically as data are written to the internal GRAM. The window address function, combined with the automatic update of internal GRAM addresses, minimizes data transfers and thereby lessens the load on the program run by the microcomputer. Since instructions are executed in 0 cycle, it is possible to write instructions consecutively.

As the following figure shows, the assignment of data to the 16 instruction bits (IB15-0) varies according to the interface in use. Instructions must adopt the data format of the interface in use.



Instruction bits

Instructions

The following are detail explanations of instructions with illustrations of instruction bits (IB15-0) assigned to each interface.

Index (IR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

The index register specifies the index (R00h to R4Fh) of the control register and the RAM control with the binary number from 0000000 to 1111111. Do not try to access to the register or instruction bits if the index is not designated in this register.

Status Read (SR)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

The status read instruction reads the internal status of the HD66789R.

L7–0: Indicate the position of the line currently driven.

Start Oscillation (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
R	1	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1

The start oscillation instruction restarts the oscillator from a halt state during the standby mode. After executing this instruction, wait at least 10 ms for the oscillators to stabilize before issuing a next instruction. For details, see the “Standby Mode” section.

“0789”H is read out when reading out this register forcibly.

Driver Output Control (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	VSPL	HSPL	DPL	EPL	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

SS: Selects the shift direction of source driver outputs. When SS = 0, the shift direction of source outputs is from S1 to S528. When SS = 1, the shift direction of source output is from S528 to S1. In addition to change the shift direction, the assignment of RGB dots to the source driver pins is changeable with the BGR bit.

To assign RGB dots to the source driver pins interchangeably from S1, set SS = 0, BGR = 0.
To assign RGB dots to the source driver pins interchangeably from S528, set SS = 1, BGR = 1.

Whenever changing the SS and BGR bits, make sure to rewrite the RAM data.

GS: Selects the shift direction of gate driver outputs. The scan direction is changeable through the instruction to conform to the scan mode by the gate driver. Set according to the assembling method of the module.

SM: Sets the scan order by the gate driver. Set according to the assembling method of the module. See "Scan Mode Setting" for details.

EPL: Sets the polarity of ENABLE pin in RGB interface mode.

EPL = "0" : ENABLE = "Low" / Write data to PD17-0.
: ENABLE = "High" / Disable data write operation.
EPL ="1" : ENABLE = "High" / Write data to PD17-0.
: ENABLE = "Low" / Disable data write operation.

The following table shows the relationship between EPL, ENABLE, and RAM access.

Table 4

EPL	ENABLE	RAM write	RAM address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

VSPL: Inverts the polarity of signals on the VSYNC pin.

VSPL = "0" : Low active.
VSPL = "1" : High active.

HSPL: Inverts the polarity of signals on the HSYNC pin.

HSPL = "0" : Low active.
HSPL = "1" : High active.

DPL: Inverts the polarity of signals on the DOTCLK pin.

DPL = "0" : Data are read on the rising edge of the DOTCLK.
DPL = "1" : Data are read on the falling edge of the DOTCLK.

NL4-0: Specifies the number of lines to an 8 multiple, to drive the LCD. The number of lines set with the NL4-0 bits does not affect the GRAM address mapping. Select a number that can cover the full size of the panel.

Table 5

NL4	NL3	NL2	NL1	NL0	Display Size	Number of lines to drive the LCD	Gate lines to be driven
0	0	0	0	0	Setting disabled	Setting disabled	Setting disabled
0	0	0	0	1	528 x 16 dots	16	G1~G16
0	0	0	1	0	528 x 24 dots	24	G1~G 24
0	0	0	1	1	528 x 32 dots	32	G1~G 32
0	0	1	0	0	528 x 40 dots	40	G1~G 40
0	0	1	0	1	528 x 48 dots	48	G1~G 48
0	0	1	1	0	528 x 56 dots	56	G1~G 56
0	0	1	1	1	528 x 64 dots	64	G1~G 64
0	1	0	0	0	528 x 72 dots	72	G1~G 72
		:			:	:	:
		:			:	:	:
1	0	0	0	0	528 x 200 dots	200	G1~G 200
1	0	0	0	1	528 x 208 dots	208	G1~G 208
1	0	0	1	0	528 x 216 dots	216	G1~G 216
1	0	0	1	1	528 x 224 dots	224	G1~G 224
1	0	1	0	0	528 x 232 dots	232	G1~G 232
1	0	1	0	1	528 x 240 dots	240	G1~G 240

Note 1) A front porch period (set with FP register) and a back porch period (set with BP register) are inserted as a blank period before and after driving all gate lines.

LCD Driving Waveform Control (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FLD 1	FLD 0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

NW5-0: Specify "n", the number of lines from 1 to 64, to invert the polarity of a C-pattern waveform every n+1 line cycle when B/C = 1.

EOR: When EOR = 1, polarity inversions of a C-pattern waveform (B/C =1) occur by applying an EOR (exclusive OR) operation to an odd/even frame select signal and an n-line inversion signal. This instruction is used when the combination of the number of lines to drive the LCD and the value of "n" is at odds with the polarity inversion. For details, see "n-line inversion alternating drive".

B/C: When B/C = 0, a field-inversion alternating waveform is generated. Polarity inversion occurs at completion of drawing one frame. When B/C=1, an n-line inversion alternating waveform is generated, where polarity inversion occur at completion of driving n lines according to the EOR, NW5-0 bits. For details, see the "n-line Inversion Alternating Drive" section.

FLD1-0: Sets the number of fields for the interlaced scan. See "Interlaced scan" for details. Set the back porch and front porch setting bits to BP3-0=3, FP3-0=5 respectively when using the interlaced scan. The interlaced scan is disabled in external display interface mode. When using an external display interface, set FLD1-0= "01".

Table 6

FLD1	FLD0	Number of fields
0	0	Setting disabled
0	1	1 field
1	0	Setting disabled
1	1	3 fields

Entry Mode (R03h)

Compare Register 1 (R04h)

Compare Register 2 (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	TRI	DFM1	DFM0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0
W	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
W	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

The HD66789R modifies write data sent from the microcomputer before writing to the internal GRAM so that the GRAM data will be rewritten in high speed, and thereby lessen the software processing load on the microcomputer. For details, see the "Graphics Operation Function" section.

TRI: The RAM write data for a pixel are transferred 3 times through the 8-bit bus when TRI = 1. When the 8-bit interface mode is not selected, set TRI to 0.

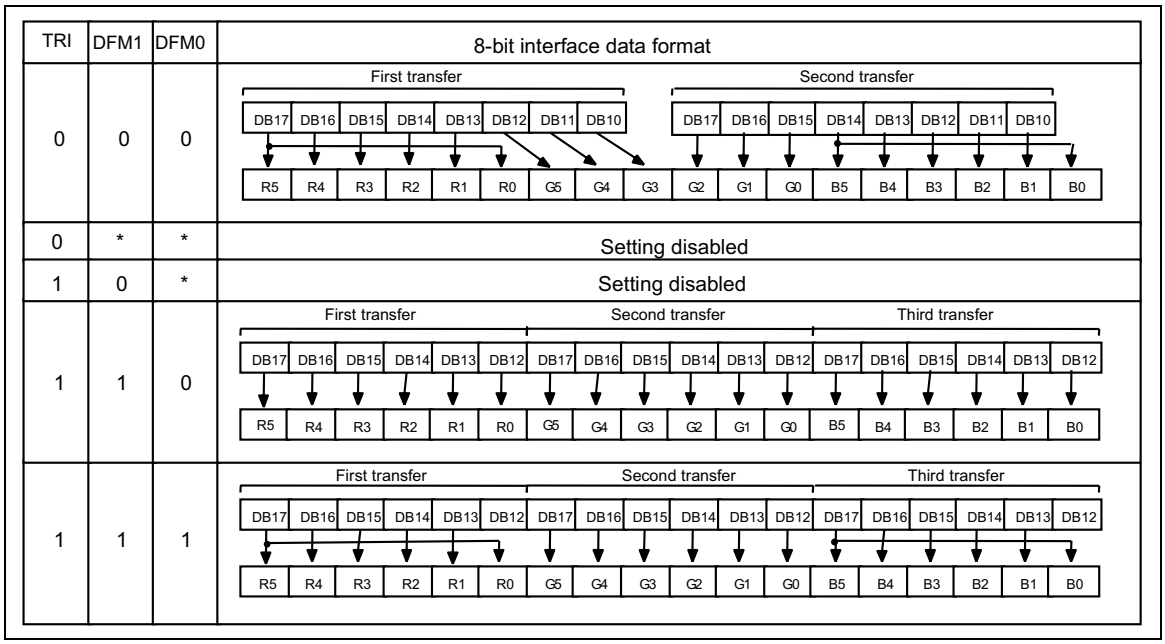
DFM1-0: Specifies the data format when TRI = 1, when using an 8-bit interface or SPI.

DFM1-0 = "10": 262k mode (6 bit x 3 transfers)
DFM1-0 = "11": 65k mode (5,6,5 bits transfers)

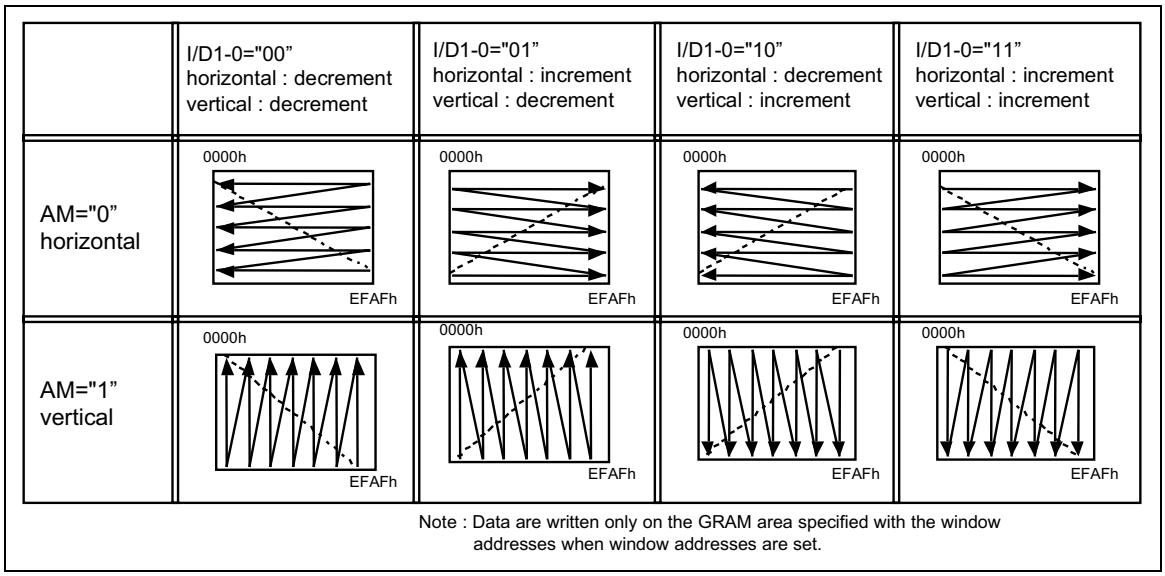
HWM: When HWM=1, data are written to the internal GRAM in high speed, where 4-word data are written to the internal GRAM at once after executing 4 RAM write operations. If the RAM write operation is terminated before it is executed 4 times, the last data will not be written. Make sure that the RAM write operation is concluded at every 4 times. For this reason, the lower 2 bits must be set to "00" when setting the AD15-0 bits (RAM address set: R21h). For details, see "High-Speed RAM Write Mode" section.

I/D1-0: The address counter is automatically incremented by 1, as writing data to GRAM when I/D1-0 = "1". The address counter is automatically decremented by 1, as writing data to GRAM when I/D1-0 = "0". The increment or the decrement is set independently for each upper (AD15-8)/lower (AD7-0) byte of an address. The address transition direction as writing data to the internal GRAM is set with the AM bit.

AM: Sets the direction of automatically updating the address counter as writing data to the internal GRAM. When AM = "0", the address counter is updated in horizontal direction. When AM = "1", the address counter is updated in vertical direction. When the window addresses are set, data are written to the internal GRAM area specified with the window addresses in the manner determined with the I/D1-0, AM bits.



8-bit interface data format

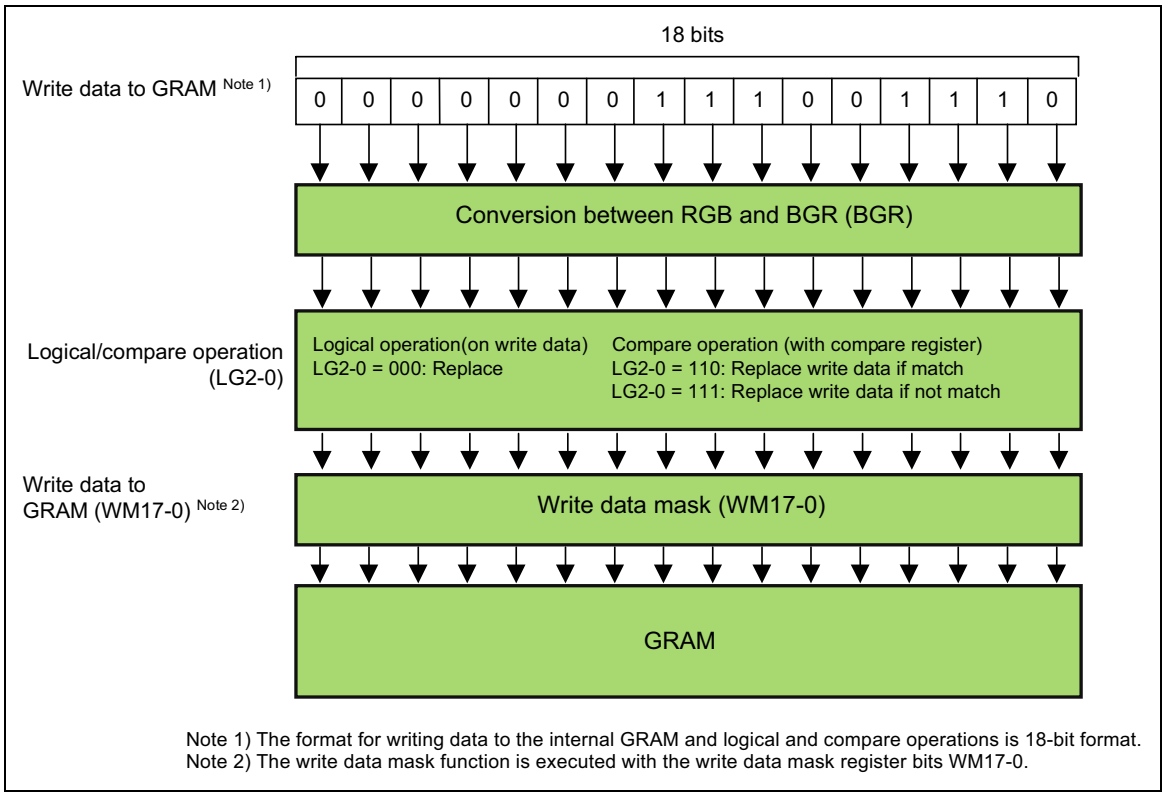


Address transition direction

LG2–0: Writes to the internal GRAM the result obtained from comparing the data written from the microcomputer with the values of the compare register (CP17–0) and performing a logical operation. For details, see the "Graphics Operation Function"

CP17–0: Sets the value of the compare register, with which data read out from the GRAM or written from the microcomputer are compared. This function is not available with the external display interface mode. In external display interface mode, make sure LG2-0 = "000".

BGR: Reverses the order of RGB dots to BGR for the 18-bit data written to the internal GRAM. When setting BGR = 1, the CP17-0, WM17-0 bits will automatically be changed accordingly.



Bit operations

Display Control 1 (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	1	GON	DTE	CL	REV	D1	D0

PT1-0: Determines the kind of source output in the non-display area in partial display mode. For details, see the "Partial Display Function" section.

Table 7

		Source Output for Non-display Area	
PT1	**PT0**	**Positive Polarity**	**Negative Polarity**
0	0	V31	V0
0	1	Setting disabled	Setting disabled
1	0	GND	GND
1	1	High impedance	High impedance

VLE2–1: When VLE1 = 1, the first screen is scrolled in the vertical direction. When VLE2 = 1, the second screen is scrolled in the vertical direction. The first and second screens cannot be scrolled simultaneously. This function is not available with the external display interface mode. In this case, make sure VLE2-1 = 0.

Table 8

VLE2	**VLE1**	**Image on 2nd Screen**	**Image on 1st Screen**
0	0	Originally designated position	Originally designated position
0	1	Originally designated position	Scrolled
1	0	Scrolled	Originally designated position
1	1	Setting disabled	Setting disabled

CL: When CL = 1, the 8-color display mode is selected. For details, see the "8-Color Display Mode" section.

Table 9

CL	**Colors**
0	262,144
1	8

SPT: When SPT = 1, liquid crystal is driven with 2 split screens. For details, see the "Partial Display Function" section. This function is not available with the external display interface mode. In this case, make sure SPT = 0.

REV: When REV = "1", the relationship between the R, G, B dot data and the source output levels is reversed to obtain a reversed grayscale image. This bit allows using the same data for a normally black display to a normally white display and vise versa. The source outputs during the front and back porches and the blank period in partial display mode are determined by the PT1-0 bits.

Table 10

		Source Output in the Display Area*	
REV	**GRAM Data**	**Positive Polarity**	**Negative Polarity**
0	18'h00000	V31	V0
	⋮	⋮	⋮
	18'h3FFFF	V0	V31
1	18'h00000	V0	V31
	⋮	⋮	⋮
	18'h3FFFF	V31	V0

GON, DTE: Determines the output levels from the gate lines as follows. When GON=0, the Vcom level becomes the GND level.

Table 11

GON	DTE	Gate Output
0	0	VGH
0	1	VGH
1	0	VGL
1	1	VGH/VGL

D1–0: A graphics display is shown when D1 = 1, and turned off when D1 = 0. When setting D1 = 0, data are retained in the internal GRAM. This means the graphics display is instantly shown when setting D1 to 1. When D1 is 0 (i.e. the display is not shown) all source outputs are set to the GND level to reduce charging/discharging current on the liquid crystal, which is generated when driving liquid crystal with inverting polarities.

If D1-0 = 01, the display operation is executed inside the HD66789R even while the external display is turned off. If D1-0 = 00, both the internal and external display operations are halted.

In combination with the GON and DTE bits, the D1-0 bits control ON/OFF of display. For details, see the "Instruction Setting Flow" section.

Table 12

D1	D0	Source Output	HD66789R Internal Operations	Gate-Driver Control Signals (CL1, FLM, M)
0	0	GND	Halt	OFF
0	1	GND	Operate	ON
1	0	Non-lit display	Operate	ON
1	1	Display	Operate	ON

Note 1) Data are written to GRAM from the microcomputer irrespective of the value of D1-0.

Note 2) In standby mode, the internal operation is equivalent to when D1-0 = "00". This does not mean the value of D1-0 register before entering the standby modes is overwritten to "00".

Display Control 2 (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	FP3	FP2	FP1	FP0	0	0	0	0	BP3	BP2	BP1	BP0

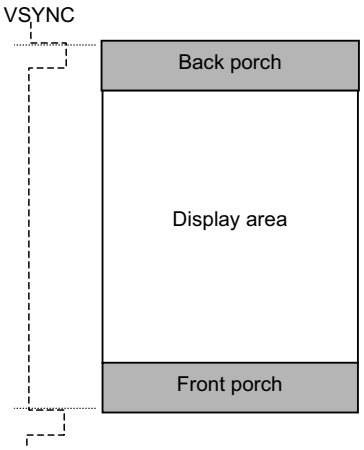
FP3-0, BP3-0: Makes a blank period setting (front and back porches), which is made at the beginning and the end of the display. FP3-0 and BP3-0 specify the number of lines for the front and back porches respectively. In setting, make sure:

BP + FP ≤ 16 lines
FP ≥ 2 lines
BP ≥ 2 lines

In external display interface mode, a back porch (BP) starts on the falling edge of VSYNC signal, followed by the display operation. After driving the number of lines set with the NL4-0 bits, a front porch starts. After the front porch, a blank period continues until the next input of the VSYNC signal.

Table 13

FP3	FP2	FP1	FP0	Number of lines for the Front Porch
BP3	**BP2**	**BP1**	**BP0**	**Number of lines for the Back Porch**
0	0	0	0	Setting disabled
0	0	0	1	Setting disabled
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
:	:	:	:	:
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	Setting disabled



Note: The output timing to the LCD is delayed 2 lines from the input of shynchronizing signal.

Back/Front porch

Set BP3-0, FP3-0 bits as follows in each of the following operation modes.

Table 14

Operation of internal clock	**FLD1-0 = 01**	BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
	FLD1-0 = 11	BP = 3 lines	FP = 5 lines	
RGB interface		BP ≥ 2 lines	FP ≥ 2 lines	FP +BP ≤ 16 lines
VSYNC interface		BP ≥ 2 lines	FP ≥ 2 lines	FP +BP = 16 lines

Display Control 3 (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	PTG 1	PTG 0	ISC3	ISC2	ISC1	ISC0

PTG1-0: Sets the scan mode by the gate driver in the non-display area.

Table 15

PTG1	PTG0	Gate outputs in non-display area	Source outputs in non-display area	Vcom output
0	0	Normal scan	According to PT1-0	VcomH/VcomL amplitude
0	1	VGL (Fixed)	According to PT1-0	VcomH/VcomL amplitude
1	0	Interval scan	According to PT1-0	VcomH/VcomL amplitude
1	1	Setting Disabled	-	-

ISC3-0: Sets the cycle of scan by the gate driver when PTG1-0 is set to "10", the interval scan in the non-display area. The scan cycle is set to n frames, where n is an odd number from 0 to 31. The polarity is inverted at every scan cycle.

Table 16

ISC3	ISC2	ISC1	ISC0	Scan cycle	(fFLM) = 60Hz
0	0	0	0	0 frame	_
0	0	0	1	3 frames	50 mS
0	0	1	0	5frames	84 mS
0	0	1	1	7 frames	117 mS
0	1	0	0	9 frames	150 mS
0	1	0	1	11 frames	184 mS
0	1	1	0	13 frames	217 mS
0	1	1	1	15 frames	251 mS
1	0	0	0	17 frames	284 mS
1	0	0	1	19 frames	317 mS
1	0	1	0	21 frames	351 mS
1	0	1	1	23 frames	384 mS
1	1	0	0	25 frames	418 mS
1	1	0	1	27 frames	451 mS
1	1	1	0	29 frames	484 mS
1	1	1	1	31 frames	518 mS

Frame Cycle Control (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN3-0: Sets a 1H (1 line) period.

Table 17

RTN3	RTN2	RTN1	RTN0	Clock Cycles per line
0	0	0	0	16 clocks
0	0	0	1	17 clocks
0	0	1	0	18 clocks
		:		:
1	1	1	0	30 clocks
1	1	1	1	31 clocks

DIV1-0: Sets the division ratio of the internal operation clocks. Internal operations are executed in synchronization with the clocks, the frequency of which is divided according to the DIV1-0 setting. When changing the number of lines, make sure to adjust the frame frequency too. For details, see "Frame Frequency Adjustment Function". This function is not available in RGB interface mode.

Table 18

DIV1	DIV0	Division Ratio	Internal Operation Clock Frequency
0	0	1	fosc / 1
0	1	2	fosc / 2
1	0	4	fosc / 4
1	1	8	fosc / 8

fosc =Frequency of RC oscillation

Formula to calculate frame frequency

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clock cycles per line} \times \text{division ratio} \times (\text{Line} + \text{BP} + \text{FP})} \quad [\text{Hz}]$$

fosc: frequency of RC oscillation
Line: number of lines (NL bit)
Division ratio: DIV bit
Clocks per line: RTN bit
FP: the number of lines for the front porch period
BP: the number of lines for the back porch period

EQ1-0: Determines the number of clocks as follows, which becomes an equalizing period. The equalization occurs only on the lines where the polarities are inverted.

Table 19

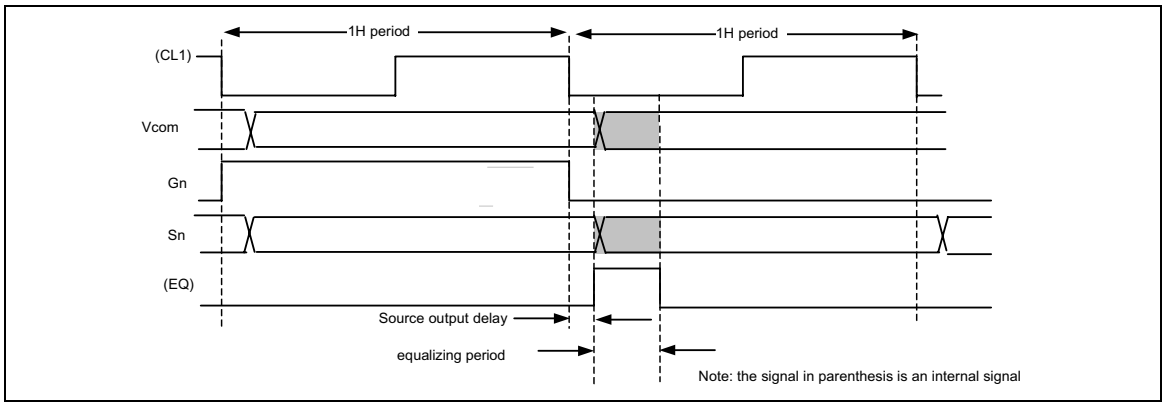
		Equalizing period	
EQ1	**EQ0**	**Internal Operation (clock: internal oscillator)**	**RGB I/F Operation (clock: DOTCLK)**
0	0	Not equalized	Not equalized
0	1	1 clock	8 clocks
1	0	2 clocks	16 clocks
1	1	3 clocks	24 clocks

SDT1-0: Specifies the delay in outputting source signal from the falling edge of the gate output.

Table 20

		Source output delay	
SDT1	**SDT0**	**Internal Operation (reference clock: internal oscillator)**	**RGB I/F Operation (reference clock: DOTCLK)**
0	0	1 clock	8 clocks
0	1	2 clocks	16 clocks
1	0	3 clocks	24 clocks
1	1	4 clocks	32 clocks

Note 1) The delay is measured from the falling edge of CL1.



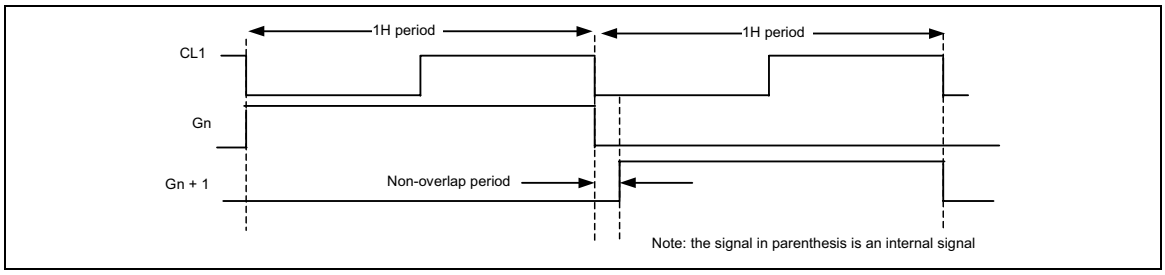
Source output delay, Equalizing period

NO1-0: Specifies the non-overlap period of between the gate outputs (DISPTMG).

Table 21

		Gate outputs non-overlap period	
NO1	**NO0**	**Internal Operation (reference clock: internal oscillator)**	**RGB I/F Operation (reference clock: DOTCLK)**
0	0	0 clock	0 clock
0	1	4 clocks	32 clocks
1	0	6 clocks	48 clocks
1	1	8 clocks	64 clocks

Note 1) The amount of non-overlap time is defined from the falling edge of the CL1.



Non-overlap period

Note that the clocks mentioned in EQ1-0, SDT1-0, NO1-0 settings refer to different clocks according to an interface mode as follows.

Table 22

Interface mode	**Reference clock**
Internal operation mode	Internal RC oscillator
RGB interface more	DOTCLK
VSYNC interface mode	Internal RC oscillator

External Display Interface Control (R0Ch)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	RM	0	0	DM1	DM0	0	0	RIM1	RIM0

RIM1–0: Set the transfer mode when the RGB interface is selected. Specifically, this setting specifies the mode in use when the RGB interface is selected with the DM and RM bits. Make the setting before display operation starts through the external display interface. Do not make the setting during display.

Table 23

RIM1	RIM0	RGB Interface Mode
0	0	18-bit RGB interface (one-time transfer/pixel)
0	1	16-bit RGB interface (one-time transfer/pixel)
1	0	6-bit RGB interface (three-time transfers/pixel)
1	1	Setting disabled

Note 1) Instruction settings to the registers are possible only through the system interface.

Note 2) Data transfers and a DOTCLK input must be executed in units of dots (R, G, and B) in 6-bit RGB interface mode.

DM1–0: Specifies the display operation mode. DM1-0 selects the interface through which the display operation is executed. DM1-0 allows switching between the internal clock operation and the external display interface mode. Do not switch between the two different external display interface modes (between RGB-I/F and VSYNC-I/F).

Table 24

DM1	DM0	Display Interface
0	0	Internal clock operation
0	1	RGB interface
1	0	VSYNC interface
1	1	Setting disabled

RM: Specifies the interface for the RAM access. RAM is accessible only through the interface determined with the RM bit. When display data are written through the RGB-I/F, set RM = 1. The RM setting is not affected by the display operation mode. This means display data can be rewritten through the system interface by setting RM = 0, while the display operation is executed through the RGB interface.

Table 25

RM	Display Interface
0	System interface/VSYNC interface
1	RGB interface

As the following table shows, the HD66789R selects an optimum interface according to the kind of display through the external display interface control setting.

Use the high-speed write mode (HWM=1) with the RGB and VSYNC interfaces to access RAM in high speed with low power consumption when displaying a moving picture.

Table 26

Display State	Operation Mode	RAM Access (RM)	Display Operation Mode (DM1-0)
Still picture	Internal clock operation	System interface (RM = 0)	Internal clock operation (DM1-0 = 00)
Moving picture	RGB interface (1)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
Rewrite still picture area while displaying a moving picture	RGB interface (2)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
Moving picture	VSYNC interface	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

Note 1) Instructions are set only through a system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not used simultaneously.

Note 3) Do not make changes to the RGB-I/F mode (RIM-0) while an RGB I/F is in operation.

Note 4) See the “External Display Interface” section for the flowcharts of mode transitions.

Note 5) Use the high-speed write mode (HWM = 1) in RGB-I/F and VSYNC-I/F modes.

Internal clock operation mode

All display operation is synchronized with signals generated from internal operating clocks in this mode. All inputs through the external display interface are invalid. The internal RAM is accessible only through the system interface.

RGB interface mode (1)

The display operation is synchronized with the frame synchronizing signal (VSYNC), line synchronizing signal (HSYNC), and dot clocks (DOTCLK) in RGB interface mode. These signals must be supplied through a display period using the RGB interface.

Display data are transferred in pixel unit through PD17-0 bits. All display data are stored in the internal RAM. The combined use of high-speed RAM write mode and a widow address function enables to display data in a moving picture area and data in internal RAM at once, which makes it possible to transfer display data only when rewriting a screen and minimize data transfers.

The front porch (FP) and the back porch (BP) periods, and the display duration (NL) are automatically calculated inside the HD66789R by internally counting the clocks of the line synchronizing signal (HSYNC) from the edge of the frame synchronizing signal (VSYNC). Take this into consideration when transferring pixel data through PD17-0.

RGB interface mode (2)

The HD66789R enables to rewrite the RAM data through the system interface while the RGB interface is selected. To rewrite the RAM data, make sure that display data are not being transferred through the RGB interface (ENABLE = High). To return to the display data transfer mode through the RGB interface, change the ENABLE bit first and then set a new address (AD15-0) in the AC and the index register to R22h.

VSYNC interface mode

The internal display operation is synchronized with the frame synchronizing signal (VSYNC) in VSYNC interface mode. A moving picture can be displayed using a system interface by writing data to the internal RAM at more than the minimum speed through a system interface from the falling edge of frame synchronizing signal (VSYNC). In this case, there are constraints in the RAM writing speed and methods. For details, see “External Display Interface”.

Only VSYNC inputs are valid in VSYNC interface mode. Other signal inputs through the external display interface are invalid.

The front porch (FP), the back porch (BP) periods and, the display duration (NL) are automatically calculated according to the settings in the register of the HD66789R from the falling edge of the frame synchronization signal (VSYNC), which serves as a reference point.

Power Control 1 (R10h)

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	SAP2	SAP1	SAP0	0	BT2	BT1	BT0	0	AP2	AP1	AP0	0	DK	SLP	STB
W	1	0	0	0	0	0	DC12	DC11	DC10	0	DC02	DC01	DC00	0	VC2	VC1	VC0

SAP2-0: Adjusts the constant current from the constant current source for the operational amplifier circuit for the source driver. Setting a larger constant current will stabilize the operational amplifier circuit, but current consumption will increase. Adjust constant current taking the display quality-current consumption tradeoff into account. During the non-display operation, set SAP2-0 = "000" to halt the operational amplifier circuit to reduce current consumption.

Table 27

SAP2	SAP1	SAP0	Op-amp Constant Current
0	0	0	Halt
0	0	1	Setting disabled
0	1	0	0.62
0	1	1	0.71

SAP2	SAP1	SAP0	Op-amp Constant Current
1	0	0	1
1	0	1	1.25
1	1	0	1.43
1	1	1	Setting disabled

BT2–0: Changes the step-up rate for the step-up circuits. Adjust the rate according to the voltage in use. To reduce current consumption, use a smaller rate.

DC02–00: Selects the operating frequency of the step-up circuit 1. A higher frequency enhances the drive capacity of the step-up circuit as well as the quality of the display, while current consumption will increase. Adjust the frequency taking the display quality-current consumption tradeoff into consideration.

DC12–10: Selects the operating frequency of the step-up circuit 2. A higher frequency enhances the drive capacity of the step-up circuit as well as the quality of the display, while current consumption will increase. Adjust the frequency taking the display quality-current consumption tradeoff into consideration.

AP2–0: Adjusts the constant current from the constant current source for the operational amplifier circuit in the LCD power supply circuit. Setting a larger constant current will stabilize the operational amplifier circuit, but current consumption will increase. Adjust the constant current taking the display quality-current consumption tradeoff into account. During the non-display operation, set AP2-0 = "000" to halt the operational amplifier circuit and the step-up circuits to reduce current consumption.

DK: Controls ON/OFF of the step-up circuit 1. When turning on the power supply, stop the startup of VLOUT1 for a moment, and wait until the VLOUT2 level is boosted completely before starting up VLOUT1. For details, see the "Power Supply Setting Flow" section.

SLP: When SLP = 1, the HD66789R enters into the sleep mode. In sleep mode, the internal display operation is halted except RC oscillators to reduce current consumption. Only power control instructions (BT2-0, DC12-10, DC02-00, AP2–0, SLP, STB, VC2-0, DK, SAP2-0, VRH4-0, VCOMG, VDV4-0, and VCM4-0 bits) are executed during the sleep mode. No change is accepted to the GRAM data or instruction sets during the sleep mode, and the GRAM data and the instructions are retained.

STB: When STB = 1, the HD66789R enters into the standby mode. In standby mode, the display operation is completely halted, and all internal operations including internal RC oscillation and reception of external clock pulses are halted. For details, see the "Standby Mode" section. Only instructions to release the HD66789R from the standby mode (STB = 0) and to start oscillators are accepted during the standby mode. GRAM data and instruction sets must be set again after releasing the HD66789R from the standby mode because they may be destroyed during the standby mode.

VC2-0: Set the reference voltage REGP for the VREG1OUT, VciOUT voltages within the range of 0.73 ~ 0.92 times the VciLVL level.

Table 28

AP2	AP1	AP0	Constant current of operational-amplifier
0	0	0	Halt
0	0	1	Setting disabled
0	1	0	0.5
0	1	1	0.75
1	0	0	1
1	0	1	1.25
1	1	0	1.5
1	1	1	Setting disabled

Table 29

DC02	DC01	DC00	Step-up circuit 1: step-up cycle	DC12	DC11	DC10	Step-up circuit 2: step-up cycle
0	0	0	Oscillation clock / 8	0	0	0	Oscillation clock / 16
0	0	1	Oscillation clock / 16	0	0	1	Oscillation clock / 32
0	1	0	Oscillation clock / 32	0	1	0	Oscillation clock / 64
0	1	1	Oscillation clock / 64	0	1	1	Oscillation clock / 128
1	0	0	Oscillation clock / 128	1	0	0	Oscillation clock / 256
1	0	1	Setting disabled	1	0	1	Setting disabled
1	1	0	Setting disabled	1	1	0	Setting disabled
1	1	1	Setting disabled	1	1	1	Setting disabled

Note: Make sure step-up 1 cycle ≥ step-up 2 cycle when setting DC02-00, DC12-10.

Table 30

BT2	BT1	BT0	VLOUT1 output (DDVDH)	VLOUT4 output (VCL)	VLOUT2 output (VGH)	VLOUT3 output (VGL)	Capacitor connection pins
0	0	0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x 6]	- (Vci1+DDVDH x 2) [x –5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
0	0	1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x 6]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
0	1	0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 3 [x 6]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
0	1	1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 +DDVDH x 2 [x 5]	- (Vci1+DDVDH x 2) [x –5]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
1	0	0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 +DDVDH x 2 [x 5]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
1	0	1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	Vci1 +DDVDH x 2 [x 5]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
1	1	0	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x 4]	- (DDVDH x 2) [x –4]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±, C22±
1	1	1	Vci1 x 2 [x2]	Vci1 x -1 [x-1]	DDVDH x 2 [x 4]	- (Vci1+DDVDH) [x –3]	DDVDH, VGH, VGL, VCL, C11±, C12±, C21±

Note 1) The numerals in the brackets [ ] show the step-up rate from the Vci1 level.

Note 2) When using DDVDH, VCL, VGH, VGL voltages, connect capacitors to the capacitor connection pins.

Note 3) Set the voltage within the following range: DDVDH = 5.5 V (Max.), VCL = - 3.3 V (Min.), VGH = 16.5 V (Max.), VGL = -16.5 V (Min.)

Table 31

VC2	VC1	VC0	VciOUT output voltage (REGP)
0	0	0	VciLVL
0	0	1	0.92 x VciLVL
0	1	0	0.87 x VciLVL
0	1	1	0.83 x VciLVL
1	0	0	0.76 x VciLVL
1	0	1	0.73 x VciLVL
1	1	0	Setting disabled
1	1	1	Setting disabled

DK	Operation of step-up circuit 1
0	Operate
1	Halt

Power Control 3 (R12h)

Power Control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
W	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

PON: Controls ON/OFF of the VLOUT3 output. To stop the output of VLOUT3, set PON = 0. To start the output of VLOUT3, set PON = 1.

VRH3-0: Sets the rate for amplifying the VREG1OUT voltage (reference voltage of VCOM and grayscale voltages) by stepping up REGP form 1.33 to 2.775 times.

VCOMG: When VCOMG = 1, the VcomL can take a negative voltage level (between 1.0V to -Vci+0.5V Max.). When VCOMG = 0, the HD66789R halts the negative voltage amplifiers to save power. When VCOMG = 0, the VDV4-0 bits are disabled. In this case, adjust the Vcom-level alternating amplitude with the VCM4-0 bits to set VcomH. VCOMG = 1 is enabled when PON = 1.

VDV4-0: Sets the Vcom-level alternating amplitude when driving with alternating Vcom voltage. VDV4-0 sets the amplitude from VREG1OUT x 0.6 to VREG1OUT x 1.23. If VCOMG = 0, the VDV4-0 bits are disabled.

VCM4-0: Sets the VcomH level (the higher level of the alternating Vcom voltage). VCM4-0 sets the amplitude from VREG1OUT x 0.4 to VREG1OUT x 0.98. To halt adjustment with the internal volumes and adjust VcomH with an external resistor from VcomR, set VCM4-0 = "11111".

Table 32

VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage	VRH3	VRH2	VRH1	VRH0	VREG1OUT voltage
0	0	0	0	REGP x 1.33	1	0	0	0	REGP x 1.90
0	0	0	1	REGP x 1.45	1	0	0	1	Setting disabled
0	0	1	0	REGP x 1.55	1	0	1	0	Setting disabled
0	0	1	1	REGP x 1.65	1	0	1	1	Setting disabled
0	1	0	0	REGP x 1.75	1	1	0	0	Setting disabled
0	1	0	1	REGP x 1.80	1	1	0	1	Setting disabled
0	1	1	0	REGP x 1.85	1	1	1	0	Setting disabled
0	1	1	1	Halt	1	1	1	1	Setting disabled

Table 33

VCM4	VCM3	VCM2	VCM1	VCM0	VcomH	VDV4	VDV3	VDV2	VDV1	VDV0	Vcom amplitude
0	0	0	0	0	VREG1OUT x 0.40	0	0	0	0	0	VREG1OUT x 0.60
0	0	0	0	1	VREG1OUT x 0.42	0	0	0	0	1	VREG1OUT x 0.63
0	0	0	1	0	VREG1OUT x 0.44	0	0	0	1	0	VREG1OUT x 0.66
:	:	:	:	:	:	:	:	:	:	:	:
0	1	1	0	0	VREG1OUT x 0.64	0	1	1	0	0	VREG1OUT x 0.96
0	1	1	0	1	VREG1OUT x 0.66	0	1	1	0	1	VREG1OUT x 0.99
0	1	1	1	0	VREG1OUT x 0.68	0	1	1	1	0	VREG1OUT x 1.02
0	1	1	1	1	Halt the internal volumes. Adjust with a variable external resistor from VcomR.	0	1	1	1	1	Setting disabled
1	0	0	0	0	VREG1OUT x 0.70	1	0	0	0	0	VREG1OUT x 1.05
1	0	0	0	1	VREG1OUT x 0.72	1	0	0	0	1	VREG1OUT x 1.08
1	0	0	1	0	VREG1OUT x 0.74	1	0	0	1	0	VREG1OUT x 1.11
:	:	:	:	:	:	1	0	0	1	1	VREG1OUT x 1.14
1	1	1	0	0	VREG1OUT x 0.94	1	0	1	0	0	VREG1OUT x 1.17
1	1	1	0	1	VREG1OUT x 0.96	1	0	1	0	1	VREG1OUT x 1.20
1	1	1	1	0	VREG1OUT x 0.98	1	0	1	1	0	VREG1OUT x 1.23
1	1	1	1	1	Halt the internal volumes. Adjust with a variable external resistor from VcomR.	1	1	*	*	*	Setting disabled

Note 1) Adjust VREG1OUT and VCM0-4 so that the VcomH level is set within the range of 3.0V~(DDVDH-0.5)V.

Note 2) Adjust VREG1OUT and VDV0-4 so that the Vcom amplitude is set to 6.0V or less.

RAM Address Set (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	AD 15	AD 14	AD 13	AD 12	AD 11	AD 10	AD 9	AD 8	AD 7	AD 6	AD 5	AD 4	AD 3	AD 2	AD 1	AD 0

AD15–0: A GRAM address set initially in the AC (Address Counter). The address counter is automatically updated in accordance with the AM, I/D bits as data are written to the internal GRAM. Data are written consecutively without resetting the address.

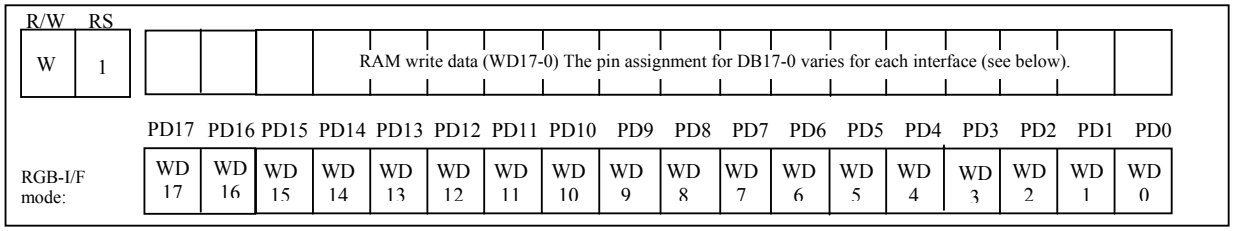
It is not possible to set AD15-0 during the standby mode. AD15-0 must be an address within the area specified with the window addresses.

When the RGB interface is selected (RM = 1), the address AD15-0 is set in the address counter every frame on the falling edge of the VSYNC signal. When the internal clock operation or the VSYNC interface is selected (RM = 0), the address AD15-0 is set when the instruction is executed.

Table 34 GRAM Address Range

AD15–AD0	GRAM Setting
“0000”H – “00AF”H	Bitmap data for G1
“0100”H – “01AF”H	Bitmap data for G2
“0200”H – “02AF”H	Bitmap data for G3
“0300”H – “03AF”H	Bitmap data for G4
:	:
“EC00”H – “ECAF”H	Bitmap data for G237
“ED00”H – “EDAF”H	Bitmap data for G238
“EE00”H – “EEAF”H	Bitmap data for G239
“EF00”H – “EFAF”H	Bitmap data for G240

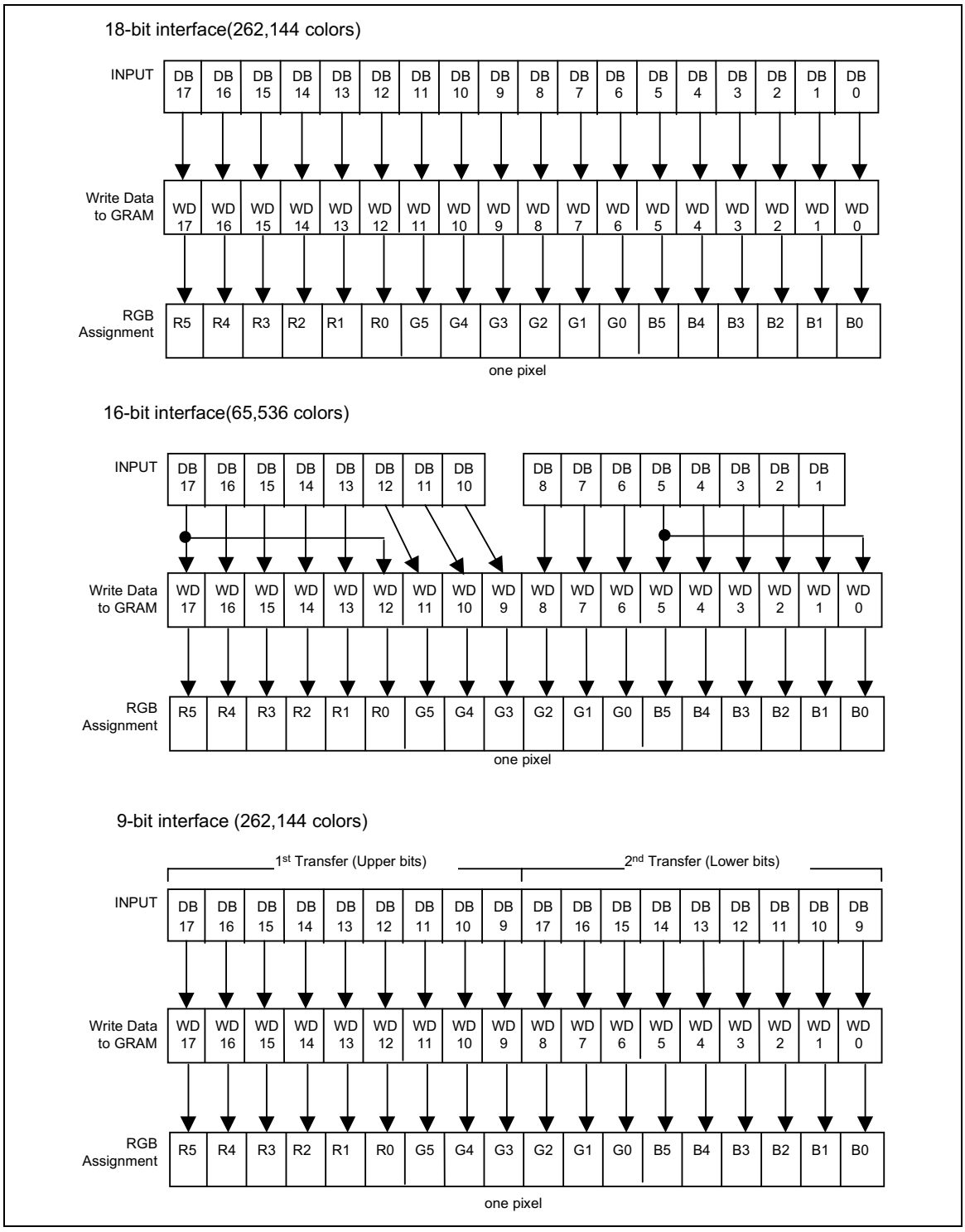
Write Data to GRAM (R22h)



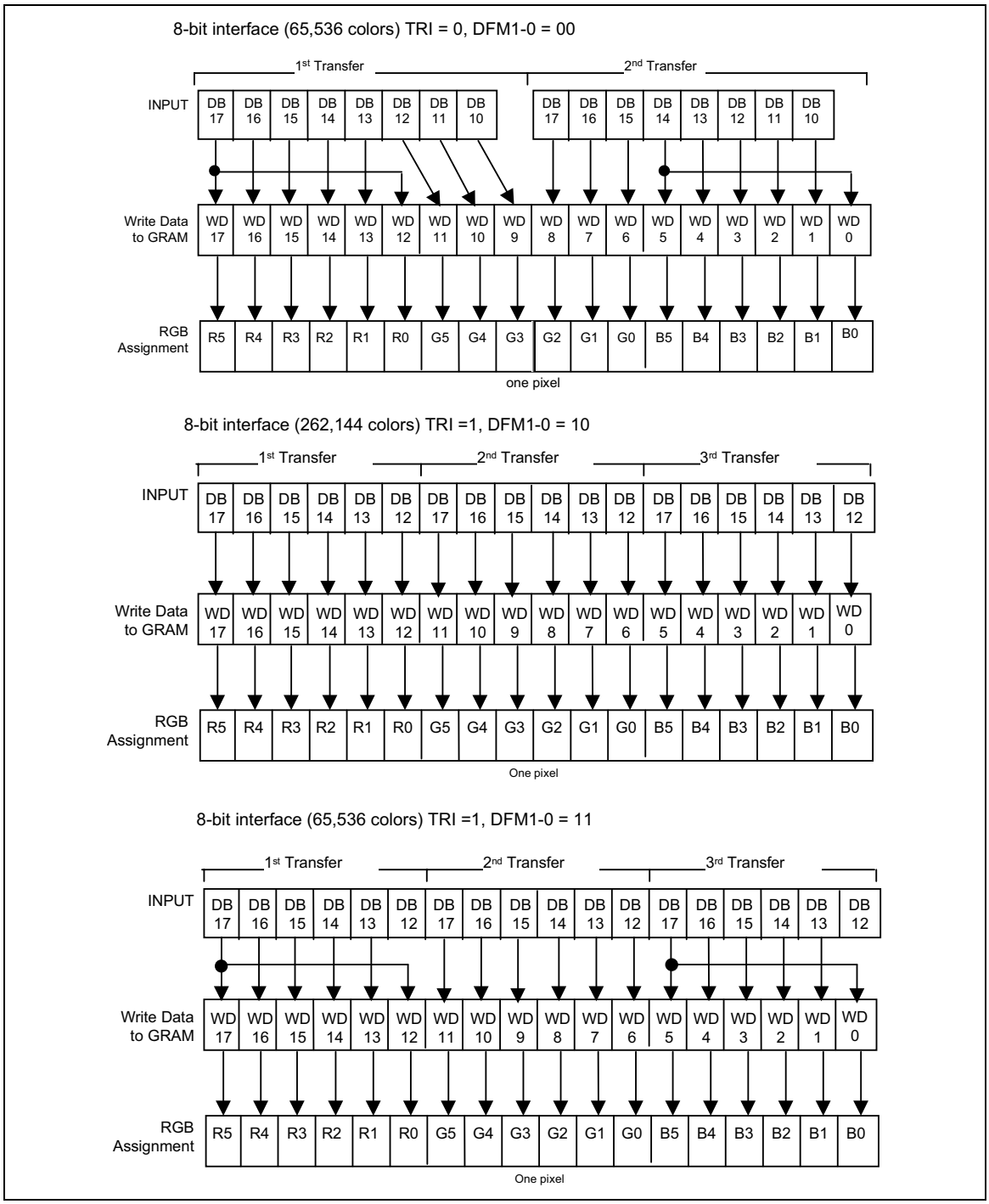
WD17–0: Data are expanded into 18 bits internally before written to the internal GRAM. The way to expand data into 18 bits is different according to the interface in use.

Grayscale levels are selected according to the data written to the GRAM. The GRAM address is automatically updated according to the AM and I/D bits as data are written to the internal GRAM. No access to the internal GRAM is allowed during the standby mode. When the 8 or 16 bit interface mode is selected, data are expanded into the 18-bit format internally by writing the same data as the MSBs of R and B dots to the LSBs of R and B dots respectively. When writing data to the internal GRAM through a system interface while using an RGB interface, make sure that writing operations through the RGB interface and the system interface do not conflict.

When the18-bit RGB interface is selected, 18-bit data are written through the PD17-0 data bus and 262,144 colors are available. When the 16-bit RGB interface is selected, the same data as the MSBs of R and B dots are also written to the LSBs of R and B dots respectively, and 65,536 colors are available.

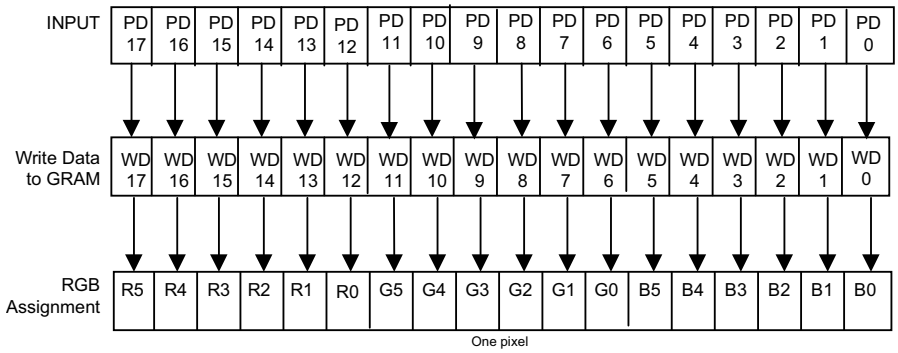


Write data to GRAM (18/16/9-bit interfaces): Bit assignment



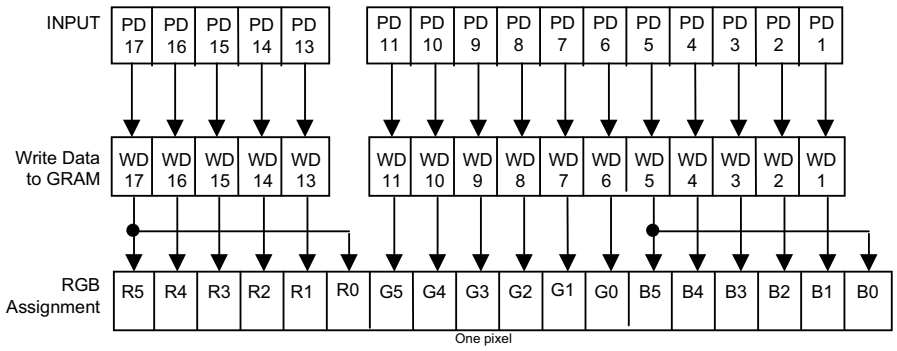
Write data to GRAM (8-bit interface): Bit assignment

18-bit RGB interface (262,144 colors)



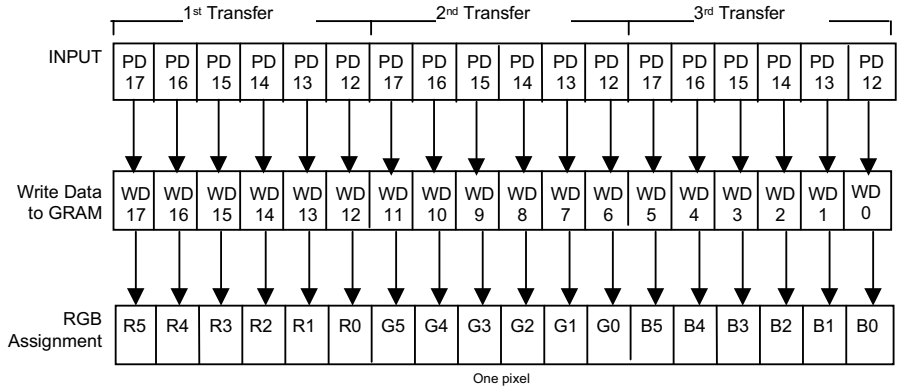
Set the index register when writing data through an RGB interface.

16-bit RGB interface (65,563 colors)



Set the index register when writing data through an RGB interface.

6-bit RGB interface (262,144 colors)



Set the index register when writing data through an RGB interface.

Write data to GRAM (18/16/6-bit RGB interfaces): Bit assignment

GRAM data and LCD output level

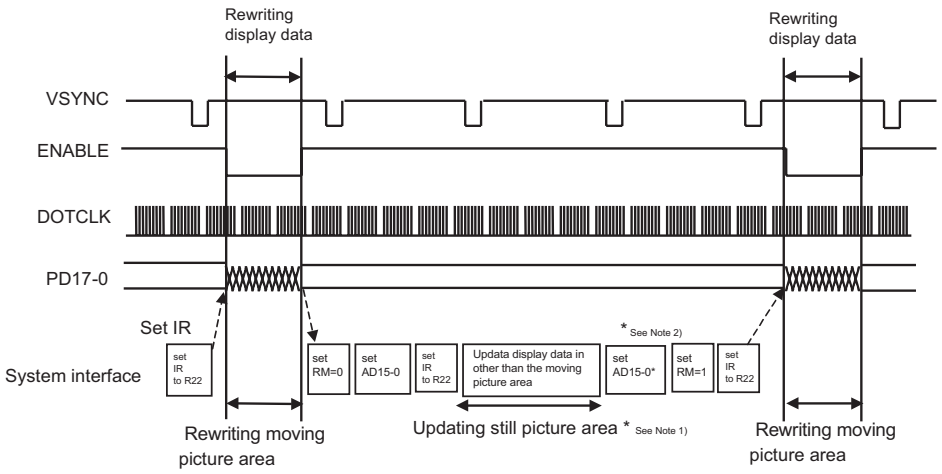
GRAM data settings RGB	Grayscale	
	Negative	Positive
000000	V0	V31
000001	(V0+V1)/2	(V30+V31)/2
000010	V1	V30
000011	(V1+V2)/2	(V29+V30)/2
000100	V2	V29
000101	(V2+V3)/2	(V28+V29)/2
000110	V3	V28
000111	(V3+V4)/2	(V27+V28)/2
001000	V4	V27
001001	(V4+V5)/2	(V26+V27)/2
001010	V5	V26
001011	(V5+V6)/2	(V25+V26)/2
001100	V6	V25
001101	(V6+V7)/2	(V24+V25)/2
001110	V7	V24
001111	(V7+V8)/2	(V23+V24)/2
010000	V8	V23
010001	(V8+V9)/2	(V22+V23)/2
010010	V9	V22
010011	(V9+V10)/2	(V21+V22)/2
010100	V10	V21
010101	(V10+V11)/2	(V20+V21)/2
010110	V11	V20
010111	(V11+V12)/2	(V19+V20)/2
011000	V12	V19
011001	(V12+V13)/2	(V18+V19)/2
011010	V13	V18
011011	(V13+V14)/2	(V17+V18)/2
011100	V14	V17
011101	(V14+V15)/2	(V16+V17)/2
011110	V15	V16
011111	(V15+V16)/2	(V15+V16)/2

GRAM data settings RGB	Grayscale	
	Negative	Positive
100000	V16	V15
100001	(V16+V17)/2	(V14+V15)/2
100010	V17	V14
100011	(V17+V18)/2	(V13+V14)/2
100100	V18	V13
100101	(V18+V19)/2	(V12+V13)/2
100110	V19	V12
100111	(V19+V20)/2	(V11+V12)/2
101000	V20	V11
101001	(V20+V21)/2	(V10+V11)/2
101010	V21	V10
101011	(V21+V22)/2	(V9+V10)/2
101100	V22	V9
101101	(V22+V23)/2	(V8+V9)/2
101110	V23	V8
101111	(V23+V24)/2	(V7+V8)/2
110000	V24	V7
110001	(V24+V25)/2	(V6+V7)/2
110010	V25	V6
110011	(V25+V26)/2	(V5+V6)/2
110100	V26	V5
110101	(V26+V27)/2	(V4+V5)/2
110110	V27	V4
110111	(V27+V28)/2	(V3+V4)/2
111000	V28	V3
111001	(V28+V29)/2	(V2+V3)/2
111010	V29	V2
111011	(V29+V30)/2	(V1+V2)/2
111100	V30	V1
111101	(V30+V31)/2	(V0+V1)/2
111110	(V30+2xV31)/3	(2xV0+V1)/3
111111	V31	V0

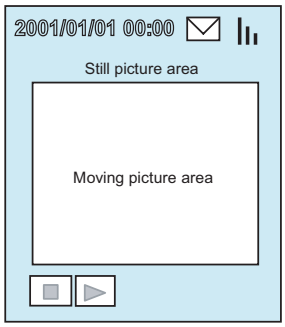
RAM Access through RGB-I/F and System I/F

In RGB interface mode, the HD66789R stores all display data in the internal RAM so that only the data of the moving picture area are transferred only in the frames of rewriting display data through the RGB interface. The HD66789R accesses RAM in high speed and reduces power consumption required for moving picture display by using high speed write mode (HWM = 1) and the window address function. In the frames other than frames of rewriting display data, the data displayed in the area other than the moving picture area can be rewritten through the system interface.

In RGB interface mode, data are written to RAM in synchronization with DOTCLK during ENABLE = "Low". To access RAM through the system interface while using the RGB interface, set ENABLE "High" to stop writing through the RGB interface. To start accessing RAM through the RGB interface after accessing RAM through the system interface, wait at least for a write/read bus cycle time. When the RAM access through the RGB interface and that through the system interfaces conflict, data will not properly be written to the internal GRAM.



Note1) The address AD15-0 is set at AC on every falling edge of VSYNC in RGB interface.
Note2) Set the address AD15-0 at AC and the index register to R22h (RAM data write/read) before RAM access through RGB interface.



Read Data Read from GRAM (R22h)

R/W	RS	
R	1	RAM Read data (RD17-0) The pin assignment for DB17-0 varies for each interface (see below).

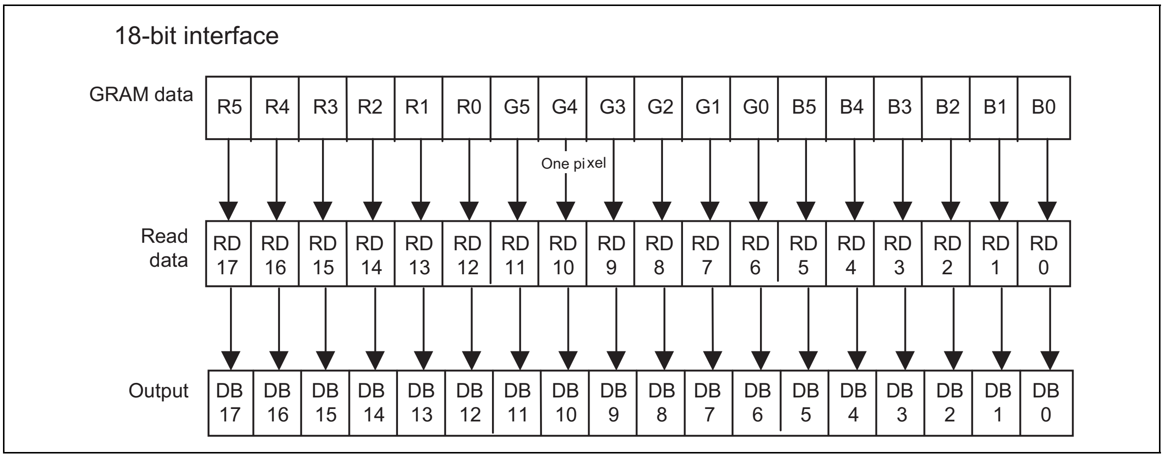
RD17–0: Reads 18-bit data from the internal GRAM. The assignment of data read out from GRAM to the DB[17:0] pins is different according to an interface.

When data are read out from the internal GRAM to the microcomputer, the first-word data read immediately after executing the RAM address set (R21h) are buffered in the internal read-data latch and data on the data bus (DB17–0) become invalid. The second-word data are read out as valid data.

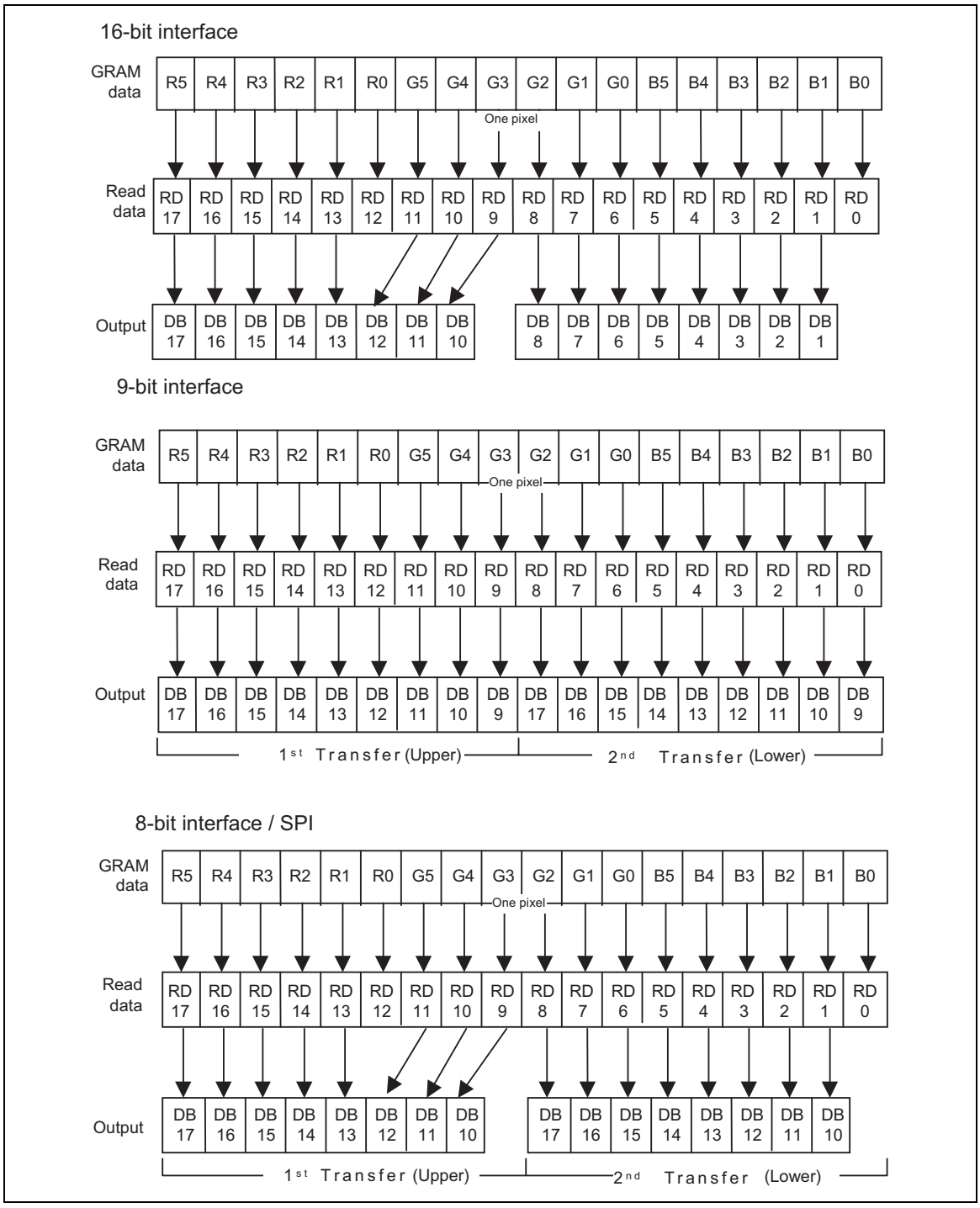
The data in the read-data latch are used when the HD66789R executes internal bit processing, such as logical operations, to complete the bit processing with a single read operation. Note that bit processing is always executed on the data internally expanded into 18 bits.

When the 8 or 16-bit interface is selected, the data in the LSBs of R and B dots are not read out.

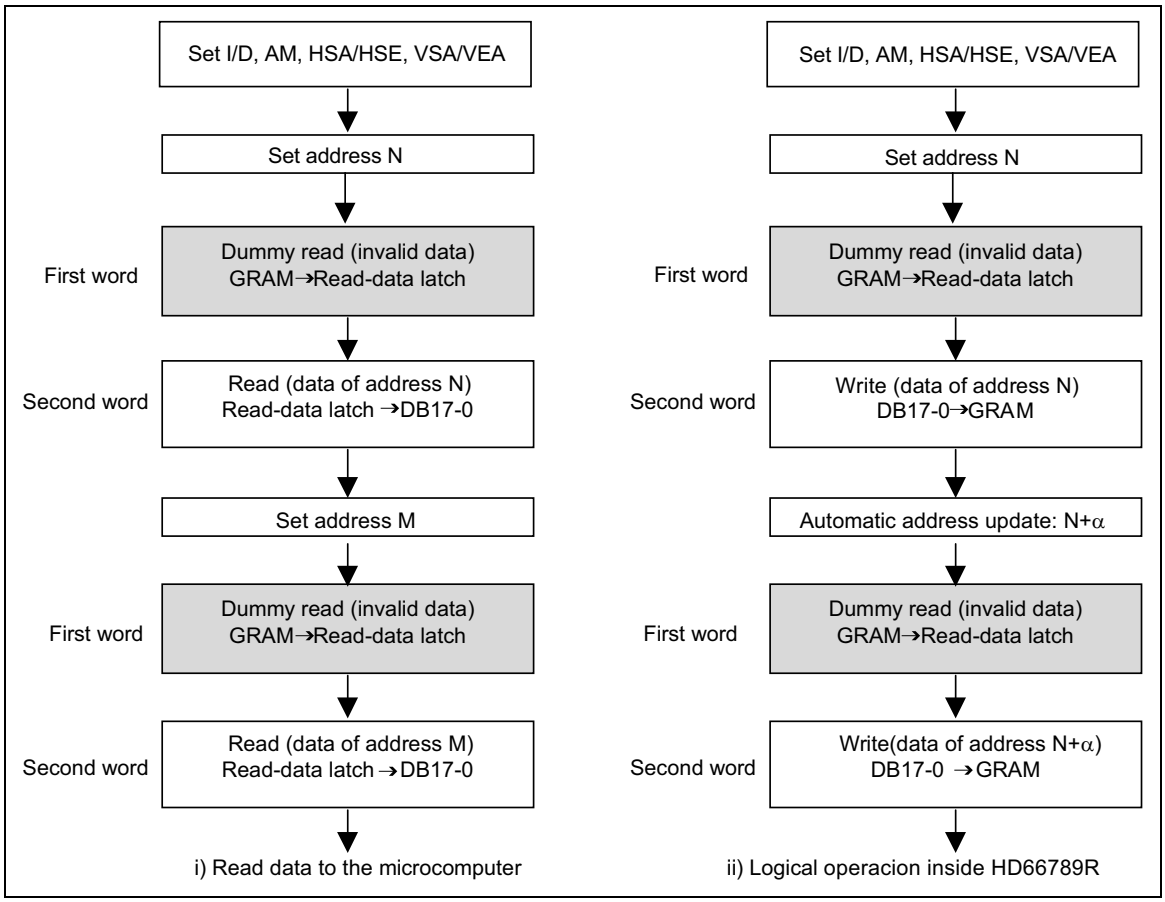
This function is not available with the RGB interface.



Read data from GRAM: 18-bit interface



Read data from GRAM: 16/9/8-bit interface



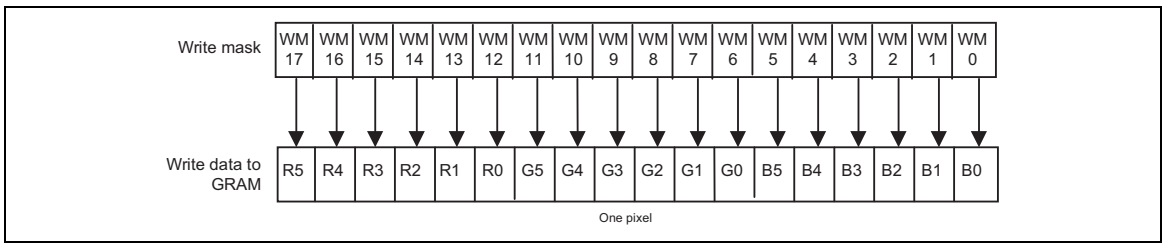
GRAM read sequence

RAM Write Data Mask (R23h)
RAM Write Data Mask (R24h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	WM 11	WM 10	WM 9	WM 8	WM 7	WM 6	0	0	WM 5	WM 4	WM 3	WM 2	WM 1	WM 0
W	1	0	0	0	0	0	0	0	0	0	0	WM 17	WM 16	WM 15	WM 14	WM 13	WM 12

WM17–0: Write-mask data in unit of bits when writing data to the internal GRAM. For example, if WM17 = 1, WM17 write-mask the MSB of GRAM write data so that it will not be written to the GRAM. WM16~WM0 also write-mask the GRAM write data of the corresponding bits when they are set to "1". For details, see the "Graphics Operation Function" section.

Note that the write mask function is always executed on 18-bit GRAM write data.. This function is not available with the RGB interface.



RAM write data mask

γ Control (R30h to R39h)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30	W	1	0	0	0	0	0	PKP1[2]	PKP1[1]	PKP1[0]	0	0	0	0	0	PKP0[2]	PKP0[1]	PKP0[0]
R31	W	1	0	0	0	0	0	PKP3[2]	PKP3[1]	PKP3[0]	0	0	0	0	0	PKP2[2]	PKP2[1]	PKP2[0]
R32	W	1	0	0	0	0	0	PKP5[2]	PKP5[1]	PKP5[0]	0	0	0	0	0	PKP4[2]	PKP4[1]	PKP4[0]
R33	W	1	0	0	0	0	0	PRP1[2]	PRP1[1]	PRP1[0]	0	0	0	0	0	PRP0[2]	PRP0[1]	PRP0[0]
R34	W	1	0	0	0	0	0	PKN1[2]	PKN1[1]	PKN1[0]	0	0	0	0	0	PKN0[2]	PKN0[1]	PKN0[0]
R35	W	1	0	0	0	0	0	PKN3[2]	PKN3[1]	PKN3[0]	0	0	0	0	0	PKN2[2]	PKN2[1]	PKN2[0]
R36	W	1	0	0	0	0	0	PKN5[2]	PKN5[1]	PKN5[0]	0	0	0	0	0	PKN4[2]	PKN4[1]	PKN4[0]
R37	W	1	0	0	0	0	0	PRN1[2]	PRN1[1]	PRN1[0]	0	0	0	0	0	PRN0[2]	PRN0[1]	PRN0[0]
R38	W	1	0	0	0	VRP1[4]	VRP1[3]	VRP1[2]	VRP1[1]	VRP1[0]	0	0	0	0	VRP0[3]	VRP0[2]	VRP0[1]	VRP0[0]
R39	W	1	0	0	0	VRN1[4]	VRN1[3]	VRN1[2]	VRN1[1]	VRN1[0]	0	0	0	0	VRN0[3]	VRN0[2]	VRN0[1]	VRN0[0]

PKP5-0[2:0] : γ fine adjustment registers for the positive polarity
PRP1-0[2:0] : γ gradient adjustment registers for the positive polarity
PKN5-0[2:0] : γ fine adjustment registers for the negative polarity
PRN1-0[2:0] : γ gradient adjustment registers for the negative polarity
VRP0[3:0]/VRP1[4:0] : amplitude adjustment resistor for the positive polarity
VRN0[3:0]/VRN1[4:0] : amplitude average adjustment resistor for the negative polarity

For details, see the "γ adjustment" section.

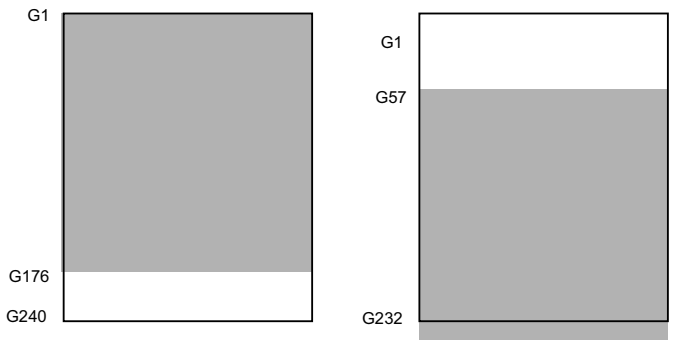
Gate Scan Position (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN4-0: Set the position of starting scan by the gate driver. Set the SCN4-0 bits to drive the gate lines to be used.

Table 35

SCN4	SCN3	SCN2	SCN1	SCN0	Scan Start Position	
					GS = 0	GS = 1
0	0	0	0	0	G1	G240
0	0	0	0	1	G9	G232
0	0	0	1	0	G17	G224
:	:	:	:	:	:	:
1	1	0	1	0	G209	G32
1	1	0	1	1	G217	G24
1	1	1	0	0	G225	G16



GS = 0
NL = 10101
SCN4-0 = 00000

GS = 0
NL = 10101
SCN4-0 = 00111

Note: Set NL4-0 and SCN4-0 so that the number for the end position of the gate line scan will not exceed 240.

Vertical Scroll Control (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7–0: Specifies the number of lines to scroll in the vertical direction from 0 to 240. The data that is scrolled out as a result of vertical scrolling are displayed from the first line of the physical display. The VL7-0 bits are enabled when the first screen vertical scroll enable bit VLE1 = 1 or the second panel vertical scroll enable bit VLE2 = 1. When VLE2-1 = 00, the display data are shown at the originally designated position. This function is not available with the external display interface.

Table 36

VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	Scrolling lines
0	0	0	0	0	0	0	0	0 line
0	0	0	0	0	0	0	1	1 line
0	0	0	0	0	0	1	0	2 lines
:	:	:	:	:	:	:	:	:
1	1	1	0	1	1	1	0	238 lines
1	1	1	0	1	1	1	1	239 lines

Note: Do no set the value that exceeds 240 to VL7-0.

1st-Screen Drive Position (R42h)

2nd-Screen Drive Position (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
W	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS17-10: Specifies the gate line from which the first screen data are shown. The number of the gate line is the value set with the SS17-10 bits + 1.

SE17-10: Specifies the gate line which is the end line to show the first screen data. The number of the gate line is the value set with the SE17-10 bits + 1. For instance, when SS17-10 = “07”H and SE17-10 = “10”H, the first screen is shown on the gate lines from G8 to G17, and gate lines G1 to G7 and G18 thereafter are driven to show black screen. Make sure that SS17-10 ≤ SE17-10 ≤ “EF”H. For details, see the “Partial Display Function” section.

SS27-20: Specifies the gate line from which the second screen data are shown. The number of the gate line is the value set with the SS27-20 bits + 1. The second screen is driven when SPT = 1.

SE27-20: Specifies the gate line that is the end line to show the second screen data. The number of the gate line is the value set with the SE27-20 bits + 1. For instance, when SPT = 1, and SS27-20 = "20"H, SE27-20 = "4F"H, the second screen is shown on the gate lines from G33 to G80.

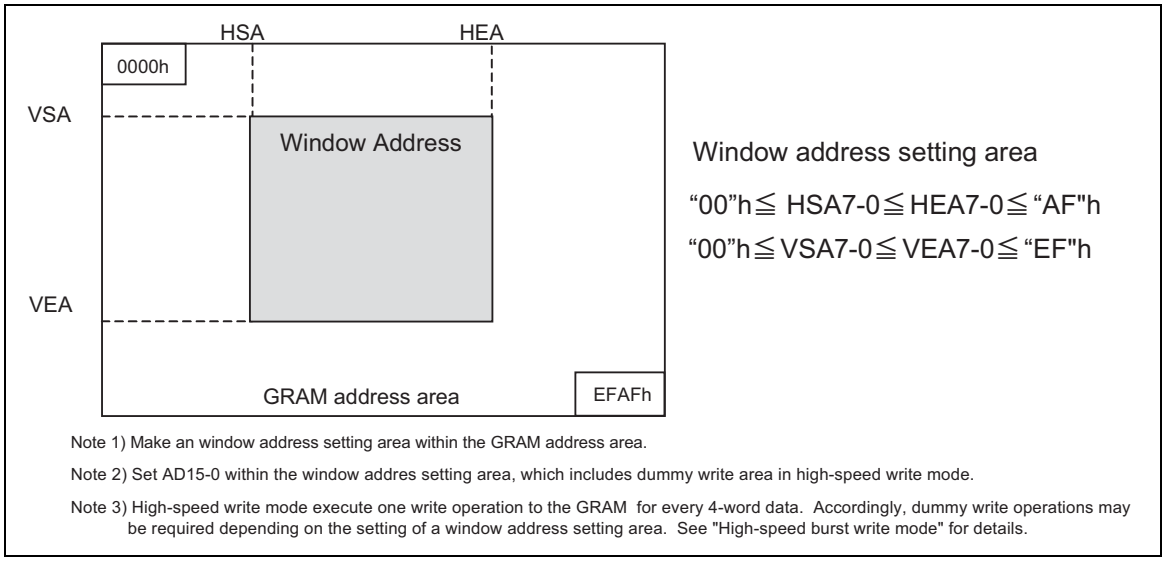
Make sure that SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ "EF"H. For details, see the "Partial Display Function" section.

Horizontal RAM Address Position (R44h)
Vertical RAM Address Position (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0
W	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA7-0/HEA7-0: HSA7-0 and HEA7-0 represent the addresses of the start and end positions of the window address area, respectively in horizontal direction. Data are written to the internal GRAM horizontally within the area specified with HEA7-0 and HSA7-0. Make sure to set the AD15-0 before the RAM write operation. In setting these bits, make sure "00"h ≤ HSA7-0 ≤ HEA7-0 ≤ "AF"h.

VSA7-0/VEA7-0: VSA7-0 and VEA7-0 represent the addresses of the start and end positions of the window address area, respectively in vertical direction. Data are written to the internal GRAM vertically within the area specified with VEA7-0 and VSA7-0. Make sure to set the AD15-0 before the RAM write operation. In setting these bits, make sure "00"h ≤ VSA7-0 ≤ VEA7-0 ≤ "EF"h.



Note 1) Make an window address setting area within the GRAM address area.

Note 2) Set AD15-0 within the window addres setting area, which includes dummy write area in high-speed write mode.

Note 3) High-speed write mode execute one write operation to the GRAM for every 4-word data. Accordingly, dummy write operations may be required depending on the setting of a window address setting area. See "High-speed burst write mode" for details.

GRAM address and window address setting areas

Instruction List

Main Category		Sub Category		Upper Code								Lower Code								Note
Upper Index	Index		Command	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0	
-	Index		Index	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID21	ID0	
SR	Status Read		Status Read	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	
0*	Display Control	00h	Oscillation Start	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	
			Device Code Read	0	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	789
		01h	Driver Output Control	0	VSPL (0)	HSPL (0)	DPL (0)	EPL (0)	SM (0)	GS (0)	SS (0)	0	0	0	NL4 (1)	NL3 (1)	NL2 (1)	NL1 (0)	NL0 (1)	
		02h	LCD AC driving Control	0	0	0	0	FLD (0)	FLD0 (1)	B/C (0)	EOR (0)	0	0	NW5 (0)	NW4 (0)	NW3 (0)	NW2 (0)	NW1 (0)	NW0 (0)	
		03h	Entry Mode	TRI (0)	DFM1 (0)	DFM0 (0)	BGR (0)	0	0	HWM (0)	0	0	0	ID1 (1)	ID0 (1)	AM (0)	LG2 (0)	LG1 (0)	LG0 (0)	
		04h	Compare Register (1)	0	0	CP11 (0)	CP10 (0)	CP9 (0)	CP8 (0)	CP7 (0)	CP6 (0)	0	0	CP5 (0)	CP4 (0)	CP3 (0)	CP2 (0)	CP1 (0)	CP0 (0)	
		05h	Compare Register (2)	0	0	0	0	0	0	0	0	0	0	CP17 (0)	CP16 (0)	CP15 (0)	CP14 (0)	CP13 (0)	CP12 (0)	
		06h	Setting Disabled																	
		07h	Display Control (1)	0	0	0	PT1 (0)	PT0 (0)	VLE2 (0)	VLE1 (0)	SPT (0)	0	0	GON 0	DTE (0)	CL (0)	REV (0)	D1 (0)	D0 (0)	
		08h	Display Control (2)	0	0	0	0	FP3 (1)	FP2 (0)	FP1 (0)	FP0 (0)	0	0	0	0	BP3 (1)	BP2 (0)	BP1 (0)	BP0 (0)	
		09h	Display Control (3)	0	0	0	0	0	0	0	0	0	0	PTG1 (0)	PTG0 (0)	ISC3 (0)	ISC2 (0)	ISC1 (0)	ISC0 (0)	
		0Ah	Setting Disabled																	
		0Bh	Frame Cycle Adjustment Control	NO1 (0)	NO0 (0)	SDT1 (0)	SDT0 (0)	EQ1 (0)	EQ0 (0)	DIV1 (0)	DIV0 (0)	0	0	0	0	RTN3 (0)	RTN2 (0)	RTN1 (0)	RTN0 (0)	
		0Ch	External Display Interface Control	0	0	0	0	0	0	0	RM (0)	0	0	DM1 (0)	DM0 (0)	0	0	RIM1 (0)	RIM0 (0)	
		0Dh	Setting Disabled																	
		0Eh	Setting Disabled																	
		0Fh	Setting Disabled																	
1*	Power Control	10h	Power Control (1)	0	SAP2 (0)	SAP1 (0)	SAP0 (0)	0	BT2 (0)	BT1 (0)	BT0 (0)	0	AP2 (0)	AP1 (0)	AP0 (0)	0	DK (1)	SLP (0)	STB (0)	
		11h	Power Control (2)	0	0	0	0	0	DC12 (0)	DC11 (0)	DC10 (0)	0	DC02 (0)	DC01 (0)	DC00 (0)	0	VC2 (0)	VC1 (0)	VC0 (0)	
		12h	Power Control (3)	0	0	0	0	0	0	0	0	0	0	0	PON (0)	VRH3 (0)	VRH2 (0)	VRH1 (0)	VRH0 (0)	
		13h	Power Control (4)	0	0	VCOM G	VDV4 (0)	VDV3 (0)	VDV2 (0)	VDV1 (0)	VDV0 (0)	0	0	0	VCM4 (0)	VCM3 (0)	VCM2 (0)	VCM1 (0)	VCM0 (0)	
		14h	Setting Disabled																	
		15h	Setting Disabled																	
		16h	Setting Disabled																	
		17h	Setting Disabled																	
		18h	Setting Disabled																	
		19h	Setting Disabled																	
		1Ah	Setting Disabled																	
		1Bh	Setting Disabled																	
		1Ch	Setting Disabled																	
		1Dh	Setting Disabled																	
		1Eh	Setting Disabled																	
		1Fh	Setting Disabled																	
2*	RAM Access	20h	Setting Disabled																	
		21h	RAM Address Set	AD15 (0)	AD14 (0)	AD13 (0)	AD12 (0)	AD11 (0)	AD10 (0)	AD9 (0)	AD8 (0)	AD7 (0)	AD6 (0)	AD5 (0)	AD4 (0)	AD3 (0)	AD2 (0)	AD1 (0)	AD0 (0)	
		22h	RAM data Write/Read	RAM WD17-0 /RAM (RD17-0)																
		23h	RAM Write Data Mask (1)	0	0	WM11 (0)	WM10 (0)	WM9 (0)	WM8 (0)	WM7 (0)	WM6 (0)	0	0	WM5 (0)	WM4 (0)	WM3 (0)	WM2 (0)	WM1 (0)	WM0 (0)	
		24h	RAM Write Data Mask (2)	0	0	0	0	0	0	0	0	0	0	WM17 (0)	WM16 (0)	WM15 (0)	WM14 (0)	WM13 (0)	WM12 (0)	
		25h	Setting Disabled																	
		26h	Setting Disabled																	
		27h	Setting Disabled																	
		28h	Setting Disabled																	
		29h	Setting Disabled																	
		2Ah	Setting Disabled																	
		2Bh	Setting Disabled																	
		2Ch	Setting Disabled																	
		2Dh	Setting Disabled																	
		2Eh	Setting Disabled																	
		2Fh	Setting Disabled																	
3*	γ Control	30h	γ Control (1)	0	0	0	0	0	PKP12 (0)	PKP11 (0)	PKP10 (0)	0	0	0	0	0	PKP02 (0)	PKP01 (0)	PKP00 (0)	
		31h	γ Control (2)	0	0	0	0	0	PKP32 (0)	PKP31 (0)	PKP30 (0)	0	0	0	0	0	PKP22 (0)	PKP21 (0)	PKP20 (0)	
		32h	γ Control (3)	0	0	0	0	0	PKP52 (0)	PKP51 (0)	PKP50 (0)	0	0	0	0	0	PKP42 (0)	PKP41 (0)	PKP40 (0)	
		33h	γ Control (4)	0	0	0	0	0	PRP12 (0)	PRP11 (0)	PRP10 (0)	0	0	0	0	0	PRP02 (0)	PRP01 (0)	PRP00 (0)	
		34h	γ Control (5)	0	0	0	0	0	PKN12 (0)	PKN11 (0)	PKN10 (0)	0	0	0	0	0	PKN02 (0)	PKN01 (0)	PKN00 (0)	
		35h	γ Control (6)	0	0	0	0	0	PKN32 (0)	PKN31 (0)	PKN30 (0)	0	0	0	0	0	PKN22 (0)	PKN21 (0)	PKN20 (0)	
		36h	γ Control (7)	0	0	0	0	0	PKN52 (0)	PKN51 (0)	PKN50 (0)	0	0	0	0	0	PKN42 (0)	PKN41 (0)	PKN40 (0)	
		37h	γ Control (8)	0	0	0	0	0	PRN12 (0)	PRN11 (0)	PRN10 (0)	0	0	0	0	0	PRN02 (0)	PRN01 (0)	PRN00 (0)	
		38h	γ Control (9)				VRP14 (0)	VRP13 (0)	VRP12 (0)	VRP11 (0)	VRP10 (0)					VRP03 (0)	VRP02 (0)	VRP01 (0)	VRP00 (0)	
		39h	γ Control (10)				VRN14 (0)	VRN13 (0)	VRN12 (0)	VRN11 (0)	VRN10 (0)					VRN03 (0)	VRN02 (0)	VRN01 (0)	VRN00 (0)	
		3Ah	Setting Disabled																	
		3Bh	Setting Disabled																	
		3Ch	Setting Disabled																	
		3Dh	Setting Disabled																	
		3Eh	Setting Disabled																	
		3Fh	Setting Disabled																	
4*	Coordination Control	40h	Gate Scan Start Position	0	0	0	0	0	0	0	0	0	0	0	SCN4 (0)	SCN3 (0)	SCN2 (0)	SCN1 (0)	SCN0 (0)	
		41h	Vertical Scroll Control	0	0	0	0	0	0	0	0	VL7 (0)	VL6 (0)	VL5 (0)	VL4 (0)	VL3 (0)	VL2 (0)	VL1 (0)	VL0 (0)	
		42h	First Screen Driving Position	SE17 (1)	SE16 (1)	SE15 (1)	SE14 (1)	SE13 (1)	SE12 (1)	SE11 (1)	SE10 (1)	SS17 (0)	SS16 (0)	SS15 (0)	SS14 (0)	SS13 (0)	SS12 (0)	SS11 (0)	SS10 (0)	
		43h	Second Screen Driving Position	SE27 (1)	SE26 (1)	SE25 (1)	SE24 (1)	SE23 (1)	SE22 (1)	SE21 (1)	SE20 (1)	SS27 (0)	SS26 (0)	SS25 (0)	SS24 (0)	SS23 (0)	SS22 (0)	SS21 (0)	SS20 (0)	
		44h	Horizontal RAM Address Position	HEA7 (1)	HEA6 (0)	HEA5 (1)	HEA4 (0)	HEA3 (1)	HEA2 (1)	HEA1 (1)	HEA0 (1)	HSA7 (0)	HSA6 (0)	HSA5 (0)	HSA4 (0)	HSA3 (0)	HSA2 (0)	HSA1 (0)	HSA0 (0)	
		45h	Vertical RAM Address Position	VEA7 (1)	VEA6 (1)	VEA5 (1)	VEA4 (0)	VEA3 (1)	VEA2 (1)	VEA1 (1)	VEA0 (1)	VSA7 (0)	VSA6 (0)	VSA5 (0)	VSA4 (0)	VSA3 (0)	VSA2 (0)	VSA1 (0)	VSA0 (0)	
		46h	Setting Disabled																	
		47h	Setting Disabled																	
		48h	Setting Disabled																	
		49h	Setting Disabled																	
		4Ah	Setting Disabled																	
		4Bh	Setting Disabled																	
		4Ch	Setting Disabled																	
		4Dh	Setting Disabled																	
		4Eh	Setting Disabled																	
		4Fh	Setting Disabled																	
5*		*	Setting Disabled																	
6*		*	Setting Disabled																	
7*		*	Setting Disabled																	

Note 1) The numeral in parenthesis in each bit cell is a default value.
Note 2) Do not access to the"Setting Disabled" indexes.

Reset Function

The HD66789R is internally initialized with a RESET input. During the reset period, the HD66789R is in a busy state and no access to the instructions or GRAM data from the MPU is accepted. The RESET period must be secured for at least 1ms. In case of power-on reset, wait until the RC oscillation frequency stabilizes after the power supply is turned on (10 ms). During this period, do not access the internal GRAM nor make the initialization setting.

Default State of Instructions:

a. Start oscillator
b. Driver output control (NL4-0 = “11101”, SS = “0”, EPL = “0”, DPL = “0”, HSPL = “0”, VSPL = “0”, GS = “0”, SM= “0”)
c. Liquid crystal alternating current drive control (FLD1-0 = “01”, B/C = “0”, EOR = “0”, NW5–0 = “000000”)
d. Entry mode set (HWM = “0”, I/D1-0 = “11”: Increment by 1, AM = “0”: Horizontal direction, LG2–0 = “000”: Replace mode, BGR = “0”, TRI = “0”, DFM1-0 = “00”)
e. Compare register (CP17–0: “00 0000 0000 0000 0000”)
f. Display control 1 (PT1-0 = “00”, VLE2-1 = “00”: No vertical scroll, SPT = “0”, DTE = “0”, CL = “0”: 65,536-color mode, REV = “0”, D1-0 = “00”: Display OFF, GON = “0”)
g. Display control 2 (BP3-0 = “1000”, FP3-0 = “1000”)
h. Display control 3 (PTG1-0 = “00”, ISC3-0 = “0000”)
i. Frame cycle control (NO1-0 = “00”, SDT1-0 = “00”, EQ1-0 = “00”: No equalization, DIV1-0 = “00”: clock/1, RTN3-0 = “0000”: 16 clocks per 1H period)
j. External display interface (RIM1-0 = “00”: 18-bit RGB interface, DM1-0 = “00”: internal clock operation, RM = “0”: System interface)
k. Power control 1 (SAP2-0 = “000”, BT2-0 = “000”, AP2–0 = “000”: liquid crystal power off, DK = “1”: DCDC1 off, SLP = “0”, STB = “0”: release from the standby mode)
l. Power control 2 (DC12-10 = “000”, DC02-00 = “000”, VC2-0 = “000”)
m. Power control 3 (PON = “0”, VRH3-0 = “0000”)
n. Power control 4 (VCOMG = “0”, VDV4-0 = “00000”, VCM4-0 = “00000”)
o. RAM address set (AD15–0 = “0000”H)
p. RAM write data mask (WM17–0 = “18’h00000”: No write-mask)
q. γ control
(PKP02-00 = “000”, PKP12-10 = “000”, PKP22-20 = “000”, PKP32-30 = “000”, PKP42-40 = “000”, PKP52-50 = “000”, PRP02-00 = “000”, PRP12-10 = “000”)
(PKN02-00 = “000”, PKN12-10 = “000”, PKN22-20 = “000”, PKN32-30 = “000”, PKN42-40 = “000”, PKN52-50 = “000”, PRN02-00 = “000”, PRN12-10 = “000”)
(VRP14-10 = “00000”, VRP03-00 = “0000”, VRN14-10 = “00000”, VRN03-00 = “0000”)
r. Gate driver scan start position SCN4-0 = “00000”
s. Vertical scroll (VL7–0 = “00000000”)
t. 1st split screen (SE17-10 = “11111111”, SS17-10 = “00000000”)
u. 2nd split screen (SE27-20 = “11111111”, SS27-20 = “00000000”)
v. Horizontal RAM address position (HEA7-0 = “10000011”, HSA7-0 = “00000000”)
w. Vertical RAM address position (VEA7-0 = “10101111”, VSA7-0 = “00000000”)

GRAM Data Initialization: The data in the internal GRAM are not initialized by the RESET input. Initialize using software during a display OFF period (D1–0 = “00”).

Default state of Output Pins:

a. Liquid crystal driver output pins (source outputs): All output the GND level
b. Oscillator output pin (OSC2): Oscillate

Interface Specifications

The HD66789R has a system interface to make an instruction setting and an external display interface to display a moving picture. The HD66789R can select an optimum interface according to the kind of display (moving or still picture) to transfer data efficiently.

As an external display interface, the HD66789R has the RGB interface and the VSYNC interface, which update screens without flicker.

In RGB-I/F mode, display operations are executed in synchronization with VSYNC, HSYNC, and DOTCLK. Display data are written according to the values of data enable signal (ENABLE), and display data in PD17-0 in synchronization with VSYNC, HSYNC, and DOTCLK. By writing display data to the internal GRAM, the HD66789R minimizes data transfers only when switching the frames of a moving picture. The window address makes it possible to specify the moving picture RAM area to be overwritten and display simultaneously the moving picture data and the pre-written RAM data in other than the moving picture area. In RGB and VSYNC interface modes, use high speed write mode (HWM = 1) when writing data to RAM in order to access RAM in high speed with less power consumption when displaying a moving picture.

In VSYNC interface mode, the frame synchronization signal (VSYNC) synchronizes the internal display operation. The VSYNC interface enables a moving picture display while using a system interface by writing data to the internal GRAM at more than a certain speed in synchronization with the falling edge of VSYNC. In this case, there are constraints in the speed and methods to write data to RAM.

The HD66789R can operate among the following 4 modes according to the display state. The display operating mode is set with the external interface control register (R00Ch). To switch between the different modes, follow the mode-switching sequence.

Table 37

Operation Mode	RAM Access Setting (RM)	Display Operation Mode (DM1-0)
Internal operating clock only (Displaying still pictures)	System interface (RM = 0)	Internal operating clock (DM1-0 = 00)
RGB interface (1) (Displaying moving pictures)	RGB interface (RM = 1)	RGB interface (DM1-0 = 01)
RGB interface (2) (Rewriting still pictures while displaying moving pictures)	System interface (RM = 0)	RGB interface (DM1-0 = 01)
VSYNC interface (Displaying moving pictures)	System interface (RM = 0)	VSYNC interface (DM1-0 = 10)

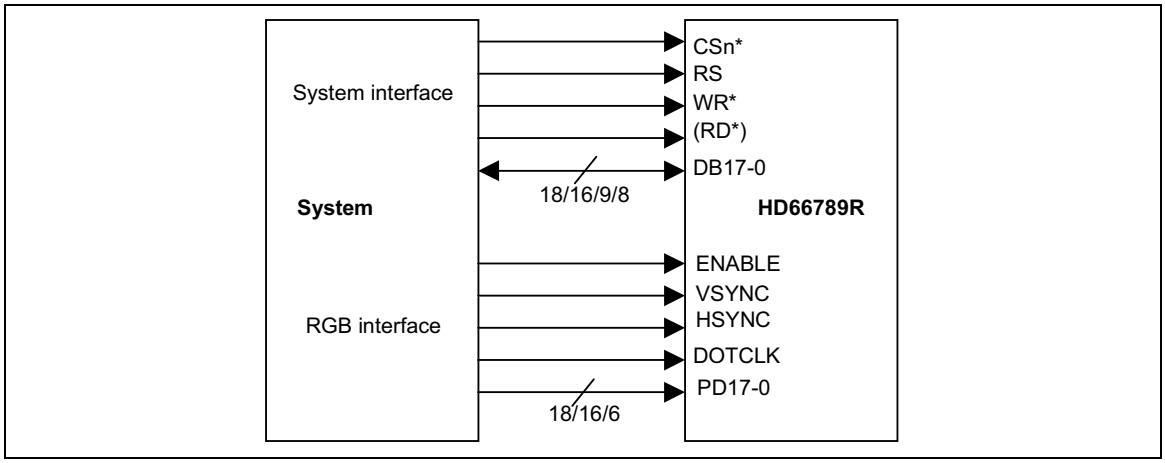
Note 1) Instructions are set only through a system interface.

Note 2) The RGB-I/F and the VSYNC-I/F are not used simultaneously.

Note 3) Do not make changes to the RGB-I/F mode (RIM-0) while an RGB I/F is in operation.

Note 4) See the “External Display Interface” section for the flowcharts of mode transitions.

Note 5) Use the high-speed write mode (HWM = 1) in RGB-I/F and VSYNC-I/F modes.



Interfaces and HD66789R

System Interface

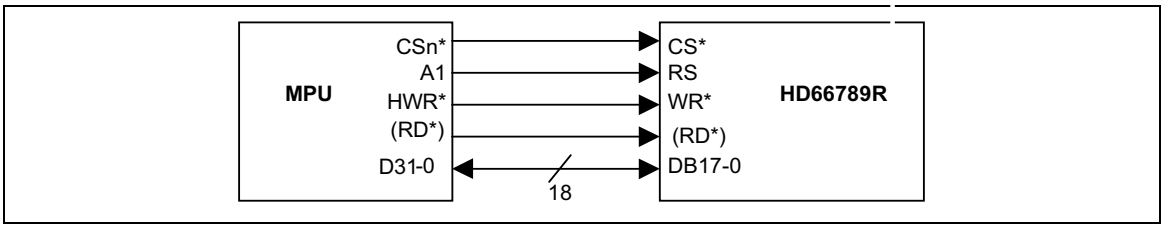
The following shows the available system interfaces with the HD66789R. The IM3-0 pins are used to select the interface. The system Interface enables instruction setting and RAM access.

Table 38

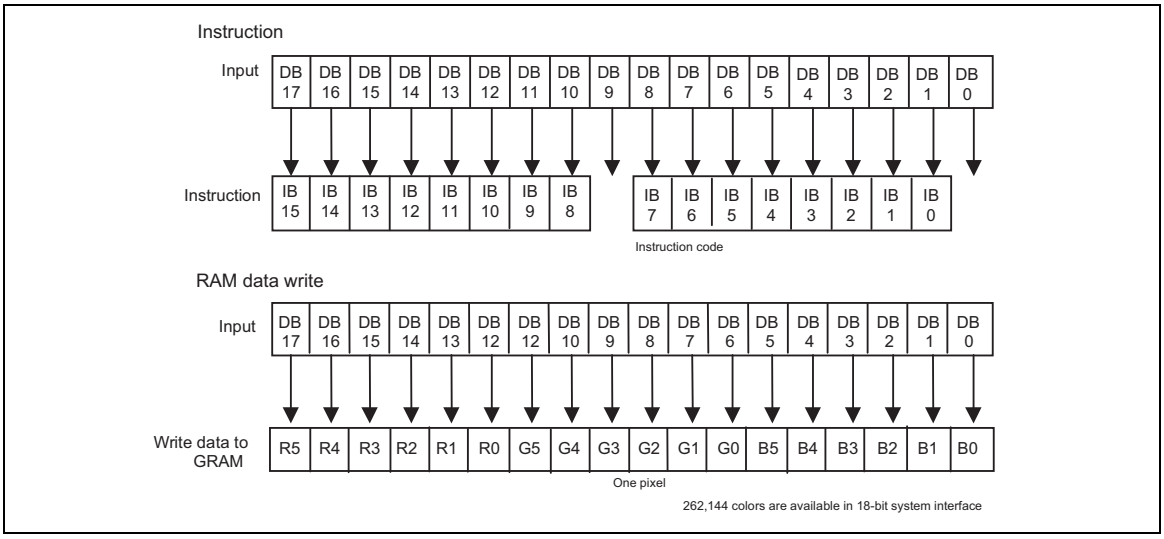
IM3	IM2	IM1	IM0	MPU-Interface Mode	DB Pins in use
0	0	0	0	Setting disabled	-
0	0	0	1	Setting disabled	-
0	0	1	0	80-system 16-bit interface	DB17 to 10 and 8-to-1
0	0	1	1	80-system 8-bit interface	DB17 to 10
0	1	0	*	Serial peripheral interface (SPI)	DB1-0
0	1	1	*	Setting disabled	-
1	0	0	0	Setting disabled	-
1	0	0	1	Setting disabled	-
1	0	1	0	80-system 18-bit interface	DB17 to 0
1	0	1	1	80-system 9-bit interface	DB17 to 9
1	1	*	*	Setting disabled	-

80-system 18-bit interface

The 80-system 18-bit parallel data transfer is selected by setting the IM3/2/1/0 pins to IOVcc/GND/IOVcc/GND levels respectively.



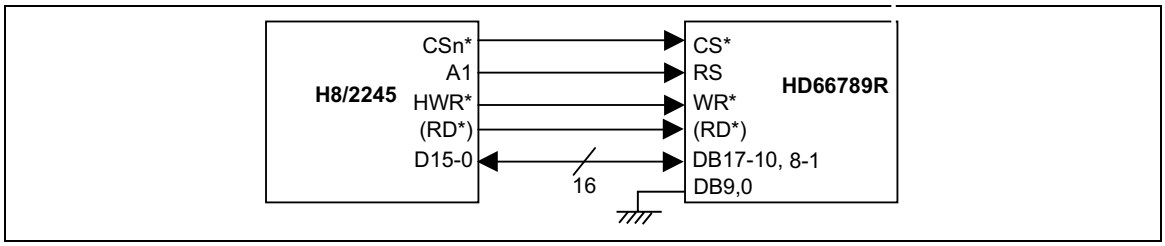
18-bit microcomputer and HD66789R



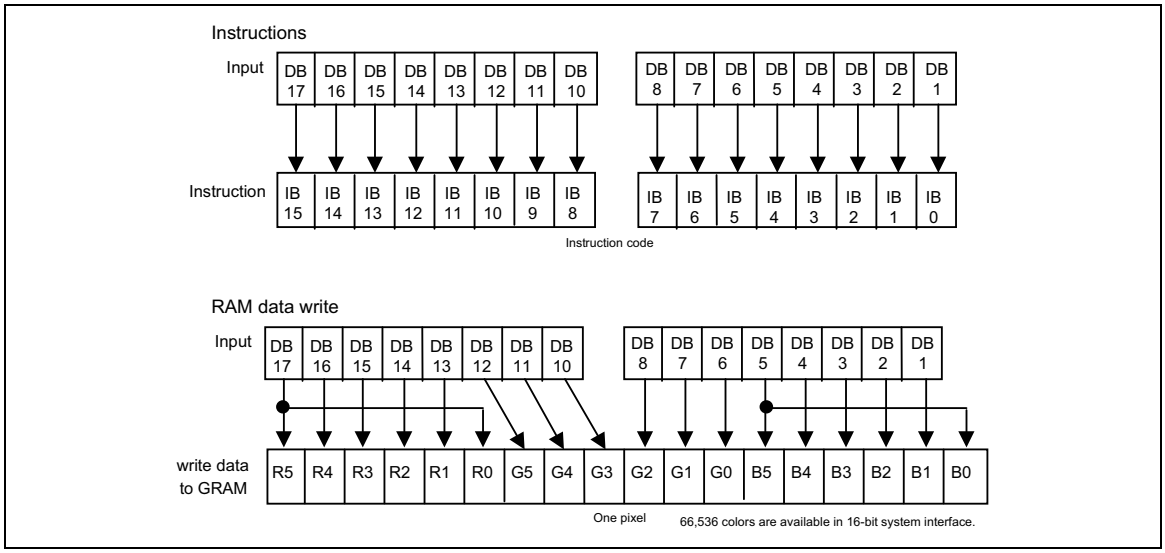
Data format for 18-bit interface

80-system 16-bit interface

The 80-system 16-bit parallel data transfer is selected by setting the IM3/2/1/0 pins to GND/GND/IOVcc/GND levels respectively.



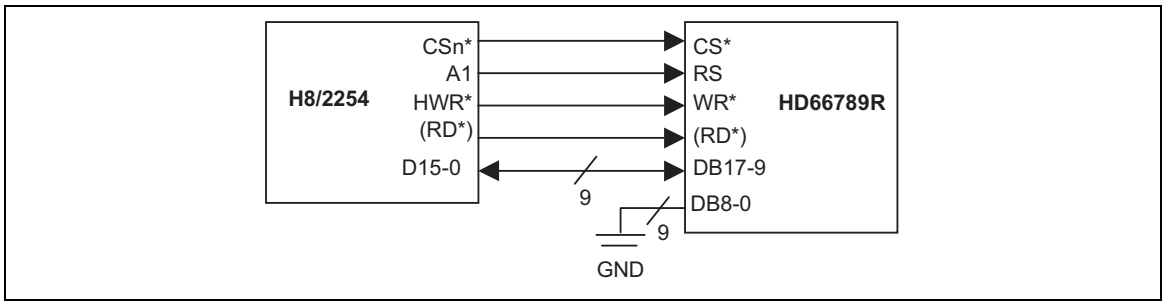
16-bit microcomputer and HD66789R



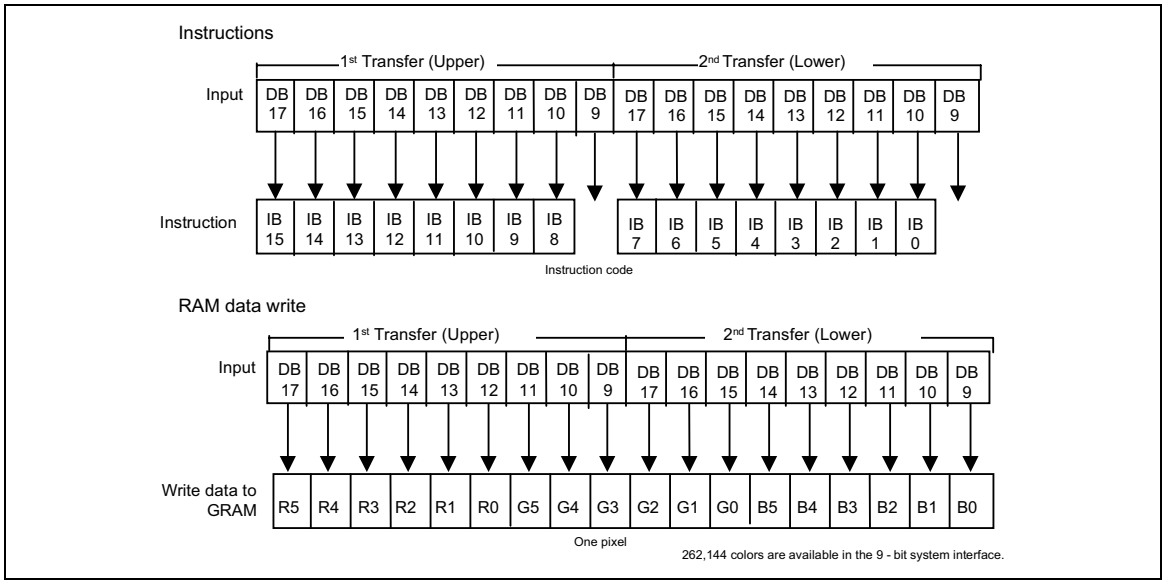
Data format for 16-bit interface

80-system 9-bit interface

The 80-system 9-bit parallel data transfer using DB17~DB9 pins is selected by setting the IM3/2/1/0 pins to IOVcc/GND/IOVcc/IOVcc levels respectively. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits (the LSB is not used), and the upper 8 bits are transferred first. The RAM write data are also divided into the upper and lower 9 bits, and the upper bits are transferred first. The unused pins DB8-0 pins must be fixed to either IOVcc or GND level. When writing the index register, the upper byte (8 bits) must be written.



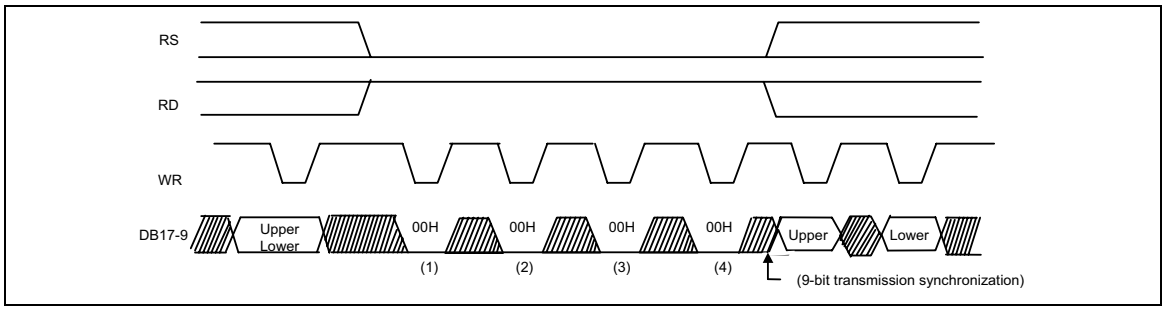
9-bit microcomputer and HD66789R



Data format for 9-bit interface

Data transfer synchronizing in 9-bit bus interface mode

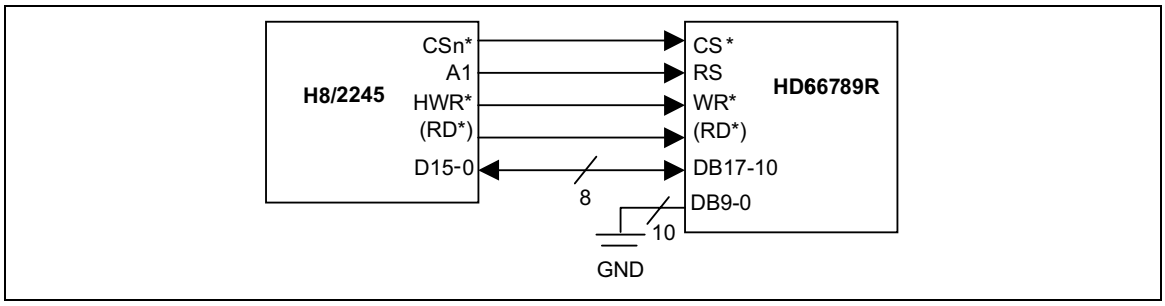
The HD66789R supports a data transfer synchronization function, which resets the counters that count transfers of upper and lower 9 bits when the 9-bit bus interface mode are selected. If there is a mismatch between the numbers of data transfers of upper and lower 9-bit data due to noise effects and so on, the "00"H instruction is written 4 times consecutively to reset the counter so that data transfer restarts with an upper bit transfer. The synchronization function, when executed periodically, will protect the display system from runaway operation.



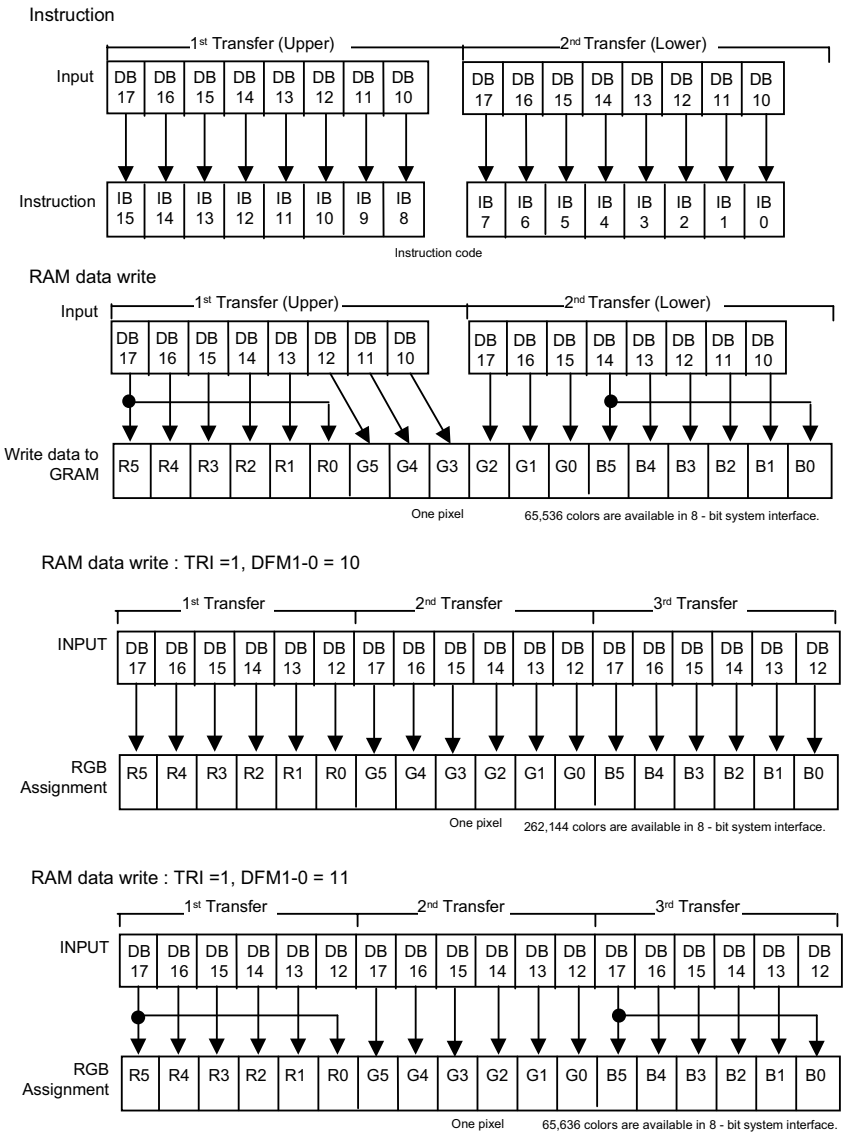
9-bit data transfer synchronization

80-system 8-bit interface

The 80-system 8-bit parallel data transfer is selected by setting the IM3/2/1/0 pins to GND/GND/IOVcc/IOVcc levels respectively. When transferring a 16-bit instruction, it is divided into upper and lower 8 bits and the upper 8 bits are transferred first. The RAM data is also divided into the upper and lower 8 bits, and the upper bits are transferred first. The RAM write data are expanded into 18 bits internally. The unused pins DB9-0, 0 must be fixed to either IOVcc or GND level. When writing the index register, the upper byte (8 bits) must be written.



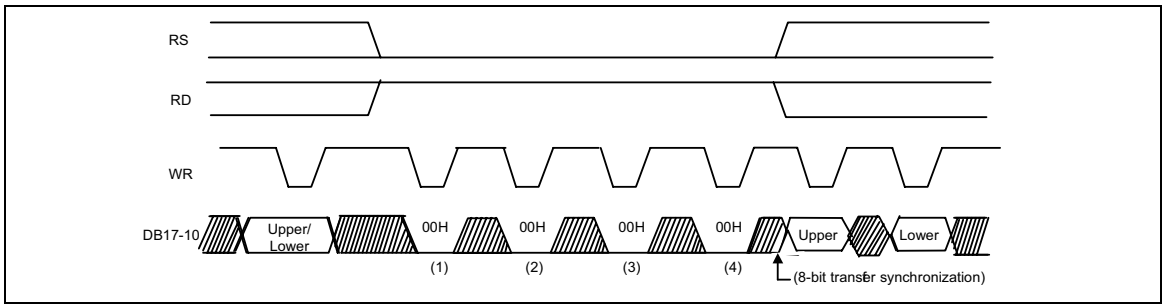
8-bit microcomputer and HD66789R



Data format for 8-bit interface

Data transfer synchronization in 8-bit bus interface mode

The HD66789R supports a data transfer synchronization function, which resets the counter that counts transfers of upper and lower 8 bits when 8-bit bus interface mode are selected. If there is a mismatch between the numbers of data transfers of upper and lower 8-bit data due to noise effects and so on, the "00"H instruction is written 4 times consecutively to reset the counter so that data transfer restarts with an upper bit transfer. The synchronization function, when executed periodically, will protect the display system from runaway operation.



8-bit data transfer synchronization

Serial Peripheral interface (SPI)

A Serial Peripheral Interface (SPI) is selected by setting the IM3/2/1 pins to GND/IOVcc/GND levels respectively. The SPI is available through the chip select line (CS), the serial transfer clock line (SCL), the serial data input (SDI), and the serial data output (SDO). In SPI mode, the IM0/ID pin functions as the ID pin and the DB15-2 pins, which are not used, must be fixed at either IOVcc or GND level.

The HD66789R recognizes the start of data transfers on the falling edge of CS input to initiate the transfer of the start byte. It recognizes the end of data transfers on the rising edge of a CS input. The HD66789R is selected when the 6-bit chip address in the start byte transferred from the transmitter and the 6-bit device identification code assigned to the HD66789R are compared and both 6-bit data correspond. When selected, the HD66789R starts taking in subsequent data. The least significant bit of the identification code is set with the ID pin. Send "01110" to the five upper bits of the identification code. Assign two different chip addresses to the HD66789R because the seventh bit of the start byte is assigned to the register select bit (RS). When RS = 0, either an index register write operation or a status read operation is executed. When RS = 1, either an instruction write operation or a RAM read/write operation is executed. The eighth bit of the start byte is to select either read or write operation (R/W bit). Data are received when the R/W bit is 0, and are transferred when the R/W bit is 1.

In SPI mode, data are written to the internal GRAM after transferring two-bytes. Data are expanded into 18 bits before written to the internal GRAM by adding one bit (the same data as the MSB of RB) next to the LSB of R and B data.

After receiving the start byte, the HD66789R starts transferring or receiving data in unit of bytes. Data transfers are executed from the MSB. All HD66789R's instructions take a 16-bit format and are executed internally from the MSB (IB15 to 0) after transferring two bytes. GRAM write data are internally expanded to the 18-bit format. After receiving the start byte, the HD66789R takes in the upper eight bits of an instruction as the first byte and the lower eight bits as second byte. The HD66789R reads 5 bytes as dummies right after reading the start byte. The HD66789R reads out data as valid data from the 6th byte.

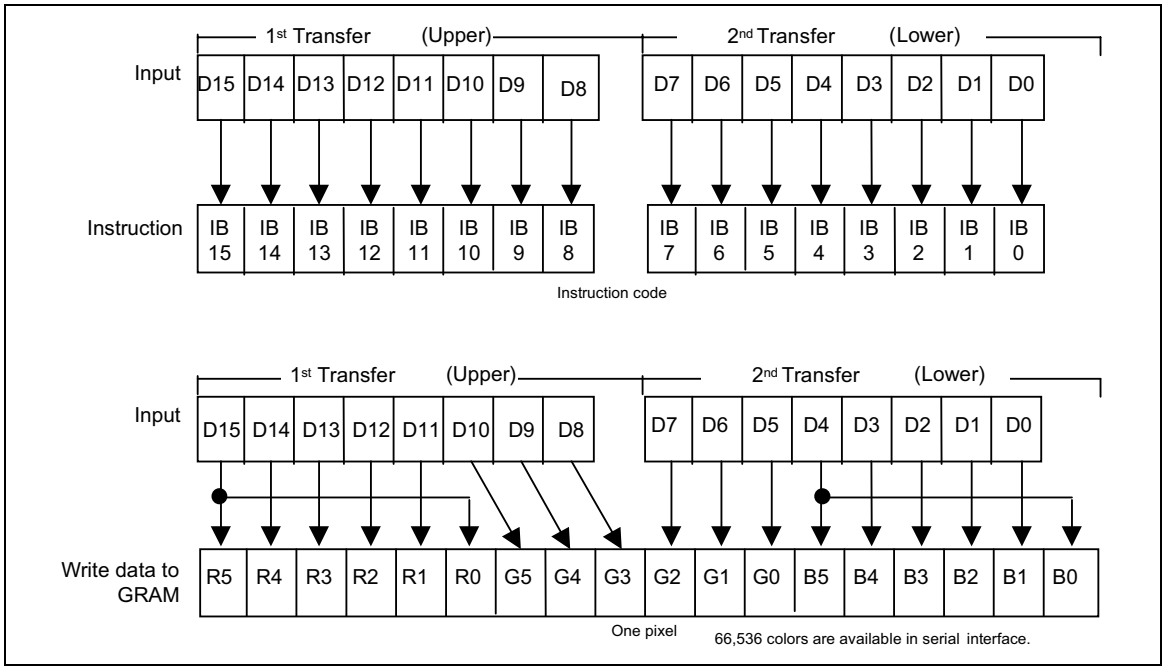
Start Byte Format

Transferred bits	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID		

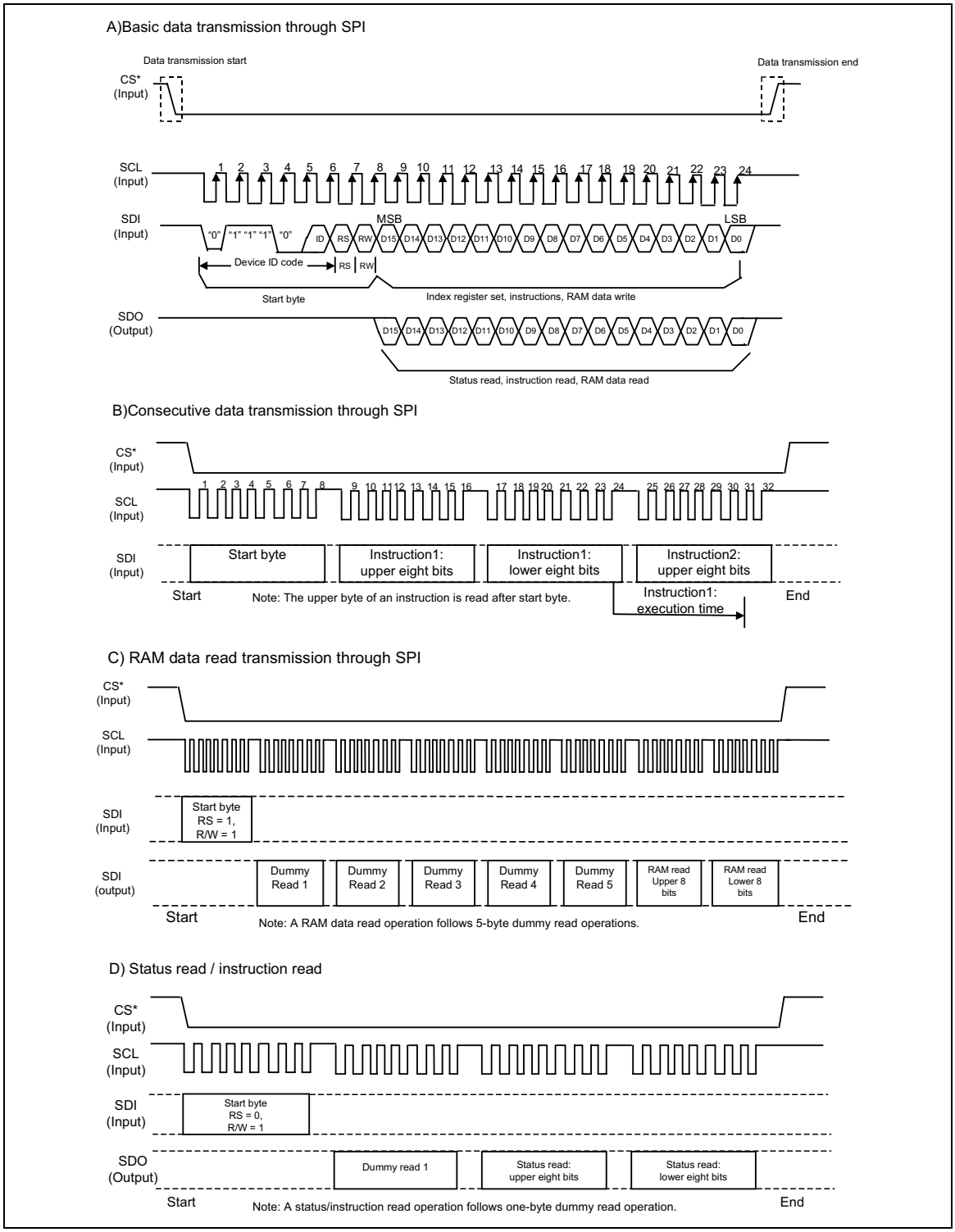
Note 1) The ID bit is set with the IM0/ID pin.

Table 39

RS	R/W	Function
0	0	Set an index register
0	1	Read a status
1	0	Write an instruction or RAM data
1	1	Read an instruction or RAM data



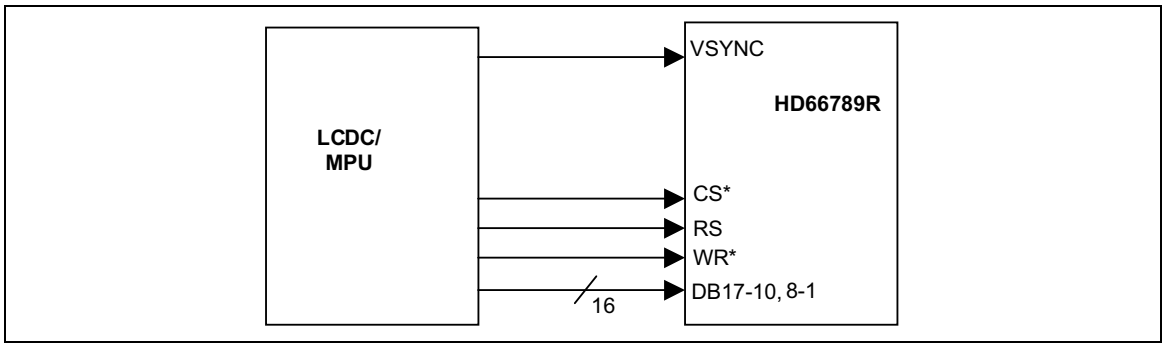
Data format for SPI



Data transfer through SPI

VSYNC Interface

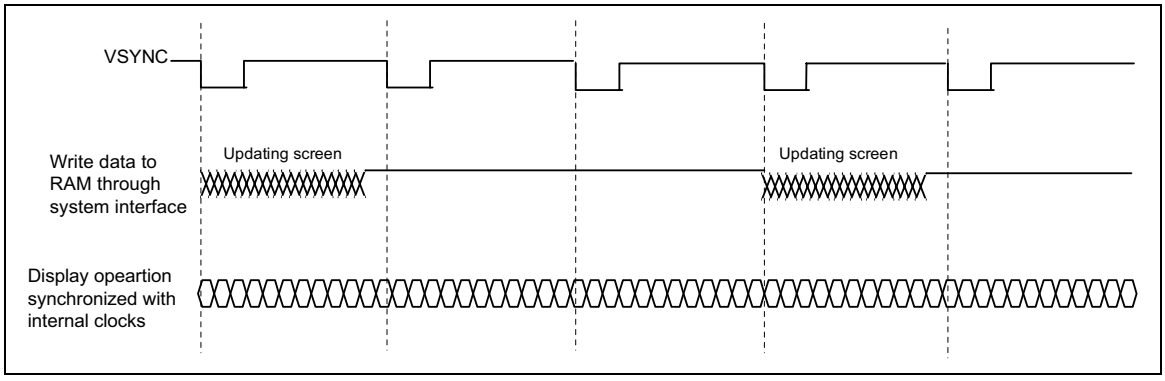
The HD66789R incorporates the VSYNC interface, which enables to display a moving picture with only a system interface and frame-synchronizing signal (VSYNC). This interface enables to display moving pictures with minimum modifications to a conventional system.



VYSNC interface

The VSYNC-I/F is selected by setting DM1-0 = 10 and RM = 0. In VSYNC I/F mode, the internal display operation is synchronized with VSYNC. The VSYNC interface enables to display a moving picture through a system interface and rewrite display data without flicker by writing data to the internal RAM through a system interface in a higher speed than the internal display operation by a certain degree.

The VSYNC interface executes the display operation only with the internal clocks generated by the internal oscillators and the input of the VSYNC signal. All display data are stored in the internal RAM so that only the data to be written over are transferred to minimize data transfers while displaying a moving picture. To access the internal RAM in high speed with low power consumption, use high-speed write mode (HWM=1).



Moving picture data transfer through VSYNC interface

The VSYNC interface has a minimum for the RAM write speed through the system interface and the internal clock frequency. It requires RAM write speed more than the theoretical value calculated from the following equation.

$$\begin{aligned} &\textit{Internal clock frequency (fosc) [Hz]} \\ &= \textit{FrameFrequency} \times (\textit{DisplayLines}(NL) + \textit{FrontPorch}(FP) + \textit{BackPorch}(BP)) \times 16(\textit{clocks}) \times \textit{fluctuation} \end{aligned}$$

$$\textit{RAMWriteSpeed}(\min.)[Hz] > \frac{176 \times \textit{DisplayLines}(NL)}{(\textit{BackPorch}(BP) + \textit{DisplayLines}(NL) - m\arg ins) \times 16(\textit{clocks}) \times \frac{1}{\textit{fosc}}}$$

Note 1) When RAM write does not start right after the falling edge of VSYNC, the time from the falling edge of VSYNC until the RAM write operation starts must also be taken into account

An example of RAM writing speed and the frequency of the internal clocks in VSYNC interface mode is as follows.

[Example]

Display size	176 RGB × 240 lines
Lines	240 lines (NL = 11110)
Back/front porch	14/2 lines (BP = 1110/FP = 0010)
Frame frequency	60 Hz

Internal clock frequency (fosc) [Hz]
= 60 Hz × (240 + 2 + 14) lines × 16 Clocks × 1.1 / 0.9 = 300 kHz

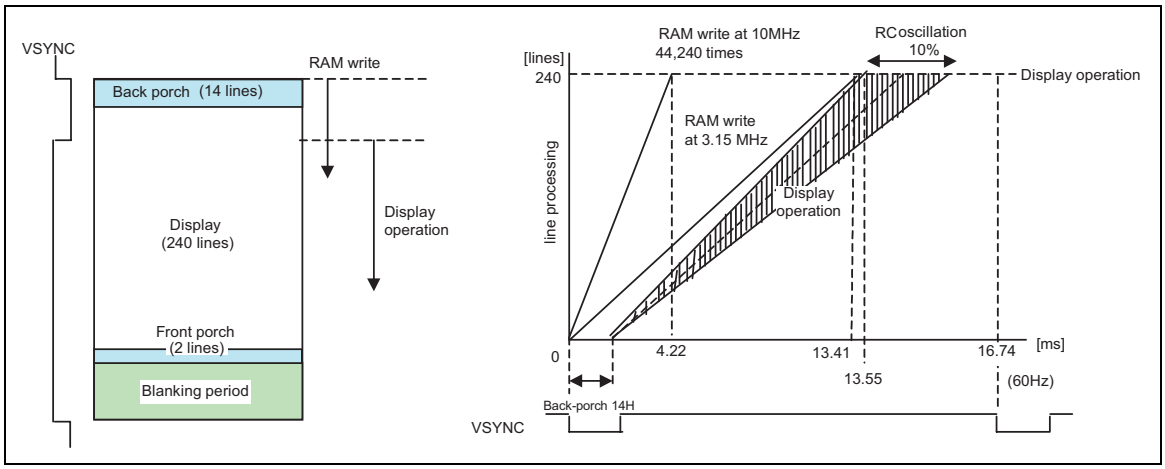
When setting an internal clock frequency, possible causes of fluctuations must also be taken into consideration. In this example, the set value for the internal clock frequency allows for the margin of ±10% from itself (the center value) for fluctuations, and the frequency including the margin must be set that the display operation be completed within one VSYNC cycle.

This example includes variations attributed to the fabrication process of LSIs and the room temperature as causes of fluctuations. Other possible causes of fluctuations, such as variations with the external resistors or voltage changes are not considered in this example. It is necessary to make a setting with enough margins to incorporate these factors.

Minimum speed for RAM writing [Hz]
> 176 × 240 / {((14 + 240 - 2) lines × 16 clock) / 300 kHz} = 3.14 MHz

The above theoretical value is calculated on the premise that the HD66789R start writing data to RAM on the falling edge of VSYNC. There must at least be a margin of 2 lines between the physical line of the display operation and the line address to for the RAM data write operation.

The RAM write speed of 3.14MHz or more on the falling edge of guarantees the completion of write operation before the HD66789R starts the display operation with regard to each line and makes it possible to rewrite the entire screen without flicker.

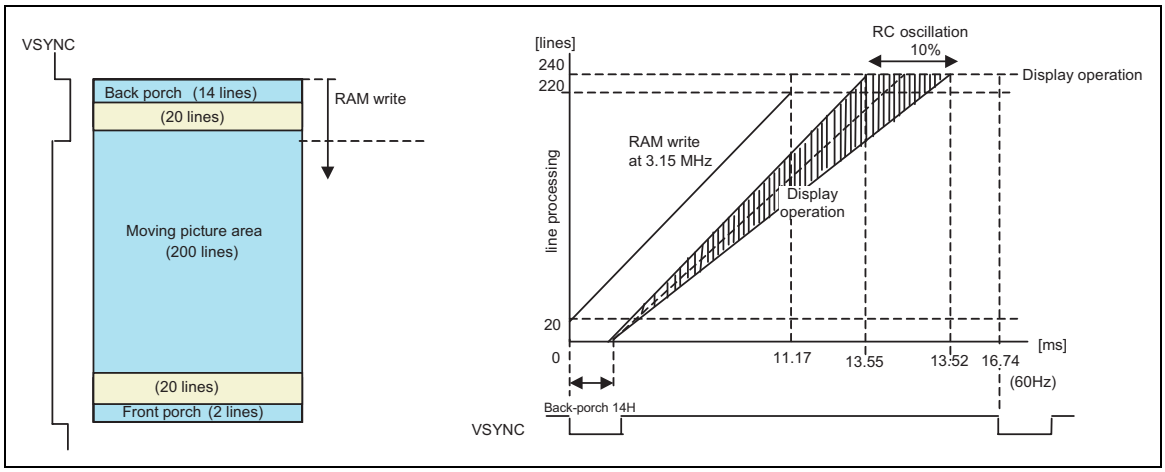


Operation through VSYNC interface

Notes to the VSYNC interface

1. The aforementioned example of calculation gives a theoretical value. In actual settings, possible causes of fluctuations such as variations with the internal oscillators should be taken into consideration. Accordingly, it is necessary to give enough margins when setting a RAM writing speed.

2. The aforementioned example of calculation gives a value for rewriting the entire screen. Therefore, if the moving picture display area is smaller than that, an extra margin will be created between the RAM write operation and the display operation with regard to each line.



RAM write margin

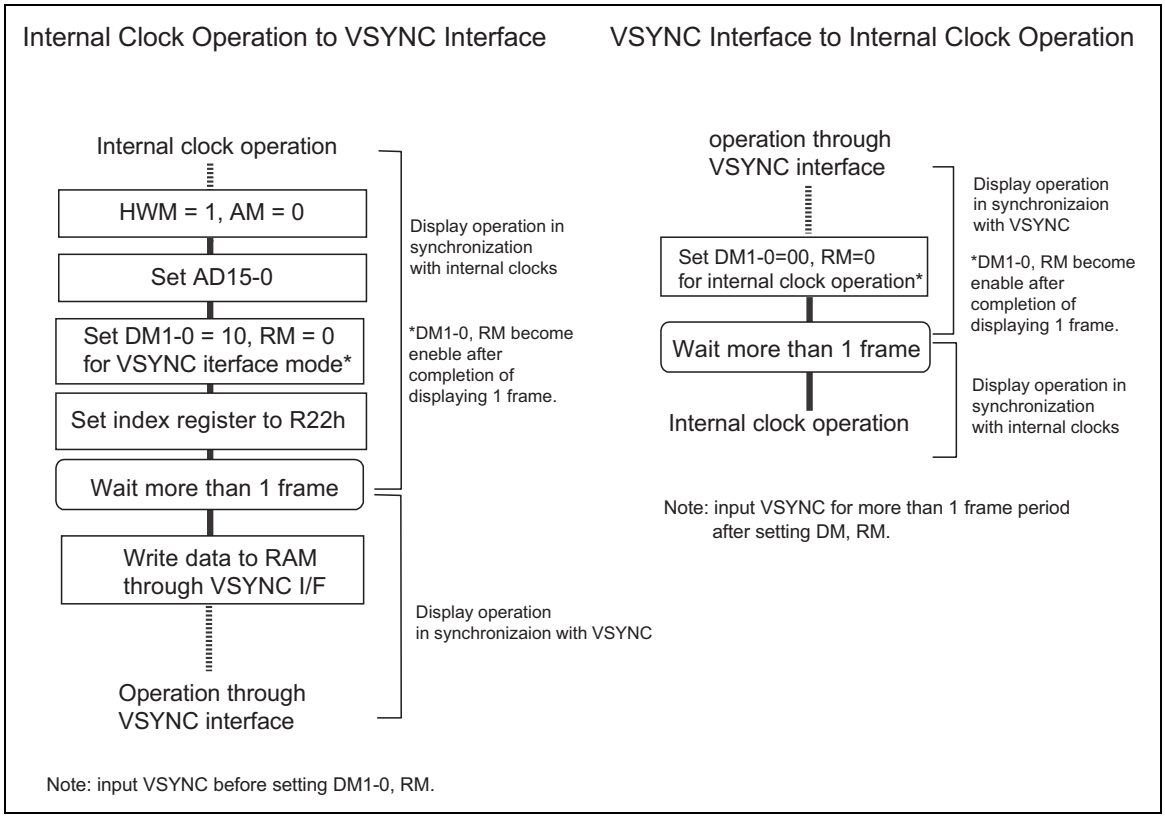
3. A front porch period continues after completion of drawing 1 frame and until the next input of VSYNC.

4. In case of switching between the internal clock operation mode (DM1-0 = 00) and the VSYNC interface mode, the new mode becomes effective after drawing one frame, which is shown when setting instructions.

5. The partial display, vertical scroll, and interlaced scan functions are not available with the VSYNC interface.

6. In VSYNC interface mode, set AM to 0 to transfer display data in the aforementioned method.

7. In VSYNC interface mode, use the high-speed write mode (HWM = 1) when writing display data to the internal RAM.



VSYNC-internal clock operation transition

External Display Interface

The following interfaces are available as the external display interface (RGB interface). The interface is selected by setting the RIM1-0 bits. RAM is accessible through the RGB interface.

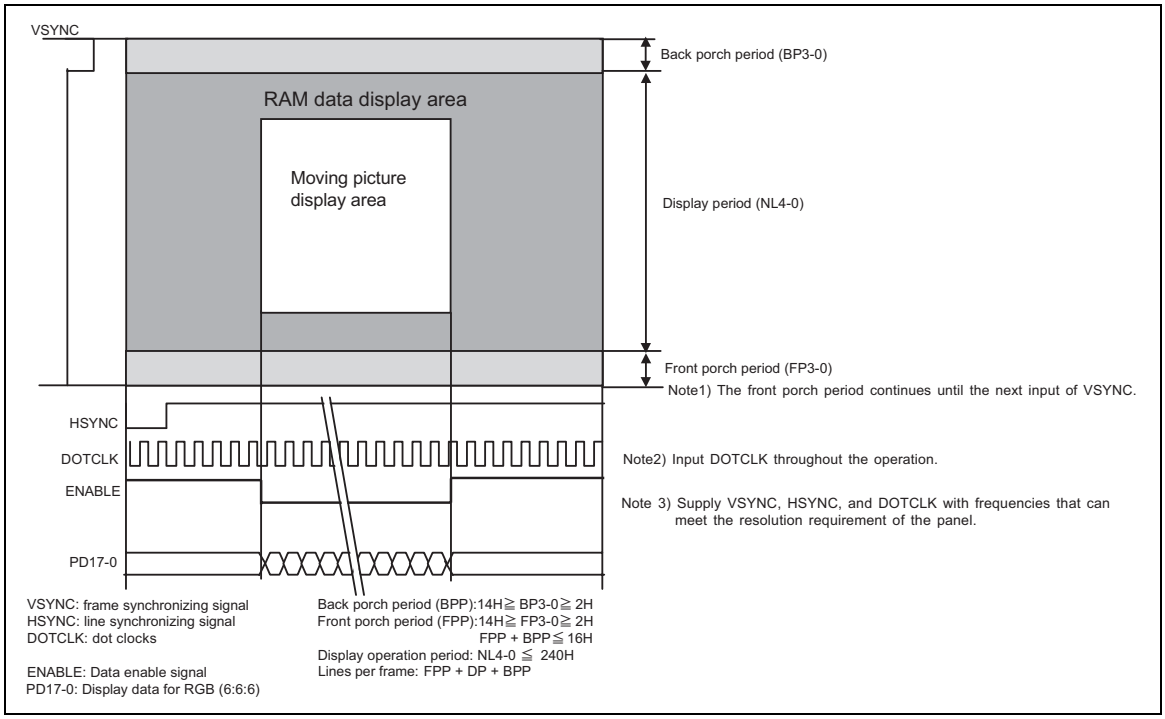
Table 40

RIM1	RIM0	RGB Interface	DB Pin
0	0	18-bit RGB interface	PD17-0
0	1	16-bit RGB interface	PD17-13, 11-1
1	0	6-bit RGB interface	PD17-12
1	1	Setting disabled	

Note 1) Multiple RGB interfaces cannot be used simultaneously.

RGB interface

The display operation through the RGB interface is synchronized with VSYNC, HSYNC, and DOTCLK. With the use of high-speed write mode (HWM=1) and the window address function, the RGB interface enables to transfer only the necessary data and rewrite only the area that needs rewriting in high speed with less power consumption. The RGB interface requires the settings of back porch and front porch periods before and after the display period, respectively.



RGB interface

ENABLE signal

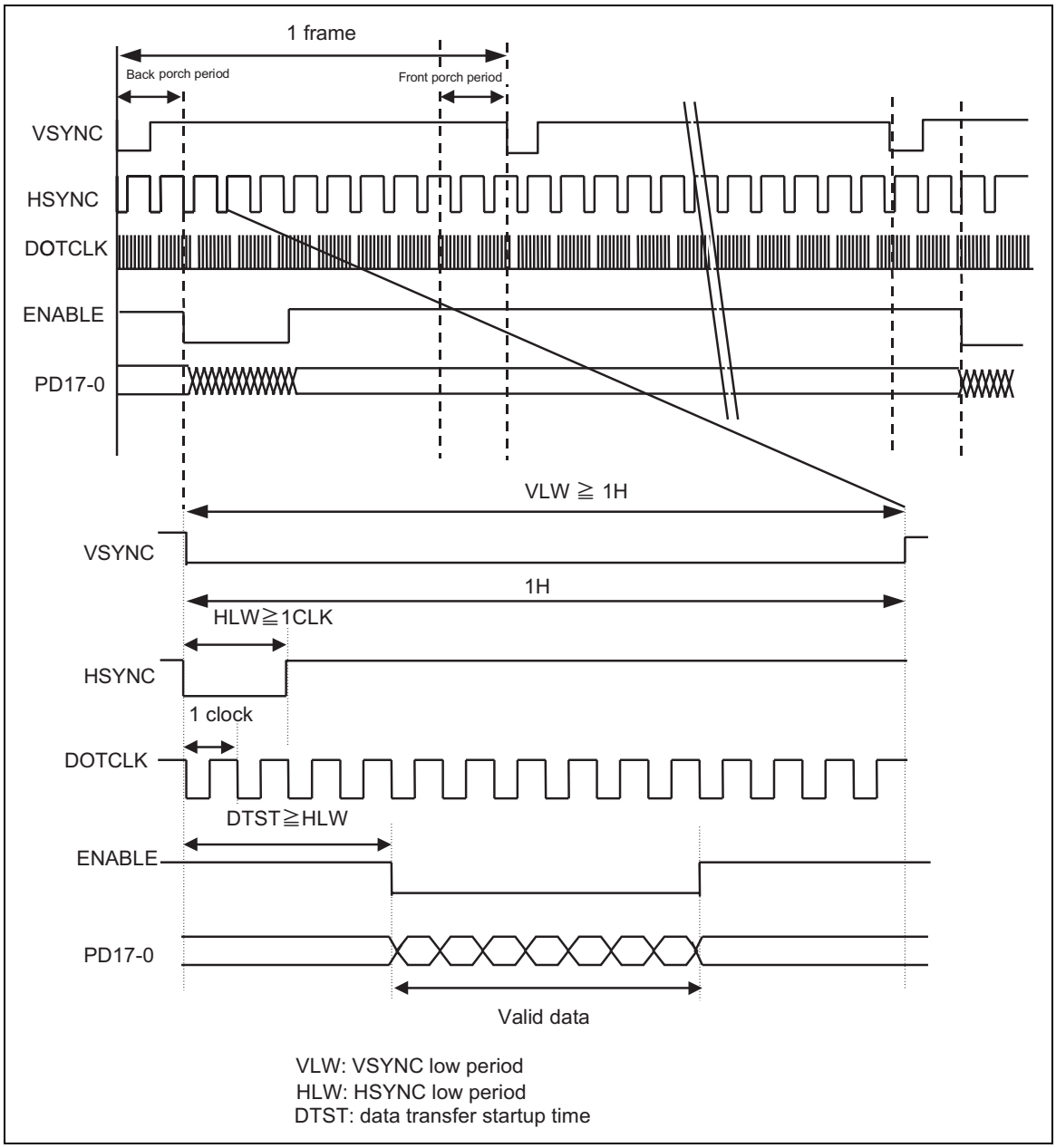
The EPL bit can change the polarity of the ENABLE signal. The relationship between the EPL bit and the ENABLE bit is as follows.

Table 41

EPL	ENABLE	RAM Write	RAM Address
0	0	Enabled	Updated
0	1	Disabled	Retained
1	0	Disabled	Retained
1	1	Enabled	Updated

RGB interface timing

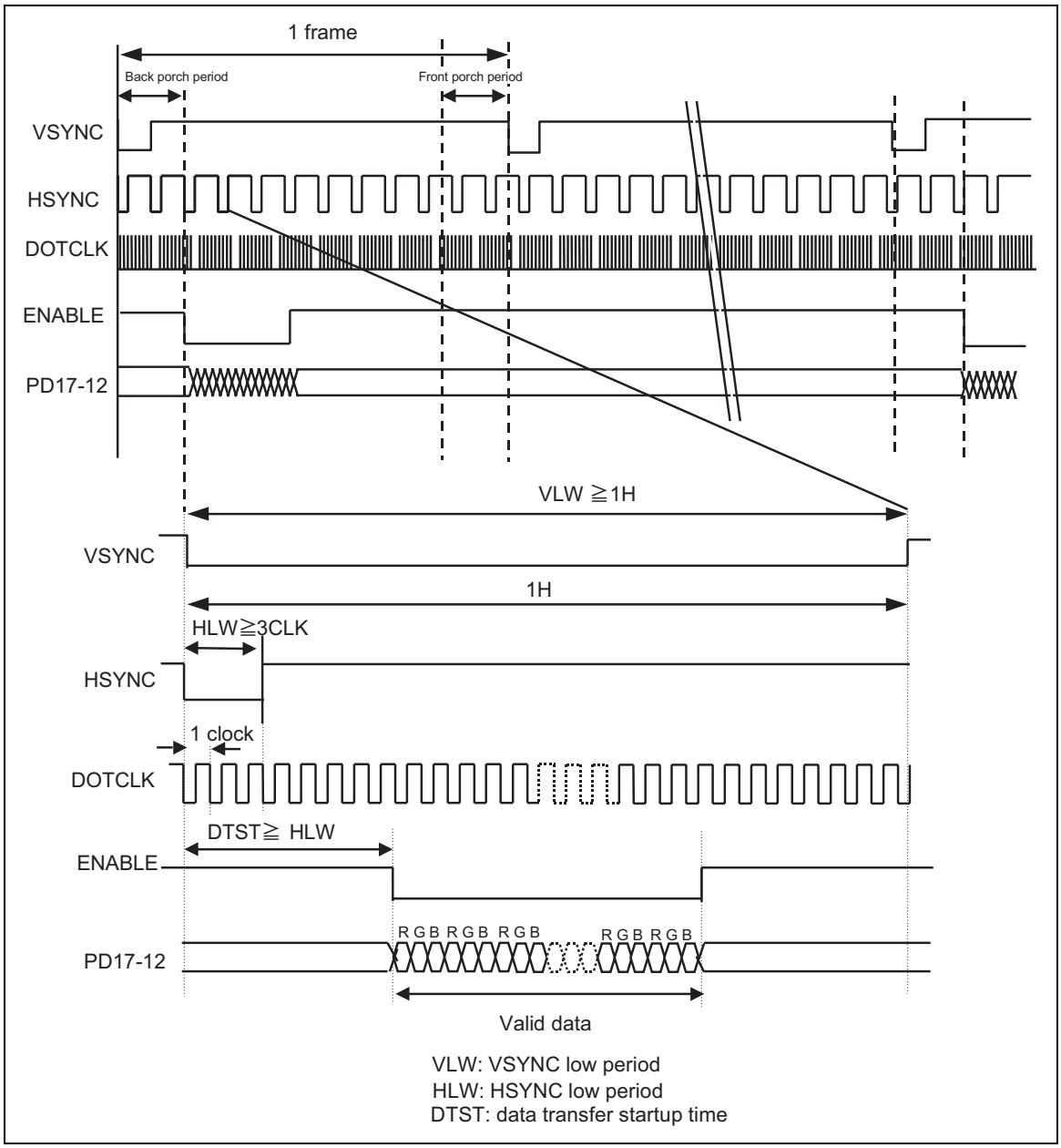
Timing chart of signals in 16/18-bit RGB interface mode



16-/18-bit RGB Interface Timing

Note 1) Use the high speed write mode (HWM = 1) to write data though the RGB interface.

Timing chart of signals in 6-bit RGB interface mode



6-bit RGB Interface Timing

Note 1) Use the high speed write mode (HWM = 1) to write data though the RGB interface.

Note 2) In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLKs.

Note 3) In 6-bit RGB interface mode, set the cycles of VSYNC, HSYNC and ENABLE to 3 multiples of DOTCLKs.

Moving picture display

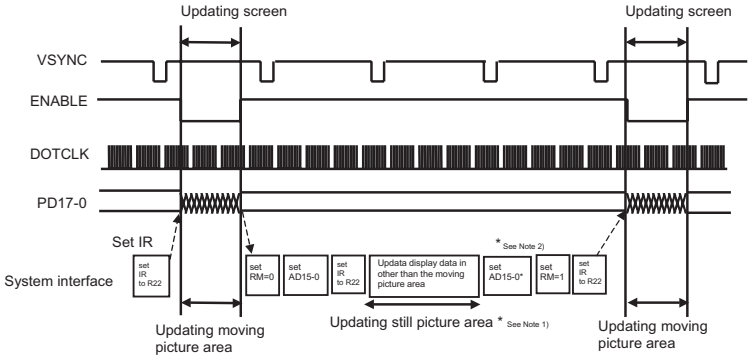
The HD66789R incorporates the RGB interface for moving picture display and RAM for storing display data, which provide the following merits in displaying a moving picture.

- The window address function enables to specify the moving picture area
- The high-speed write mode enables RAM access in high speed with less power consumption
- Only the data written over the moving picture area are transferred
- The reduction in data transfers contributes to the reduction in power consumption by the entire system
- The combined use with the system interface allows rewriting data in the still picture area, such as icons, while displaying a moving picture

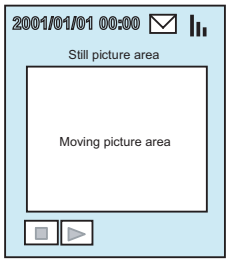
RAM access through system interface in RGB-I/F mode

The HD66789R allows RAM access through the system interface while using the RGB interface. In RGB interface mode, data are written to the internal RAM in synchronization with DOTCLK inputs while ENABLE is "Low". When writing data to the RAM through the system interface, set ENABLE "High" to stop writing data through the RGB interface. Then set RM = 0 to make the RAM accessible through the system interface. When reverting to the RGB interface mode, wait for a read/write bus cycle. Then, set RM = 1 and the index register to R22h to start accessing RAM though the RGB interface. A conflict between the RAM accesses through the two interfaces will not guarantee a proper RAM write operation.

The following is an example of displaying a moving picture through the RGB interface while rewriting the data in the still picture area through the system interface.



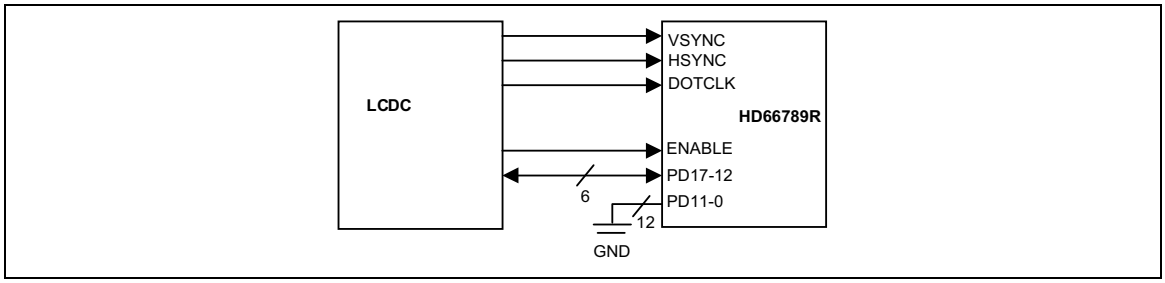
Note1) The address AD15-0 is set in the AC on every falling edges of VSYNC in RGB interface mode.
Note2) Set the address AD15-0 in the AC and the index register to R22h (RAM data write/read) before RAM access through RGB interface.
Note 3) Use the high-speed write mode when writing data through the RGB interface.



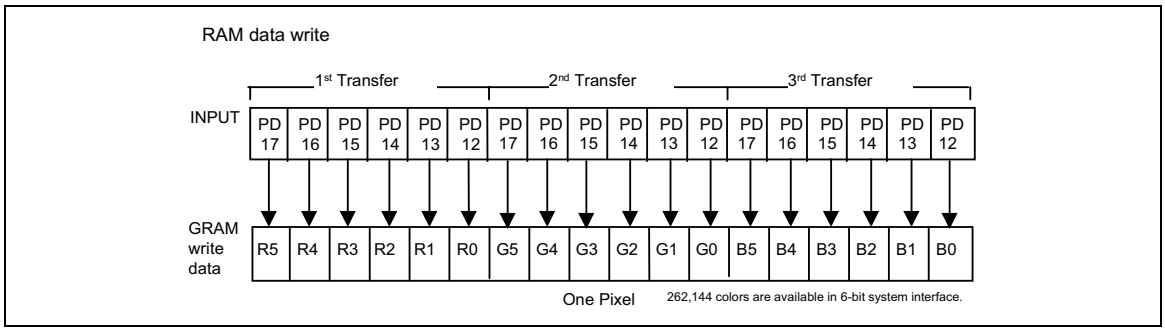
6-bit RGB interface

The 6-bit RGB interface is selected by setting the RIM1-0 bits to "10". The Display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation through the 6-bit RGB data bus (PD17-12) according to the data enable signal (ENABLE). Unused pins (PD11 to 0) must be fixed to either Vcc or GND level.

Instructions are set only through a system interface.



6-bit RGB interface

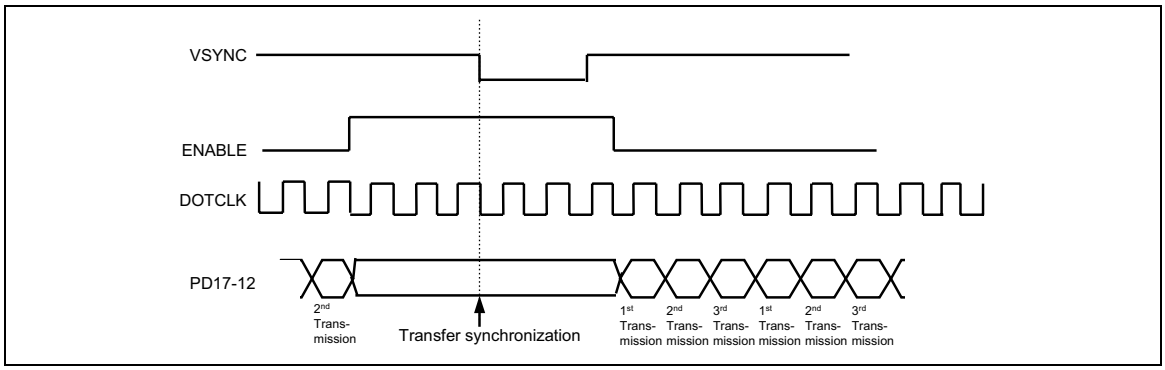


Data format for 6-bit interface

Data transfer synchronization in 6-bit RGB interface mode

The HD66789R incorporates transfer counters to count the first, second, third data transfers in 6-bit RBG interface mode. The transfer counters are always reset to the state of the first data transfer on the falling edge of VSYNC. If there is a mismatch in the number of data transfers, the counters are reset to the state of the first data transfer at the start of each frame (on the falling edge of VSYNC) and data transfers will restart correctly from the next frame. In case of displaying a moving picture, which requires consecutive data transfers, this function will minimize the effect from the data transfer mismatch and will help the display system to return to a normal state.

Note that the internal display operation is executed in units of pixels (RGB: 3 DOTCLKs). Accordingly, each DOTCLK input must correspond to the transfer of each dot of a pixel. Otherwise, data transfer mismatch will occur and will result in malfunctions in displaying the current and the next frames.

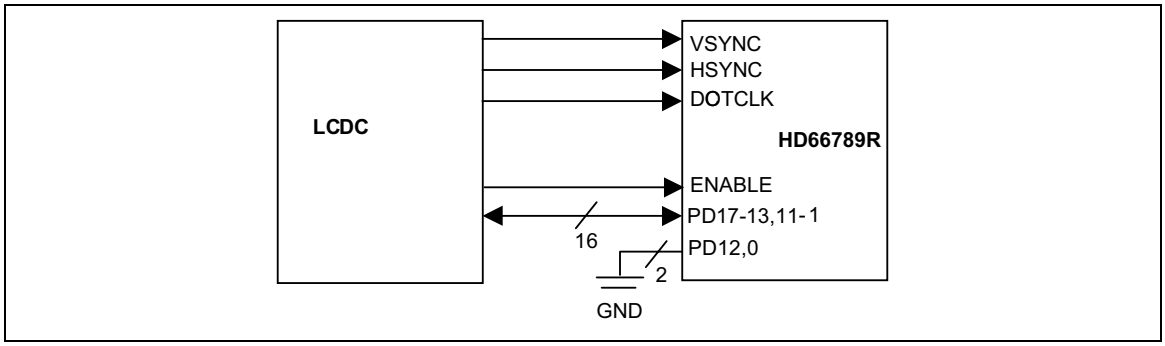


6-bit data transfer synchronization

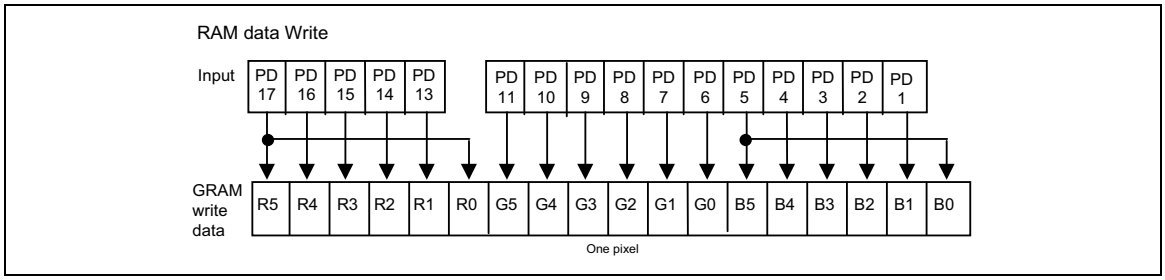
16-bit RGB interface

The 16-bit RGB interface is selected by setting the RIM1-0 bits to 01. The display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation through the 16-bit RGB data bus (PD17-13, 11-1) according to the data enable signal (ENABLE).

Instructions are set only through system interface.



16-bit RGB interface

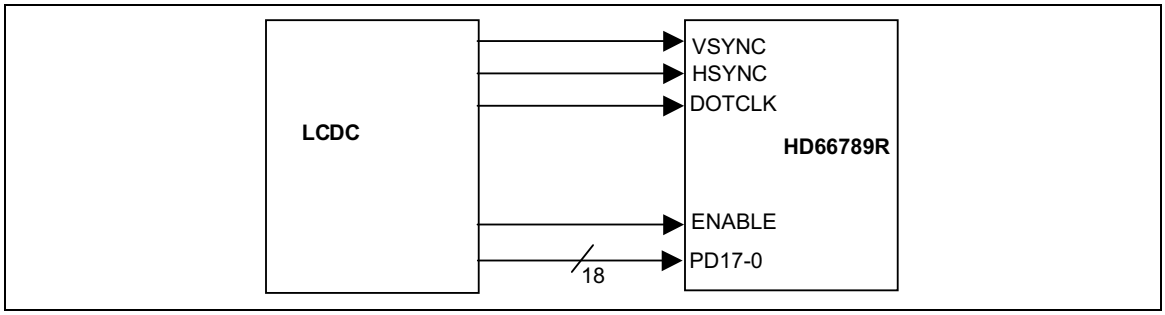


Data format for 16-bit interface

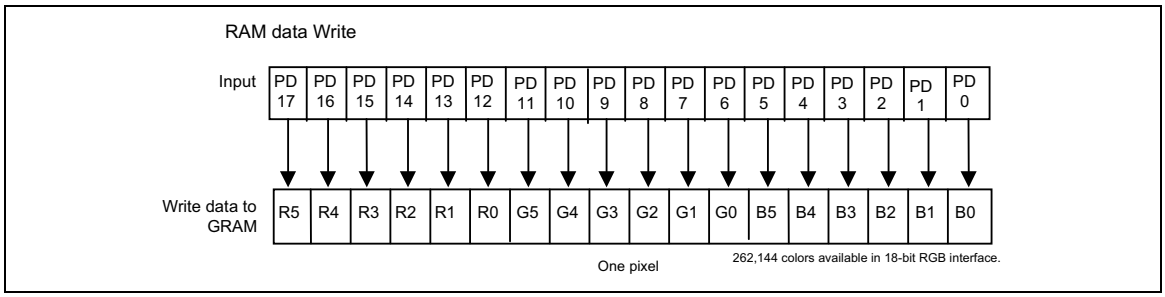
18-bit RGB interface

The 18-bit RGB interface is selected by setting the RIM1-0 bits to 00. The display operation is synchronized with the VSYNC, HSYNC, and DOTCLK signals. Display data are transferred to the internal RAM in synchronization with the display operation through the 18-bit RGB data bus (PD17-0) according to the data enable signal (ENABLE).

Instructions are set only through a system interface.



18-bit RGB interface



Data format for 18-bit interface

Notes to external display interface

1. The following functions are not available in RGB interface mode.

Table 42

Function	External Display Interface	Internal Display Operation
Partial display	Not available	Available
Scroll function	Not available	Available
Interlaced scan	Not available	Available
Graphics operation function	Not available	Available

2. The VSYNC, HSYNC, and DOTCLK signals must be supplied throughout the RGB-I/F display operation.

3. When setting the NO1-0, SDT1-0, and EQ1-0 bits in RGB-I/F mode, the reference clock is DOTCLK, not internal operation clocks.

4. In 6-bit RGB interface mode, each dot of a pixel, R, G, and B is transferred in synchronization with DOTCLK. In other words, it takes 3 DOTCLKs to transfer one pixel. Make sure to transfer data in units of dots in 6-bit RGB interface mode.

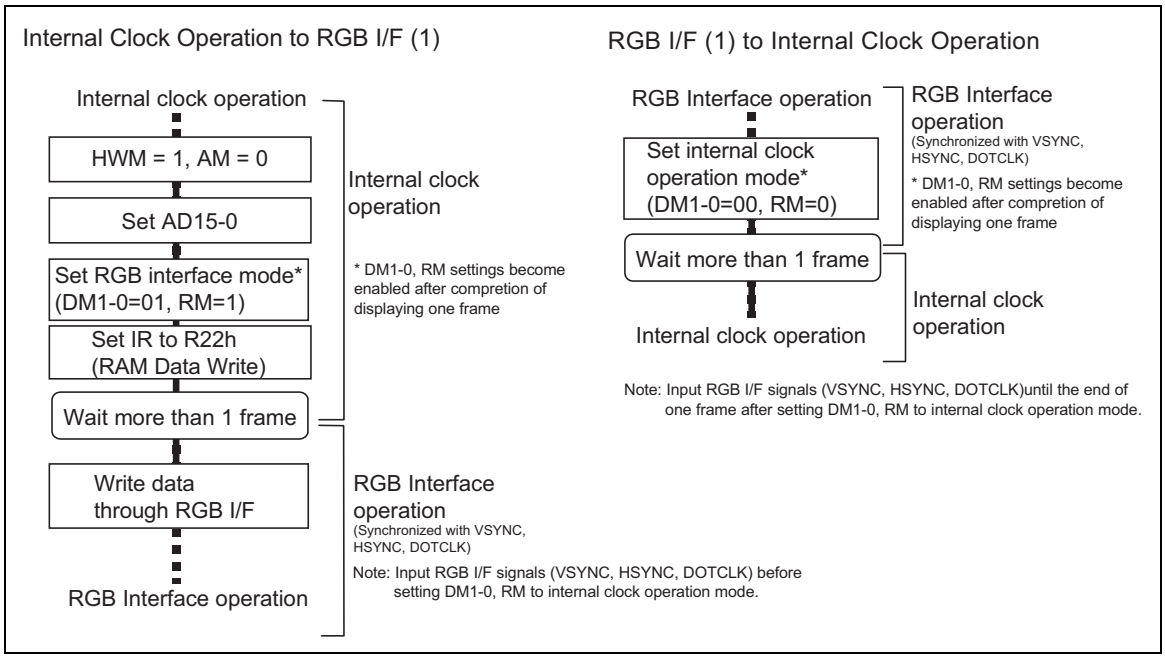
5. In 6-bit RGB interface mode, each dot of one pixel (R, G and B) is transferred in synchronization with DOTCLK. Accordingly, set each cycle of VSYNC, HSYNC and ENABLE to a 3 multiple of DOTCLK.

6. When switching between the internal operation mode and the external display interface mode, follow the sequence below.

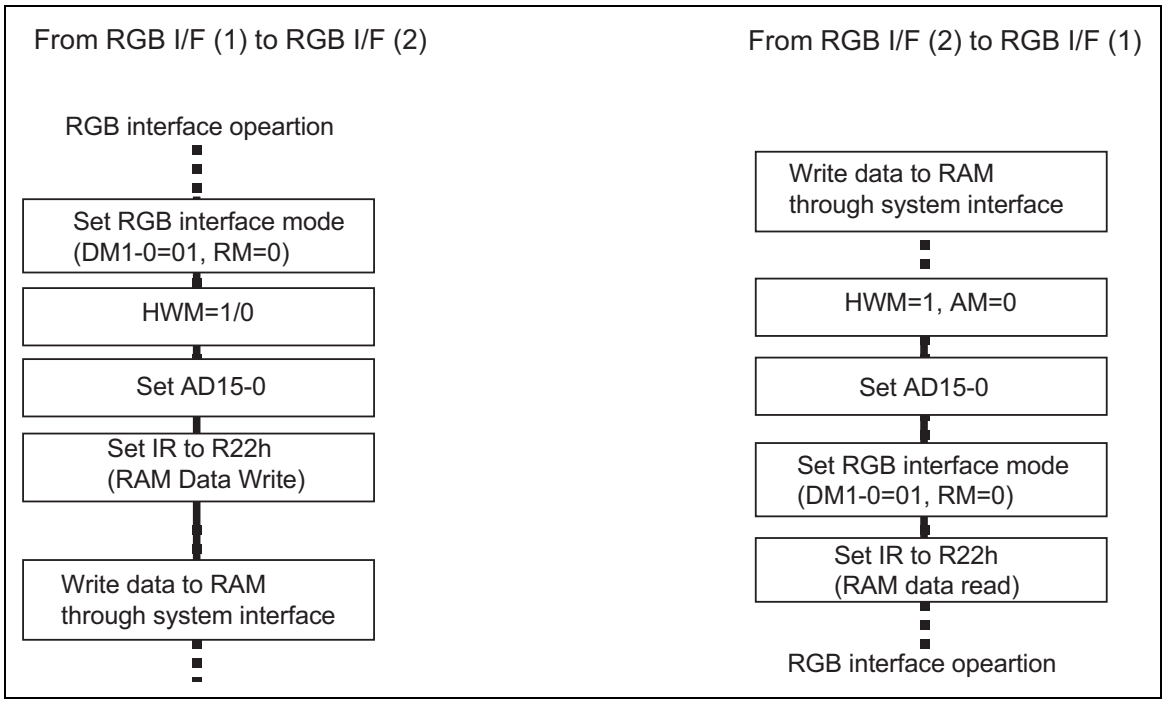
7. In RGB interface mode, a front porch period continues after displaying one frame until the next VSYNC input.

8. In RGB interface mode, use the high-speed write mode (HWM = 1) to write data to the internal GRAM.

9. In RGB interface mode, the RAM address (AD15-0) is set in the address counter for every frame on the falling edge of VSYNC.



Transition between the Internal Clock Operation Mode and RGB Interface Mode

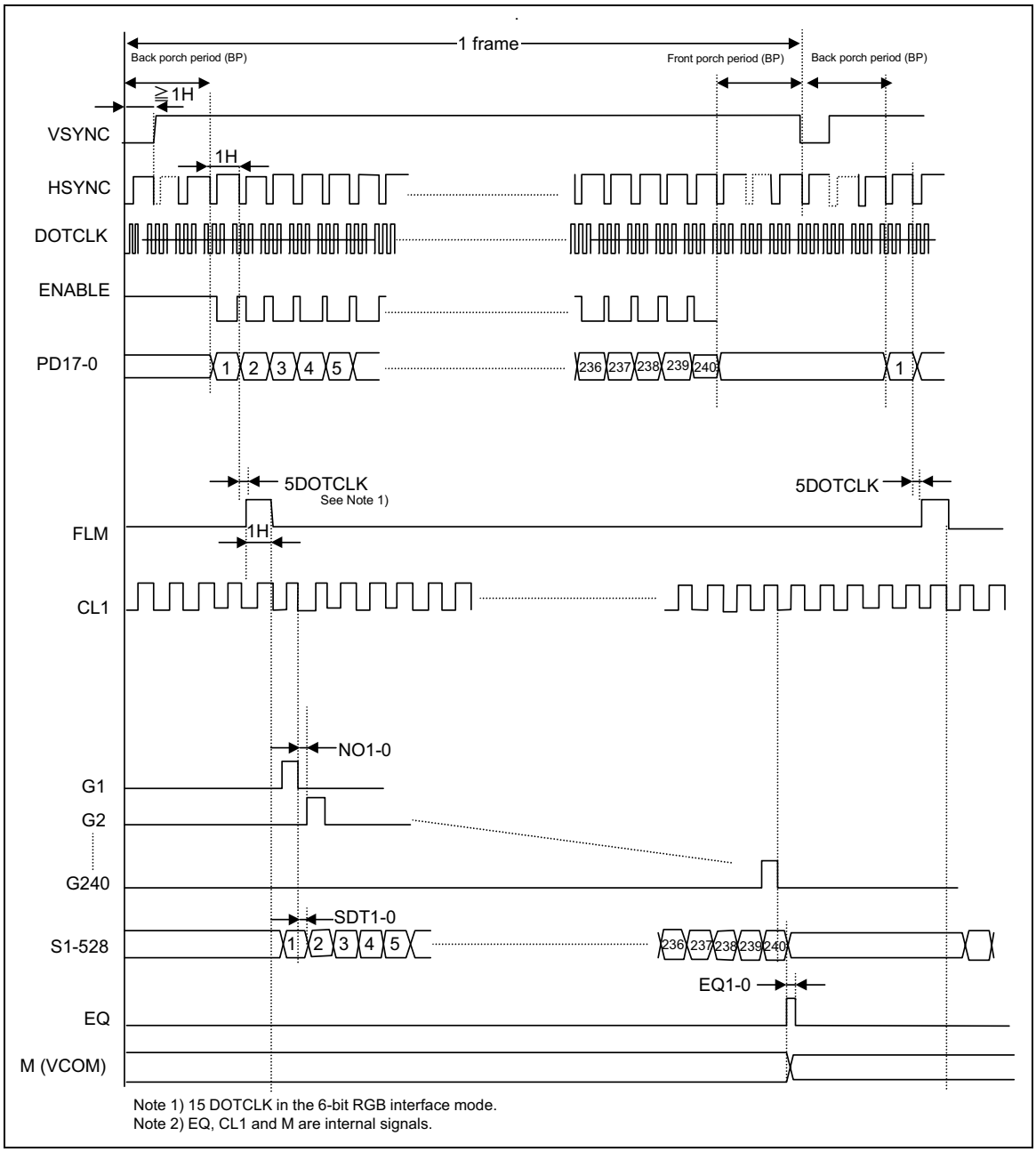


RAM data write sequence through system interface in RGB-I/F mode

Timing relationship with the LCD panel control signals

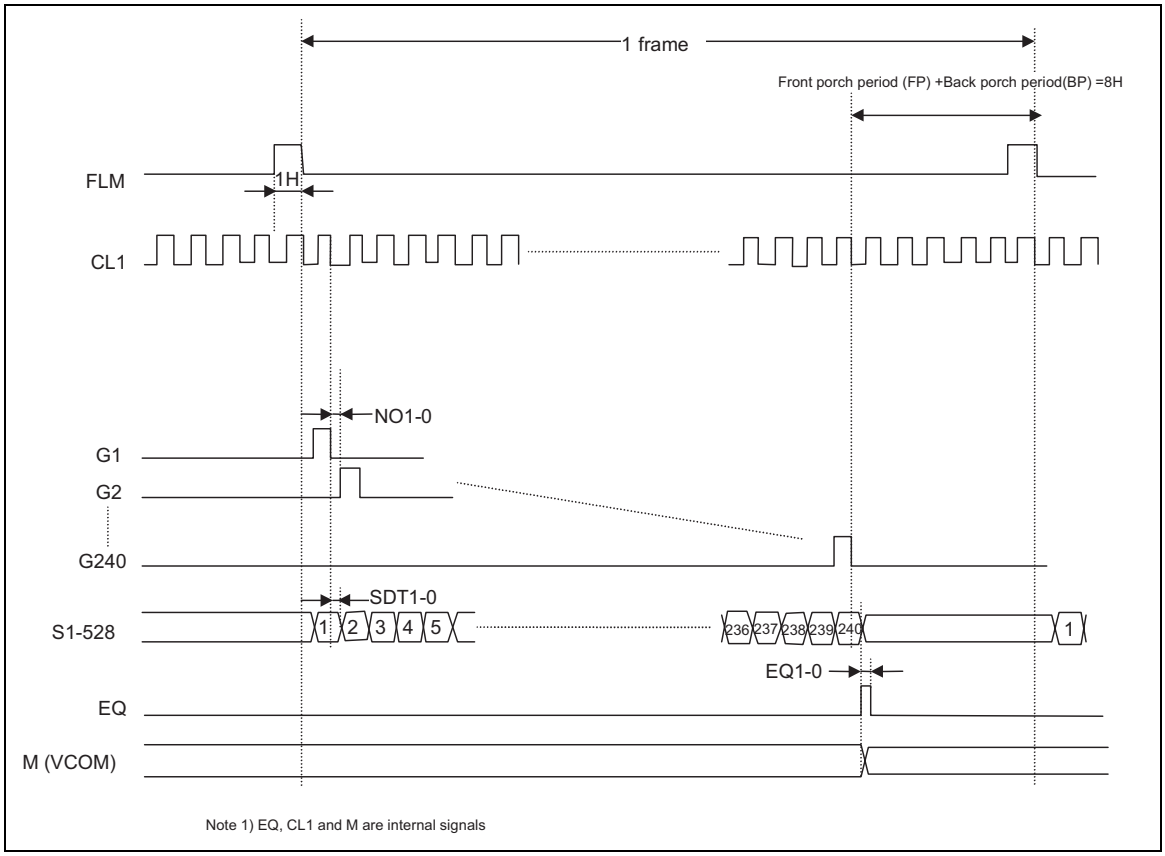
The relationships with the LCD panel control signals in the internal operation mode and in RGB interface mode are as follows.

RGB interface mode



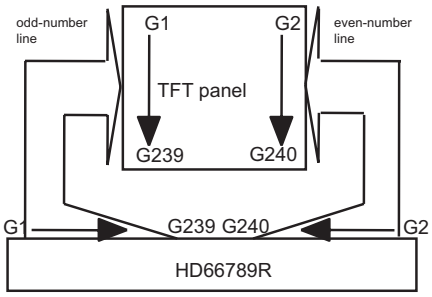
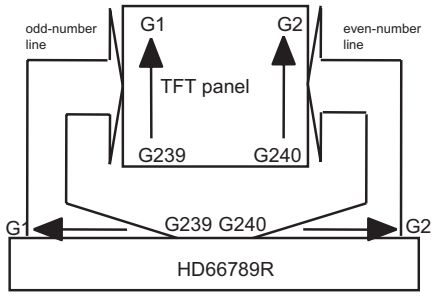
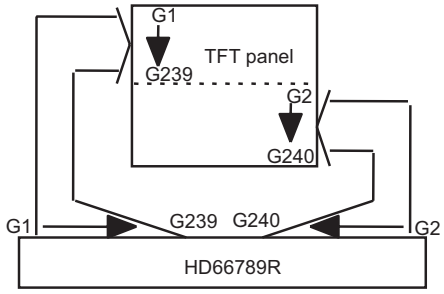
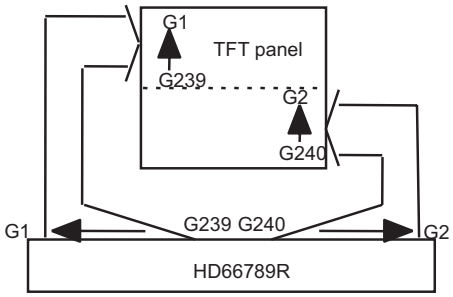
Note 1) 15 DOTCLK in the 6-bit RGB interface mode.
Note 2) EQ, CL1 and M are internal signals.

Internal clock mode



Scan Mode Setting

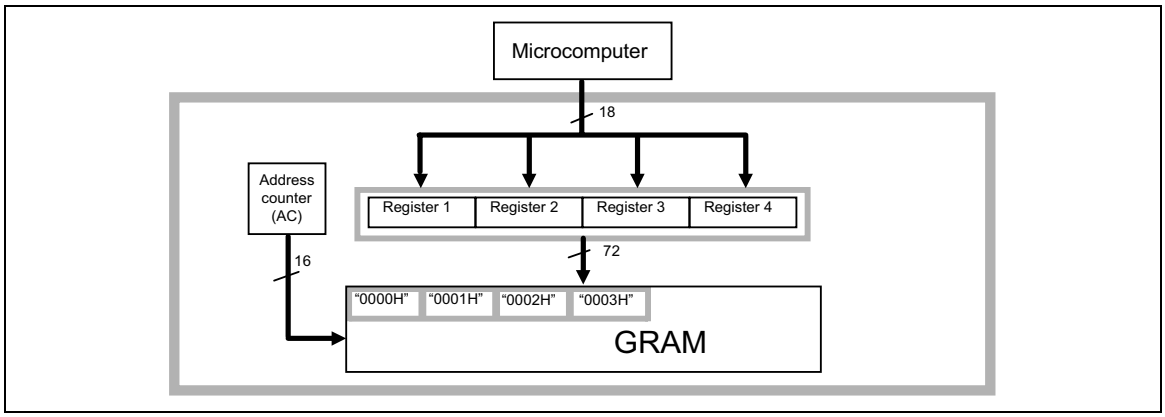
The HD66789R allows changing the shift direction of gate outputs with combination of the SM, GS bits to realize various ways of connecting the LCD panel and the HD66789R.

SM	GS	Scan direction	
0	0		G1, G2, G3, G4,…. G237, G238, G239, G240
0	1		G240, G239, G238, G237,…. G4, G3, G2, G1
1	0		G1, G3, G5,…. G237, G239, G2, G4, G6,…. G238, G240
1	1		G240, G238, G236,…. G4, G2, G239, G237, G235,…. G3, G1

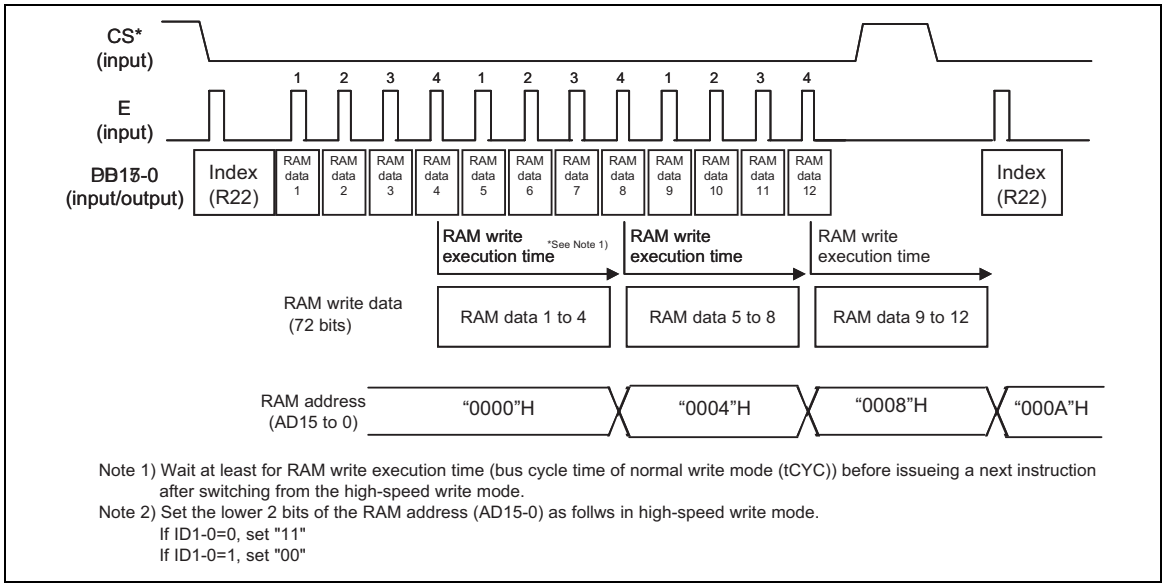
High-Speed RAM Write Function

The HD66789R has a high-speed RAM-write function that enables writing data to the internal RAM about one forth the time of the normal RAM write operation. This function makes the HD66789R available to the applications requiring high-speed display data rewrite operation, such as displaying a colored moving picture and so on.

In high-speed RAM-write mode (HWM), RAM write data are temporarily stored to the internal register of the HD66789R. When a data write operation of one word to the internal register is executed 4 times, the data are written to the internal RAM of the HD66789R at once. Since the data latched in the register are written to the internal RAM at once, it is possible to write next data to the internal register while the data are being written to the internal RAM. The high-speed RAM write mode enables consecutive high-speed access to the internal RAM, which is required for moving picture display and other operations.

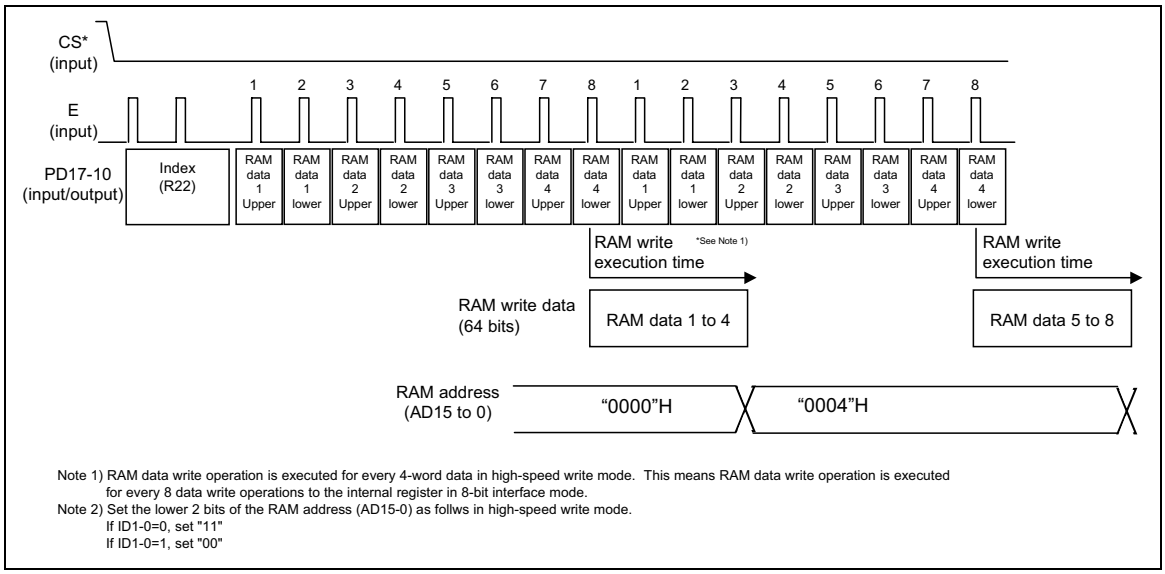


Operational flow of High-Speed RAM Write



Note 1) Wait at least for RAM write execution time (bus cycle time of normal write mode (tCYC)) before issueing a next instruction after switching from the high-speed write mode.
Note 2) Set the lower 2 bits of the RAM address (AD15-0) as follws in high-speed write mode.
If ID1-0=0, set "11"
If ID1-0=1, set "00"

High-Speed Consecutive Write Operation to RAM



Note 1) RAM data write operation is executed for every 4-word data in high-speed write mode. This means RAM data write operation is executed for every 8 data write operations to the internal register in 8-bit interface mode.
Note 2) Set the lower 2 bits of the RAM address (AD15-0) as follws in high-speed write mode.
If ID1-0=0, set "11"
If ID1-0=1, set "00"

Example of high-speed consecutive write operation in 8-bit interface mode

Notes to the high-speed RAM write mode

1. Logical and compare operations are not available with the high-speed write operation.

2. RAM write operation is executed for every 4-word data. Set the lower 2 bits of the RAM address (AD15-0) before the RAM write operation as follows.

   If ID0=0, set "11".
   If ID0=1, set "00".

3. The data write operation to the internal RAM is executed for every 4-word data. If the data write operation is terminated before it is executed 4 times, the last data will not be written to the internal RAM.

4. When the index register is set to R22H in high-speed RAM write mode, the first write operation is always executed. In this case, the RAM data read operation cannot be operated simultaneously. During the RAM read operation, make sure to set HWM to 0.

5. The high-speed RAM write mode is not operable with the normal RAM write mode. When the mode is switched to the other, make sure to set a RAM address (AD15-0) in the address counter after switching the mode.

6. When writing data in high speed RAM write mode within a window address setting area, dummy write operations may be required for some window address area settings. See "High-Speed RAM Write with Window Address Function" for details.

Table 43

	Normal RAM Write (HWM=0)	**High-Speed RAM Write (HWM=1)**
Logical operation	Available	Not available
Compare operation	Available	Not available
BGR function	Available	Available
Write mask function	Available	Available
RAM address set	Set for every one word	ID0 =0: Set the lower two bits to 11 ID0 =1: Set the lower two bits to 00
RAM read	Executed for every one word	Not available
RAM write	Executed for every one word	Dummy writing may be required for some window address settings
Window address	Set for every one word	Horizontal range (HSA/HSE): more than 4 words Horizontal write operation: 4N (N≥2) times
External display interface	Available	Available
AM Setting	AM = 1/0	AM = 0

High-Speed RAM Write with Window Address Function

To rewrite data in an arbitrary set rectangular area on the internal RAM consecutively in high speed, the number of write operation should be made 4 multiple times by adding dummy write operations if necessary.

The number of dummy write operations executed at the start and the end of data write operations is determined when the horizontal window address setting bits (HSA1-0, HEA1-0) are set. The total write operations including dummy write operations must be 4 multiple times per line.

Table 44 Number of Dummy Write Operations in High-Speed RAM Write (HSA Bits)

HSA1	HSA0	Number of Dummy Write Operations inserted in horizontal direction at the start
0	0	0
0	1	1
1	0	2
1	1	3

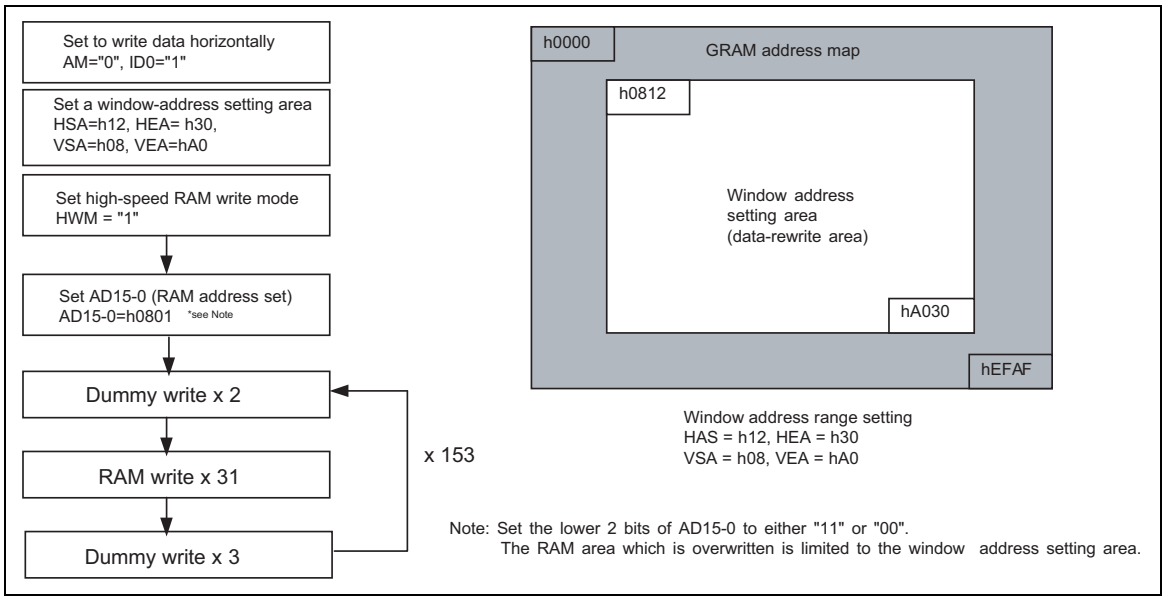
Table 45 Number of Dummy Write Operations in High-Speed RAM Write (HEA Bits)

HEA1	HEA0	Number of Dummy Write Operations Inserted in horizontal direction at the end
0	0	3
0	1	2
1	0	1
1	1	0

The number of RAM access including the dummy writes operation when writing data in the horizontal direction must be made 4 × N times:
Horizontal RAM write =
start dummy write operations + data write operations + end dummy write operations= 4 × N (times)

An example of a RAM write operation in high speed RAM write mode within a window address setting area is as follows.

In the following example, the RAM data in a window address setting area are written over consecutively in high speed by inserting two dummy write operations at the start of the line and three dummy write operations at the end of the line. The number of dummy write operations is determined when the HSA1-0 and HEA1-0 bits are set to “10” and “00”, respectively



High-Speed RAM Write with Window Address Function

Window Address Function

The window address function enables consecutive data write operations to the rectangular area on the internal RAM, which is defined by the horizontal address registers (start: HSA7-0, end: HEA 7-0) and the vertical address registers (start: VSA7-0, end: VEA7-0).

The AM bit determines the address transition direction (either increment or decrement) to allow writing data, including picture data, consecutively without taking wraparound positions into consideration.

The window address setting area must be set within the GRAM address map area. Also, set AD15-0 (a RAM address) within the window address setting area.

[Window address setting range]

(Horizontal direction) 00H ≤ HSA7-0 ≤ HSA7-0 ≤ "AF"H

(Vertical direction) 00H ≤ VSA7-0 ≤ VEA7-0 ≤ "EF"H

[RAM address set (AD15-0) setting range (within a window address setting area)]

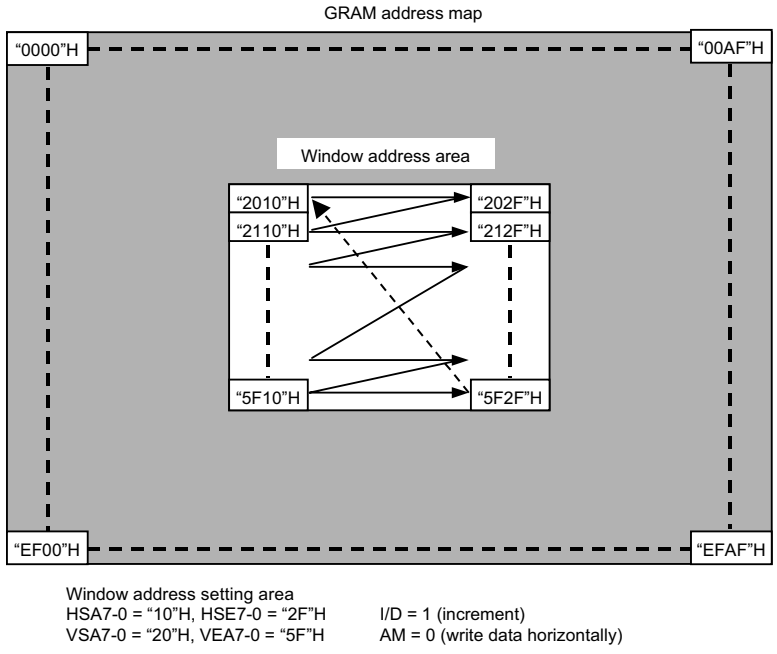
(RAM address) HSA7-0 ≤ AD7-0 ≤ HEA7-0

VSA7-0 ≤ AD15-8 ≤ VEA7-0

Note: In high-speed RAM write mode, the lower two bits of the RAM address (AD15-0) must be set as follows.

ID0=0: Set the lower two bits to 11.

ID0=1: Set the lower two bits to 00.



Graphics Operation Function

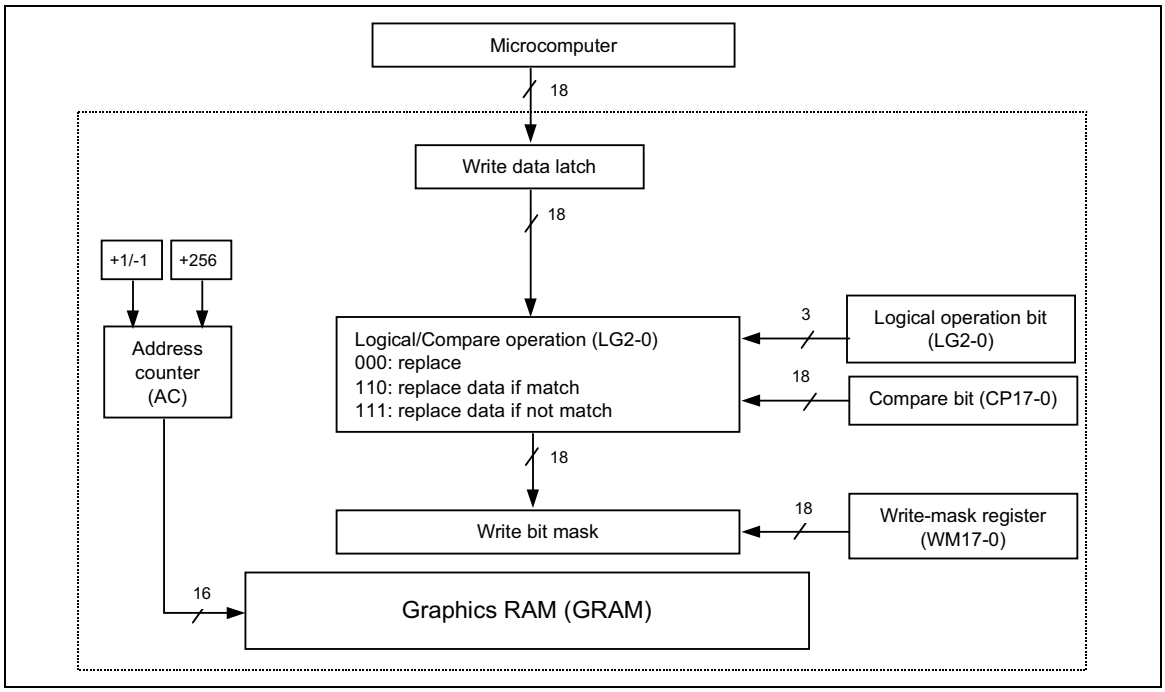
The HD66789R significantly lessen the graphics processing load on software run by the microcomputer with 18-bit bus architecture and graphics bit operations. The graphics bit operations include:

1. Write data mask function that selectively rewrites some of the bits of 18-bit write data.
2. Conditional rewrite function that compares the write data sent from the microcomputer and the data in the compare register and writes the data only when a condition is satisfied.

The graphics bit operations are executed with the entry mode register bits and the RAM write data mask register bits in combination with read or write operations with microcomputers.

Table 46

No.	Operation Mode	Bit Setting			Operation and Usage
		I/D	AM	LG2–0	
1	Write mode 1	0/1	0	000	Horizontal data replacement
2	Write mode 2	0/1	1	000	Vertical data replacement
3	Write mode 3	0/1	0	110 111	Conditional horizontal data replacement
4	Write mode 4	0/1	1	110 111	Conditional vertical data replacement

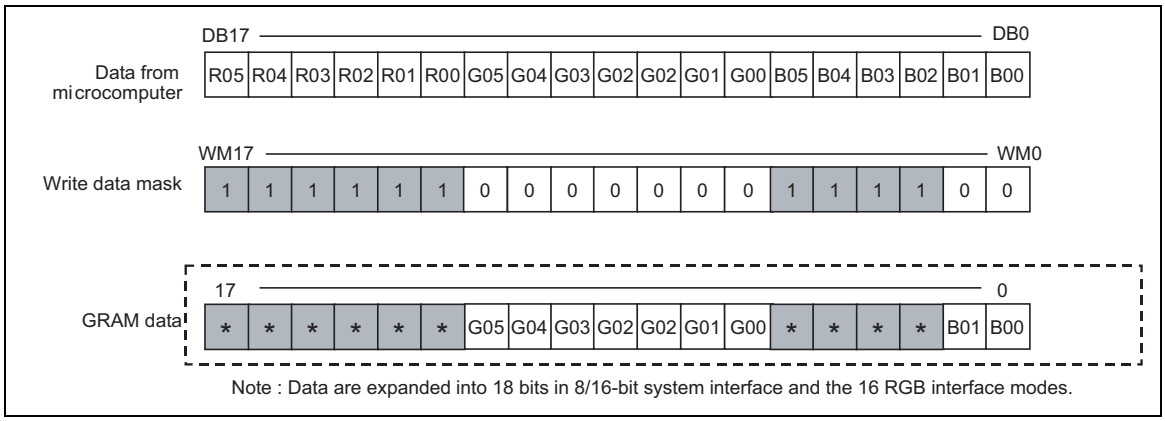


Graphics operations

Write-data Mask Function

The write data mask function controls the operation of writing 18-bit data to the internal GRAM in bit unit. The HD66789R expands 16-bit data sent from the microcomputer into 18-bit data internally. In case of 18-bit interface mode, data are not expanded.

The write data mask function enables writing the bits of RAM write data when the corresponding bits of the write data mask resister (WM17–0) are given "0" and disables writing the bits of RAM data when the corresponding bits of the write data mask register (WM17–0) are given "1". In the letter case, the GRAM data are not overwritten but retained. This function is useful when only data of one specific pixel are rewritten or a particular display color is selectively changed.

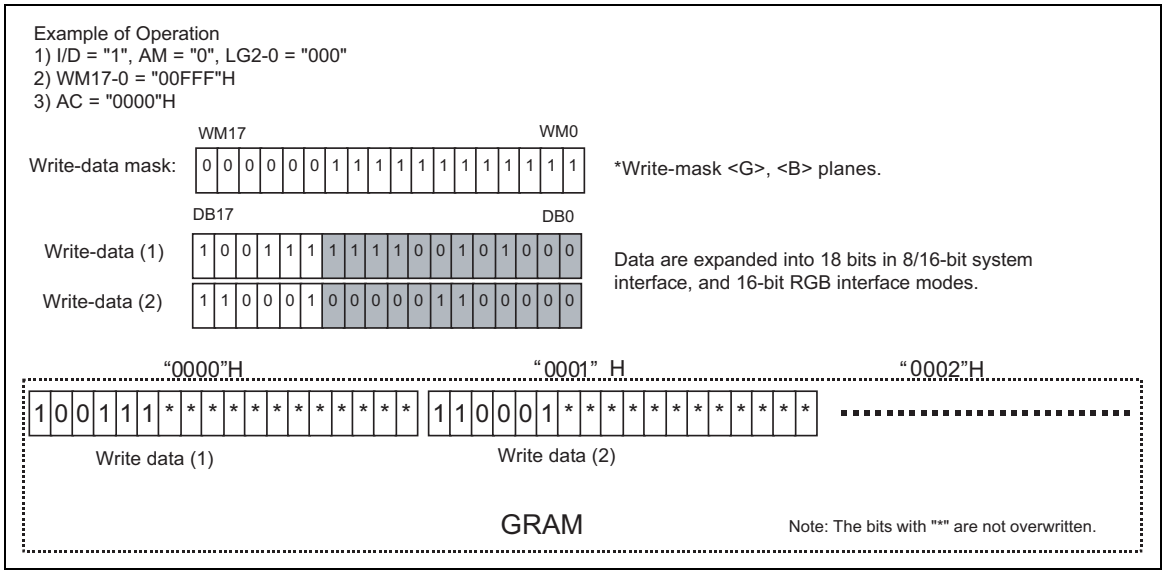


Write data mask function

Graphics Operation Processing Examples

1. Write mode 1: AM = 0, LG2–0 = 000

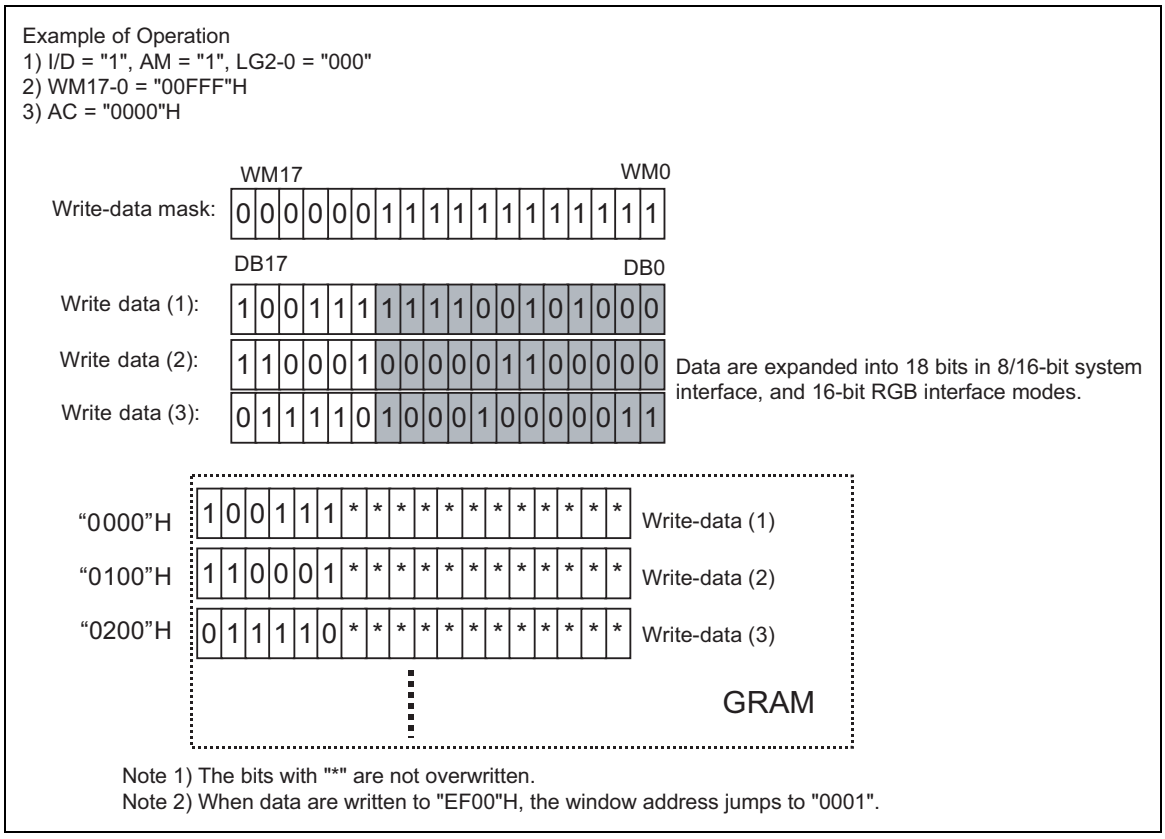
This mode is used when data are horizontally written in high-speed mode. It is also used to initialize the graphics RAM (GRAM) or to draw a line horizontally. The write-data mask function (WM17-0) is also available with this operation mode. After writing data to RAM, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the address at the opposite side of the next line below when reaching either the left or the right edge of the GRAM.



Write Mode 1

2. Write mode 2: AM = 1, LG2–0 = 000

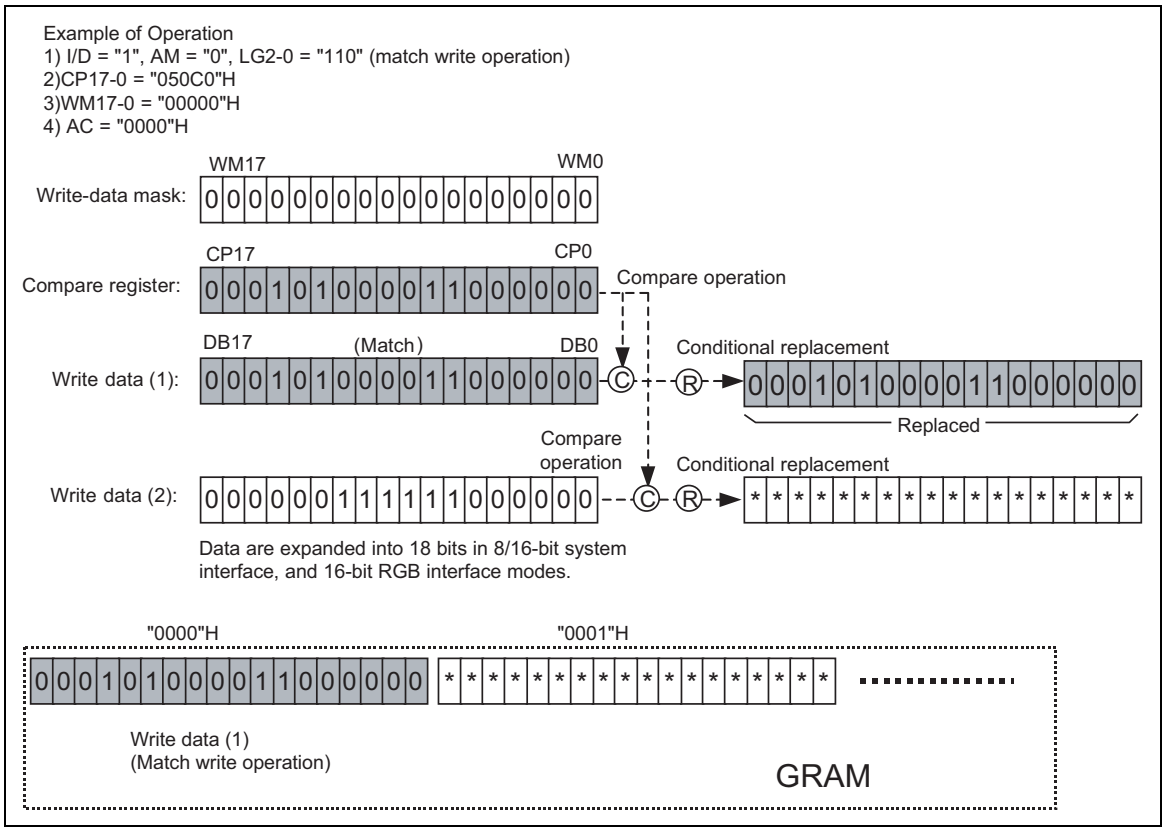
This mode is used when data are vertically written in high-speed mode. It is also used to initialize the graphics RAM (GRAM), develop font patterns or draw a line vertically. The write-data mask function (WM17-0) is also available with this operation mode. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the address at the top of either the next right row (ID = 1) or the next left row (I/D = 0) according to the I/D setting, when reaching the bottom of the GRAM.



Write Mode 2

3. Write mode 3: AM = 0, LG2–0 = 110/111

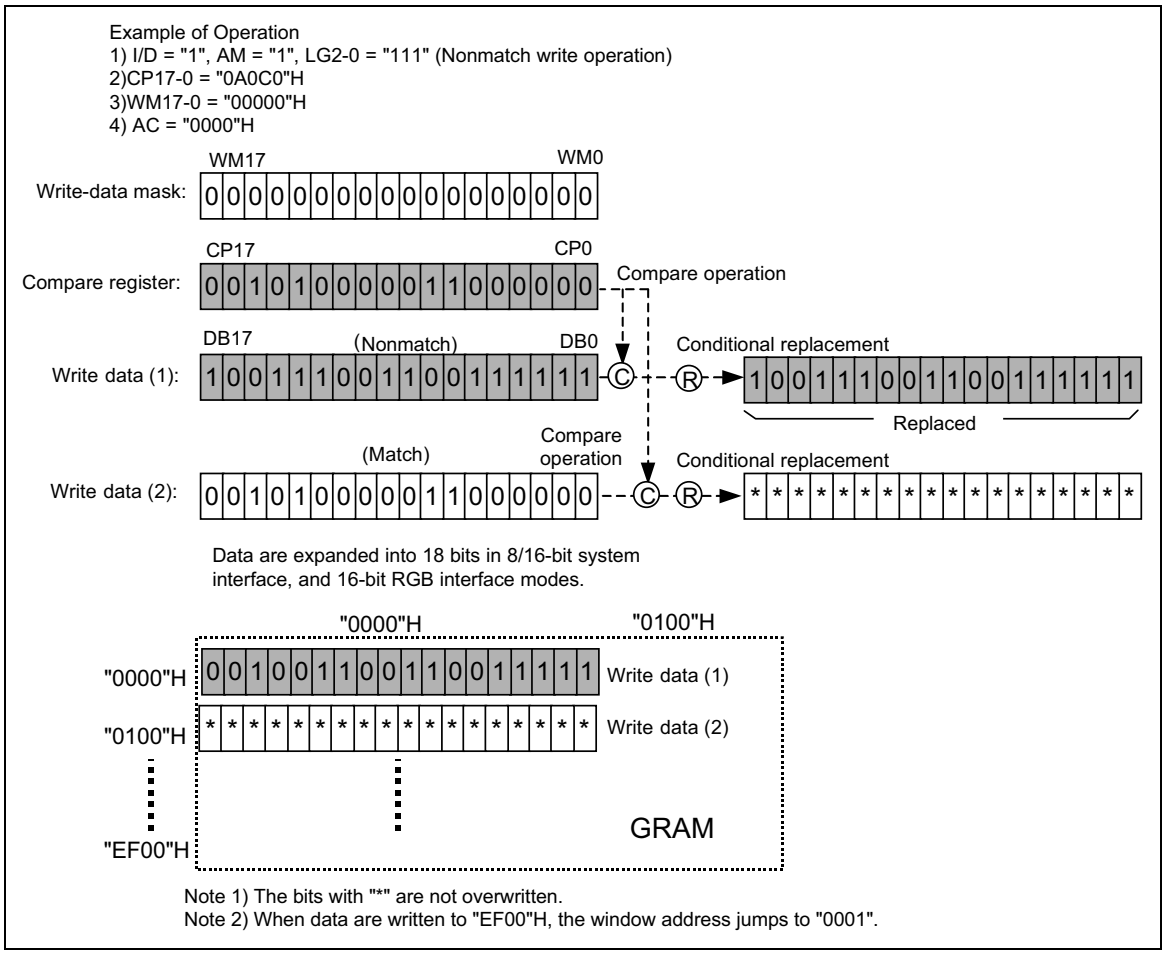
This mode is used when data are horizontally written by comparing the write data and the values of the compare register (CP17-0). When the result of comparison satisfies a condition, data sent from the microcomputer are written to the internal GRAM. The write-data mask function (WM17-0) is also available with this operation mode. After writing data to RAM, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and jumps to the address at the opposite side of the next line below when reaching either the left or the right edge of the GRAM.



Write Mode 3

4. Write mode 4: AM = 1, LG2–0 = 110/111

This mode is used when data are vertically written by comparing the write data and the values of the compare register (CP17-0). When the result of comparison satisfies a condition, data sent from the microcomputer are written to the internal GRAM. The write-data mask function (WM17-0) is also available with this operation mode. After writing data, the address counter (AC) automatically increments by 256, and automatically jumps to the address at the top of either the next right row (ID = 1) or the next left row (I/D = 0) according to the I/D setting, when reaching the bottom of the GRAM.

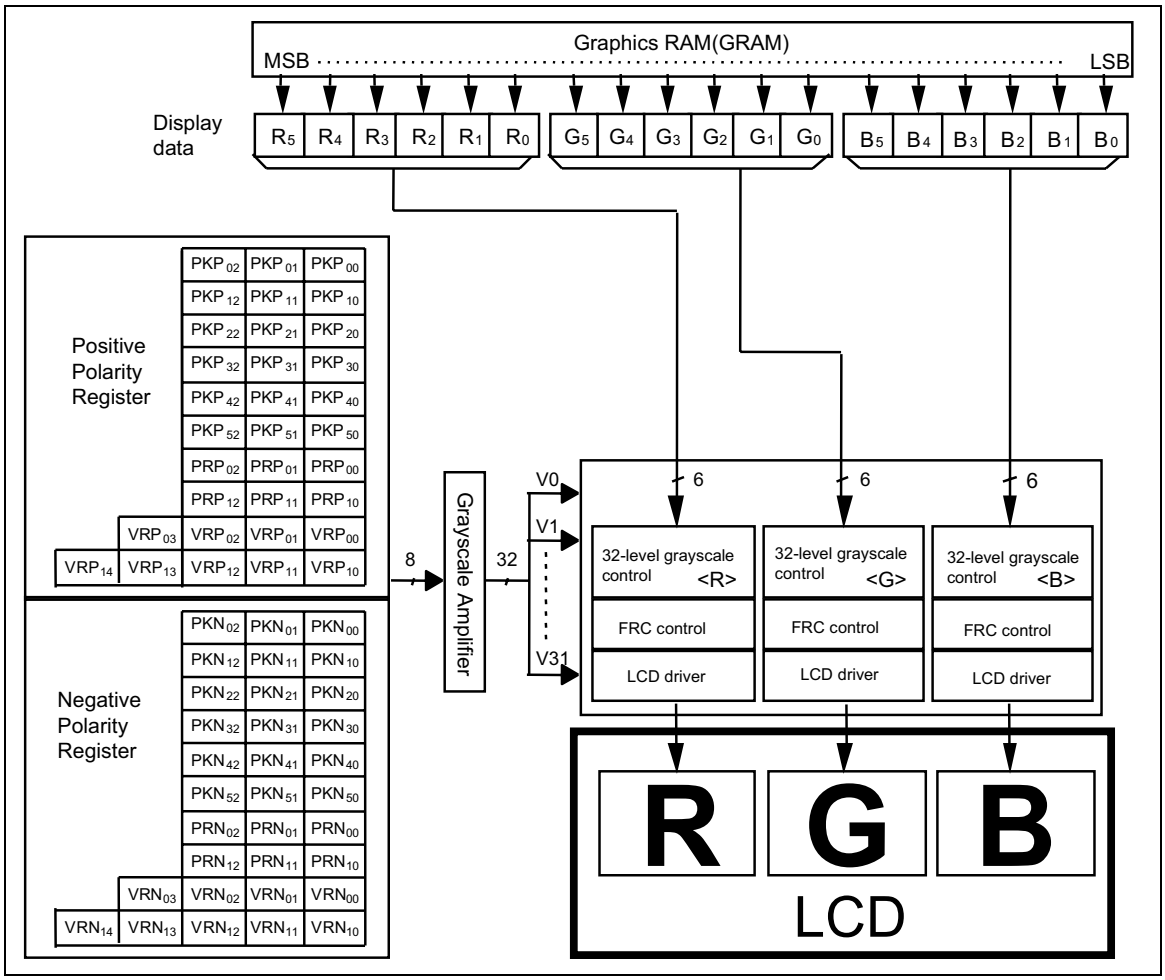


Note 1) The bits with "*" are not overwritten.
Note 2) When data are written to "EF00"H, the window address jumps to "0001".

Write Mode 4

γ-Correction Function

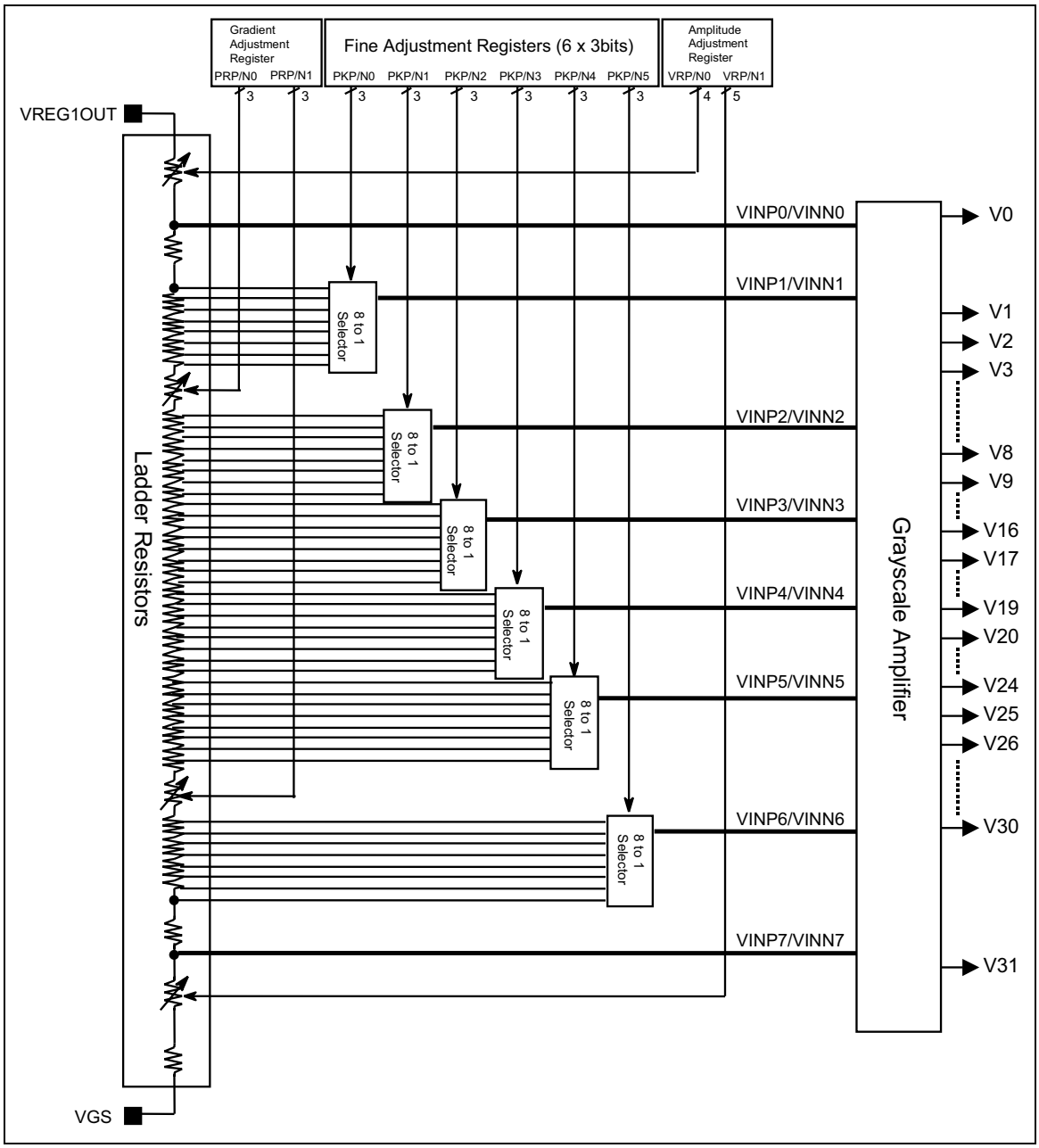
The HD66789R incorporates a γ-correction function to display in 262,144 colors simultaneously. The γ-correction is executed with the gradient-adjustment and fine-adjustment registers, which determines eight grayscales. The HD66789R incorporates gradient-adjustment and fine-adjustment registers for both positive and negative polarities. The register set of each polarity can be set independently so as to conform to the characteristics of the liquid crystal panel.

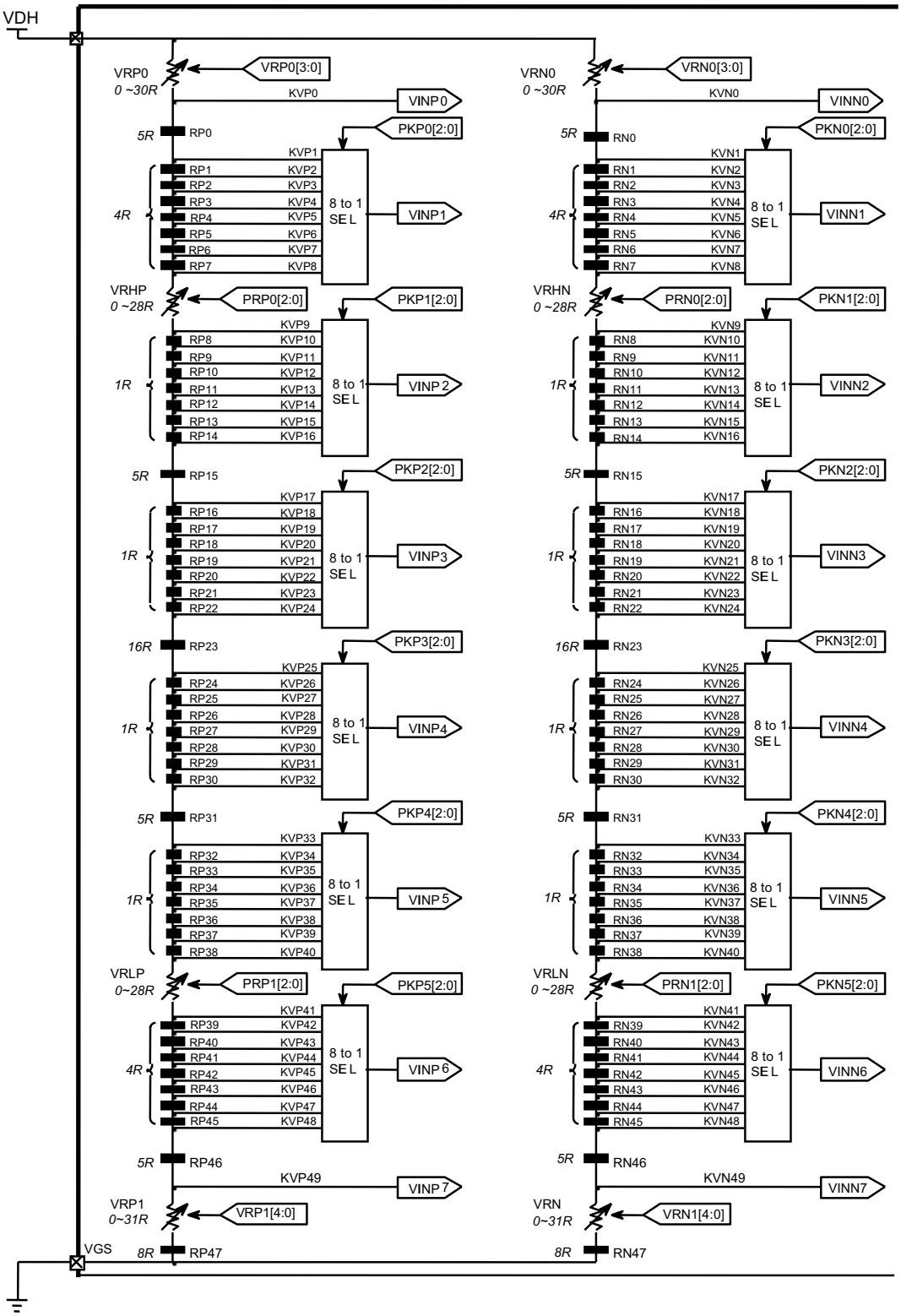


Grayscale Amplifier Block configuration

The following figure illustrates the configuration of grayscale amplifier block of the HD66789R.

The eight grayscales (VINP0-7/VINN0-7) are generated using the gradient adjustment and fine adjustment registers. Each of the grayscale level VINP01-6/VINN1-6 is further divided by the internal ladder resistors to generate 32 grayscales (V0~V31).

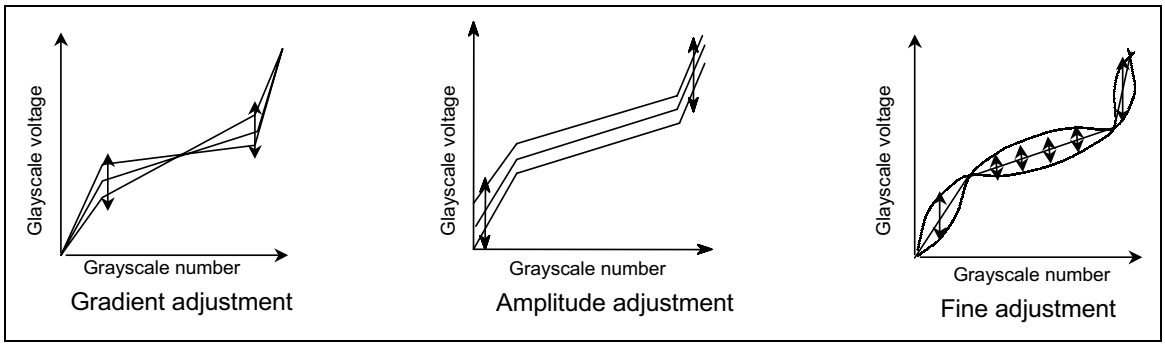




Ladder Resistors and 8-to-1 Selectors

γ-Correction Register

The γ-correction register sets an appropriate grayscale voltage that can conform to the γ-characteristics of the liquid crystal panel. The γ-correction register consists of the following 3 groups of registers, gradient, amplitude, and fine-tuning registers, which can adjust grayscales in relation to the grayscale number and the grayscale voltage characteristics. Each register group consists of a positive polarity register set and a negative polarity register set, which are set independently to each other. The reference value and RGB are common to all registers.



1. Gradient adjustment registers

The gradient adjustment registers are used to adjust the gradient around the middle of the grayscale number and the grayscale voltage characteristics without changing a dynamic range. To adjust the gradient, the values of the grayscale voltage generating variable resistors (VRHP(N)/VRLP(N)) in the middle of the ladder resistor block are controlled. The registers consist of those for the positive and negative polarities to allow asymmetric drive.

2. Amplitude adjustment registers

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. To adjust the amplitude, the values of the grayscale voltage generating variable resistors (VRP(N)1/0) in the upper and lower parts of the ladder resistor block are adjusted. Same with the gradient registers, the amplitude adjustment registers consist of those for the positive and negative polarities.

3. Fine adjustment registers

The fine adjustment registers are used to fine-adjust the grayscale voltage level. To fine-adjust the grayscale voltage level, each reference voltage level (VINP1-6/VINN1-6) is determined by the value of the corresponding fine adjustment register in the 8-to-1 selector, where 8 voltage levels generated by the ladder register are fed. Same with the other registers, the fine adjustment registers consist of those for the positive and negative polarities.

Table 47

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	PRP0 [2:0]	PRN0 [2:0]	Variable resistor VRHP (N)
	PRP1 [2:0]	PRN1 [2:0]	Variable resistor VRLP (N)
Amplitude adjustment	VRP0 [3:0]	VRN0 [3:0]	Variable resistor VRP (N)0
	VRP1 [4:0]	VRN1 [4:0]	Variable resistor VRP (N)1
Fine adjustment	PKP0 [2:0]	PKN0 [2:0]	8-to-1 selector (grayscale voltage V0)
	PKP1 [2:0]	PKN1 [2:0]	8-to-1 selector (grayscale voltage V4)
	PKP2 [2:0]	PKN2 [2:0]	8-to-1 selector (grayscale voltage V10)
	PKP3 [2:0]	PKN3 [2:0]	8-to-1 selector (grayscale voltage V21)
	PKP4 [2:0]	PKN4 [2:0]	8-to-1 selector (grayscale voltage V27)
	PKP5 [2:0]	PKN5 [2:0]	8-to-1 selector (grayscale voltage V31)

Ladder resistors and 8-to-1 selector

Block configuration

The block diagram of page **116** consists of two ladder resistor blocks including variable resistors, and 8-to-1 selectors which selects the grayscale reference voltages (VINP(N)1~6) among the 8 voltage levels generated by the ladder resistors. The variable resistors and the 8-to-1 selectors are controlled by the above-mentioned γ correction registers. The block includes pins to connect a volume resistor externally to compensate the differences in use of different panels.

Variable resistors

The HD66789R uses variable resistors for the following three purposes: gradient adjustment (VRHP(N)/VRLP(N)); amplitude adjustment (1) (VRP(N)0); and the amplitude adjustment (2) (VRP(N)1). The value of resistance is determined by the gradient adjustment and amplitude adjustment registers as below.

Table 48

Gradient adjustment		Amplitude adjustment (1)		Amplitude adjustment (2)	
Contents of Register PRP(N) 0/1[2:0]	Resistance VRHP(N) VRLP(N)	Contents of Register VRP(N)0[3:0]	Resistance VRP(N)0	Contents of Register VRP(N)1[4:0]	Resistance VRP(N)1
000	0R	0000	0R	00000	0R
001	4R	0001	2R	00001	1R
010	8R	0010	4R	00010	2R
011	12R	:	:	:	:
100	16R	:	:	:	:
101	20R	1101	26R	11101	29R
110	24R	1111	28R	11110	30R
111	28R	1111	30R	11111	31R

8-to-1 selector

The 8-to-1 selector selects one voltage level among eight voltage levels generated by the ladder resistor according to the value represented by the fine adjustment register, and output it as a reference voltage (VINP(N)1~6). The table below shows the correspondence between the value of the fine adjustment register and the selected voltage level for each of the reference voltages (VINP(N)1~6).

Table 49 Fine adjustment registers and selected voltage

The value of Register	Selected Voltage					
PKP(N)[2:0]	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

The grayscale levels (V0-V31) are calculated from the following equations.

equations for calculating voltage (Positive polarity) (1)

Pin	Equation	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - Δ V*VRP0/SUMRP	-	VINP0
KVP1	VREG1OUT - Δ V* VRP0+5R)/SUMRP	PKP02-00 = "000"	VINP1
KVP2	VREG1OUT - Δ V* VRP0+9R)/SUMRP	PKP02-00 = "001"	
KVP3	VREG1OUT - Δ V* VRP0+13R)/SUMRP	PKP02-00 = "010"	
KVP4	VREG1OUT - Δ V* VRP0+17R)/SUMRP	PKP02-00 = "011"	
KVP5	VREG1OUT - Δ V* VRP0+21R)/SUMRP	PKP02-00 = "100"	
KVP6	VREG1OUT - Δ V* VRP0+25R)/SUMRP	PKP02-00 = "101"	
KVP7	VREG1OUT - Δ V* VRP0+29R)/SUMRP	PKP02-00 = "110"	
KVP8	VREG1OUT - Δ V* VRP0+33R)/SUMRP	PKP02-00 = "111"	
KVP9	VREG1OUT - Δ V*(VRP0+33R+VRHP)/SUMRP	PKP12-10 = "000"	VINP2
KVP10	VREG1OUT - Δ V*(VRP0+34R+VRHP)/SUMRP	PKP12-10 = "001"	
KVP11	VREG1OUT - Δ V*(VRP0+35R+VRHP)/SUMRP	PKP12-10 = "010"	
KVP12	VREG1OUT - Δ V*(VRP0+36R+VRHP)/SUMRP	PKP12-10 = "011"	
KVP13	VREG1OUT - Δ V*(VRP0+37R+VRHP)/SUMRP	PKP12-10 = "100"	
KVP14	VREG1OUT - Δ V*(VRP0+38R+VRHP)/SUMRP	PKP12-10 = "101"	
KVP15	VREG1OUT - Δ V*(VRP0+39R+VRHP)/SUMRP	PKP12-10 = "110"	
KVP16	VREG1OUT - Δ V*(VRP0+40R+VRHP)/SUMRP	PKP12-10 = "111"	
KVP17	VREG1OUT - Δ V*(VRP0+45R+VRHP)/SUMRP	PKP22-20 = "000"	VINP3
KVP18	VREG1OUT - Δ V*(VRP0+46R+VRHP)/SUMRP	PKP22-20 = "001"	
KVP19	VREG1OUT - Δ V*(VRP0+47R+VRHP)/SUMRP	PKP22-20 = "010"	
KVP20	VREG1OUT - Δ V*(VRP0+48R+VRHP)/SUMRP	PKP22-20 = "011"	
KVP21	VREG1OUT - Δ V*(VRP0+49R+VRHP)/SUMRP	PKP22-20 = "100"	
KVP22	VREG1OUT - Δ V*(VRP0+50R+VRHP)/SUMRP	PKP22-20 = "101"	
KVP23	VREG1OUT - Δ V*(VRP0+51R+VRHP)/SUMRP	PKP22-20 = "110"	
KVP24	VREG1OUT - Δ V*(VRP0+52R+VRHP)/SUMRP	PKP22-20 = "111"	
KVP25	VREG1OUT - Δ V*(VRP0+68R+VRHP)/SUMRP	PKP32-30 = "000"	VINP4
KVP26	VREG1OUT - Δ V*(VRP0+69R+VRHP)/SUMRP	PKP32-30 = "001"	
KVP27	VREG1OUT - Δ V*(VRP0+70R+VRHP)/SUMRP	PKP32-30 = "010"	
KVP28	VREG1OUT - Δ V*(VRP0+71R+VRHP)/SUMRP	PKP32-30 = "011"	
KVP29	VREG1OUT - Δ V*(VRP0+72R+VRHP)/SUMRP	PKP32-30 = "100"	
KVP30	VREG1OUT - Δ V*(VRP0+73R+VRHP)/SUMRP	PKP32-30 = "101"	
KVP31	VREG1OUT - Δ V*(VRP0+74R+VRHP)/SUMRP	PKP32-30 = "110"	
KVP32	VREG1OUT - Δ V*(VRP0+75R+VRHP)/SUMRP	PKP32-30 = "111"	
KVP33	VREG1OUT - Δ V*(VRP0+80R+VRHP)/SUMRP	PKP42-40 = "000"	VINP5
KVP34	VREG1OUT - Δ V*(VRP0+81R+VRHP)/SUMRP	PKP42-40 = "001"	
KVP35	VREG1OUT - Δ V*(VRP0+82R+VRHP)/SUMRP	PKP42-40 = "010"	
KVP36	VREG1OUT - Δ V*(VRP0+83R+VRHP)/SUMRP	PKP42-40 = "011"	
KVP37	VREG1OUT - Δ V*(VRP0+84R+VRHP)/SUMRP	PKP42-40 = "100"	
KVP38	VREG1OUT - Δ V*(VRP0+85R+VRHP)/SUMRP	PKP42-40 = "101"	
KVP39	VREG1OUT - Δ V*(VRP0+86R+VRHP)/SUMRP	PKP42-40 = "110"	
KVP40	VREG1OUT - Δ V*(VRP0+87R+VRHP)/SUMRP	PKP42-40 = "111"	
KVP41	VREG1OUT - Δ V*(VRP0+87R+VRHP+VRLP)/SUMRP	PKP52-50 = "000"	VINP6
KVP42	VREG1OUT - Δ V*(VRP0+91R+VRHP+VRLP)/SUMRP	PKP52-50 = "001"	
KVP43	VREG1OUT - Δ V*(VRP0+95R+VRHP+VRLP)/SUMRP	PKP52-50 = "010"	
KVP44	VREG1OUT - Δ V*(VRP0+99R+VRHP+VRLP)/SUMRP	PKP52-50 = "011"	
KVP45	VREG1OUT - Δ V*(VRP0+103R+VRHP+VRLP)/SUMRP	PKP52-50 = "100"	
KVP46	VREG1OUT - Δ V*(VRP0+107R+VRHP+VRLP)/SUMRP	PKP52-50 = "101"	
KVP47	VREG1OUT - Δ V*(VRP0+111R+VRHP+VRLP)/SUMRP	PKP52-50 = "110"	
KVP48	VREG1OUT - Δ V*(VRP0+115R+VRHP+VRLP)/SUMRP	PKP52-50 = "111"	
KVP49	VREG1OUT - Δ V*(VRP0+120R+VRHP+VRLP)/SUMRP	-	VINP7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV : Voltage difference between VREG1OUT and VGS.

Equations for calculating voltage (Positive polarity) (2)

Grayscale Voltage	Equation
V0	VINP0
V1	V4+(VINP1-V4)*(15/24)
V2	V4+(VINP1-V4)*(8/24)
V3	V4+(VINP1-V4)*(4/24)
V4	VINP2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V20+(V8-V20)*(4/24)
V10	VINP3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINP4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINP5
V28	VINP6+(V27-VINP6)*(20/24)
V29	VINP6+(V27-VINP6)*(16/24)
V30	VINP6+(V27-VINP6)*(9/24)
V31	VINP7

Note : Make sure DDVDH - V0 > 0.5V
DDVDH - V4 > 1.1V

Equations for calculating voltage (Negative polarity) (1)

Pin	Equation	Fine adjustment register value	Reference Voltage
KVP0	VREG1OUT - ΔV*VRN0/SUMRN	-	VINN0
KVN1	VREG1OUT - ΔV* VRN0+5R)/SUMRN	PKN 02-00 = "000"	VINN1
KVN2	VREG1OUT - ΔV* VRN0+9R)/SUMRN	PKN 02-00 = "001"	
KVN3	VREG1OUT - Δ V* VRN0+13R)/SUMRN	PKN 02-00 = "010"	
KVN4	VREG1OUT - Δ V* VRN0+17R)/SUMRN	PKN 02-00 = "011"	
KVN5	VREG1OUT - Δ V* VRN0+21R)/SUMRN	PKN 02-00 = "100"	
KVN6	VREG1OUT - Δ V* VRN0+25R)/SUMRN	PKN 02-00 = "101"	
KVN7	VREG1OUT - Δ V* VRN0+29R)/SUMRN	PKN 02-00 = "110"	
KVN8	VREG1OUT - Δ V* VRN0+33R)/SUMRN	PKN 02-00 = "111"	
KVN9	VREG1OUT - Δ V*(VRN0+33R+VRHN)/SUMRN	PKN 12-10 = "000"	VINN2
KVN10	VREG1OUT - Δ V*(VRN0+34R+VRHN)/SUMRN	PKN 12-10 = "001"	
KVN11	VREG1OUT - Δ V*(VRN0+35R+VRHN)/SUMRN	PKN 12-10 = "010"	
KVN12	VREG1OUT - Δ V*(VRN0+36R+VRHN)/SUMRN	PKN 12-10 = "011"	
KVN13	VREG1OUT - Δ V*(VRN0+37R+VRHN)/SUMRN	PKN 12-10 = "100"	
KVN14	VREG1OUT - Δ V*(VRN0+38R+VRHN)/SUMRN	PKN 12-10 = "101"	
KVN15	VREG1OUT - Δ V*(VRN0+39R+VRHN)/SUMRN	PKN 12-10 = "110"	
KVN16	VREG1OUT - Δ V*(VRN0+40R+VRHN)/SUMRN	PKN 12-10 = "111"	
KVN17	VREG1OUT - Δ V*(VRN0+45R+VRHN)/SUMRN	PKN 22-20 = "000"	VINN3
KVN18	VREG1OUT - Δ V*(VRN0+46R+VRHN)/SUMRN	PKN 22-20 = "001"	
KVN19	VREG1OUT - Δ V*(VRN0+47R+VRHN)/SUMRN	PKN 22-20 = "010"	
KVN20	VREG1OUT - Δ V*(VRN0+48R+VRHN)/SUMRN	PKN 22-20 = "011"	
KVN21	VREG1OUT - Δ V*(VRN0+49R+VRHN)/SUMRN	PKN 22-20 = "100"	
KVN22	VREG1OUT - Δ V*(VRN0+50R+VRHN)/SUMRN	PKN 22-20 = "101"	
KVN23	VREG1OUT - Δ V*(VRN0+51R+VRHN)/SUMRN	PKN 22-20 = "110"	
KVN24	VREG1OUT - Δ V*(VRN0+52R+VRHN)/SUMRN	PKN 22-20 = "111"	
KVN25	VREG1OUT - Δ V*(VRN0+68R+VRHN)/SUMRN	PKN 32-30 = "000"	VINN4
KVN26	VREG1OUT - Δ V*(VRN0+69R+VRHN)/SUMRN	PKN 32-30 = "001"	
KVN27	VREG1OUT - Δ V*(VRN0+70R+VRHN)/SUMRN	PKN 32-30 = "010"	
KVN28	VREG1OUT - Δ V*(VRN0+71R+VRHN)/SUMRN	PKN 32-30 = "011"	
KVN29	VREG1OUT - Δ V*(VRN0+72R+VRHN)/SUMRN	PKN 32-30 = "100"	
KVN30	VREG1OUT - Δ V*(VRN0+73R+VRHN)/SUMRN	PKN 32-30 = "101"	
KVN31	VREG1OUT - Δ V*(VRN0+74R+VRHN)/SUMRN	PKN 32-30 = "110"	
KVN32	VREG1OUT - Δ V*(VRN0+75R+VRHN)/SUMRN	PKN 32-30 = "111"	
KVN33	VREG1OUT - Δ V*(VRN0+80R+VRHN)/SUMRN	PKN 42-40 = "000"	VINN5
KVN34	VREG1OUT - Δ V*(VRN0+81R+VRHN)/SUMRN	PKN 42-40 = "001"	
KVN35	VREG1OUT - Δ V*(VRN0+82R+VRHN)/SUMRN	PKN 42-40 = "010"	
KVN36	VREG1OUT - Δ V*(VRN0+83R+VRHN)/SUMRN	PKN 42-40 = "011"	
KVN37	VREG1OUT - Δ V*(VRN0+84R+VRHN)/SUMRN	PKN 42-40 = "100"	
KVN38	VREG1OUT - Δ V*(VRN0+85R+VRHN)/SUMRN	PKN 42-40 = "101"	
KVN39	VREG1OUT - Δ V*(VRN0+86R+VRHN)/SUMRN	PKN 42-40 = "110"	
KVN40	VREG1OUT - Δ V*(VRN0+87R+VRHN)/SUMRN	PKN 42-40 = "111"	
KVN41	VREG1OUT - Δ V*(VRN0+87R+VRHN+VRLP)/SUMRN	PKN 52-50 = "000"	VINN6
KVN42	VREG1OUT - Δ V*(VRN0+91R+VRHN+VRLP)/SUMRN	PKN 52-50 = "001"	
KVN43	VREG1OUT - Δ V*(VRN0+95R+VRHN+VRLP)/SUMRN	PKN 52-50 = "010"	
KVN44	VREG1OUT - Δ V*(VRN0+99R+VRHN+VRLP)/SUMRN	PKN 52-50 = "011"	
KVN45	VREG1OUT - Δ V*(VRN0+103R+VRHN+VRLP)/SUMRN	PKN 52-50 = "100"	
KVN46	VREG1OUT - Δ V*(VRN0+107R+VRHN+VRLP)/SUMRN	PKN 52-50 = "101"	
KVN47	VREG1OUT - Δ V*(VRN0+111R+VRHN+VRLP)/SUMRN	PKN 52-50 = "110"	
KVN48	VREG1OUT - Δ V*(VRN0+115R+VRHN+VRLP)/SUMRN	PKN 52-50 = "111"	
KVN49	VREG1OUT - Δ V*(VRN0+120R+VRHN+VRLP)/SUMRN	-	VINN7

SUMRP : Sum of positive ladder resistors = 128R+VRHP+VRLP+VRP0+VRP1
SUMRN : Sum of negative ladder resistors = 128R+VRHN+VRLN+VRN0+VRN1
ΔV: Voltage difference between VREG1OUT and VGS

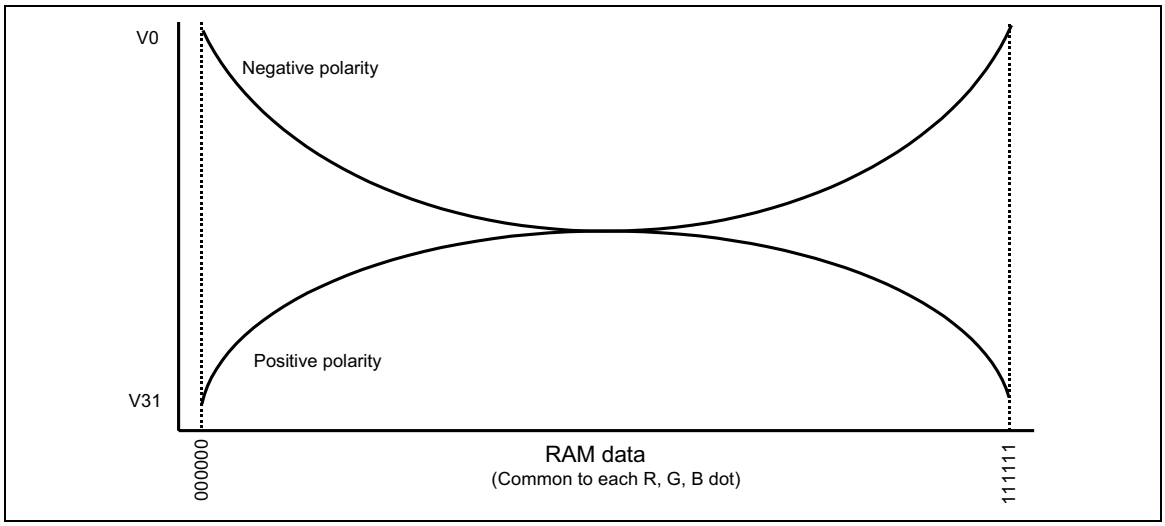
Equations for calculating voltage (Negative polarity) (2)

Grayscale Voltage	Equation
V0	VINN0
V1	V4+(VINN1-V4)*(15/24)
V2	V4+(VINN1-V4)*(8/24)
V3	V4+(VINN1-V4)*(4/24)
V4	VINN2
V5	V10+(V4-V10)*(20/24)
V6	V10+(V4-V10)*(16/24)
V7	V10+(V4-V10)*(12/24)
V8	V10+(V4-V10)*(8/24)
V9	V20+(V8-V20)*(4/24)
V10	VINN3
V11	V21+(V10-V21)*(21/24)
V12	V21+(V10-V21)*(19/24)
V13	V21+(V10-V21)*(17/24)
V14	V21+(V10-V21)*(15/24)
V15	V21+(V10-V21)*(13/24)
V16	V21+(V10-V21)*(11/24)
V17	V21+(V10-V21)*(9/24)
V18	V21+(V10-V21)*(7/24)
V19	V21+(V10-V21)*(5/24)
V20	V21+(V10-V21)*(3/24)
V21	VINN4
V22	V27+(V21-V27)*(20/24)
V23	V27+(V21-V27)*(16/24)
V24	V27+(V21-V27)*(12/24)
V25	V27+(V21-V27)*(8/24)
V26	V27+(V21-V27)*(4/24)
V27	VINN5
V28	VINN6 +(V27-VINN6)*(20/24)
V29	VINN6 +(V27-VINN6)*(16/24)
V30	VINN6 +(V27-VINN6)*(9/24)
V31	VINN7

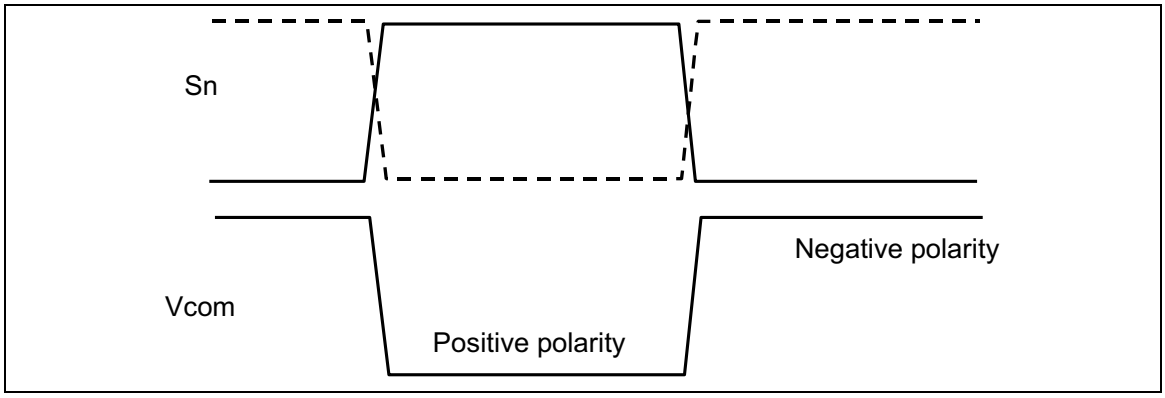
Note : Make sure DDVDH - V0 > 0.5V
DDVDH - V4 > 1.1V

Relationship between RAM data and output levels

The relationship between the RAM data and the source output levels is as follows.



RAM data and the output voltage

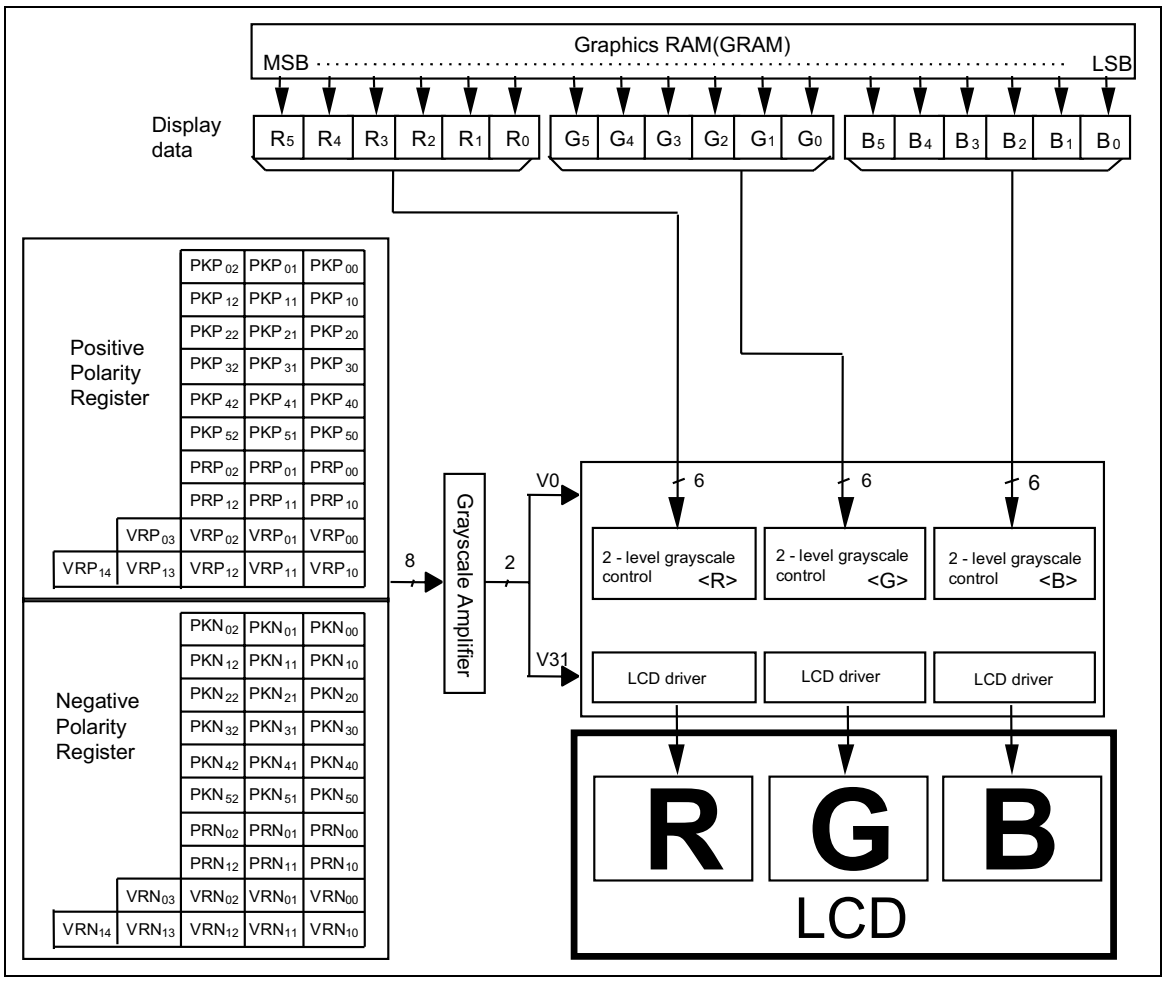


Source output and Vcom

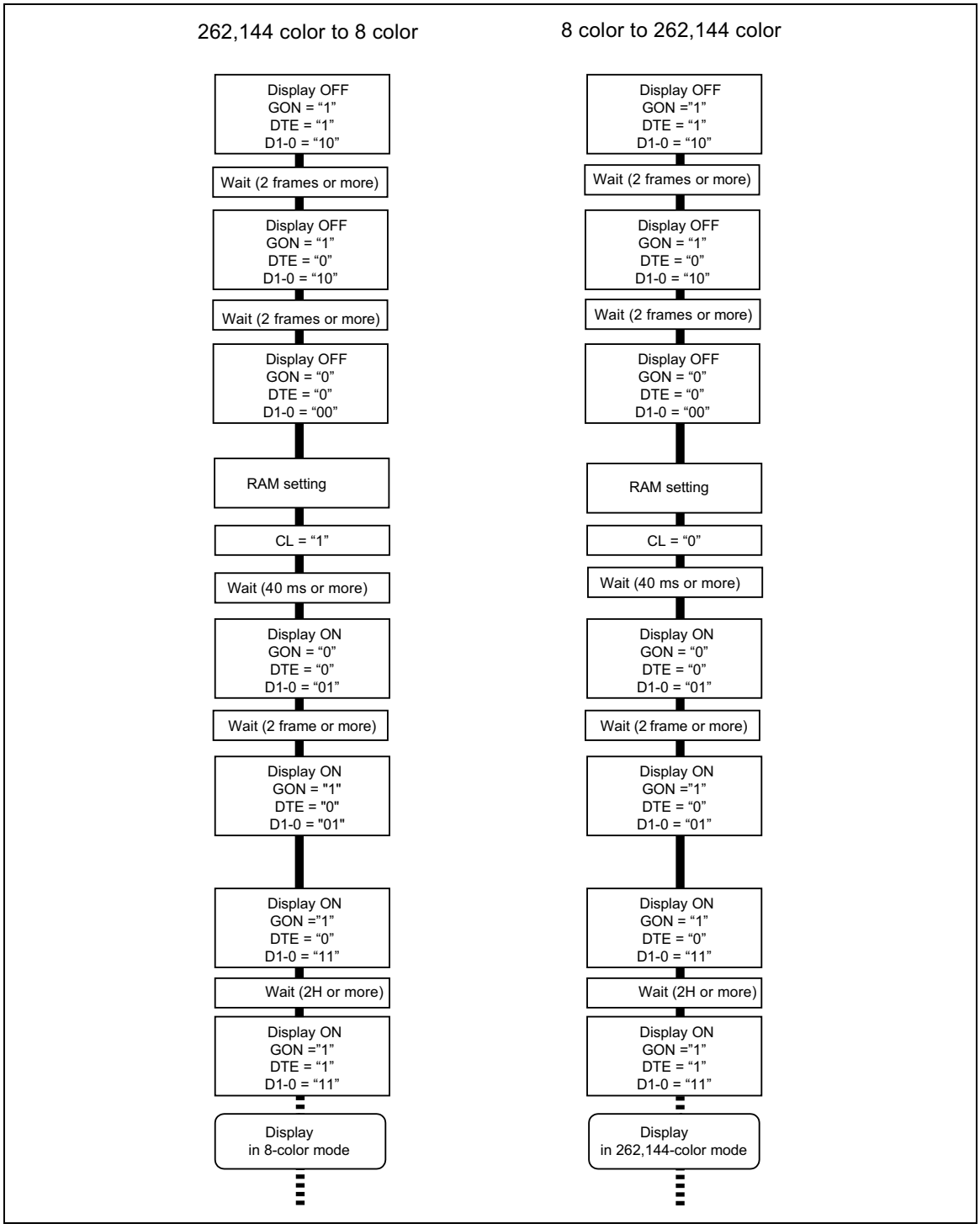
8-color Display Mode

The HD66789R incorporates a 8-color display mode. In 8-colocr mode, available grayscale levels are V0 and V31, and the power supplies of the other levels (V1-V30) are halted to reduce power consumption.

The γ- adjustment registers, PKP0-PKP5 and PKN0-PKN5, are disabled in 8-color display mode. Since power supplies for V1-V30 are halted, the RGB data in the internal GRAM should be rewritten to either "000000" or "111111" to select either V0 or V31 level before setting this mode.

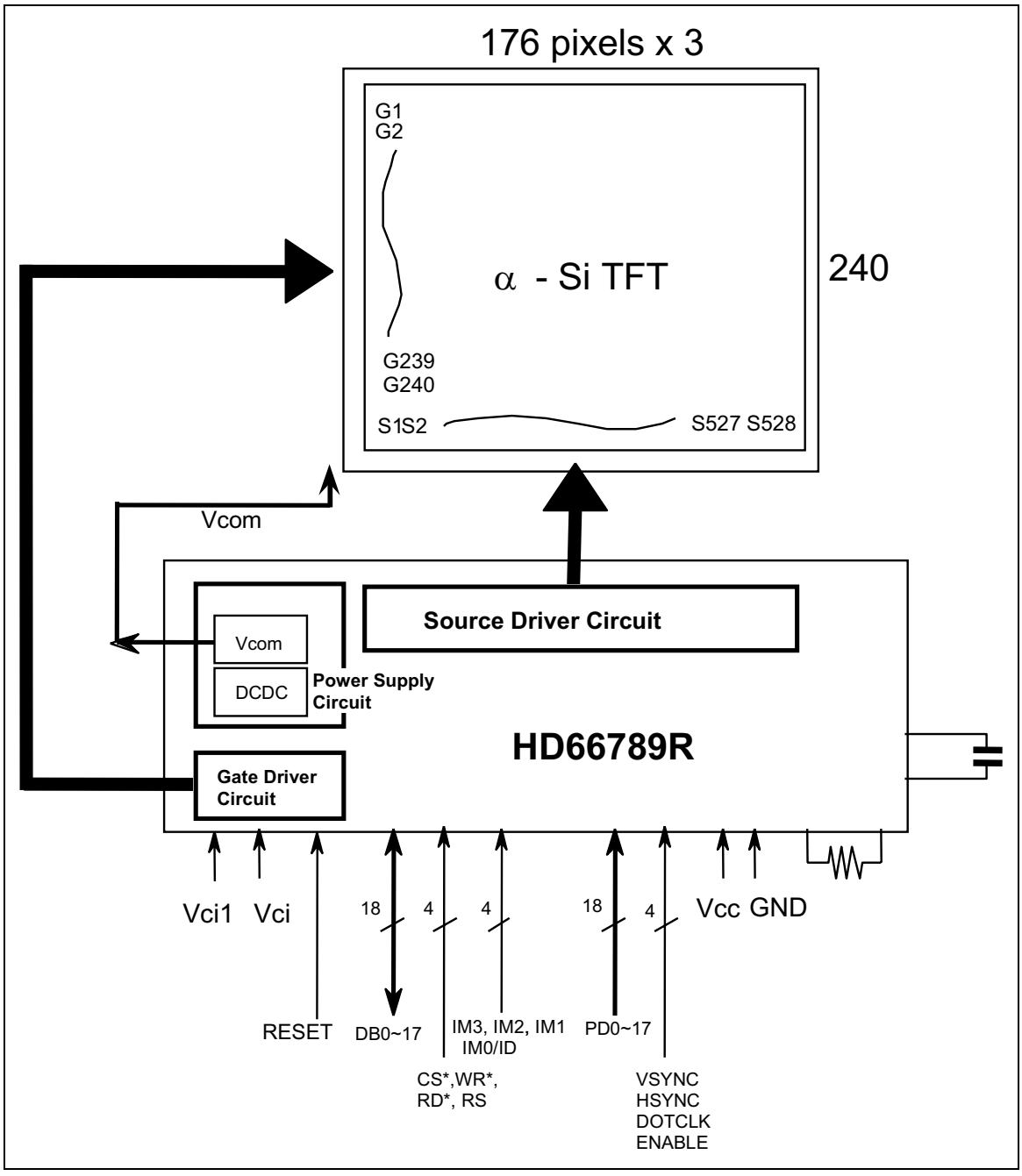


To switch between the 262, 144-color mode and the 8-color mode, follow the sequence below.



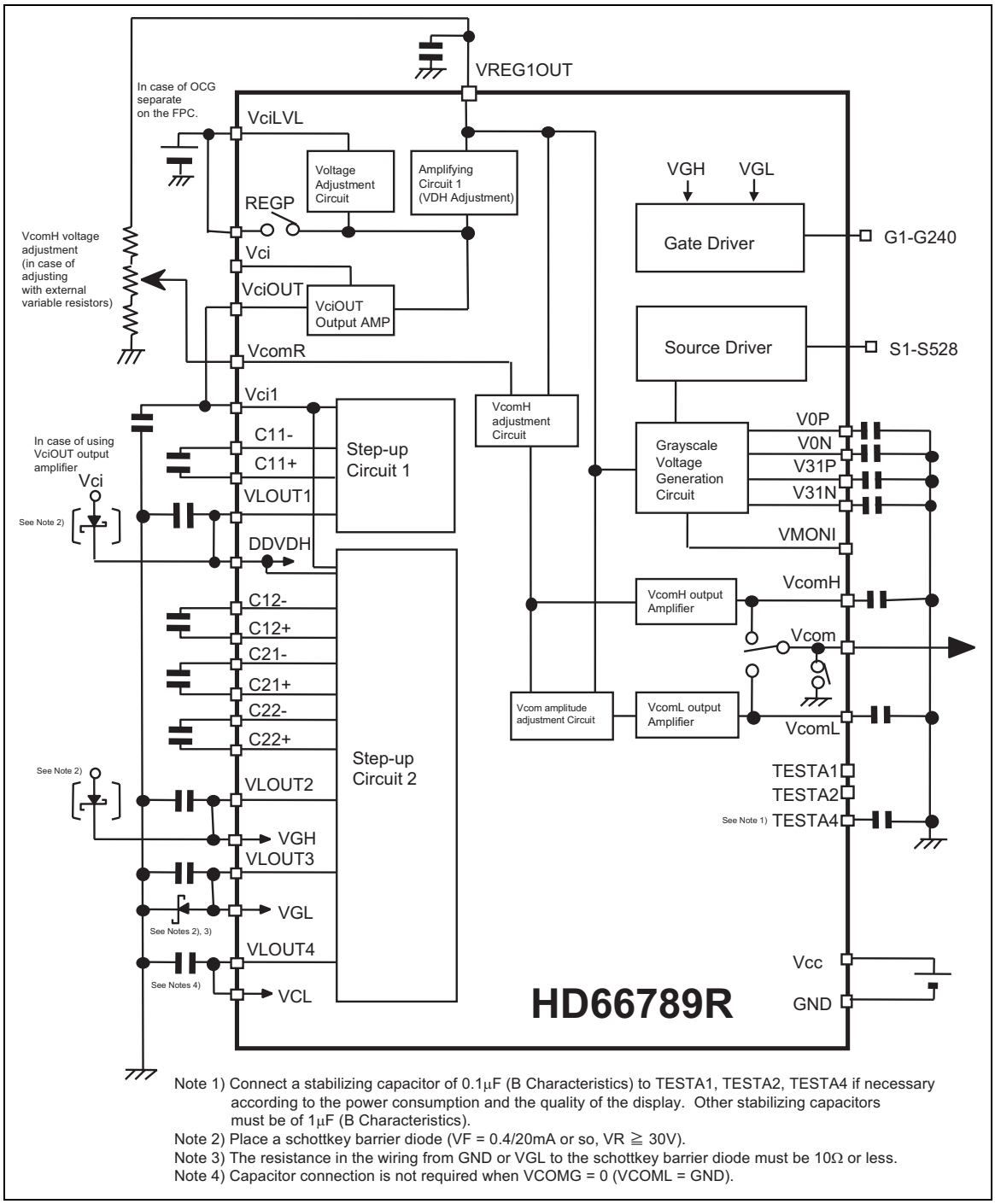
System Configuration

The following figure illustrates an example of a TFT-LCD panel of 176 x 240 dots with the HD66789R.



Configuration of power supply circuit

The internal configuration of power supply circuit of the HD66789R to generate supply voltages to drive a liquid crystal panel is as follows.



Note 1) Connect a stabilizing capacitor of 0.1μF (B Characteristics) to TESTA1, TESTA2, TESTA4 if necessary according to the power consumption and the quality of the display. Other stabilizing capacitors must be of 1μF (B Characteristics).
Note 2) Place a schottkey barrier diode (VF = 0.4/20mA or so, VR ≧ 30V).
Note 3) The resistance in the wiring from GND or VGL to the schottkey barrier diode must be 10Ω or less.
Note 4) Capacitor connection is not required when VCOMG = 0 (VCOML = GND).

Specification of external elements connected to the power supply circuit

The following table shows specifications of external elements connected to the HD66789R's power supply circuit.

Table 50 Capacitor

Capacity	Recommended voltage	Pins to connect
1 μF (B characteristics)	6V	VREG1OUT, VciOUT, VLOUT4, VcomH, VcomL, C11+/-, C12+/-
	10V	VLOUT1, C21+/-, C22+/-
	25V	VLOUT2, VLOUT3
0.1 μF (B characteristics)	6V	V0P, V0N, V31P, V31N

Table 51 Schottkey diode

Feature	Pins to connect
VF < 0.4V / 20mA at 25°C, VR ≥30V (Recommended diode: HSC226)	GND – VGL (Vci – VGH) (Vci – DDVDH)

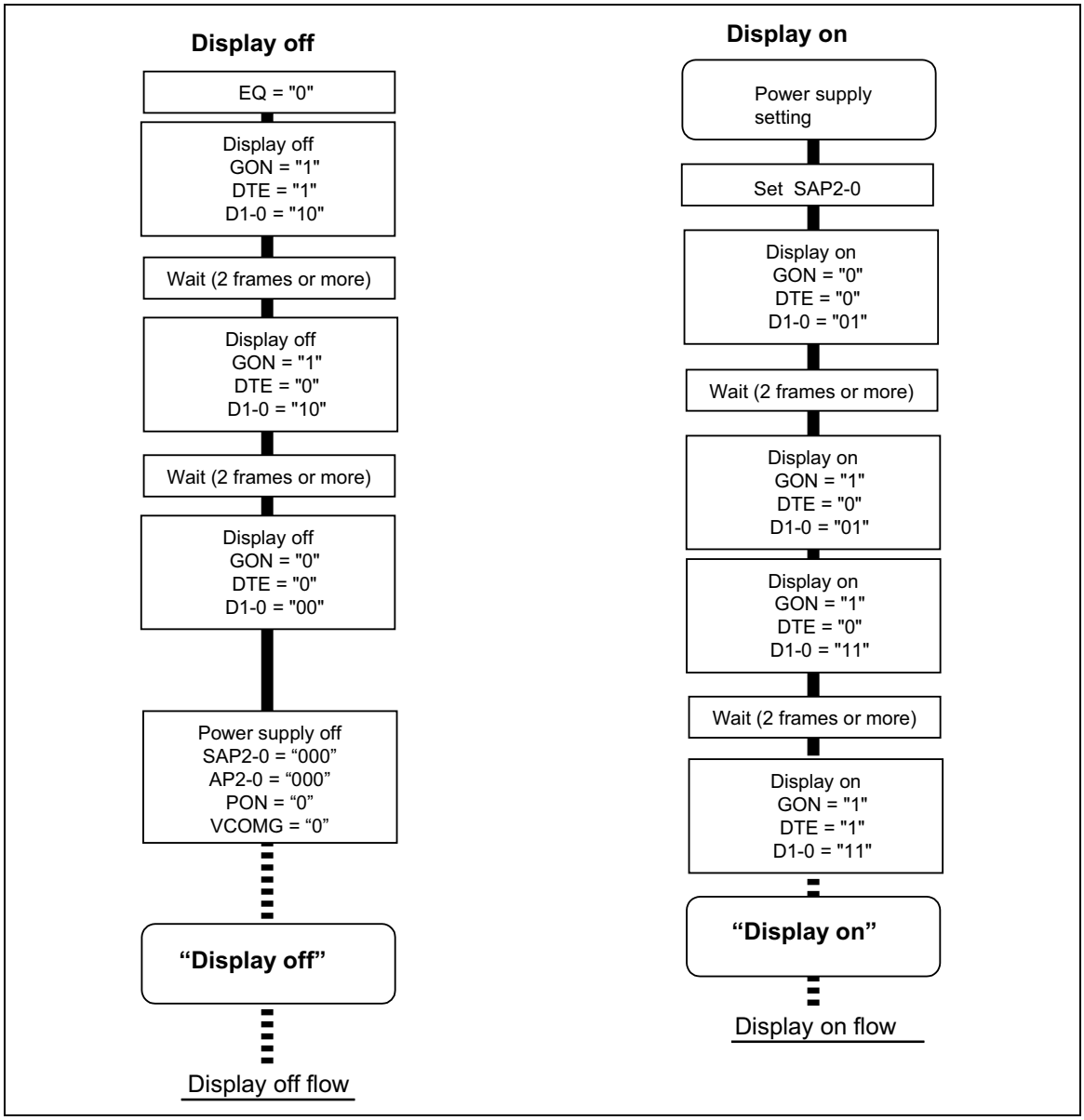
Table 52 Variable resistor

Resusabce	Pins to connect
> 200 kΩ	VcomR

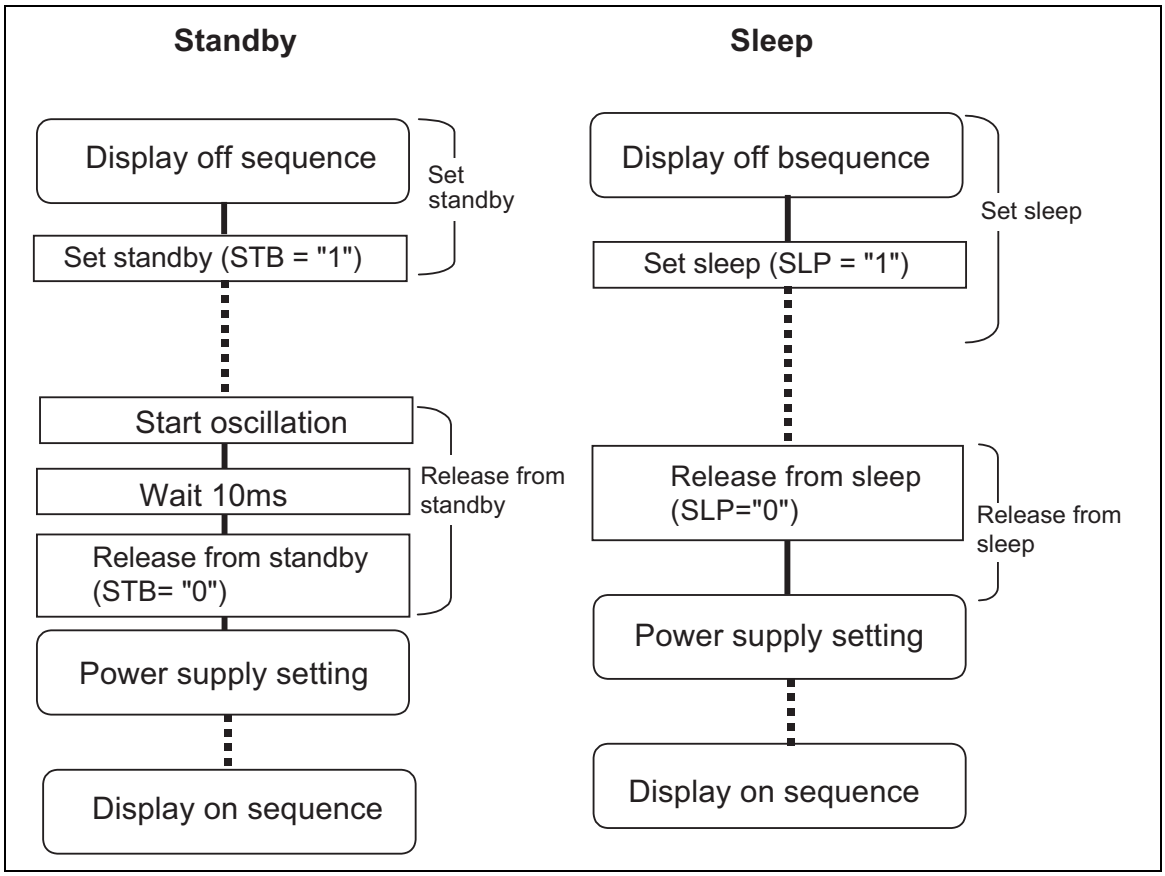
Instruction Setting Flow

Make each of the following instruction setting according to the following sequence.

Display ON/OFF

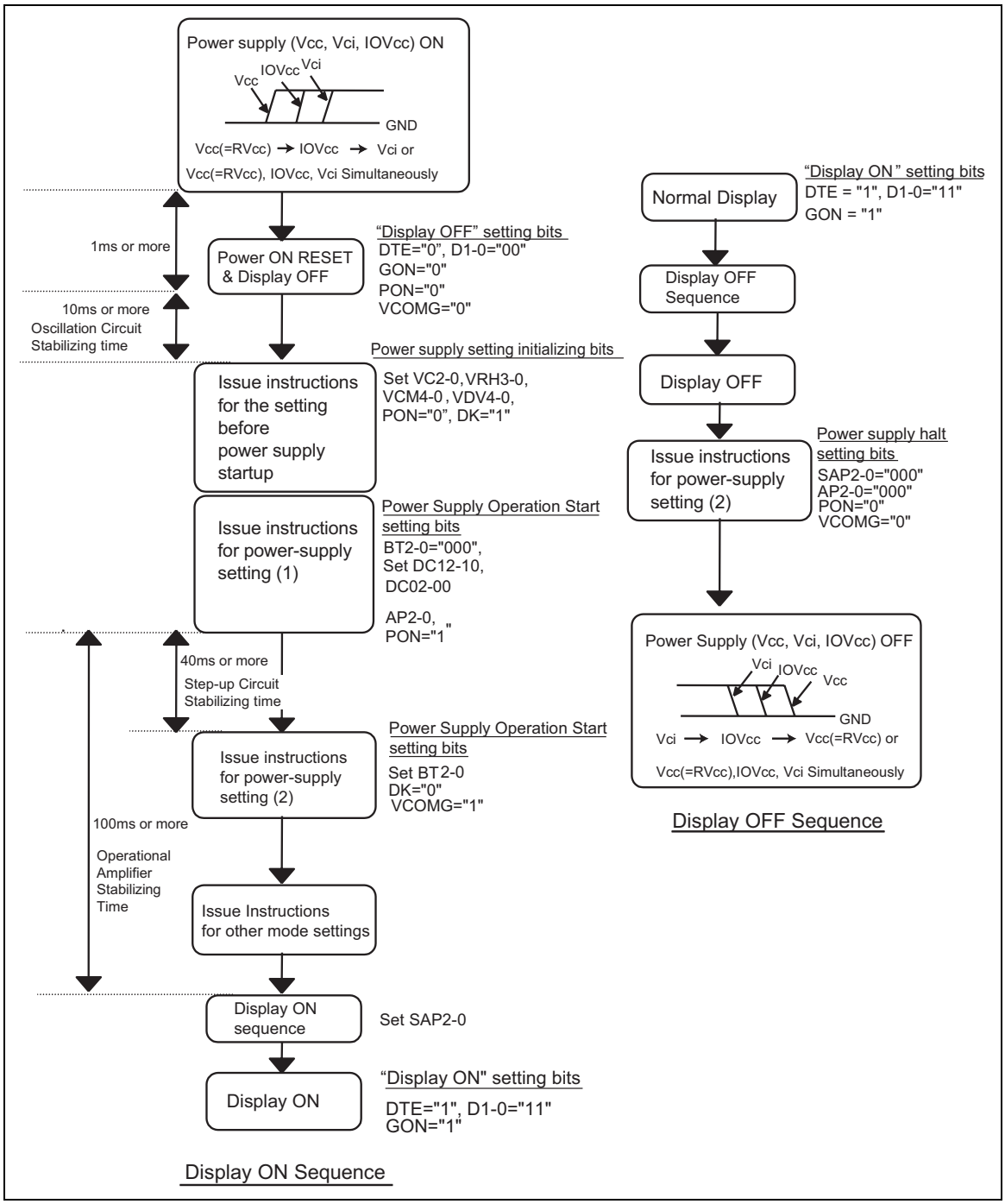


Standby and Sleep



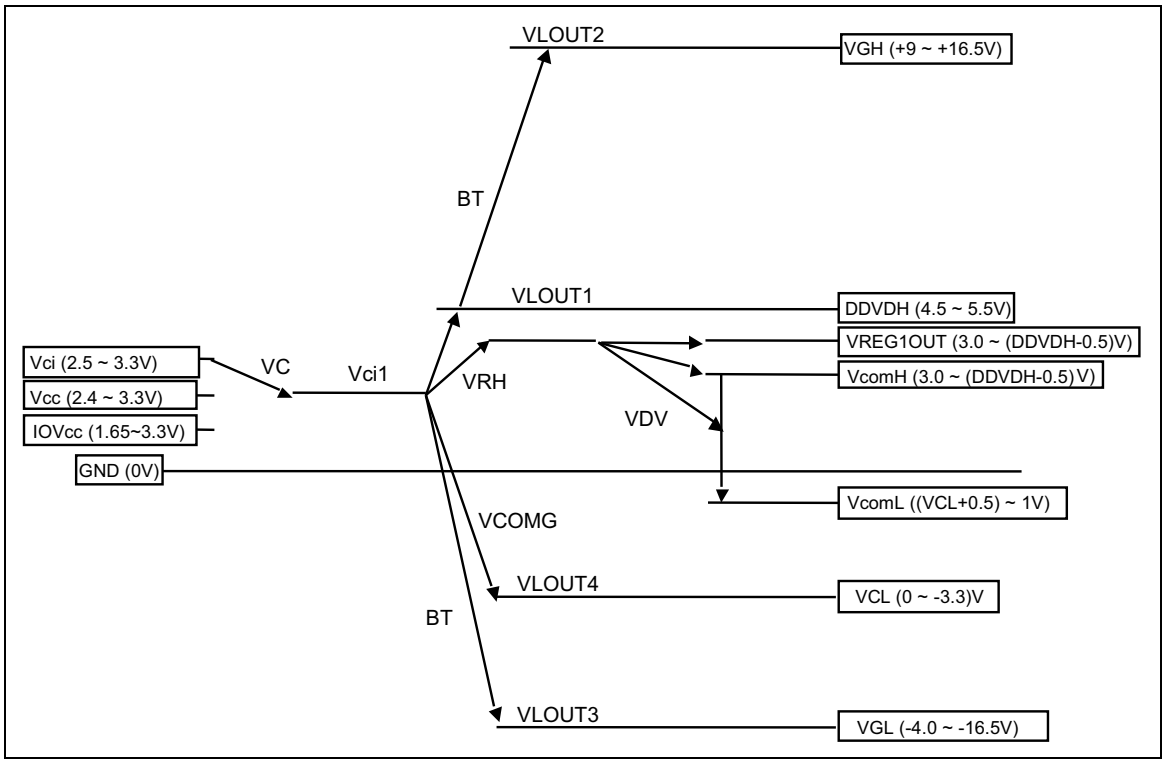
Power Supply Setting

Whenever start supplying power, follow the sequences below. The time for oscillator, step-up circuits and operational amplifiers to stabilize depends on the external resistors and capacitors.



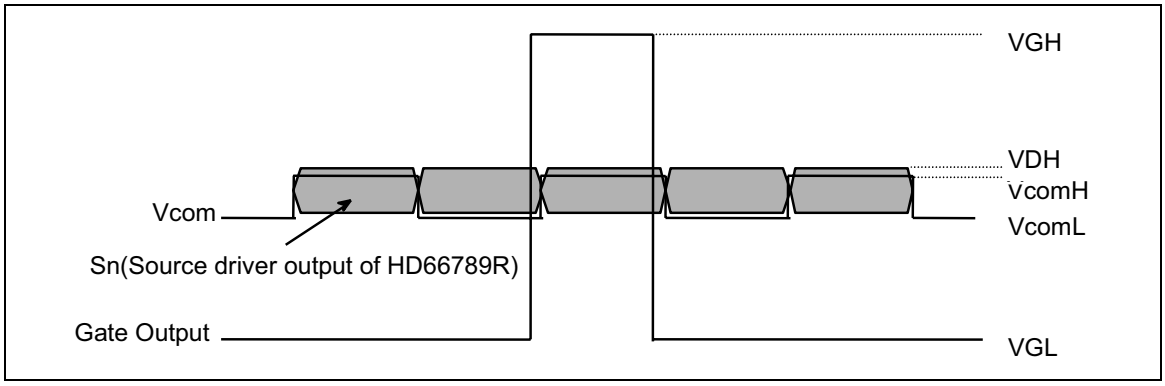
Pattern Diagram for Voltage Setting

The following are the pattern diagram for the voltage setting and the voltage applied to the TFT display.



Pattern diagram for voltage setting

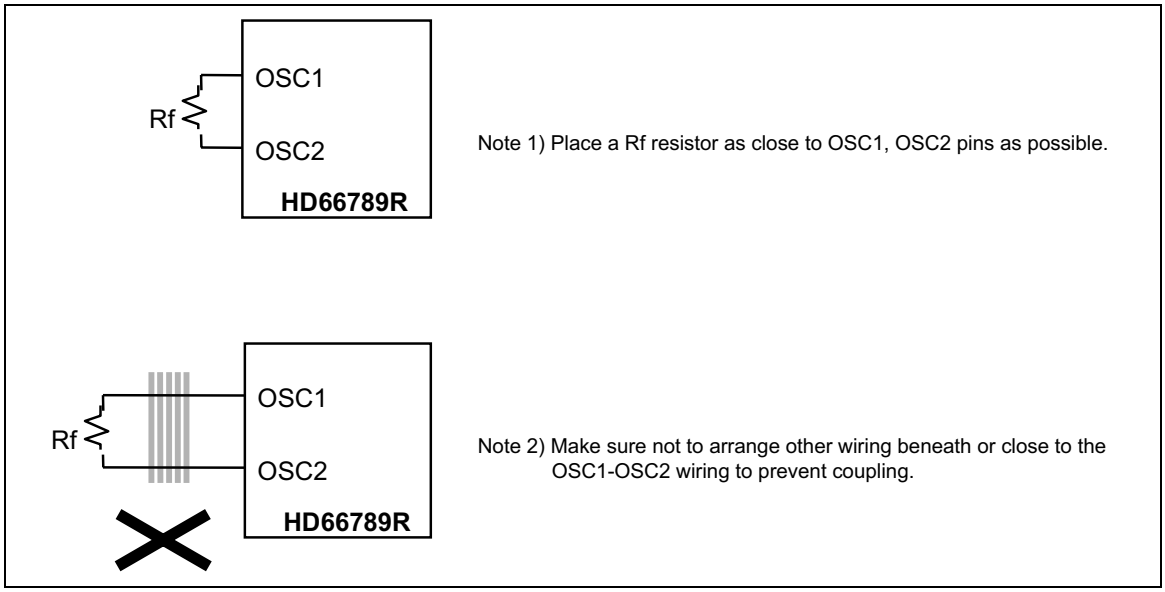
Note 1) DDVDH, VGH, VGL, VCL outputs are susceptible to voltage drop from the set voltages (ideal voltage) due to current consumption. (DDVDH – VREG1OUT) > 0.5V, (VcomL – VCL) > 0.5V are the relationships between the actual voltage levels. When the Vcom voltage alternating cycle is high (e.g. polarity inverts every line), large current will be consumed. In this case, check the voltage before use.



Applied voltage to the TFT display

Oscillator

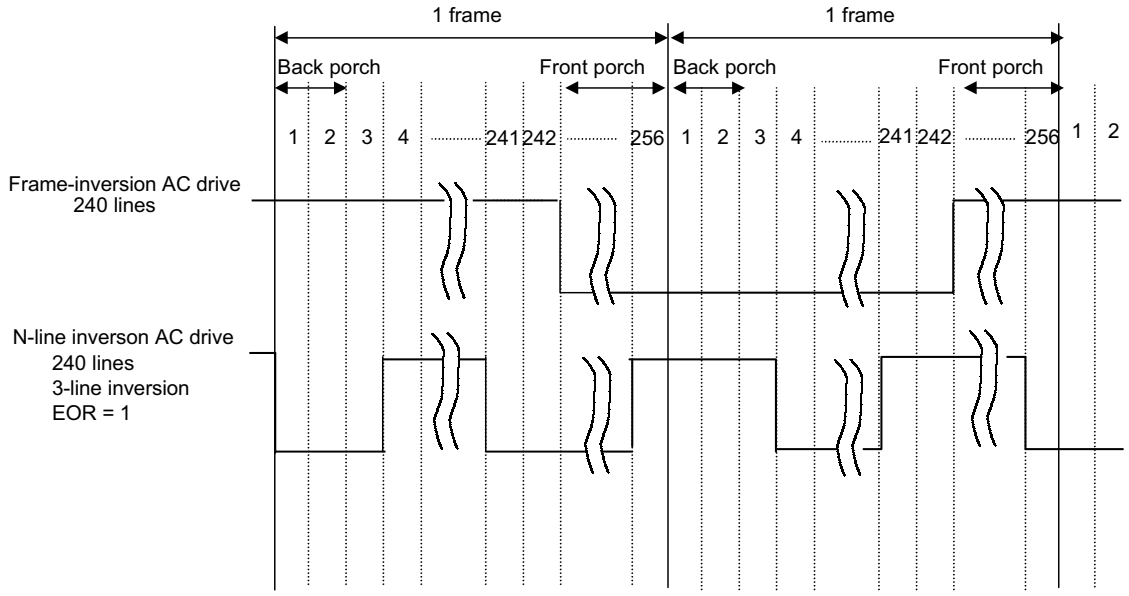
The HD66789R generates oscillation with the internal RC oscillator by placing an external oscillation resistor between the OSC1 and OSC2 pins. The oscillation frequency varies depending on the values of external resistors, the distance of wiring, and the operating supply voltages. For example, placing an Rf resistor of a large value, or lowering the supply voltage will lower the oscillation frequency. See the "Notes to Electrical Characteristics" section for the relationship between the value of Rf resistor and the oscillation frequency.



n-line inversion alternating drive

The HD66789R, in addition to the frame-inversion liquid crystal alternating current drive, supports the n-line inversion alternating current drive, where the polarity of liquid crystal is inverted in unit of n lines, where n takes a number from 1 to 64. The n-line inversion alternating current drive is a function to overcome problems associated with the quality of the display.

In determining n (the value represented by the NW bits +1), which represents the number of lines that determines the timing of liquid crystal polarity inversion, check the quality of the display on the liquid crystal panel in use. Note that setting a smaller number of lines will raise the frequency of liquid crystal polarity inversion and increase charging/discharging current on liquid crystal cells.



Note: set EOR = "1" with n-line inversion alternating current drive to prevent direct bias from reacing liquid crystal cells

Interlaced Scan

The HD66789R supports interlaced scanning that splits one frame into n fields when driving an LCD to prevent flicker.

To determine the number of fields (n: value represented by the FLD bits), check the quality of the display on the liquid crystal panel in use. The following table shows the scan (gate) lines in each of the three fields. The figure illustrates the output waveforms of 3-field interlaced scan.

Table 53

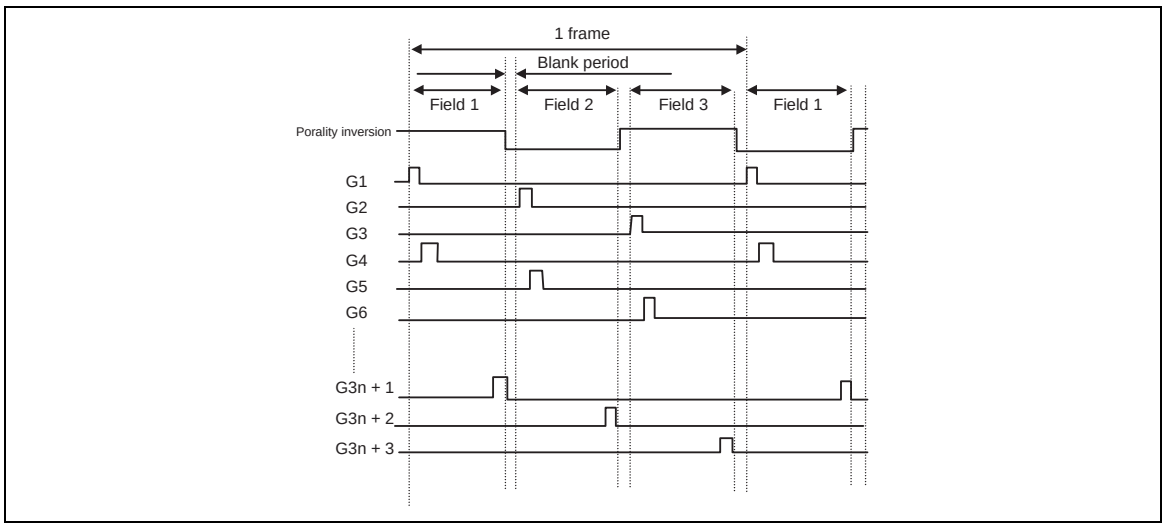
GS = 0

FLD1-0		01		11	
Gate \ Field		-	1	2	3
G1		*	*		
G2		*		*	
G3		*			*
G4		*	*		
G5		*		*	
G6		*			*
G7		*	*		
G8		*		*	
G9		*			*
:		:	:	:	:
G237		*			*
G238		*	*		
G239		*		*	
G240		*			*

GS = 1

FLD1-0		01		11	
Gate \ Field		-	1	2	3
G240		*	*		
G239		*		*	
G238		*			*
G237		*	*		
G236		*		*	
G235		*			*
G234		*	*		
G233		*		*	
G232		*			*
:		:	:	:	:
G4		*			*
G3		*	*		
G2		*		*	
G1		*			*

*: Driven gate lines

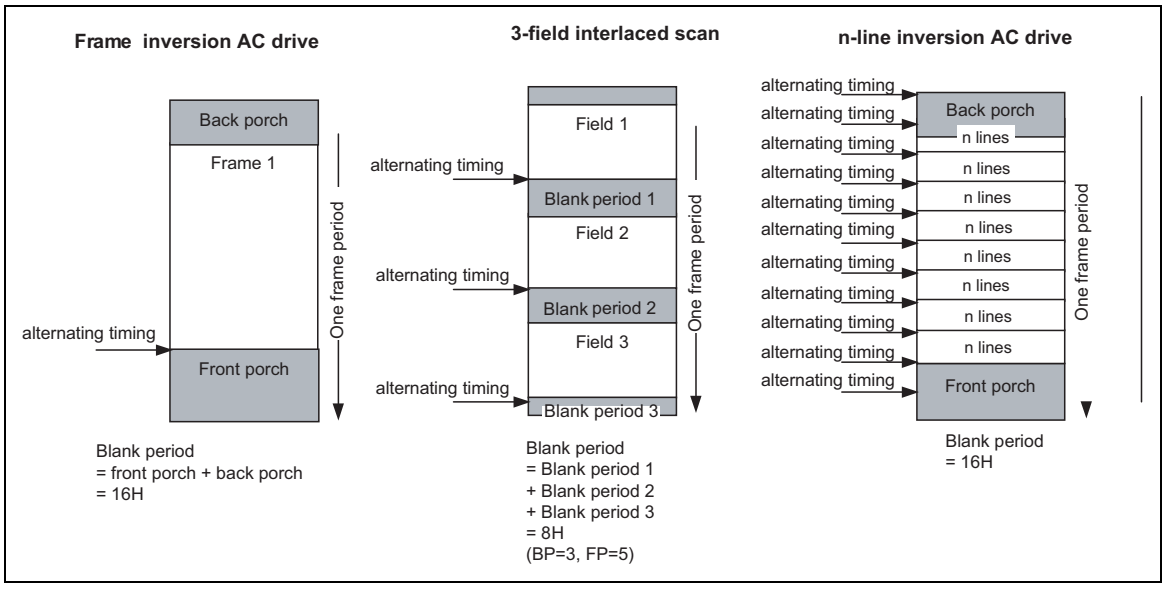


Gate output timing of 3-field interlaced scan

Alternating Timing

The following figure illustrates the liquid crystal polarity inversion timing in different driving formulas. In case of frame-inversion alternating drive, the polarity is inverted after drawing one frame, followed by a blank period lasting for a 16H period, where all outputs from the gate lines become the VGL level. In case of 3-field interlaced scan, polarity is inverted after drawing one field, followed by a blank period that adds up to a 8H period in one frame. In case of n-line inversion alternating drive, polarity is inverted as drawing n lines, and a blank period lasting for a 16H period is inserted after drawing one frame.

In interlaced drive, make sure to set the numbers of back and front porches to 3 lines and 5 lines, respectively.



Frame-Frequency Adjustment Function

The HD66789R has a frame frequency adjustment function. The frame frequency for driving LCDs can be adjusted by instructions (with DIV, RTN bits) without changing the oscillation frequency.

To switch frame frequencies between when displaying a moving picture and when displaying a still picture, set a high oscillation frequency in advance. By doing so, it becomes possible to set a low frame frequency when displaying a still picture to save power and a high frame frequency when displaying a moving picture to conform to high-speed screen rewriting demand

Relationship between Liquid Crystal Drive Duty and Frame Frequency

The relationship between the liquid crystal drive duty and the frame frequency is calculated from the following equation. The frame frequency can be adjusted by instructions with the 1H period adjustment bit (RTN bit) and the operation clock division bit (DIV bit).

(Equation to calculate frame frequency)

$$\text{Frame frequency} = \frac{\text{fosc}}{\text{Clocks per line} \times \text{division ratio} \times (\text{Line+BP+FP})} \quad [\text{Hz}]$$

fosc: RC oscillation frequency
Line: number of lines (NL bit)
Clocks per line: RTN bit
Division ratio: DIV bit
Number of lines for front porch: FP
Number of lines for back porch: BP

Example of Calculation: when maximum frame frequency = 60 Hz

Number of lines: 240 lines
1H period: 16 clock cycles (RTN3-0 = “0000”)
Operational clock division ratio: 1/1

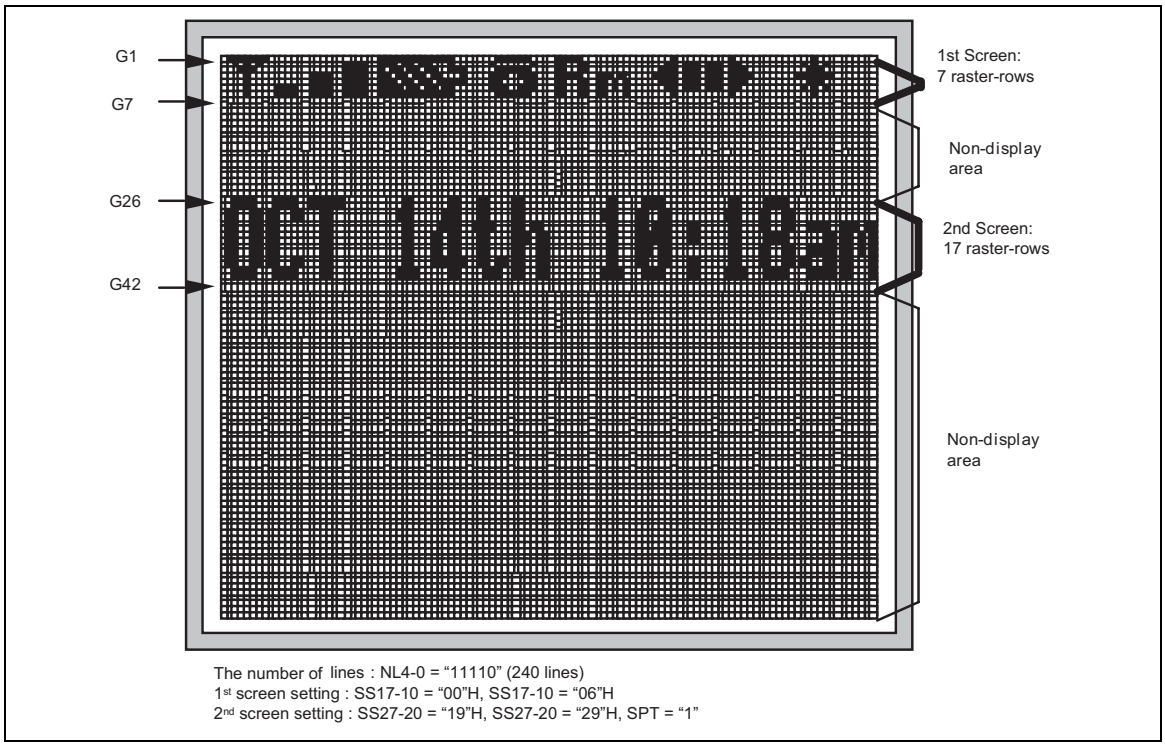
$$\text{fosc} = 60\ \text{Hz} \times (0 + 16)\ \text{clock} \times 1/1 \times (240 + 16)\ \text{lines} = 246\ (\text{kHz})$$

In this case, the RC oscillation frequency becomes 246kHz. Adjust the external resistor of the RC oscillator to 246kHz.

Partial Display Function

The HD66789R allows selectively driving two screens at arbitrary positions set with the screen-drive position registers (R42 and R43). Only the lines to display two screens are selectively driven to reduce current consumption.

The first screen drive position register (R42) specifies the start line (SS17-10) and the end line (SE17-10) to display the first screen. The second screen drive position register (R43) specifies the start line (SS27-20) and the end line (SE27-20) to display the second screen. The second screen control is effective when the SPT bit is set to 1. The total number of lines driven to display the first and second screens must be less than the number of lines set with the NL4-0 bits.



Notes to the setting of 1st/2nd screen drive position registers

When setting the start line (SS17-10) and the end line (SE17-10) of the first screen drive position register (R42), and the start line (SS27-20) and the end line (SE27-20) of the second screen drive position register (R43), it is necessary to satisfy the following conditions to display screens correctly.

Table 54 One Screen Drive (SPT = 0)

Register Settings	Display Operation
(SE17-10) - (SS17-10) = NL	Full screen display The area of (SE17-10) - (SS17-10) is normally displayed.
(SE17-10) - (SS17-10) < NL	Partial screen display The area of (SE17-10) - (SS17-10) is normally displayed. The rest of the area shows a white screen irrespective of data in the internal RAM.
(SE17-10) - (SS17-10) > NL	Setting disabled

Note 1) SS17-10 ≤ SE17-0 ≤ "EF"H

Note 2) When SPT = "0", SS27-20 and SE27-20 are disabled.

Table 55 Two Screen Drive (SPT = 1)

Register Settings	Display Operation
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) = NL	Full screen display The area of (SE27-20) - (SS17-10) is normally displayed.
((SE17-10) - (SS17-10)) + ((SE27-20) - (S27-20)) < NL	Partial screen display The area of (SE27-10) - (SS17-10) is normally displayed. The rest of the area shows a white screen irrespective of data in the internal RAM.
((SE17-10) - (SS17-10)) + ((SE27-20) - (SS27-20)) > NL	Setting disabled

Note 1) Make sure that SS17-10 ≤ SE17-10 < SS27-20 ≤ SE27-20 ≤ "EF"H.

Note 2) Make sure that ((SE27-20) - (SS17-10)) ≤ NL.

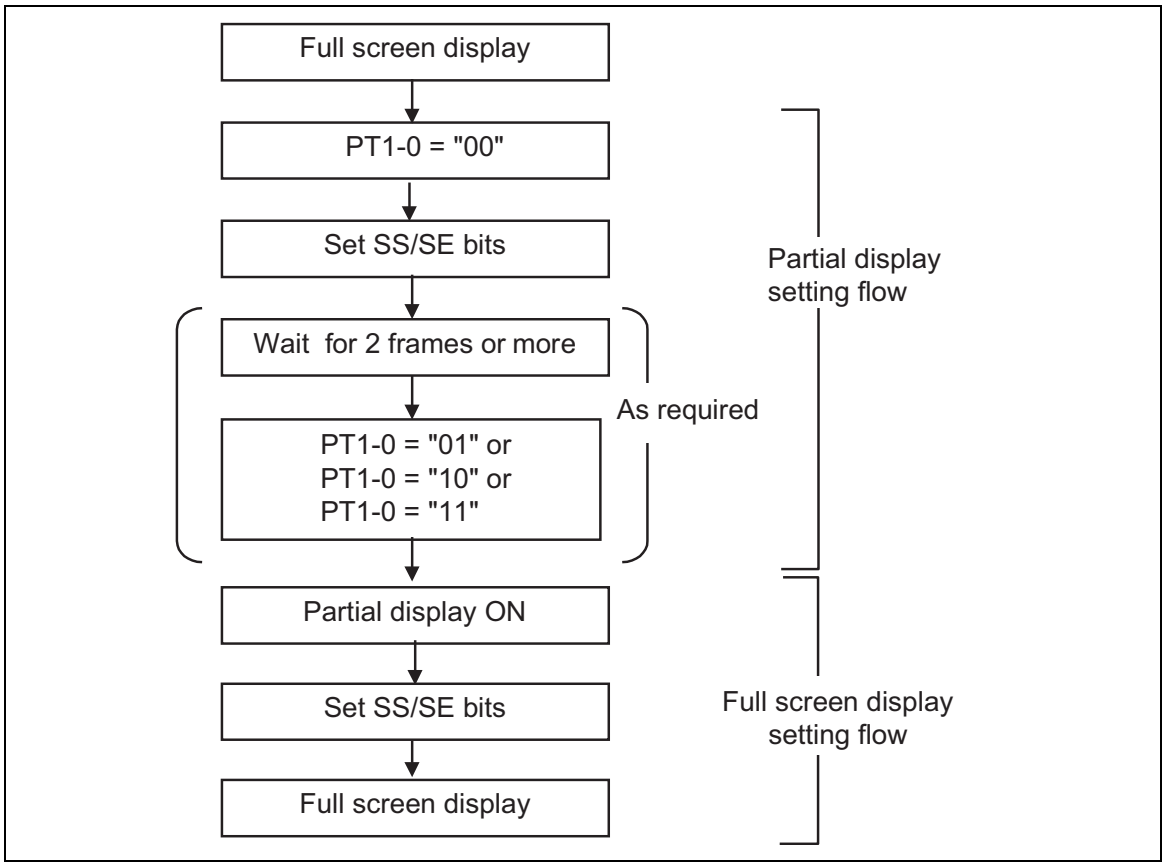
The outputs from the source driver in the non-display area of partial display are changeable according to the characteristics of the display panel with PT1-0 bits.

Table 56 Source outputs in non-display areas

		Source Output in the Non-display Area	
PT1	PT0	Positive Polarity	Negative Polarity
0	0	V31	V0
0	1	Setting disabled	
1	0	GND	GND
1	1	High-Z	High-Z

Partial display setting sequence

Follow the sequences below when setting the partial display.



Absolute Maximum Ratings

Table 57

Item	Symbol	Unit	Value	Notes
Power supply voltage (1)	Vcc, RVcc, IOVcc	V	-0.3 ~ + 4.6	1, 2
Power supply voltage (2)	Vci - AGND	V	-0.3 ~ + 4.6	1, 3
Power supply voltage (3)	DDVDH - AGND	V	-0.3 ~ + 6.0	1, 4
Power supply voltage (4)	AGND -VCL	V	-0.3 ~ + 4.6	1,
Power supply voltage (5)	DDVDH - VCL	V	-0.3 ~ + 9.0	1, 5
Power supply voltage (6)	VGH - AGND	V	-0.3 ~ + 18.5	1, 6
Power supply voltage (7)	AGND - VGL	V	-0.3 ~ + 18.5	1, 7
Input voltage	Vt	V	-0.3 ~ Vcc + 0.3	1
Operating temperature	Topr	°C	-40 ~ + 85	1, 8
Storage temperature	Tstg	°C	-55 ~ + 110	1

Note 1) If used beyond the absolute maximum ratings, the LSI may be destroyed. It is strongly recommended to use the LSI within the limits of its electrical characteristics during the normal operation. The reliability of LSI is not guaranteed if used in the conditions above the limits, and it may lead to malfunction.

Note 2) Make sure (High) (RVcc=Vcc) ≥ GND (Low), (High) IOVcc ≥ GND (Low).

Note 3) Make sure (High) Vci ≥ GND (Low).

Note 4) Make sure (High) DDVDH ≥ AGND (Low).

Note 5) Make sure (High) DDVDH ≥ VCL (Low).

Note 6) Make sure (High) VGH ≥ AGND (Low).

Note 7) Make sure (High) AGND ≥ VGL (Low).

Note 8) The DC/AC characteristics of die and wafer products is guaranteed at 85 ºC.

Electrical Characteristics

DC Characteristics

Table 58 (V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V, Ta = –40 ~ +85°C*) * see Note 1

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
Input high voltage	V_{IH}	V	IOV_{CC} = 1.65 to 3.3 V	0.8 IOV_{CC}	—	IOV_{CC}	2, 3
Input low voltage	V_{IL}	V	IOV_{CC} = 1.65 to 3.3 V	–0.3	—	0.2 IOV_{CC}	2, 3
Output high voltage (DB0-17 pins, FLM)	V_{OH1}	V	IOV_{CC} = 1.65 to 3.3 V I_{OH} = -0.1mA	0.8 IOVcc	—	—	2
Output low voltage (DB0-17 pins, FLM)	V_{OL1}	V	IOV_{CC} = 1.65 to 3.3 V I_{OL} =0.1mA	—	—	0.2 IOVcc	2
I/O leakage current	I_{Li}	µA	Vin = 0 to IOVcc	- 1	—	1	4
Current consumption: normal operation (IOVcc-GND)+(Vcc-GND)+(Rvcc-GND)	I_{OP1}	µA	RC oscillation: fosc = 315kHz (240 lines) IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	155	260	5, 6
Current consumption: 8-color (26-line partial) display (IOVcc-GND)+(Vcc-GND)+(Rvcc-GND)	I_{OP2}	µA	RC oscillation: fosc = 315kHz (26-line partial) IOVcc=Vcc=RVcc=3.0V, Ta=25°C, RAM data: “0000”h	—	100	—	6
Current consumption: RAM access mode (1) Normal write mode HWM=0 (IOVcc-GND)+(Vcc-GND)+(Rvcc-GND)	I_{RAM1}	mA	IOVcc=2.4V, Vcc=RVcc=2.4V, tCYCW=250ns, Ta=25°C, 80/8-bit I/F, TRI=0, Consecutive RAM access during display operation	—	11.0	—	6
Current consumption: RAM access mode (2) High-speed write mode HWM=1 (IOVcc-GND)+(Vcc-GND)+(Rvcc-GND)	I_{RAM2}	mA	IOVcc=2.4V, Vcc=RVcc=2.4V, tCYCW=250ns, Ta=25°C, 80/8-bit I/F, TRI=0, Consecutive RAM access during display operation	—	3.3	—	6
Current consumption: Standby mode (IOVcc-GND)+(Vcc-GND)+(Rvcc-GND)	I_{ST}	µA	IOVcc=Vcc=RVcc=Vci= 3V, Ta ≤ 50°C	—	0.4	10	5
			IOVcc=Vcc=RVcc=Vci= 3V, Ta > 50°C	—	—	30	
LCD power supply current: 266,144 color display (Vci-GND)	I_{ci}	mA	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =315kHz (240 lines), fFLM=70Hz, Ta=25°C, RAM data:”0000”h, REV=0, SAP=100, AP=100, DC0=000, DC1=010, VRN14-00=0, VRP14-00=0, PKP52-00=0, PKN52-00=0, PRP12-00=0, PRN12-00=0, B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=10000, VCOMG=1, CL=0 No panel load	—	1.4	1.68	5, 6

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
LCD power supply current: 8 color display (Vci-GND)	I_{ci}	mA	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =315kHz, fFLM=40Hz, Ta=25°C, RAM data:"0000"h, REV=0, SAP=010, AP=010, DC0=001, DC1=011, VRN14-00=0, VRP14-00=0, PKP52-00=0, PKN52-00=0, PRP12-00=0, PRN12-00=0, B/C=0, BT=001, VC=001, VRH=0011, VCM=10011, VDV=01110, VCOMG=1, CL=1, PTG=10, ISC=0111 No panel load	—	0.15	—	5, 6
Output voltage difference	ΔVo	mV	—	—	5	—	7
Average output voltage fluctuation	ΔV	mV	—	—	—	35	8

Step-up circuit Characteristics

Table 59

Item		Unit	Test Condition	Min	Typ	Max	Notes
Step-up output voltage	VLOUT1	V	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =400kHz Ta=25°C,VC=001, AP=100, SAP=100, BT=000, DC0=001, C11=C12=C21=C22=1uF/Characteristics B, VLOUT1=VLOUT2=VLOUT3 =VLOUT4=1uF/Characteristics B, No panel load, I_{load} = -1mA	5.0	5.3	—	10
	VLOUT2	V	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =400kHz Ta=25°C,VC=001, AP=100, SAP=100, BT=000, DC0=000, DC1=010 C11=C12=C21=C22=1uF/Characteristics B, VLOUT1=VLOUT2=VLOUT3 =VLOUT4=1uF/Characteristics B, No panel load, I_{load} = -100uA	15.7	16.2	—	10
	VLOUT3	V	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =400kHz Ta=25°C,VC=001, AP=100, SAP=100, BT=000, DC0=000, DC1=010 C11=C12=C21=C22=1uF/Characteristics B, VLOUT1=VLOUT2=VLOUT3 =VLOUT4=1uF/Characteristics B, No panel load, I_{load} = +100uA	-12.9	-13.5	—	10
	VLOUT4	V	IOVcc=Vcc=RVcc= 3V, Vci=3V RC oscillation: fosc =400kHz Ta=25°C,VC=001, AP=100, SAP=100, BT=000, DC0=000, DC1=010 C11=C12=C21=C22=1uF/Characteristics B, VLOUT1=VLOUT2=VLOUT3 =VLOUT4=1uF/Characteristics B, No panel load, I_{load} = +200uA	-2.1	-2.6	—	10
Input voltage	Vci	V		2.5	—	3.3	

AC Characteristics

(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V, Ta = –40 ~ +85°C*) * see Note 1

Table 60 Clock Characteristics (V_{CC} = 2.4 to 3.3 V)

Item	Symbol	Unit	Test Condition	Min	Typ	Max	Notes
R-C oscillation clock	f_{OSC}	kHz	Rf = 150kΩ, V_{CC} = 3 V	244	305	366	9

80-system Bus Interface Timing Characteristics (18/16-bit I/F)

Table 61 Normal Write Mode (HWM=0) (V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	150	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	70	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 1	0	—	—
	Read (RS to CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 1	2	—	—
Write data setup time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{HWR}	ns	Figure 1	5	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

Table 62 High-Speed Write Mode (HWM=1) (V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	100	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 1	0	—	—
	Read (RS to CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 1	2	—	—
Write data setup time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{HWR}	ns	Figure 1	5	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

80-system Bus Interface Timing Characteristics (9/8-bit I/F)

Table 63 Normal/High-speed Write Mode (HWM=0/1)
(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 2.0 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	100	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	40	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 1	0	—	—
	Read (RS to CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 1	2	—	—
Write data setup time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{HWR}	ns	Figure 1	5	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

Table 64 Normal/High-speed Write Mode (HWM=0/1)
(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 2.0 ~ 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Bus cycle time	Write	t_{CYCW}	ns	Figure 1	75	—	—
	Read	t_{CYCR}	ns	Figure 1	500	—	—
Write low-level pulse width		PW_{LW}	ns	Figure 1	30	—	—
Read low-level pulse width		PW_{LR}	ns	Figure 1	250	—	—
Write high-level pulse width		PW_{HW}	ns	Figure 1	30	—	—
Read high-level pulse width		PW_{HR}	ns	Figure 1	200	—	—
Write/Read rise/fall time		$t_{WRr, WRf}$	ns	Figure 1	—	—	25
Setup time	Write (RS to CS*, WR*)	t_{AS}	ns	Figure 1	0	—	—
	Read (RS to CS*, RD*)				10		
Address hold time		t_{AH}	ns	Figure 1	2	—	—
Write data setup time		t_{DSW}	ns	Figure 1	25	—	—
Write data hold time		t_{HWR}	ns	Figure 1	5	—	—
Read data delay time		t_{DDR}	ns	Figure 1	—	—	200
Read data hold time		t_{DHR}	ns	Figure 1	5	—	—

Serial Peripheral Interface timing characteristics

Table 65 Normal/High-speed Write Mode (HWM=0/1)
(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item		Symbol	Unit	Timing diagram	Min	Typ	Max
Serial clock cycle time	Write (received)	t_{SCYC}	us	Figure 2	100	—	20,000
	Read (transmitted)	t_{SCYC}	us	Figure 2	350	—	20,000
Serial clock high-level pulse width	Write (received)	t_{SCH}	ns	Figure 2	40	—	—
	Read (transmitted)	t_{SCH}	ns	Figure 2	150	—	—
Serial clock low-level pulse width	Write (received)	t_{SCL}	ns	Figure 2	40	—	—
	Read (transmitted)	t_{SCL}	ns	Figure 2	150	—	—
Serial clock rise/fall time		t_{scr}, t_{scf}	ns	Figure 2	—	—	20
Chip select setup time		t_{CSU}	ns	Figure 2	20	—	—
Chip select hold time		t_{CH}	ns	Figure 2	60	—	—
Serial input data setup time		t_{SISU}	ns	Figure 2	30	—	—
Serial input data hold time		t_{SIH}	ns	Figure 2	30	—	—
Serial output data delay time		t_{SOD}	ns	Figure 2	—	—	130
Serial output data hold time		t_{SOH}	ns	Figure 2	5	—	—

Reset Timing Characteristics

Table 66 (V_{CC} = RVcc = 1.8 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
Reset low-level width	t_{RES}	ms	Figure 3	1	—	—
Reset rise time	t_{rRES}	µs	Figure 3	—	—	10

LCD driver output Characteristics

Table 67

Item	Symbol	Unit	Test condition	Min	Typ	Max	Note
Driver output delay time	t_{dd}	µs	Vcc=3V, DDVDH=5.5V, VREG1OUT=5.0V, RC oscillation: fosc =315kHz (240 lines), Ta=25°C REV=0, SAP=010, AP=010, VRN14-00=0, VRP14-00=0, PKP52-00=0, PKN52-00=0, PRP12-00=0, PRN12-00=0, Load resistance R=10kΩ, Load capacitance C=20pF • when the level changes from a same grayscale level on all pins • Time to reach +/-35mV when Vcom polarity inverts	—	35	—	11

RGB Interface timing characteristics

Table 68 18/16-bit I/F, High-speed Write Mode (HWM=1)
(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 4	0	—	1
ENABLE setup time	tENS	ns	Figure 4	10	—	—
ENABLE hold time	tENH	ns	Figure 4	20	—	—
DOTCLK “Low” level pulse width	PW_{DL}	ns	Figure 4	40	—	—
DOTCLK “High” level pulse width	PW_{DH}	ns	Figure 4	40	—	—
DOTCLK cycle time	tCYCD	ns	Figure 4	100	—	—
Data setup time	tPDS	ns	Figure 4	10	—	—
Data hold time	tPDH	ns	Figure 4	40	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 4	—	—	25

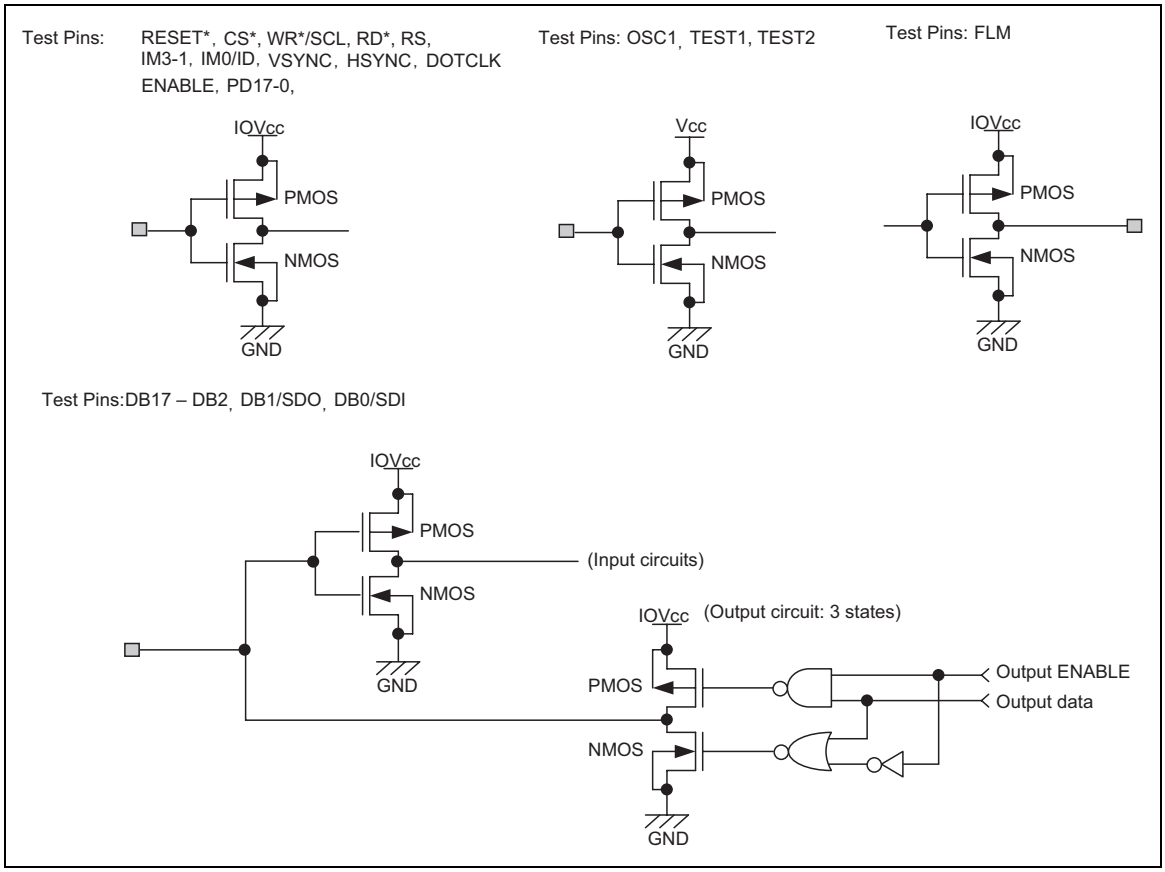
Table 69 6-bit I/F, High-speed Write Mode (HWM=1)
(V_{CC} = RVcc = 2.4 ~ 3.3 V, IOVcc = 1.65 ~ 3.3 V)

Item	Symbol	Unit	Timing diagram	Min	Typ	Max
VSYNC/HSYNC setup time	tSYNCS	clocks	Figure 4	0	—	1
ENABLE setup time	tENS	ns	Figure 4	10	—	—
ENABLE hold time	tENH	ns	Figure 4	20	—	—
DOTCLK “Low” level pulse width	PW_{DL}	ns	Figure 4	30	—	—
DOTCLK “High” level pulse width	PW_{DH}	ns	Figure 4	30	—	—
DOTCLK cycle time	tCYCD	ns	Figure 4	80	—	—
Data setup time	tPDS	ns	Figure 4	10	—	—
Data hold time	tPDH	ns	Figure 4	30	—	—
DOTCLK, VYSNC, HSYNC rise/fall time	Trgbr, trgbf	ns	Figure 4	—	—	25

Notes to Electrical Characteristics

1. The DC/AC electrical characteristics of bare die and wafer products are guaranteed at 85°C.

2. The following figures illustrate the configurations of I pin, I/O pin, and O pin.

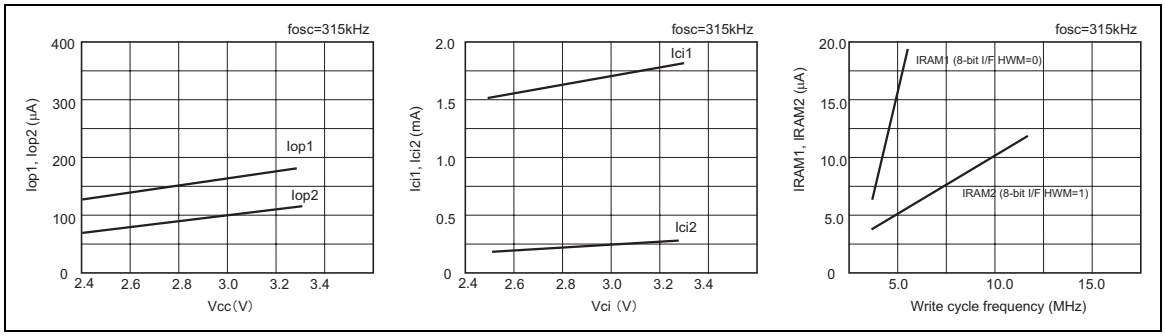


3. TEST1, TEST2, TESTV1, DCTEST pins must be grounded, IM3/2/1, IM0/ID pins must be fixed to either the GND level or the IOVcc level.

4. This excludes the current through the output drive MOS.

5. This excludes the current flowing through the input/output units. Make sure that the input level is fixed because transient current in the input circuit will increase when the CMOS input level is in a middle range. The current consumption is unaffected by whether the CS*pin is “High” or “Low” while no access through the interface pins is executed.

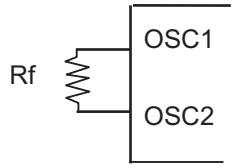
6. The relationship between voltages and the current consumption is as follows.



7. The output voltage difference is the difference in the voltages of neighboring source outputs for the same display data. This value is shown just for a referential purpose.

8. The average output voltage variation is the difference in the average source output voltages among chips. The average source output voltage is measured for each chip with the same display data.

9. This applies to internal oscillators when an external oscillation resistor Rf is used.



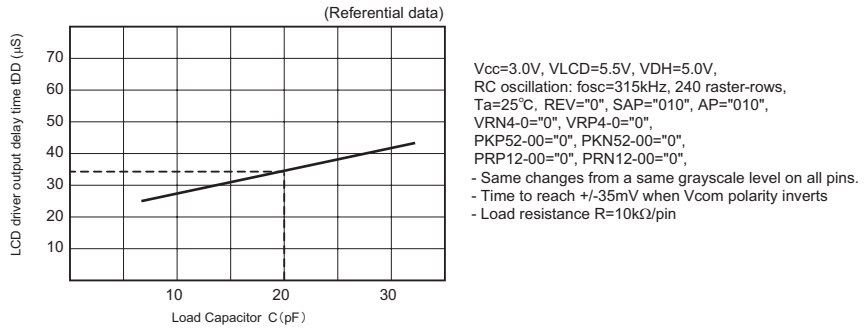
The oscillation frequency may change according to the capacitors of OSC1 and OSC2 pins. Connect the OSC1 and OSC2 pins with the possible shortest wiring.

Table 70 Referential data

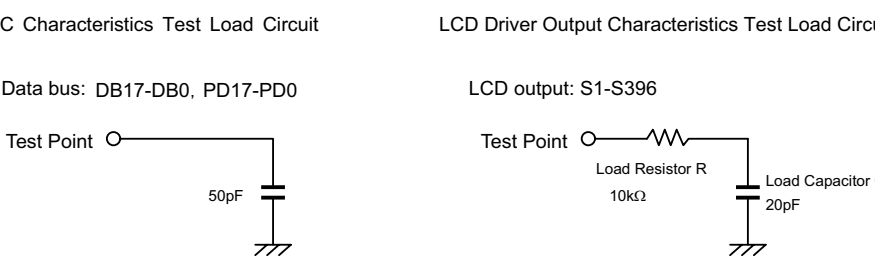
Oscillation Resistance (kΩ)	RC oscillation frequency: fosc (kHz)		
	Vcc = 2.4 V	Vcc = 3.0V	Vcc = 3.3V
110kΩ	372	401	411
150kΩ	284	305	311
180kΩ	243	258	263
200 kΩ	222	235	240
240 kΩ	188	198	202
270 kΩ	169	177	181
300 kΩ	153	161	163
390 kΩ	121	126	128
430 kΩ	110	115	116

10. The wiring resistance when used for a COG module is not included. No load is applied to the pins except the one to be measured. See “Load current characteristics (reference data)” for details.

11. The delay time of LCD driver outputs depends on the load of the LCD panel. Adjust the frame frequency and a cycle per line by checking the quality of display on the actual panel in use.

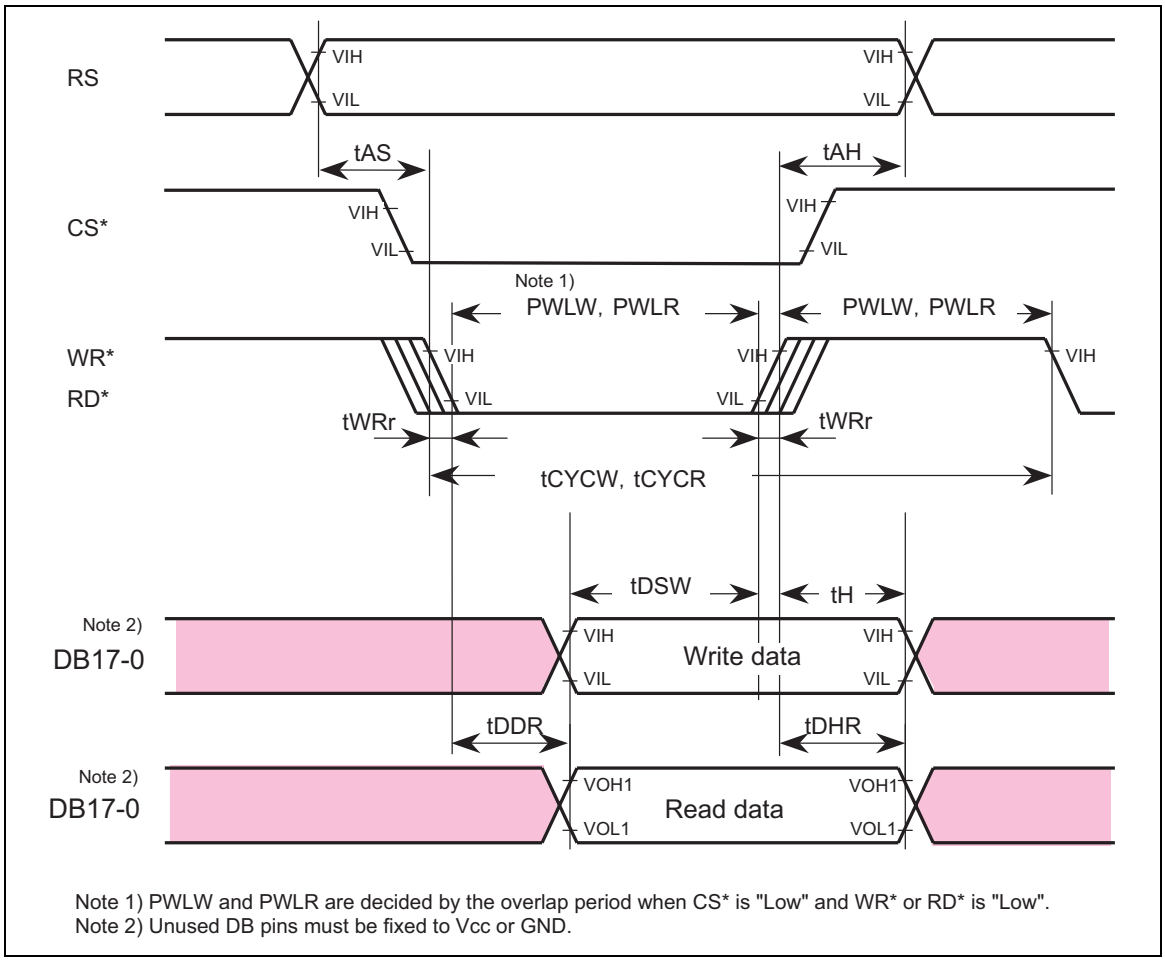


Example of test circuits



Timing characteristics diagram

80-system bus interface operation



Note 1) PWLW and PWLR are decided by the overlap period when CS* is "Low" and WR* or RD* is "Low".
Note 2) Unused DB pins must be fixed to Vcc or GND.

Figure 1

Serial Peripheral Interface Operation

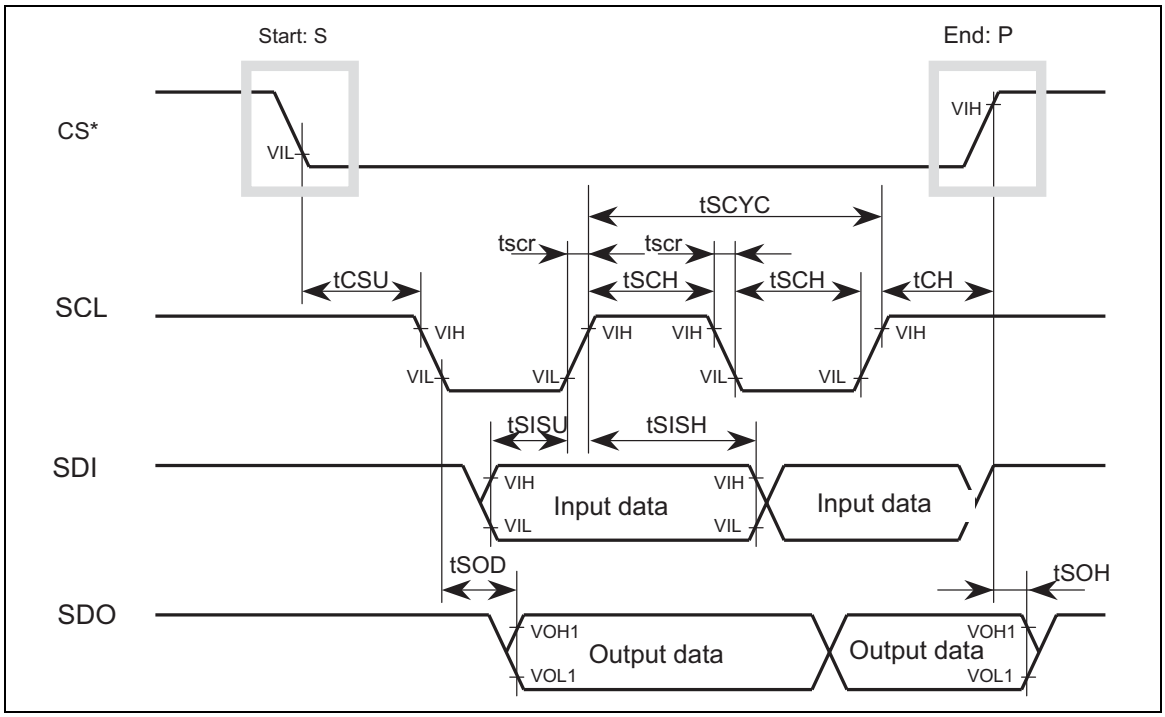


Figure 2

Reset operation

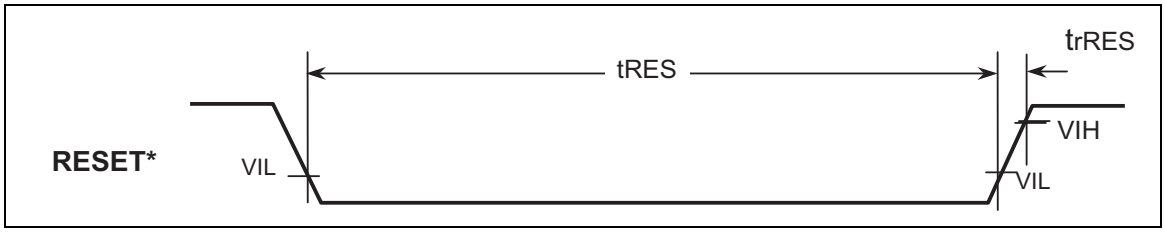


Figure 3

RGB interface

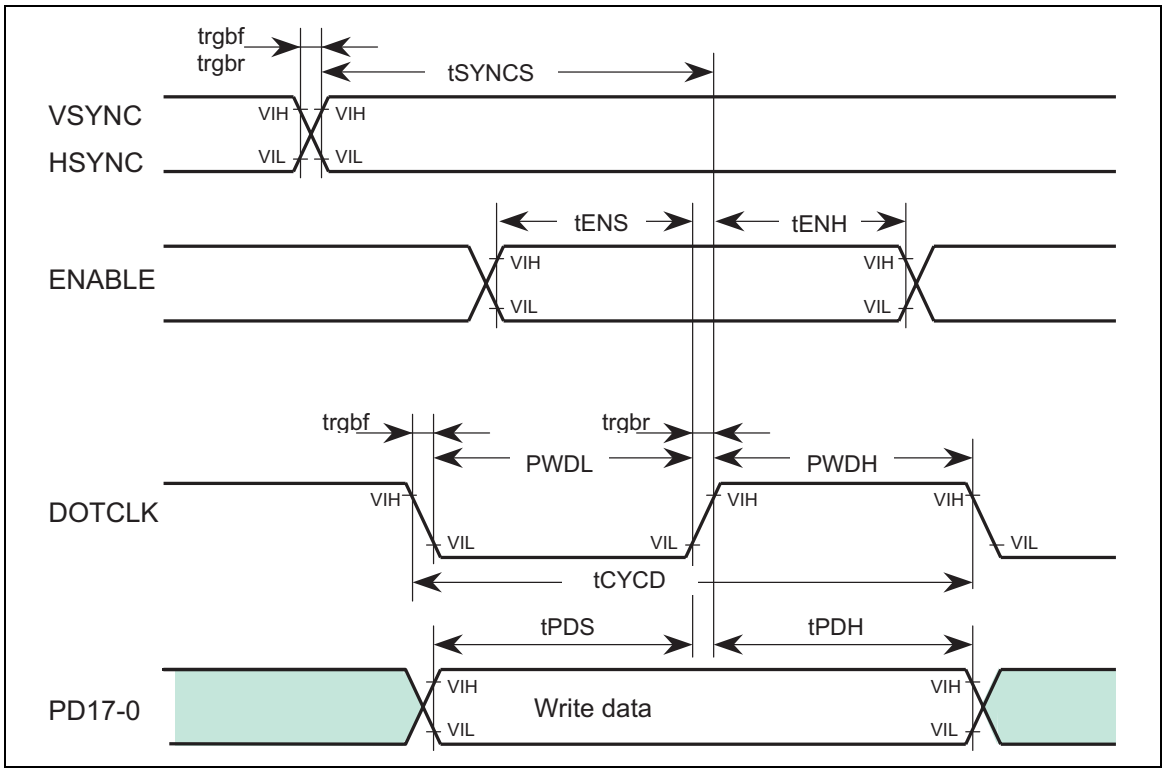


Figure 4

LCD driver outputs

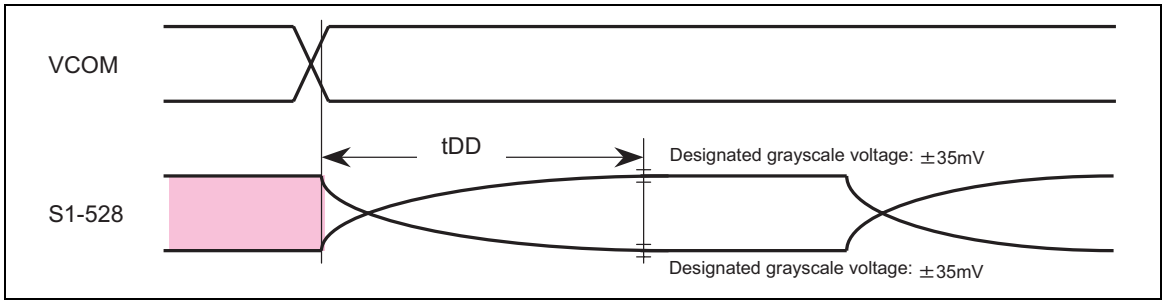
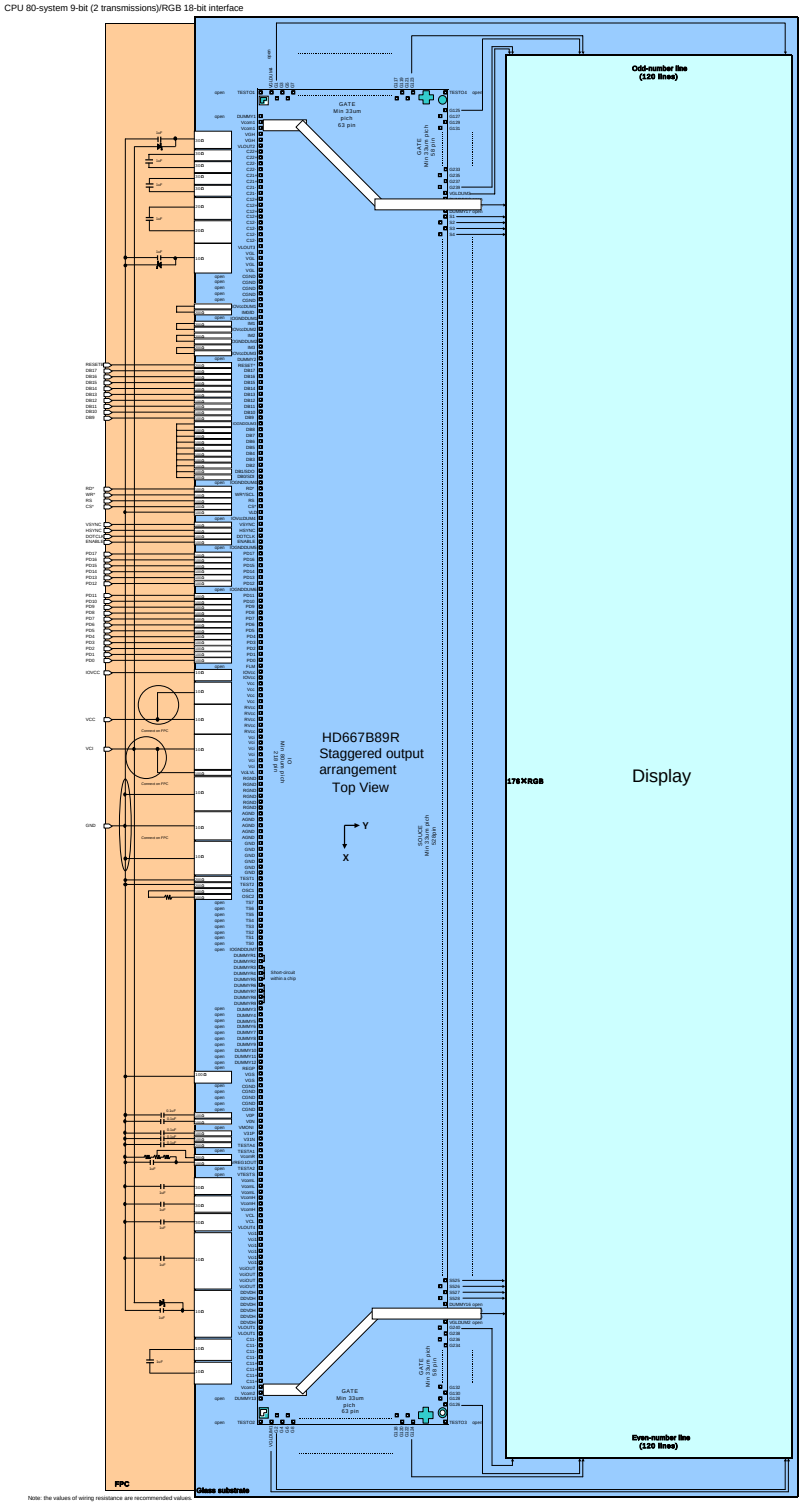


Figure 5

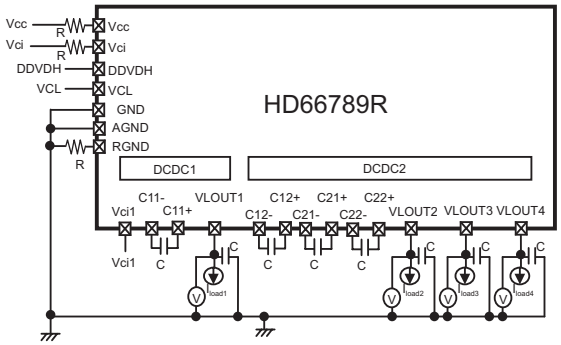
Example of connecting the HD66789R to a Panel



Load current characteristics (Referential data)

1. VLOUT1

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied Voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V

	External Capacitor
C	1[μF]/B Char.

	Clock cycle
fosc	400[kHz]

	Resistance
R	10[Ω]

(3) Test description

Measure the dependency of load current (I_{load1}) using the step-up clock cycle of VLOUT1 as a parameter (No load applied to pins that are not tested).

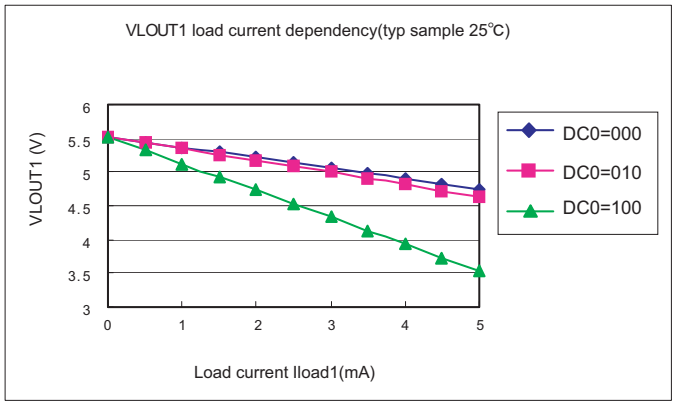
(4) Test Result

(a) VLOUT1 Load Current Characteristics 1
(Parameter: step-up cycle)

Notes:
Register setting
VC="001"
AP="100"
BT="000"
DC0="000" (1/8)
DC0="010" (1/32)
DC0="100" (1/128)

DC1="000" (1/16)

CL="0"
D="00"
GON="0"
DTE="0"

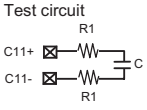


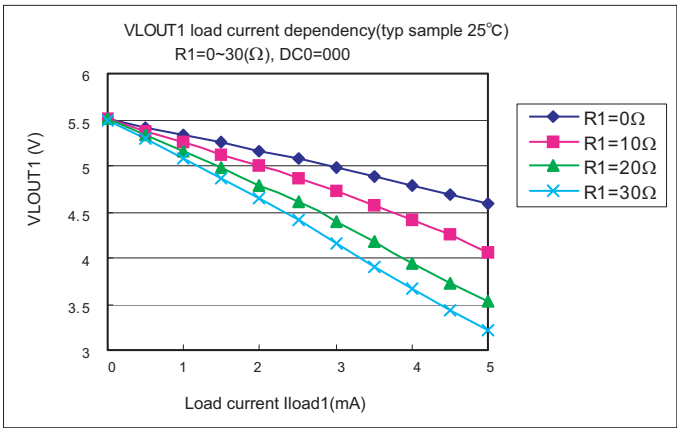
(b) VLOUT1 Load Current Characteristics 2
(Parameter: Resistance with step-up capacitor)

Notes:
Register setting
VC="001"
AP="100"
BT="000"
DC0="000" (1/8)
DC1="000" (1/16)

CL="0"
D="00"
GON="0"
DTE="0"

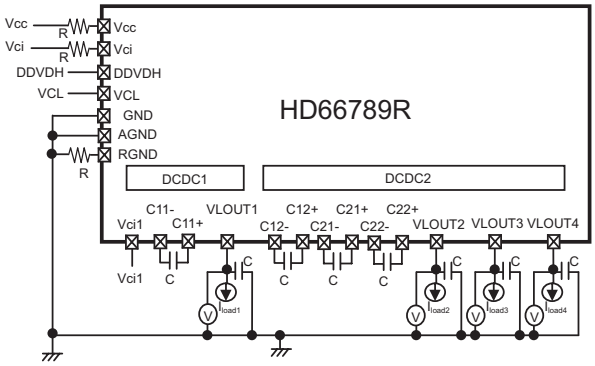
Test circuit





2. VLOUT2

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied Voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V

	External Capacitor
C	1[μ F]/B Char.

	Clock cycle
fosc	400[kHz]

	Resistance
R	10[Ω]

(3) Test description

(a) Measure the dependency of load current (I_{load2}) using the step-up clock cycle of VLOUT2 as a parameter (No load applied to pins that are not tested).

(b) Measure the dependency of load current (I_{load2}) using the step-up scale of VLOUT2 as a parameter (No load applied to pins that are not tested).

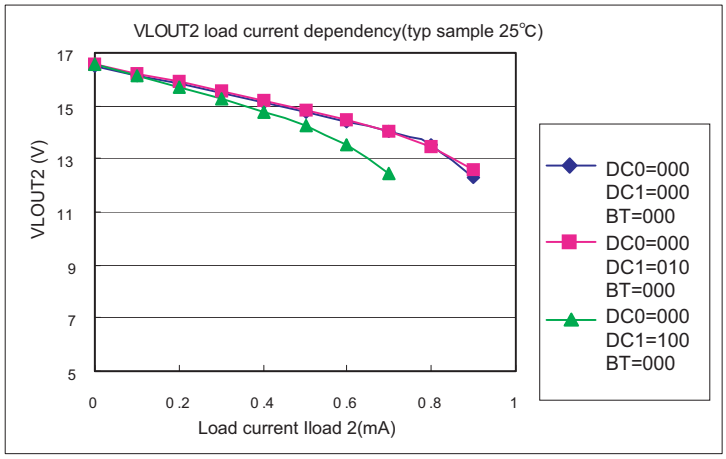
(4) Test Result

(a) VLOUT2 Load Current Characteristics 1 (Parameter: step-up cycle)

Notes:
Register setting
VC="001"
AP="100"
BT="000"
DC0="000" (1/8)

DC1="000" (1/16)
DC0="010" (1/64)
DC0="100" (1/256)

CL="0"
D="00"
GON="0"
DTE="0"

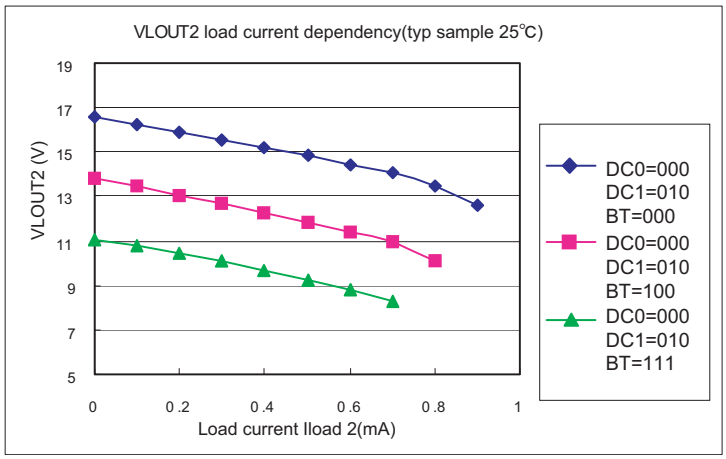


(b) VLOUT2 Load Current Characteristics 2 (Parameter: Resistance with step-up capacitor)

Notes:
Register setting
VC="001"
AP="100"
DC0="000"
DC1="010"

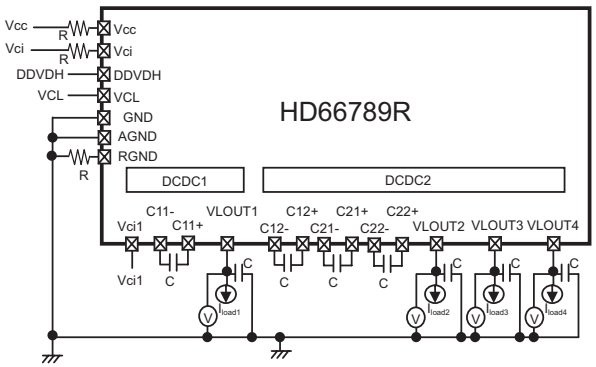
BT="000" (x6, x -5)
BT="100" (x5, x -4)
BT="111" (x4, x -3)

CL="0"
D="00"
GON="0"
DTE="0"



3. VLOUT3

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied Voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V

	External Capacitor
C	1[μF]/B Char.

	Clock cycle
fosc	400[kHz]

	Resistance
R	10[Ω]

(3) Test description

(a) Measure the dependency of load current (I_{load3}) using the step-up clock cycle of VLOUT3 as a parameter (No load applied to pins that are not tested).

(b) Measure the dependency of load current (I_{load3}) using the step-up scale of VLOUT3 as a parameter (No load applied to pins that are not tested).

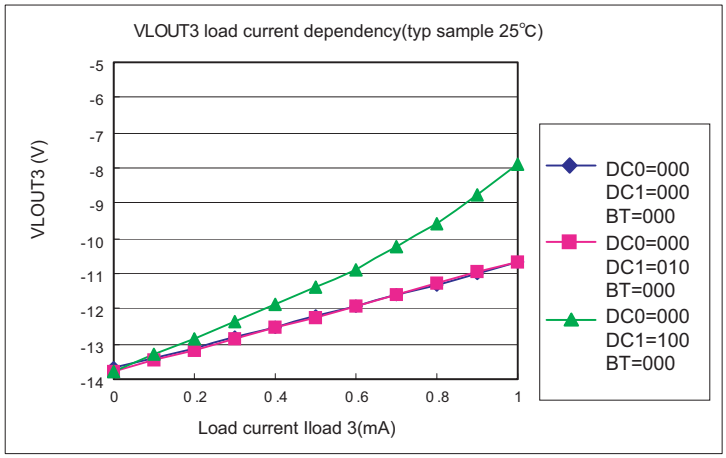
(4) Test Result

(a) VLOUT3 Load Current Characteristics 1 (Parameter: step-up cycle)

Notes:
Register setting
VC="001"
AP="100"
BT="000"
DC0="000" (1/8)

DC1="000" (1/16)
DC0="010" (1/64)
DC0="100" (1/256)

CL="0"
D="00"
GON="0"
DTE="0"

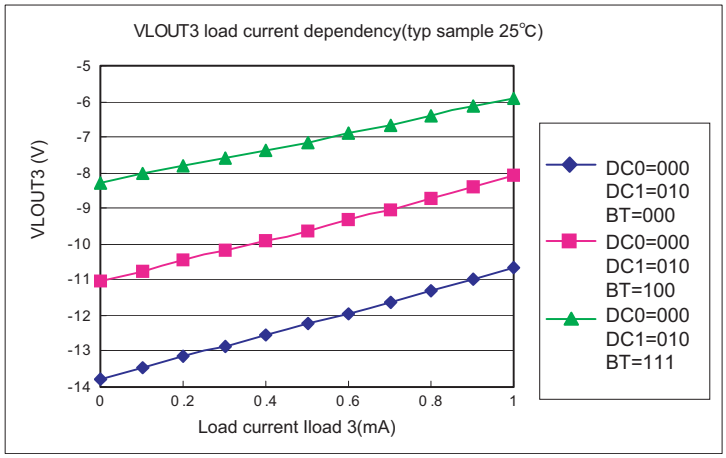


(b) VLOUT3 Load Current Characteristics 2 (Parameter: Resistance with step-up capacitor)

Notes:
Register setting
VC="001"
AP="100"
DC0="000"
DC1="010"

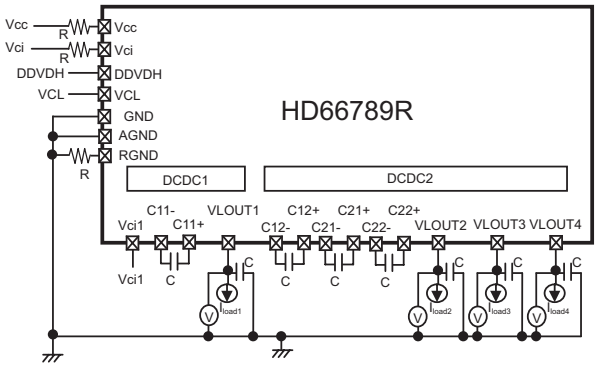
BT="000" (x6, x -5)
BT="100" (x5, x -4)
BT="111" (x4, x -3)

CL="0"
D="00"
GON="0"
DTE="0"



4. VLOUT4

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied Voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V

	External Capacitor
C	1[μF]/B Char.

	Clock cycle
fosc	400[kHz]

	Resistance
R	10[Ω]

(3) Test description

Measure the dependency of load current (I_{load4}) using the step-up clock cycle of VLOUT4 as a parameter (No load applied to pins that are not tested).

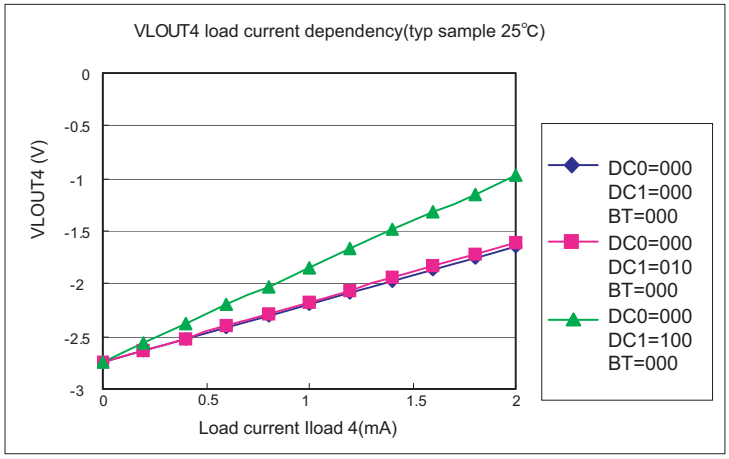
(4) Test Result

(a) VLOUT4 Load Current Characteristics
(Parameter: step-up cycle)

Notes:
Register setting
VC="001"
AP="100"
BT="000"
DC0="000" (1/8)

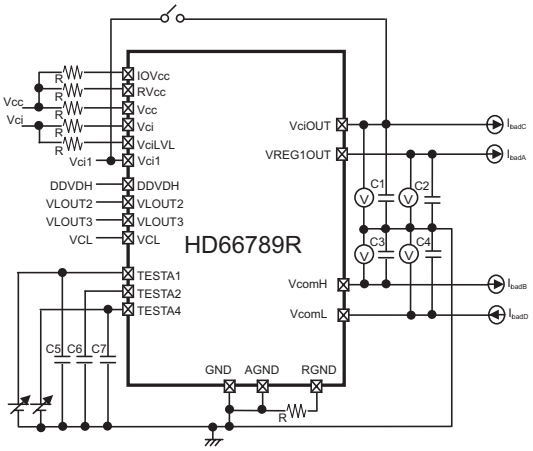
DC1="000" (1/16)
DC0="010" (1/64)
DC0="100" (1/256)

CL="0"
D="00"
GON="0"
DTE="0"



5. VciOUT Amplifier

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied voltage
Vcc	3.00V
Vci	3.00V
Vci1	See Note 2)
DDVDH	Vci1 x -2
VLOUT2	Vci1 x 6
VLOUT3	Vci1 x -5
VCL	Vci1 x -1

	Resistance
R	10[Ω]

	Stabilizing Capacitor
C1	1[μF]/B Char.
C2	1[μF]/B Char.
C3	1[μF]/B Char.
C4	1[μF]/B Char.
C5	0.1[μF]/B Char.
C6	0.1[μF]/B Char.
C7	0.1[μF]/B Char.

(3) Test description

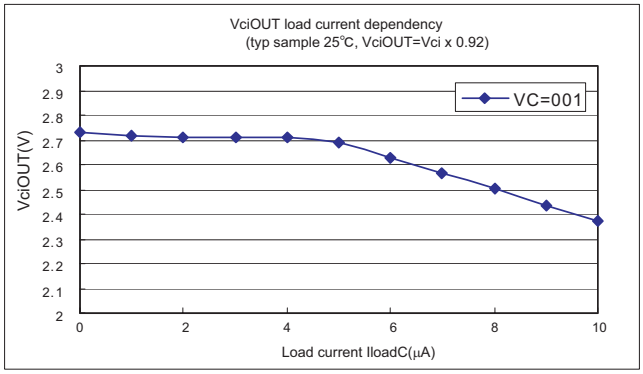
Measure the dependency of VciOUT load current (I_{loadC}) with the register setting VC[2-0] (No load applied to pins that are not tested).

Note 1) The TEST(n) pins are exclusively used for the test purpose. Do not use them as output open.
Note 2) Input the calculated value of VciOUT, which is set with the register VC[2-0].

(4) Test Result

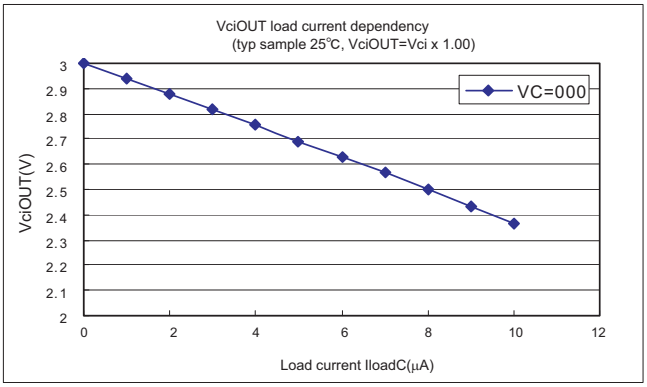
(a) VciOUT Load Current Characteristics 1
VciOUT=REGP x 0.92

Notes:
Register setting
VC="001" (x 0.92)
AP="100"



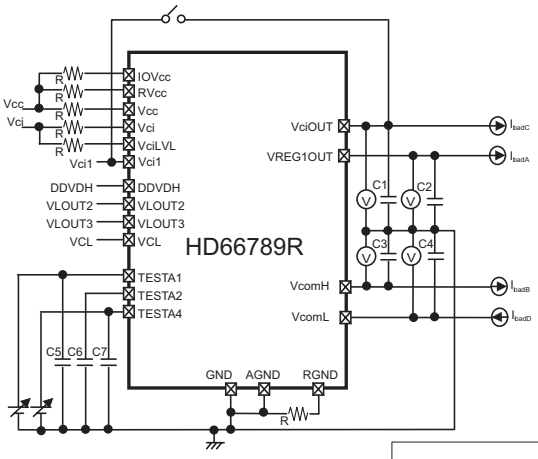
(b) VciOUT Load Current Characteristics 2
VciOUT=REGP x 1.00

Notes:
Register setting
VC="000" (x 1.00)
AP="100"



6. VREG1OUT Amplifier

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V
VLOUT2	+16.50V
VLOUT3	-13.76V
VCL	-2.76V

	Resistance
R	10[Ω]

	Stabilizing Capacitor
C1	1[μF]/B Char.
C2	1[μF]/B Char.
C3	1[μF]/B Char.
C4	1[μF]/B Char.
C5	0.1[μF]/B Char.
C6	0.1[μF]/B Char.
C7	0.1[μF]/B Char.

(3) Test description

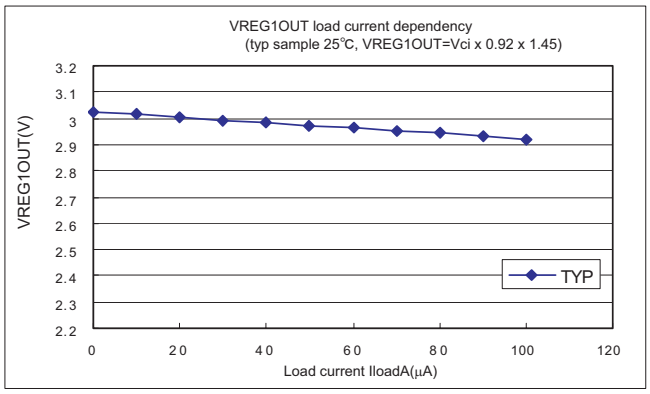
Measure the dependency of VREG1OUT load current (I_{loadA}) with the register setting VRH[3-0] (No load applied to pins that are not tested).

Notes: The TEST(n) pins are exclusively used for the test purpose. Do not use them as output open.

(4) Test Result

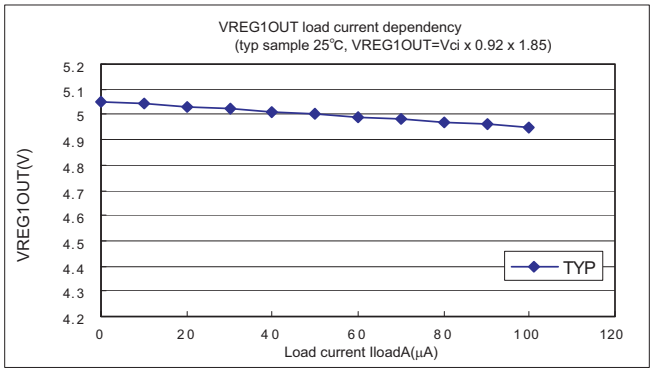
(a) VREG1OUT Load Current Characteristics 1
VREG1OUT=REGP x 1.45

Notes:
Register setting
VC="001"
AP="100"
VRH="0001" (x1.45)



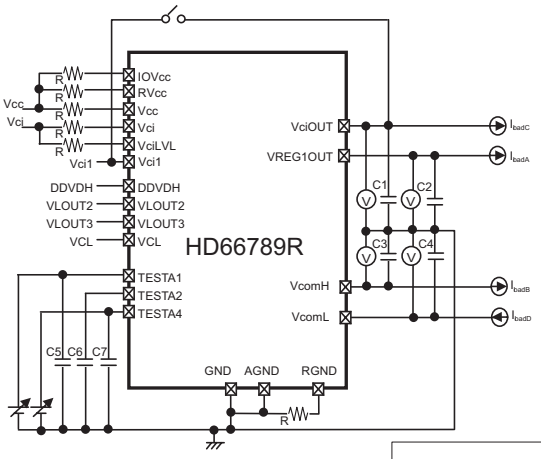
(b) VREG1OUT Load Current Characteristics 2
VREG1OUT=REGP x 1.85

Notes:
Register setting
VC="001"
AP="100"
VRH="0110" (x1.85)



7. VcomH Amplifier

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V
VLOUT2	+16.50V
VLOUT3	-13.76V
VCL	-2.76V

	Resistance
R	10[Ω]

	Stabilizing Capacitor
C1	1[μF]/B Char.
C2	1[μF]/B Char.
C3	1[μF]/B Char.
C4	1[μF]/B Char.
C5	0.1[μF]/B Char.
C6	0.1[μF]/B Char.
C7	0.1[μF]/B Char.

(3) Test description

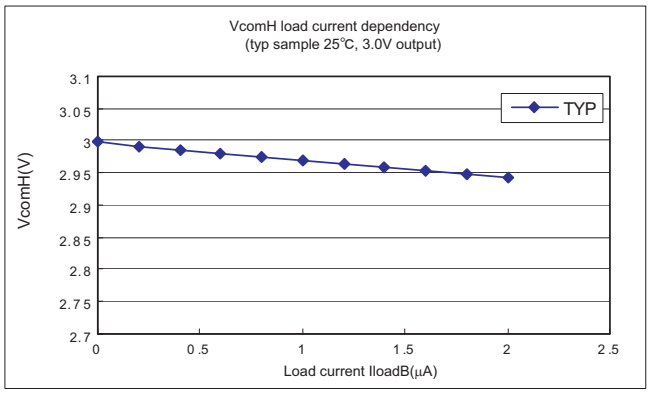
Measure the dependency of VcomH load current (I_{loadB}) with level input to TESTA1 (No load applied to pins that are not tested).

Notes: The TEST(n) pins are exclusively used for the test purpose. Do not use them as output open.

(4) Test Result

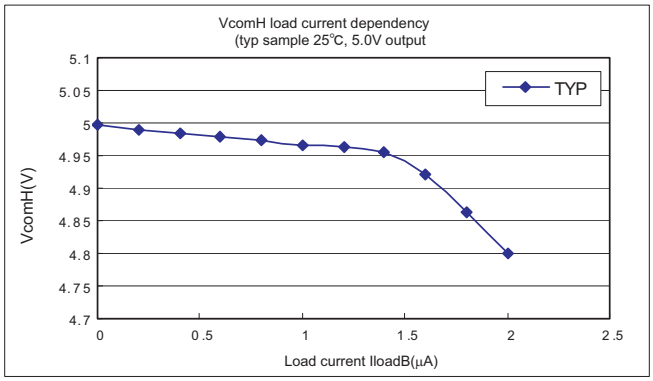
(a) VcomH Load Current Characteristics 1
3.0V output

Notes:
Register setting
VC="001"
AP="100"



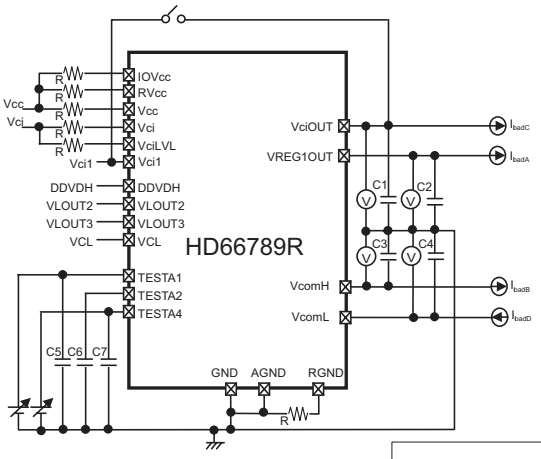
(b) VcomH Load Current Characteristics 2
5.0V output

Notes:
Register setting
VC="001"
AP="100"



8. VcomL Amplifier

(1)Test Circuit



(2) Test Conditions

25℃, TYP Sample

	Applied voltage
Vcc	3.00V
Vci	3.00V
Vci1	2.76V
DDVDH	5.52V
VLOUT2	+16.50V
VLOUT3	-13.76V
VCL	-2.76V

	Resistance
R	10[Ω]

	Stabilizing Capacitor
C1	1[μF]/B Char.
C2	1[μF]/B Char.
C3	1[μF]/B Char.
C4	1[μF]/B Char.
C5	0.1[μF]/B Char.
C6	0.1[μF]/B Char.
C7	0.1[μF]/B Char.

(3) Test description

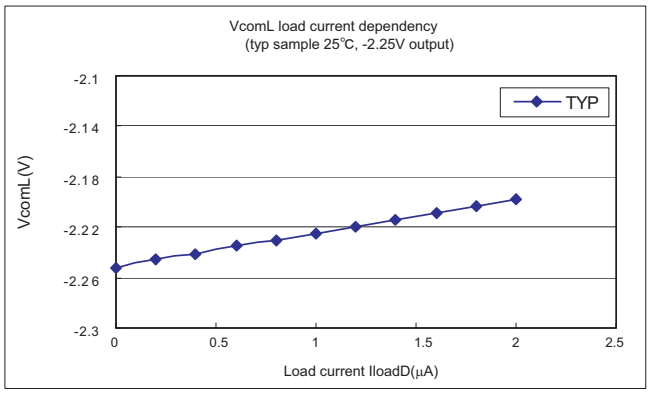
Measure the dependency of VcomL load current (I_{loadD}) with level input to TESTA4 (No load applied to pins that are not tested).

Notes: The TEST(n) pins are exclusively used for the test purpose. Do not use them as output open.

(4) Test Result

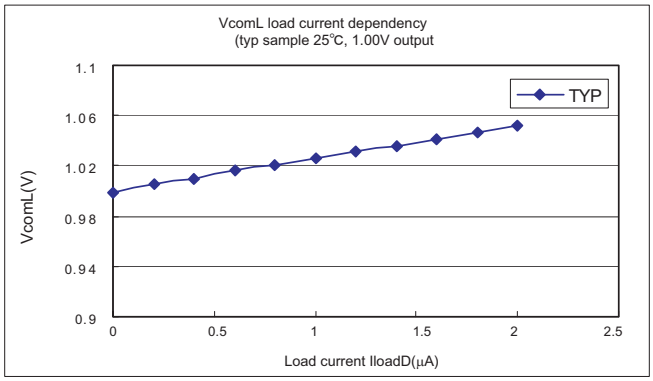
(a) VcomL Load Current Characteristics 1
-2.25V output

Notes:
Register setting
VC="001"
AP="100"



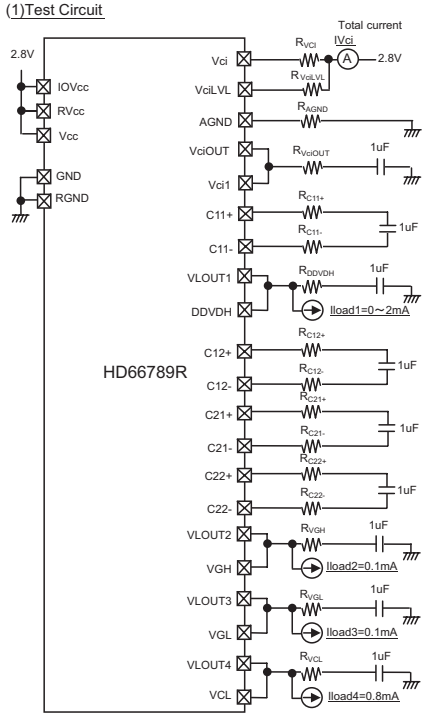
(b) VcomL Load Current Characteristics 2
1.00V output

Notes:
Register setting
VC="001"
AP="100"



9. Step-up load current characteristics with added wiring resistances

(1)Test Circuit



(2) Test Conditions

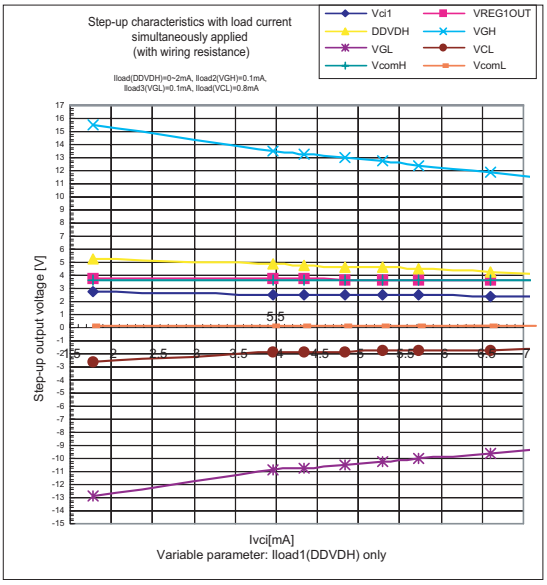
Test Circuit	See left
Instruction setting	AP="011", BT="000", DC0="000", DC1="000", VC="000", CL="0", VCM="11110", DVD="01100", VCOMG="1", PON="1", GON="1", DTE="1", D="11"
Vci	2.8V
Vcc=IOVcc=RVcc	2.8V

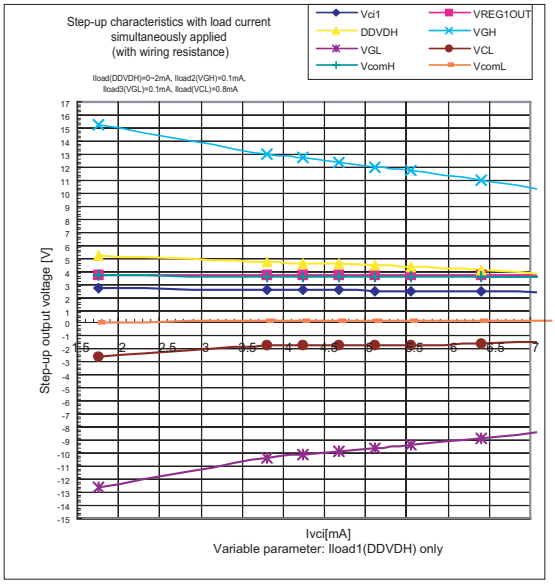
Load current	
Iload1(DDVDH)	0 ~ 2mA
Iload2(VGH)	0.1mA
Iload3(VGL)	0.1mA
Iload4(VCL)	0.8mA

Wiring resistance	
R_{Vci}	10ohm
R_{AGND}	10ohm
R_{VciOUT}	10ohm
R_{C11+}	10ohm
R_{C11-}	10ohm
R_{DDVDH}	10ohm
R_{C12+}	20ohm
R_{C12-}	30ohm
R_{C21+}	30ohm
R_{C21-}	30ohm
R_{C22+}	30ohm
R_{C22-}	30ohm
R_{VGH}	30ohm
R_{VGL}	10ohm
R_{VCL}	30ohm

(3) Test Description

Add a wiring resistance element to each pin of step-up circuit. Load current is applied on each step-up power supply (DDVDH, VGH, VGL, VCL). Measure total current (IVci) and each step-up voltage characteristic with a variable parameter of Iload1 (DDVDH). No load on S1~S528, G1~G240.





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Colophon 0.0

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
1.00	2003.12.09	First issue (Error corrections and changes from the HD66789 ver1.00) p.14, p.15, p.16:PAD arrangement, PAD coordinate p.43 Description of EQ1-0 bits p.58 GRAM data and LCD output level (change "-" to "+") p.65 Description of SCN4-0 bits		
1.01	2003.12.24	p.14 Delete "T.B.D." from the chip size (No change in the size) p.151 Add Note 10 to "Notes to the electrical characteristics".		