HD66850F

Color LCD Interface Engine (CLINE)

HITACHI

Description

The HD66850F CLINE interface controller converts multi-color video signals for CRT display into color or monochrome LCD data.

This device enables an LCD system to replace a CRT display system without any changes to the original display system. It automatically adapts to display modes of the IBM-VGA (Video Graphics Array™) system, facilitating the configuration of an LCD system.

The CLINE can control TN-type (Twisted Nematic) color and monochrome LCDs and can display a maximum of 4096 color levels or 16 gray levels.

Note: Video Graphics Array is a trademark of International Business Machines Corporation, U.S.A.

Features

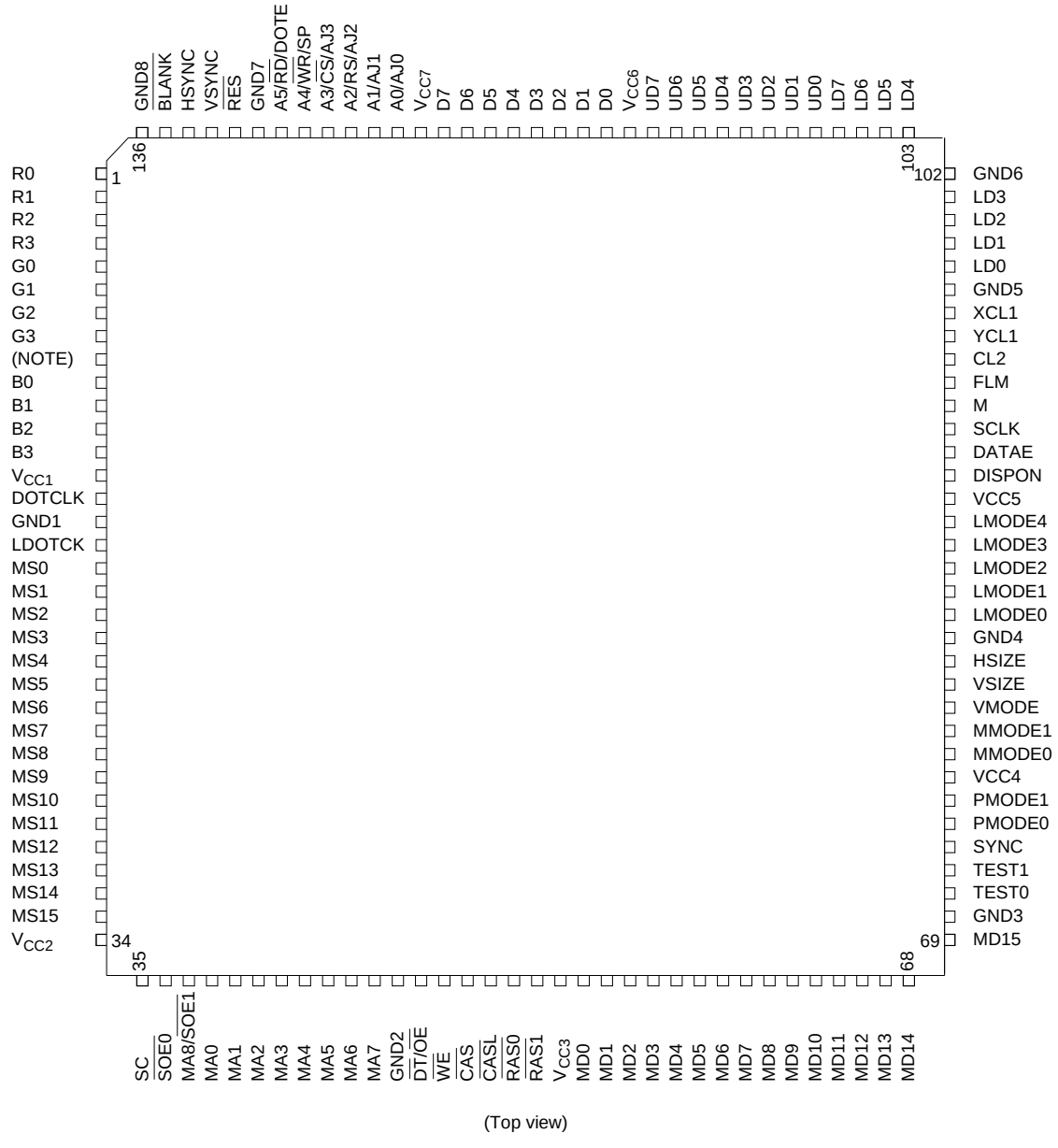
- Various LCD panel sizes supported
  - — 640 or 720 dots wide
  - — 32 to 512 lines high
- Programmable display size
  - — 32 to 720 dots wide
  - — 32 to 512 lines high
- Easy-to-see display
  - — Centering
  - — Stretching (display stretched to fill out the panel)
- Improved gradation display quality using the pulse width modulation method
- Desired gradation levels assignable to each display color through the use of internal gradation level palettes
- Changeable LCD frame frequency
  - — Through the use of a multi-port RAM frame buffer
  - — Within the range of 1/2 to 2 times of CRT display dot clock frequency
- High-speed operating frequency: 32 MHz (CRT display dot clock)
- Recommended LCD drivers: HD66110ST (column) and HD66115T (common)
- Single power supply: +5 V

Ordering Information

Type No.	Package
HD66850F	136-pin plastic QFP (FP-136)

Hitachi semiconductor

Pin Arrangement



(Top view)

Note: Pin No. 9 is not used; must be fixed low.

Pin Description

Type	Symbol	Pin No.	Pin Name	I/O	Function
Power supply	$V_{CC}1$ – $V_{CC}7$	14, 34, 53, 76, 88, 115, 124	V_{CC1} – V_{CC7}	—	All of these pins must beAll connected to a +5V supply
	GND1 – GND8	16, 46, 70, 82, 97, 102, 131, 136	GND1 – GND7	—	All of these pins must be grounded.
MPU/ROM or program interface	D0 – D7*1	(M) 116 – 123	Data 0 – 7	I/O	Transfer data between internal registers and MPU
	D0 – D7*1	(R) 116 – 123	Data 0 – 7	I	Input data to internal registers from external ROM
	DOTE	(P) 130	Dot clock edge change	I	Switches RGB data latch timing High: Data latched at the rising edge of DOTCLK pulses Low: Data latched at the falling edge of DOTCLK pulses
	$\overline{RD}$	(M) 130	Read	I	Inputs a read signal for reading data from internal registers
	A5	(R) 130	Address 5	O	Outputs external ROM address 5
	SP	(P) 129	Spread display select I	I	Selects either of the following display size modes High: Double – width display Low: Normal display
	$\overline{WR}$	(M) 129	Write	I	Inputs a write signal for writing data to internal registers
	A4	(R) 129	Address 4	O	Outputs external ROM address 4
	AJ3	(P) 128	Adjust 3	I	Adjusts the display timing signal (table 1)
	$\overline{CS}$	(M) 128	Chip select	I	Inputs a chip select signal to select the CLINE High: The CLINE not selected Low: The CLINE selected
	A3	(R) 128	Address 3	O	Outputs external ROM address 3
	AJ2	(P) 127	Adjust 2	I	Adjusts the display timing signal (table 1)
	RS	(M) 127	Register select	I	Inputs a register select signal to select either CLINE data registers or index register High: Data registers Low: The index register
	A2	(R) 127	Address 2	O	Outputs external ROM address 2
	AJ0, AJ1*2	(P) 125, 126	Adjust 0, 1	I	Adjust the display timing signal (table 1)
	A0, A1*2	(R) 125, 126	Address 0, 1	O	Output external ROM addresses 0 and 1, respectively

(M): For MPU programming method (R): For ROM programming method (P): For pin programming method
I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
CRT interface	R0 – R3*3	1 – 4	Red serial data 0 – 3	I	Input CRT display R data
	G0 – G3*3	5 – 8	Green serial data 0 – 3	I	Input CRT display G data or monochrome data
	B0 – B3*3	10 – 13	Blue serial data 0 – 3	I	Input CRT display B data: For monochrome display, B1 selects 16-gray-scale display and B0 indicates the type of CRT display data input. B1 = high: Prohibited B1 = low: 16-level gray scale display B0 = high: 64-color data input B0 = low: 16-level gray scale data input
	DOTCLK	15	Dot clock	I	Inputs the dot clock pulses for CRT display
	HSYNC	134	Horizontal synchronization	I	Inputs the CRT horizontal synchronization signal
	VSYNC	133	Vertical synchronization	I	Inputs the CRT vertical synchronization signal
	$\overline{\text{BLANK}}$	135	Blanking	I	Inputs a display timing siganl indicating horizontal or vertical display period, or a blank signal indicating the display period with border area period
LCD interface	UD4 – UD7*4	111 – 114	LCD upper panel data 4 – 7	O	Output LCD upper panel data or R data
	UD0 – UD3*4	107 – 110	LCD upper panel data 0 – 3	O	Output LCD upper panel data or G data
	LD4 – LD7*4	103 – 106	LCD lower panel data 4 – 7	O	Output LCD lower panel data or B data
	LD0 – LD3*4	98 – 101	LCD lower panel data 0 – 3	O	Output LCD lower panel data or I data
	XCL1*4	96	X-driver latch clock	O	Outputs the LCD data latch clock pulses for X-drivers
	YCL1	95	Y-driver shift clock	O	Outputs the LCD data line shift clock pulses for Y-drivers
	CL2	94	X-driver shift clock	O	Outputs the LCD data line shift clock pulses for X-drivers
	FLM	93	First line maker	O	Outputs the first line maker for Y-drivers

I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
LCD interface	M	92	M	O	Outputs a signal for converting LCD drive signals to AC
	SCLK	91	Shift clock	O	Outputs clock pulse with a frequency identical to CL2 but without a retrace period
	DATAE*4	90	Data enable	O	Indicates LCD data display period
	DISPON*4	89	Display on	O	Controls LCD on/off
	LDOTCK	17	LCD dot clock	I	Inputs LCD dot clock pulses
Buffer memory interface	MD0 – MD15*5	54 – 69	Memory data 0 – 15	O	Output data to be written to buffer memory
	MS0 – MS15*6	18 – 33	Memory serial data 0 – 15	I	Input data read from buffer memory
	MA0 – MA7*5	38 – 45	Memory address 0 – 7	O	Output buffer memory addresses 0 – 7
	MA8/ $\overline{\text{SOE1}}$*5	37	Memory address 8/ serial output enable 1	O	Outputs buffer memory address 8 when 1-Mbit RAMs are used or outputs a serial data output enable signal when 256-kbit RAMs are used
	$\overline{\text{SOE0}}$*5	36	Serial output enable 0	O	Output a serial data output enable signal for buffer memory
	$\overline{\text{WE}}$*5	48	Write enable	O	Outputs a write enable signal for buffer memory
	$\overline{\text{DT}}$/$\overline{\text{OE}}$*5	47	Data transfer/output enable	O	Outputs a data transfer signal or an output enable signal for buffer memory
	$\overline{\text{RAS0}}$, $\overline{\text{RAS1}}$*5	51, 52	Row address strobe 0, row address strobe 1	O	Outputs a row address strobe signal for buffer memory
	$\overline{\text{CAS}}$, $\overline{\text{CASL}}$*5	49, 50	Column address strobe	O	Outputs a column address strobe signal for buffer memory
	SC*5	35	Serial clock	O	Outputs serial read clock pulses for buffer memory
Mode control	PMODE0, PMODE1	74, 75	Program mode 0, Program mode 1	I	Select a CLINE programming method (table 2)
	LMODE0 – LMODE4	83 – 87	LCD mode 0 – 4	I	Select a display mode (table 9)
	MMODE0, MMODE1	77, 78	Memory mode 0, 1	I	Select a memory configuration (table 3)
	SYNC	73	Synchronization	I	Select a basic clock for LCD High: DOTCLK Low: LDOTCK

I/O: Input/Output

Type	Symbol	Pin No.	Pin Name	I/O	Function
Mode control (cont)	VMODE	79	VGA mode	I	Specifies a CRT display system High: Non-VGA system Low: VGA system
	VSIZE	80	LCD vertical size	I	Specifies the vertical size of the LCD panel High: 480 lines Low: 400 lines
	HSIZE	81	LCD horizontal size	I	Specifies the horizontal size of the LCD panel High: 720 dots Low: 640 dots
	$\overline{RES}$	132	Reset	I	Inputs an external reset signal
	TEST0, TEST1	71, 72	Test 0, 1	I	Used for tests; Must be grounded

I/O: Input/Output

Notes: 1. Must be fixed low for pin programming method.
2. Must be fixed low for MPU programming method.
3. Must be fixed low when not used.
4. Must be left disconnected when not used.
5. Must be left disconnected when buffer memory is not used.
6. Must be fixed low when buffer memory is not used.

Table 1 Display Timing Signal Fine Adjustment

Pin				Number of Dots Adjusted
AJ3	AJ2	AJ1	AJ0	
0	0	0	0	0
0	0	0	1	–1
0	0	1	0	–2
1	0	0	0	0
1	0	0	1	+1
1	0	1	0	+2
1	0	1	1	+3
1	1	0	0	+4
1	1	0	1	+5
1	1	1	0	+6

Note: – (minus) indicates advancing the phase of the display timing signal,
+ (plus) indicates delaying the phase of the display timing signal.

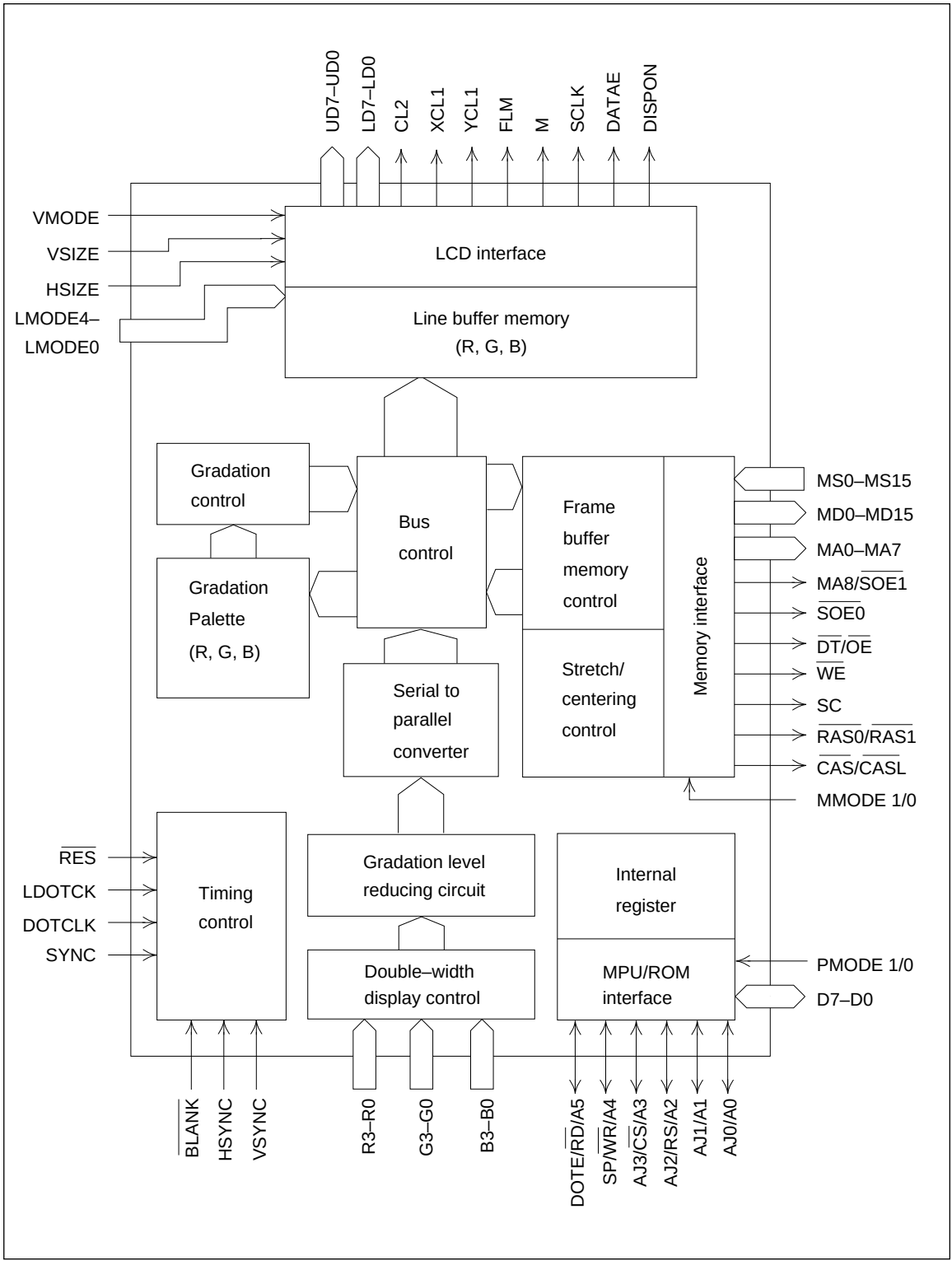
Table 2 Programming Method Selection

Pin		
PMODE1	**PMODE0**	**Programming Method**
0	0	Pin
0	1	Internal registers (MPU)
1	0	Internal registers (ROM)
1	1	Prohibited

Table 3 Memory Configuration Selection

Pin		
MMODE1	**MMODE0**	**Memory Configuration**
0	0	1-Mbit RAM
0	1	256-kbit RAM
1	0	No memory
1	1	No memory (when the CRT controller supports dual screen display)

Block Diagram



CLINE registers are summarized in table 4.

Table 4 Register List

		Index Reg				Reg.		Program	Read/	Data Bits							
$\overline{CS}$	RS	3	2	1	0	No.	Register Name	Units	Write	7	6	5	4	3	2	1	0
1	—	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
0	0	0	0	0	0	IR	Index	—	W	—	—	—	—	IA3	IA2	IA1	IA0
0	1	0	0	0	0	R0	Control	—	R/W	—	—	—	STE	CRE	CCE	SP	DISP ON
0	1	0	0	0	1	R1	Input timing control	Dot	R/W	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0
0	1	0	0	1	0	R2	Horizontal display size	Character	R/W	—	DH6	DH5	DH4	DH3	DH2	DH1	DH0
0	1	0	0	1	1	R3	Vertical display size (high-order)	Line	R/W	—	—	—	—	—	—	—	DV8
0	1	0	1	0	0	R4	Vertical display size (low-order)	Line	R/W	DV7	DV6	DV5	DV4	DV3	DV2	DV1	DV0
0	1	0	1	0	1	R5	Centering raster	Line (Raster)	R/W	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
0	1	0	1	1	0	R6	Centering character	Character	R/W	—	—	—	CC4	CC3	CC2	CC1	CC0
0	1	0	1	1	1	R7	Border color control	—	R/W	—	—	—	BM	BCI	BCR	BCG	BCB
0	1	1	0	0	0	R8	Stretching control	Line	R/W	—	—	—	—	SF3	SF2	SF1	SF0
0	1	1	0	0	1	R9	Stretching index (high-order)	Line	R/W	SI15	SI14	SI13	SI12	SI11	SI10	SI9	SI8
0	1	1	0	1	0	R10	Stretching index (low-order)	Line	R/W	SI7	SI6	SI5	SI4	SI3	SI2	SI1	SI0
0	1	1	0	1	1	R11	Gradation level palette address	—	W	—	—	PS1	PS0	PA3	PA2	PA1	PA0
0	1	1	1	0	0	R12	Gradation level palette data	—	R/W	—	—	PD5	PD4	PD3	PD2	PD1	PD0
0	1	1	1	0	1	R13	Gradation display clock period (high-order)	Dot	R/W	—	—	—	—	—	—	—	GC8
0	1	1	1	1	0	R14	Gradation display clock period (low-order)	Dot	R/W	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0
0	1	1	1	1	1	R15	Reserved	—	—	—	—	—	—	—	—	—	—

Notes: 1. Bits marked with * cannot either read from or written to.
2. Bits marked with – are invalid and must be initialized to 0s; they cannot be read.

System Description

Figure 1 shows an example of a VGA-compatible display system implemented with the CLINE. In this system, a color palette HD153119 (Hitachi), which is capable of digital output, is used with a VGA-compatible CRT controller. The CLINE receives digital color data and display sychronization signals from the color pallette and the CRT controller, respectively, and displays 4096-color images on a color LCD, or 16-level grayscale images on a monochrome LCD. With minor modification of the existing CRT display system, simultaneous LCD and CRT display is possible.

Addition of an external frame buffer memory (dual-port RAM) allows the LCD frame frequency to be increased above that of a CRT. This enables easy-to-see gradation display and the control of LCDs having a dual screen configuration.

CLINE operation may be controlled by internal registers through the 80-family MPU bus or an external ROM (as shown in the figure), or simply by pins.

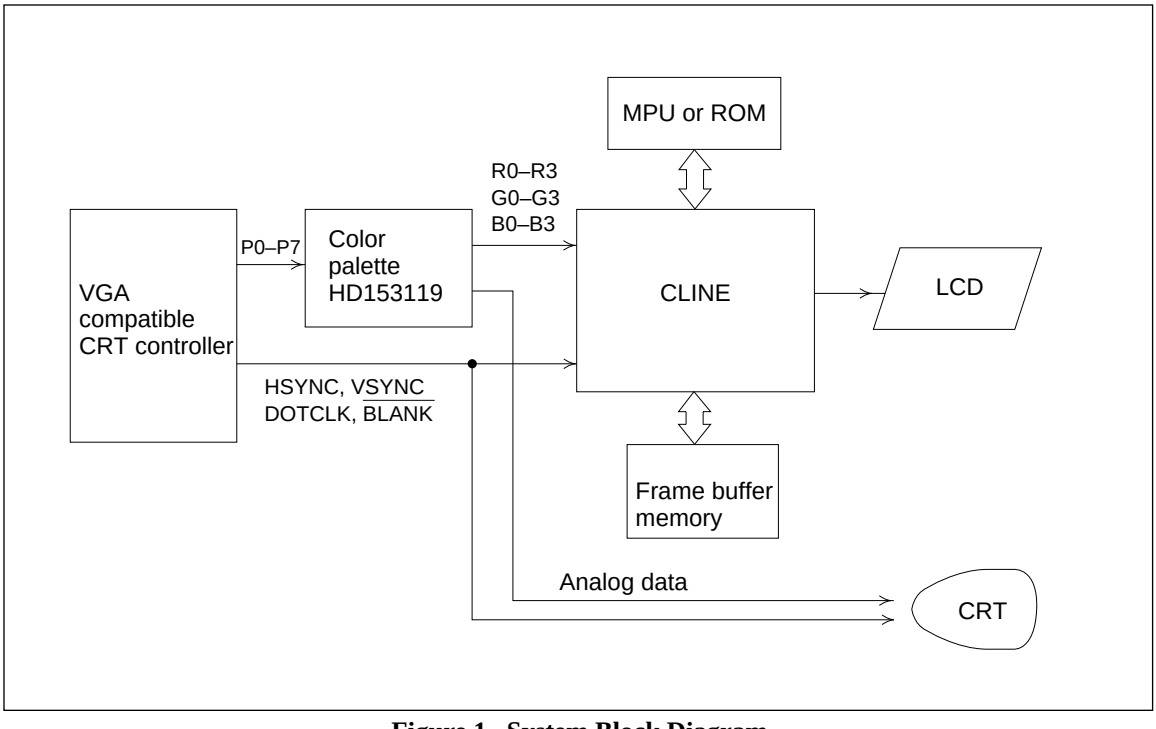


Figure 1 System Block Diagram

Functional Description

Programming Methods

To control CLINE functions, set the appropriate pins and/or internal registers according to the functions used. Controlling methods include pin and internal register programming methods. Internal register programming includes the MPU and ROM programming methods. Any of the three methods can be selected by the combined setting of pins PMODE0 and PMODE1 (table 2).

The pin programming method uses pins to control CLINE functions, and the internal register programming method uses data written to the internal registers to control the functions.

Figure 2 (a) shows a connection example of the CLINE and MPU buses for the MPU programming method. The CLINE bus, which is compatible with the 80-family microprocessor bus, can be directly connected to the host MPU bus.

Figure 2 (b) shows a connection example of the CLINE and ROM for the ROM programming method. In this case, data is automatically loaded into internal registers from the external ROM attached for this purpose. Note that with the ROM programming method, the reset signal must be applied before rewriting the internal registers or gradation level palettes.

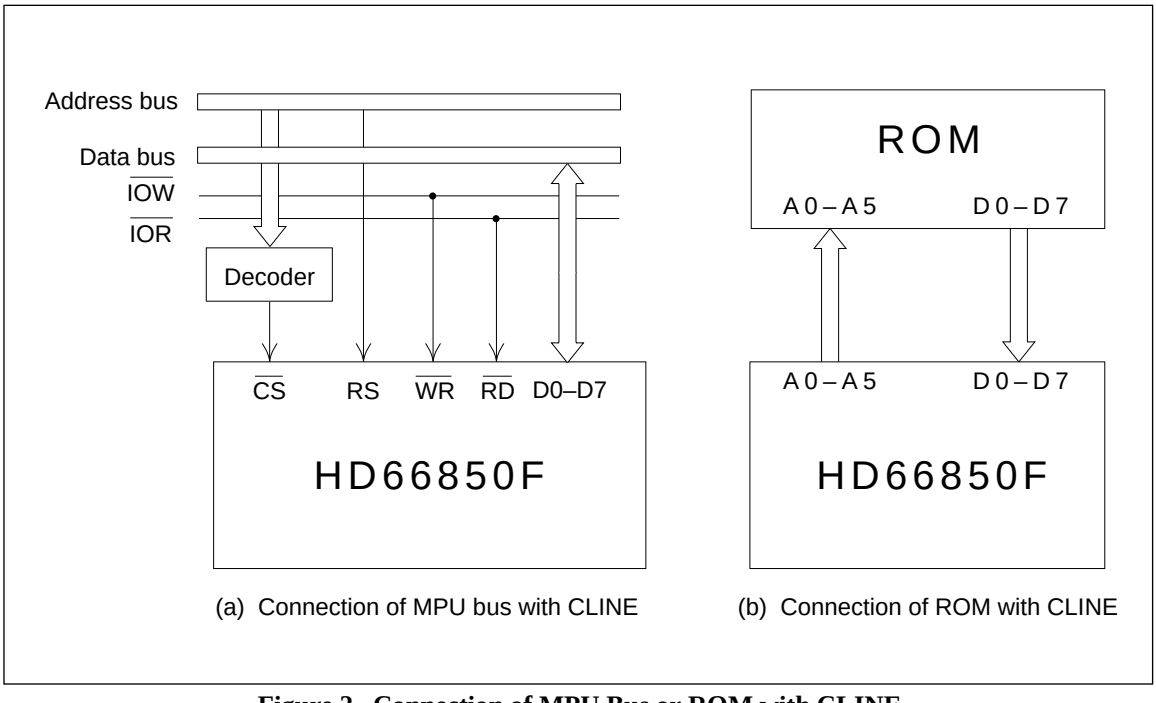


Figure 2 Connection of MPU Bus or ROM with CLINE

Automatic Adaptation to VGA Display Modes

VGA CRT display system display size varies depending on the display mode. (VGA display sizes are: 320, 360, 640, or 720 dots wide and 350, 400, or 480 lines high.) The CLINE identifies the current display mode from VSYNC and HSYNC signal polarities and the display period length, and changes the display size automatically (tables 5 and 6). This function is enabled by setting the VMODE pin low. The CLINE, based on this function, automatically sets the necessary registers (R0, R2, R3, R4, R5, R6, R8, R9, and/or R10) corresponding to the parameters of the display size, double-width display, gradation display clock, and stretching/centering display functions. (In MPU or ROM programming method, selection of vertical centering (bit 3 of R0) or stretching (bit 4 of R0) is not automatic.) Consequently, in VGA display modes, rewriting these registers is disabled.

Note that display stretching and centering are unavailable when buffer memory is not used in the system, even in VGA display modes. In these cases, a display of different vertical size would be placed in the upper section of the LCD panel, resulting in a blank area in the lower section. Centering the display in a system without memory requires external circuits or BIOS tuning.

When displaying an image 720 dots wide (9 dots × 80 characters) on an LCD panel 640 dots wide, the CLINE removes the ninth horizontal dot of each character to prevent losing the far-right portion of the image.

Table 5 Automatic Vertical Display Size Settings for VGA Display Modes

VSYNC	HSYNC	Display Size	Border Rasters	Displayed Rasters
Negative	Positive	350 lines	1-6	7-356
Positive	Negative	400 lines	1-7	8-407
Negative	Negative	480 lines	1-8	9-488

Table 6 Automatic Horizontal Display Size Settings for VGA Display Modes

BLANK Signal High Level

Pulse Width	Display Size	Border Dots	Displayed Dots
256-335 dots	320 dots (256-color)	1-5	6-325
336-359 dots	320 dots (16-color)	1-8	9-328
360-511 dots	360 dots	1-9	10-369
640-703 dots	640 dots	1-8	9-648
704-767 dots	720 dots	1-9	10-729

LCD Panel Size

LCD panel size is specified by either pins or internal registers.

For VGA modes, vertical panel size of 400 or 480 lines can be selected by the VSIZE pin and horizontal panel size of 640 or 720 lines by the HSIZE pin.

For non-VGA modes, the panel size is also specified by the VSIZE and HSIZE pins in pin programming method. In internal register programming method, vertical display size is specified by the vertical display size register (R3 and R4), within the range of 2 to 512 lines. Here, note that the vertical display size specified by R3 and R4 is the CRT display vertical size. When this size differs from the LCD panel vertical size, centering or stretching function must be used. Refer to the following equations for calculating the number of centering rasters and the stretching ratio. For the definition of the centering rasters, see figure 23, Centering Rasters,

- For centering

  LCD panel vertical size (line) =
  CRT display vertical size (line) + centering rasters (lines) $\times$ 2

- For stretching

  LCD panel vertical size (line) =
  CRT display vertical size (line) $\times$ stretching ratio

Since LCD panel horizontal size is limited to 640 or 720 dots even in internal register programming method, centering function must be used as well so that the total number of horizontal dots including the CRT display area and border areas become 640 or 720. Refer to the following equation to calculate the number of centering characters. For the definition of the border areas and centering characters, see figure 25, Centering Characters.

LCD panel horizontal size (dot) =
{number of horizontal display characters +
(number of centering characters $\times$ 2)} $\times$ 8

Double-Width Display

Some CRT display systems have a low-resolution display mode of 320 horizontal dots in addition to a high-resolution display mode of 640 horizontal dots. In this case, the CRT display system lowers the dot clock frequency to reduce one line of data to 320 dots. If such data is supplied to the LCD system of 640 horizontal dots as-is, the entire display will be placed on the left section of the panel with the right half blank. To accommodate this situation, the CLINE doubles the width of the low-resolution display. This function is enabled by the SP/WR/A4 pin in pin programming method or the SP bit (bit 1) of the control register (R0) in internal register programming method (table 7). In either method, for VGA display systems, the CLINE detects low-resolution display mode and automatically enables double-width display.

Table 7 Double-Width Display Usage

Programming Method	CRT System Mode	Setting
Pin: SP	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display
Internal register: Control register bit 1 (SP bit)	VGA	Automatic
	Non-VGA	0: Normal display
		1: Double-width display

Stretching and Centering Display

When the display size differs from the LCD panel size, data will be displayed on the upper-left section of the LCD panel with blank space to the right and/or below if no countermeasures are taken. To provide a user-friendly display, the CLINE can stretch a display to fill out the panel or center a display. Both stretching and centering functions are enabled by control register (R0) bits 2, 3, and 4.

Note that stretching and centering functions are available only in a system where buffer memory is used. This is because these functions are realized through adjustment of memory access. Similarly, stretching and centering functions are unavailable in non-VGA modes when the CLINE is controlled by the pin programming method. Simultaneous use of the vertical centering and stretching functions is also impossible.

In the internal register programming method, horizontal centering function is controlled by the centering character register (R6) within the range of 1 to 32 characters (8 to 256 dots), while vertical centering function is controlled by the centering raster register (R5) within the range of 1 to 256 lines.

Stretching function is controlled by the stretching control register (R8) and the stretching index register (R9 and R10) so as to double the vertical display size at most.

Figure 3 shows display examples using stretching/centering functions. In these examples, a display of 640 dots × 350 lines is displayed on an LCD panel of 720 dots × 400 lines, using stretching/centering functions.

For VGA modes, in both internal register programming and pin programming methods, necessary parameters are automatically calculated from the relationship between display size and the LCD panel size and set in the appropriate registers. Consequently, there is no need to account for display size.

However, the vertical centering or stretching function can be selected in the internal register programming method. (In pin programming method, the stretching function is automatically selected.) Table 8 describes the use of the stretching and centering function.

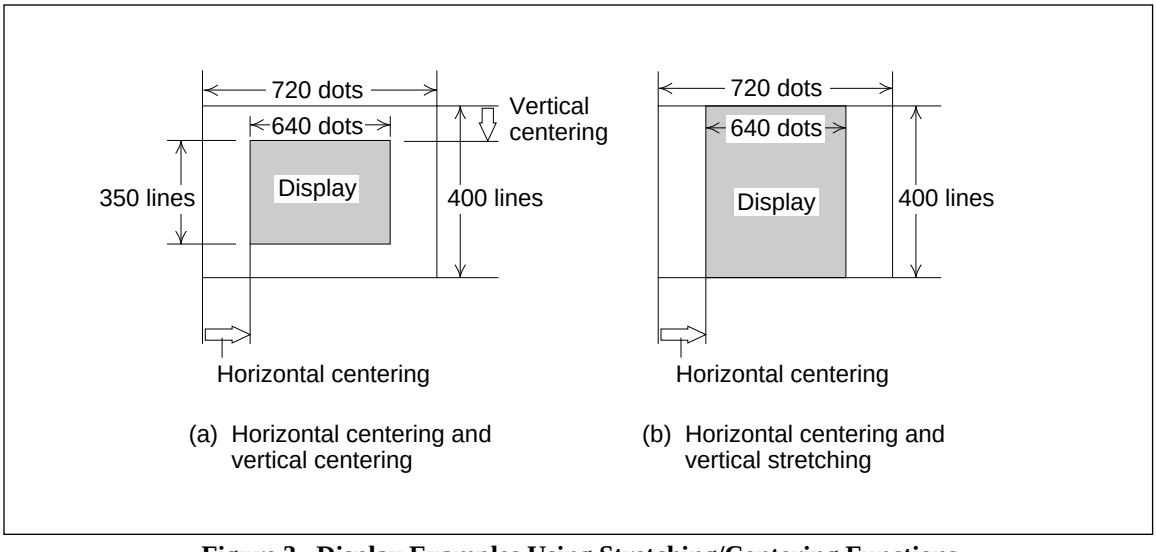


Figure 3 Display Examples Using Stretching/Centering Functions

Table 8 Stretching and Centering Function Usage

Direction	Programming Method	CRT System Mode	Display Arranging Function	Setting
Vertical	Pin	VGA	Stretching	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Stretching or centering	Automatic *2
		Non-VGA	Stretching or centering	Necessary
Horizontal	Pin	VGA	Centering	Automatic
		Non-VGA	None	— *1
	Internal register	VGA	Centering	Automatic
		Non-VGA	Centering	Necessary

Notes: 1. Display size must be LCD panel size.
2. Either stretching or centering function must be selected by the internal register.

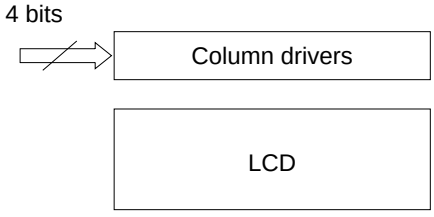
Display Modes

Display Mode Settings and LCD Module Configurations: The CLINE supports 20 display modes, depending on the settings of the LMODE4 to LMODE0 pins. The display mode includes display color mode (color or monochrome), screen configuration (single or dual), gradation display method, and width of data transfer to LCD drivers. Table 9 lists the display modes and figures 4 (a) to 4 (g) show the corresponding LCD module configurations.

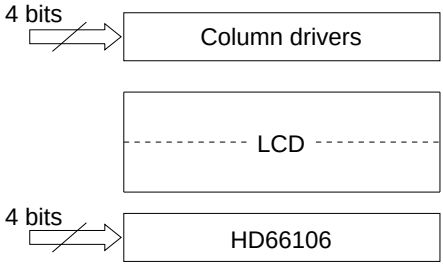
Table 9 Display Modes and LCD Module Configurations

Mode No.	Pin: LMODE 4	3	2	1	0	Display Color Mode (Gradation Display Method)	Screen Config.	Data Width	LCD Module Config.
1	0	0	0	0	0	Monochrome: black and white	Single	4	Fig. 4 (a)
2	0	0	0	0	1		Dual	4	Fig. 4 (b)
3	0	0	0	1	0		Single	8	Fig. 4 (c)
4	0	0	0	1	1		Dual	8	Fig. 4 (d)
5	0	0	1	0	0	Monochrome: 16 gray levels (Frame-based data thinning)	Single	4	Fig. 4 (a)
6	0	0	1	0	1		Dual	4	Fig. 4 (b)
7	0	0	1	1	0		Single	8	Fig. 4 (c)
8	0	0	1	1	1		Dual	8	Fig. 4 (d)
9	0	1	0	0	0	Monochrome: 16 gray levels (1/2 pulse width modulation)	Single	4	Fig. 4 (a)
10	0	1	0	0	1		Dual	4	Fig. 4 (b)
11	0	1	0	1	0		Single	8	Fig. 4 (c)
12	0	1	0	1	1		Dual	8	Fig. 4 (d)
13	1	0	0	0	0	16 colors	Single	2	Fig. 4 (e)
14	1	0	0	1	0		Single	4	Fig. 4 (f)
15	1	0	0	1	1	8 colors	Single	8	Fig. 4 (g)
16	1	0	1	0	0	4096 color (Frame-based data thinning)	Single	2	Fig. 4 (e)
17	1	0	1	1	0		Single	4	Fig. 4 (f)
18	1	0	1	1	1		Single	8	Fig. 4 (g)
19	1	1	0	1	0	4096 color (1/2 pulse width modulation)	Single	4	Fig. 4 (f)
20	1	1	0	1	1		Single	8	Fig. 4 (g)

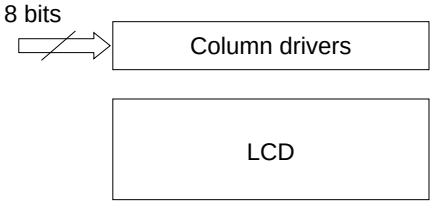
Note: Modes 15, 18, and 20 are interleaving structure modes.



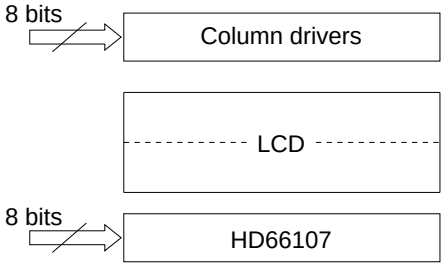
(a) Single screen, 4-bit data width



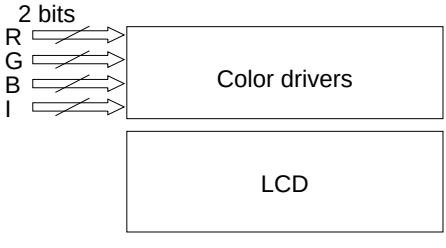
(b) Dual screen, 4-bit data width



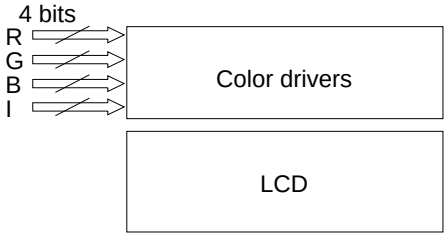
(c) Single screen, 8-bit data width



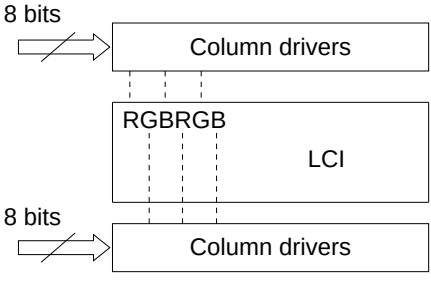
(d) Dual screen, 8-bit data width



(e) Single screen, 2-bit data width, color drivers



(f) Single screen, 4-bit data width, color drivers



(g) Single screen, 8-bit data width, interleaving structure

Figure 4 LCD Module Configurations by Display Modes

Gradation Level Reduction: Although a CRT display system can represent information for over 100,000 color levels, an LCD cannot handle so much information.

Consequently, CRT color or gradation level information must be reduced in order for the CLINE to display it. Reduction methods vary depending on the input color or gradation level information, the LCD panel (color or monochrome), and other factors. Table 10 lists gradation level reduction for CLINE modes, where "Input Bits" indicates CRT display color data and "Reduced Data" indicates input to the gradation level palettes.

Input Display Data Connection: Input display data connection and pin settings depend on the CRT input mode (color or gradation level information) and the LCD panel used.

- When monochrome LCD panel is used (LMODE4 = 0)

  — 64-color input and 16-level grayscale output (modes 5-12)

  The B0 pin must be set to 1, and the B1 pin to 0. Unused display data input pins must be fixed to 0. See figure 5 (a).

  — 16-level grayscale input and 16-level grayscale output (modes 5-12)

  Both B0 and B1 pins must be set to 0. Unused display data input pins must be fixed to 0. See figure 5 (b).

- When color LCD panel is used (LMODE4 = 1)

  — 64-color input and 16- or 8-color output (modes13-15)

  Two-bit R, G, and B data must be input to the R2-R3, G2-G3, and B2-B3 pins, respectively. Unused display data input pins must be fixed to 0). See figure 6 (a).

  — 4096-color input and 4096-color output (modes 16-20)

  Four-bit R, G, and B data must be input to the R0-R3, G0-G3, and B0-B3 pins, respectively. If the input has more than 4096 colors, use the high-order four bits of each color. See figure 6 (b).

Table 10 Gradation Level Reduction for CLINE Display Modes

Input Mode	Input Bits R	G	B	CLINE Display Mode	Reduced Data 3	2	1	0	LCD Panel	Gradation Level Reduction (Bits)
4096 colors	4	4	4	4096 color levels	D3	D2	D1	D0	Color	12 → 12
64 colors	2	2	2	16 colors	R	G	B	I	Color	6 → 4
64 colors	2	2	2	16 gray levels	D3	D2	D1	D0	Monochrome	6 → 4
16 gray levels	—	4	—	16 gray levels	D3	D2	D1	D0	Monochrome	4 → 4
16 gray levels	—	4	—	Monochrome (black & white)	All 0s or all 1s				Monochrome	4 → 1

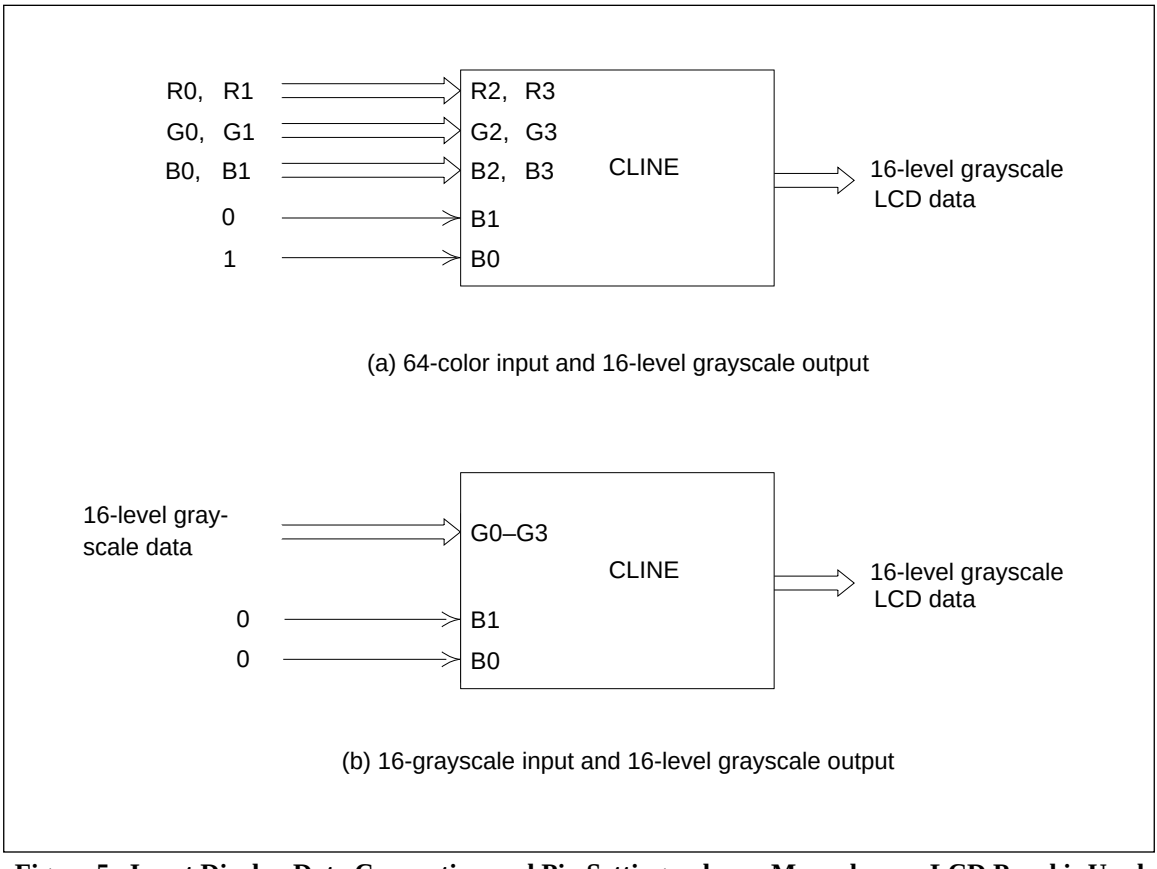
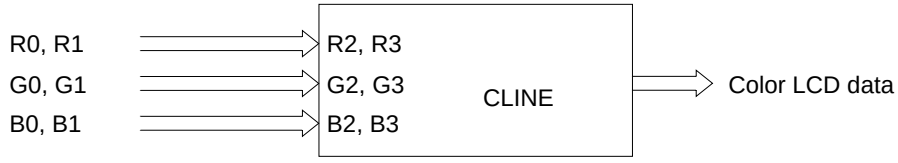
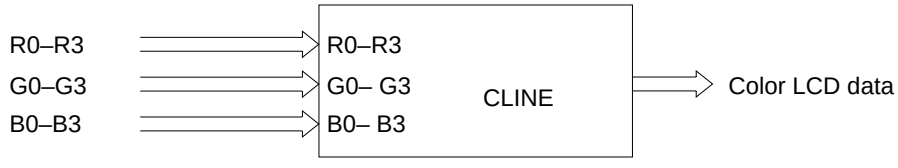


Figure 5 Input Display Data Connection and Pin Settings when a Monochrome LCD Panel is Used



(a) 64-color input and 16- or 8-color output



(b) 4096-color input and 4096-color output

Figure 6 Input Display Data Connection and Pin Settings when a Color LCD Panel is Used

LCD Data Output: The CLINE uses pins UD7–UD0 and LD7–LD0 for display data output. Output data from these pins depend on the display mode, as shown in table 11. However, data output timings are basically the same in all display modes. Display data output timing for modes 15 and 18 (8-bit color data transfer, bidirectional connection, without pulse width modulation) is shown in figure 7. Display data output timing for the LCD display modes with pulse width modulation is slightly different. This type of example is shown in figure 8. Figure 8 shows the display data output timing in mode 10 (1/2 pulse width modulation, 4-bit monochrome data transfer, and dual screen configuration).

However, LCD lower panel data LD3–LD0 are not shown in the figure.

Table 11 LCD Data Output Pins and Display Data by Display Modes

	Monochrome Modes				Color Modes				
Pin	4-Bit/ Single Screen	4-Bit/ Dual Screen	8-Bit/ Single Screen	8-Bit/ Dual Screen	2-Bit	4-Bit	8-Bit		
UD7	—	—	D7	UD7	—	R3	R15	G10	B5
UD6	—	—	D6	UD6	—	R2	B15	R9	G4
UD5	—	—	D5	UD5	R1	R1	G14	B9	R3
UD4	—	—	D4	UD4	R0	R0	R13	G8	B3
UD3	D3	UD3	D3	UD3	—	G3	B13	R7	G2
UD2	D2	UD2	D2	UD2	—	G2	G12	B7	R1
UD1	D1	UD1	D1	UD1	G1	G1	R11	G6	B1
UD0	D0	UD0	D0	UD0	G0	G0	B11	R5	G0
LD7	—	—	—	LD7	—	B3	G15	B10	R4
LD6	—	—	—	LD6	—	B2	R14	G9	B4
LD5	—	—	—	LD5	B1	B1	B14	R8	G3
LD4	—	—	—	LD4	B0	B0	G13	B8	R2
LD3	—	LD3	—	LD3	—	(I3)	R12	G7	B2
LD2	—	LD2	—	LD2	—	(I2)	B12	R6	G1
LD1	—	LD1	—	LD1	(I1)	(I1)	G11	B6	R0
LD0	—	LD0	—	LD0	(I0)	(I0)	R10	G5	B0

Notes: 1. The left bit corresponds to MSB.
2. U and L indicate upper panel and lower panel data, respectively.
3. Data in parentheses are for 16-color display.
4. — indicates that the corresponding pins are not used; must be left disconnected.

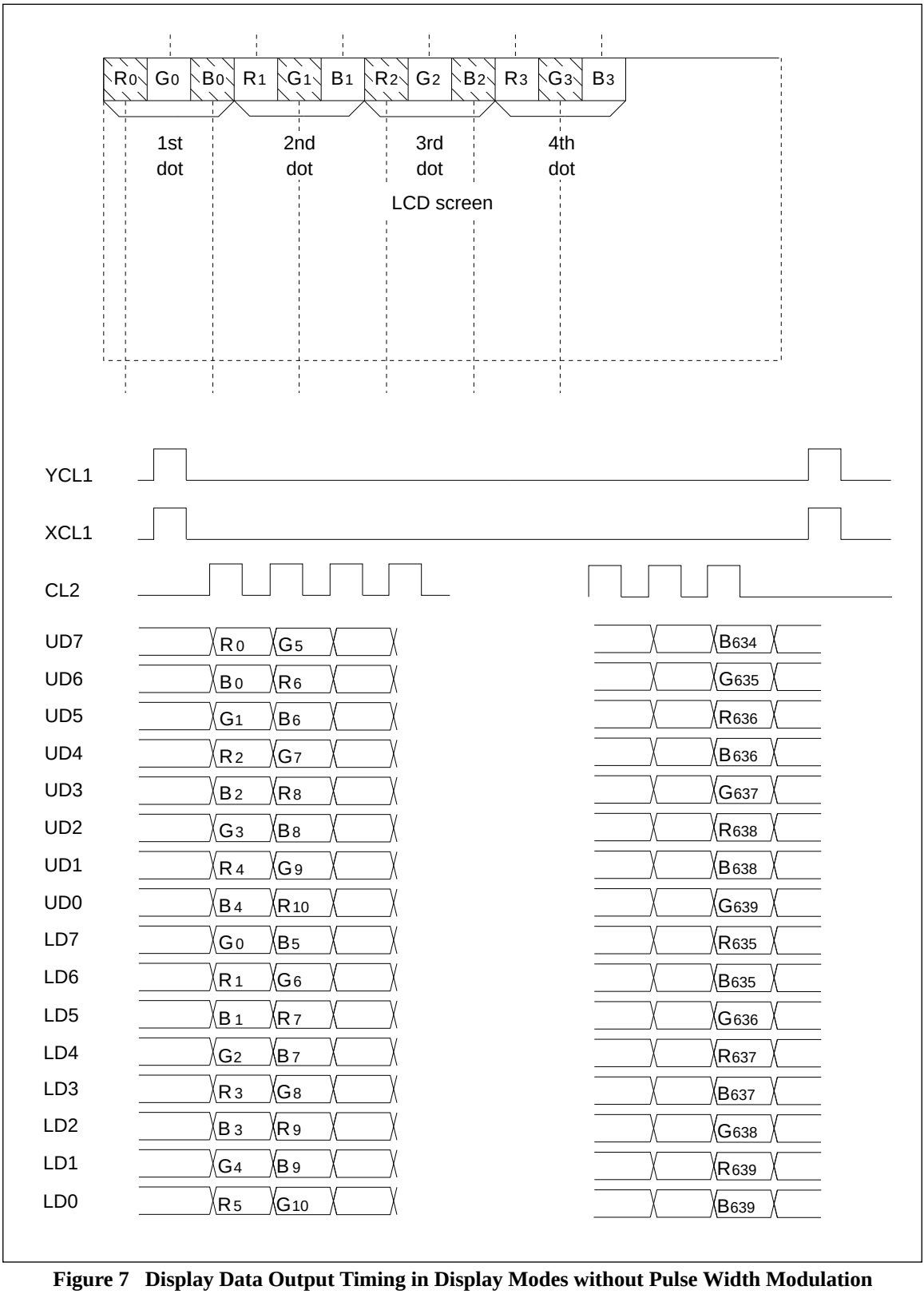


Figure 7 Display Data Output Timing in Display Modes without Pulse Width Modulation (Modes 15 and 18)

In figure 8, data P0–0, P4–0, ... P636–0 make up the first set of data for one line to be output to LCD drivers via pin UD3. Likewise, data P0–1, P4–1, ... P636–1 make up the second set of data. The combination of the first and second sets of data determines the display status as follows: (first data, second data) = (0, 0): display off; (1, 0): 1/2 pulse width modulation; and (1, 1): display on. For more details, refer to the Gradation Display Methods section.

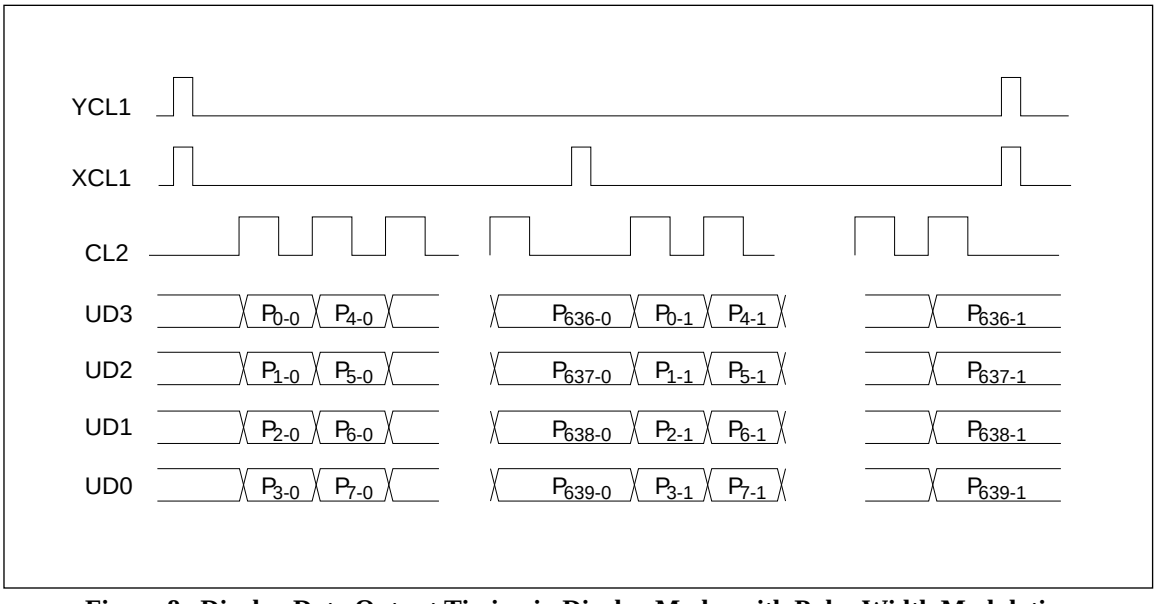


Figure 8 Display Data Output Timing in Display Modes with Pulse Width Modulation (Mode 10)

Gradation Display Methods

The CLINE supports the frame-based data thinning method and pulse width modulation method for gradation display.

Frame-Based Data Thinning Method: In the frame-based data thinning method, the CLINE thins out the display data in line or dot units in the specified frames.

Pulse Width Modulation Method: In the pulse width modulation method, the CLINE combines 1/2 pulse width modulation and frame-based data thinning. In this case, data is output from X-drivers twice in one line-selection period (figure 9).

Consequently, the X-driver latch clock must be different from the Y-driver shift clock, and a conventional LCD module configuration cannot be used. Therefore, clock XCL1 must be supplied to X-drivers and clock YCL1 to Y-drivers (figure 10).

The XCL1 period is specified by the gradation display clock period register (R13 and R14) when no buffer memory is used in non-VGA modes and in the internal register programming method. (Pulse width modulation is unavailable when buffer memory is not used in non-VGA modes, pin programming method.) In the other cases, the register is automatically set, since the YCL1 period is fixed (table 12).

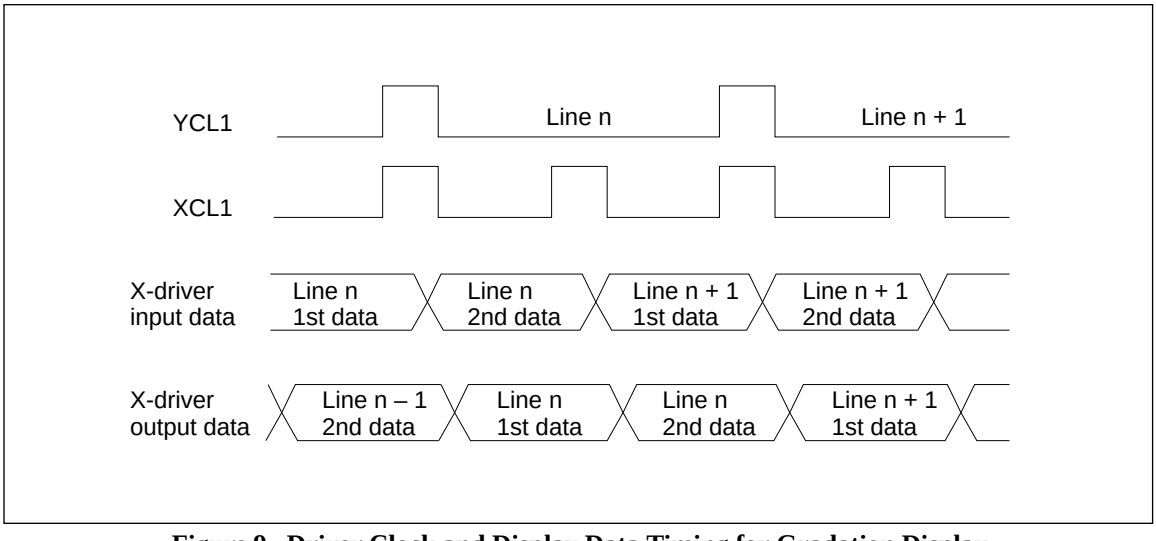


Figure 9 Driver Clock and Display Data Timing for Gradation Display with 1/2 Pulse Width Modulation

Table 12 XCL1 Period Setting

Memory Mode		XCL1 Period	Setting
With-memory		Half of YCL1 period for 1/2 pulse with modulation method	Automatic
Without-memory	VGA	Half of YCL1 period for 1/2 pulse width modulation method	Automatic (See note below)
	Non-VGA		
	Internal register programming	Conforms to gradation display clock register (R13, R14) settings	Required (R13, R14)
	Pin programming	—	

Note: Total number of horizontal dots must be 400, 450, 800, or 900 for displaying 320, 360, 640, or 720 dots, respectively.

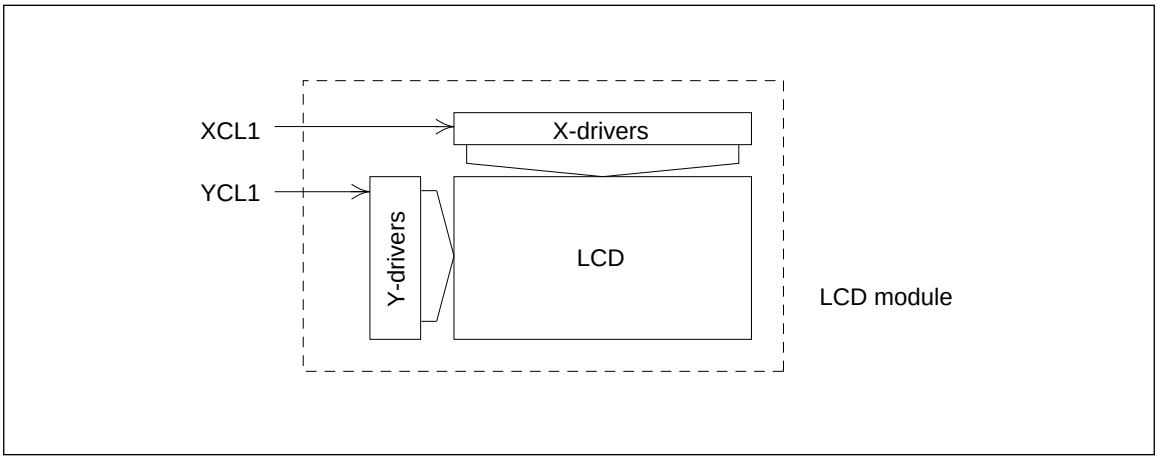


Figure 10 X- and Y-Driver Clock Connection for Pulse Width Modulation Method

Gradation Level Palettes

Gradation display quality depends greatly on LCD panel characteristics.

Consequently, uniform gradation display may be impossible for some panels. To accommodate this situation, the CLINE incorporates a set of gradation level palettes that can assign any gradation level to any CRT display color as desired.

16 levels are available for gradation display using the frame-based data thinning method and 31 levels using 1/2 pulse width modulation method. Appropriate levels can be selected for the LCD panel used.

The R-, G-, and B-palettes are used for color level display modes, while only the R-palette is used for 16-level grayscale display modes.

In pin programming and MPU programming methods, these palettes are automatically loaded after reset with appropriate data for frame-based data thinning modes and 1/2 pulse width modulation modes. The automatically set data cannot be rewritten in the pin programming method, but can be rewritten, any time after 100 µs have elapsed after reset, in MPU programming method.

By contrast, in the ROM programming method, these palettes are not automatically set. Thus writing the necessary data to the palettes is always required.

Table 13 shows the relationship between the values set in the palettes (through R12) and gradation levels. Values other than those shown here disable correct display.

Table 13 Relationship between Gradation Levels and Palette (R12) Values

(a) Frame-based data thinning modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	1	0	0	0	0	0	0.00
1	1	0	0	0	0	1	0.14
2	1	0	0	0	1	0	0.20
3	1	0	0	0	1	1	0.29
4	1	0	0	1	0	0	0.33
5	1	0	0	1	0	1	0.40
6	1	0	0	1	1	0	0.43
7	1	0	0	1	1	1	0.50
8	1	0	1	0	0	0	0.57
9	1	0	1	0	0	1	0.60
10	1	0	1	0	1	0	0.66
11	1	0	1	0	1	1	0.71
12	1	0	1	1	0	0	0.75
13	1	0	1	1	0	1	0.80
14	1	0	1	1	1	0	0.86
15	1	0	1	1	1	1	1.00

(b) 1/2 pulse width modulation modes

Gradation Level No.	Palette Data (R12 Data Bits) 5	4	3	2	1	0	Gradation Level
0	0	1	0	0	0	0	0.00
1	0	1	0	0	0	1	0.07
2	0	1	0	0	1	0	0.10
3	0	1	0	0	1	1	0.14
4	0	1	0	1	0	0	0.17
5	0	1	0	1	0	1	0.20
6	0	1	0	1	1	0	0.21
7	0	1	0	1	1	1	0.25
8	0	1	1	0	0	0	0.29
9	0	1	1	0	0	1	0.30
10	0	1	1	0	1	0	0.33
11	0	1	1	0	1	1	0.36
12	0	1	1	1	0	0	0.38
13	0	1	1	1	0	1	0.40
14	0	1	1	1	1	0	0.43
15	0	1	1	1	1	1	0.50
16	1	1	0	0	0	0	0.50
17	1	1	0	0	0	1	0.57
18	1	1	0	0	1	0	0.60
19	1	1	0	0	1	1	0.64
20	1	1	0	1	0	0	0.67
21	1	1	0	1	0	1	0.70
22	1	1	0	1	1	0	0.71
23	1	1	0	1	1	1	0.75
24	1	1	1	0	0	0	0.79
25	1	1	1	0	0	1	0.80
26	1	1	1	0	1	0	0.83
27	1	1	1	0	1	1	0.86
28	1	1	1	1	0	0	0.88
29	1	1	1	1	0	1	0.90
30	1	1	1	1	1	0	0.93
31	1	1	1	1	1	1	1.00

Display On/Off Control

When the LCD drivers used have an LCD on/off control pin, display can be controlled with the CLINE DISPON signal. When the LCD drivers used do not have an LCD on/off control pin, the CLINE can turn off display by transferring all-0 display data to the drivers.

Display will be turned on with the DISPON pin = 1, turns the display off while DISPON = 0. The DISPON pin is equivalent to the DISPON bit (bit 0) of the control register.

In the pin programming method, display is on except for four frames after reset. The four frame display-off time period prevents random display at power-on. In the MPU programming method, display is turned off at reset, but can be freely turned on or off after four frames after reset by rewriting the corresponding register bit. In the ROM programming method, a 1 must be written to the DISPON bit to turn on display. Like in other programming methods, display is off for four frames after reset.

LDOTCK Frequency and Data Transfer Rate

The LDOTCK frequency (f_{LDOTCK}) for asynchronous mode is calculated from the following equation:

$$f_{LDOTCK} = (Nhd + 48) \times Nvd \times f_F$$

Nhd: Number of dots contained in one horizontal line of the LCD panel
Nvd: Number of horizontal lines from the LCD panel top to bottom
f_F: Frame frequency

In this case, the following relationship must hold true:

$$1/2 \times f_{DOTCLK} < f_{LDOTCK} < 2 \times f_{DOTCLK}$$

f_{DOTCLK}: Dot clock frequency

The data transfer rate to LCD drivers depends on the mode in which the CLINE is used. Specifically, the rate depends on screen configura-tion (single or dual), data transfer width (bit count), and gradation display methods. For example, the data transfer rate will be doubled for 1/2 pulse width gradation display. This is because data must be transferred two times during one line-selection period. The data transfer rate (f_{CL2}: CL2 frequency) is calculated from the following equation ($f_{LDOTCK} = f_{DOTCLK}$ for synchronous mode):

$$f_{CL2} = \frac{f_{LDOTCK} \times l}{n \times m}$$

n: Number of panels composing one screen
— 1 for modes 1, 3, 5, 7, 9, 11, 13-20
— 2 for modes 2, 4, 6, 8, 10, 12

m: Number of bits transferred at one time
— 2 for modes 13, 16
— 4 for modes 1, 2, 5, 6, 9, 10, 14, 15, 17-20
— 8 for modes 3, 4, 7, 8, 11, 12

l: Constant for each gradation display
— 1 for modes 1-8, 13-18
— 2 for modes 9-12, 19, 20

Synchronous/Asynchronous Modes and Memory

The CLINE has two timing modes: asynchronous and synchronous.

In asynchronous mode, dot clock pulses for the CRT system (DOTCLK) are different from those for the LCD system (LDOTCK) in frequency to accommodate frame frequency conversion. This requires buffer memory as shown in figure 11 (a). In this mode, dual screen LCD panels can be used.

In synchronous mode, dot clock pulses for the CRT system are identical to those for the LCD system, thus requiring no buffer memory in principle (synchronous without-memory mode (figure 11 (b)). However, synchronous without-memory mode cannot support dual screen LCD panels.

The CLINE has another mode in which dual screen LCD panels can be used and fewer memory devices are required. This is called “synchronous with-memory mode” (figure 11 (c)). In this mode, the number of memory devices can be reduced to a half or a third that of asynchronous mode. This is because RGB data sent from the CRT system is processed for gradation display before being written into buffer memory. (In asynchronous mode, on the other hand, R, G, and B data sent from the CRT system is separately written into the R-plane, G-plane, and B-plane memories, respectively.)

Table 14 summarizes these modes.

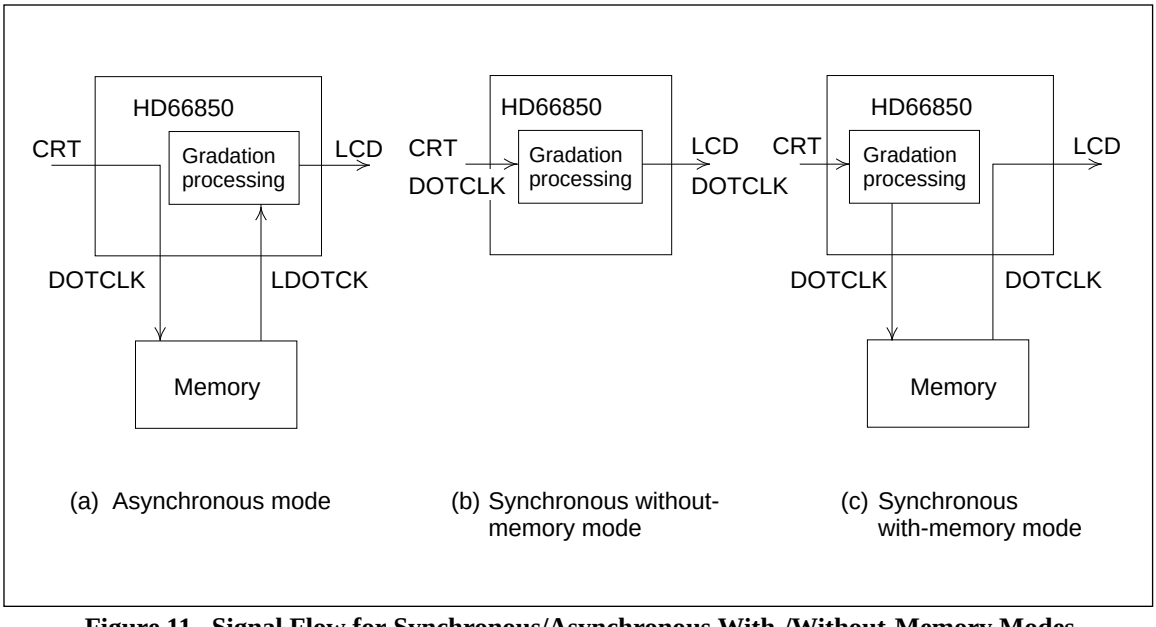


Figure 11 Signal Flow for Synchronous/Asynchronous With-/Without-Memory Modes

The CLINE uses dual port RAMs for buffer memory, enabling high-speed display and independent use of an LCD dot clock and a CRT dot clock.

The CLINE supports three types of memory configurations: 64 k × 4 bits (256 k), 256 k × 4 bits (1 M), and 128 k × 8 bits (1 M), any of which can be selected with the MMODE0 and MMODE1 pins (table 3).

The number of memory devices required depends on the LCD panel size and the display mode. However, it depends only on LCD panel vertical size and not on horizontal size since the CLINE uses memory as shown in figure 12. For example, one 256-kbit memory device is required for the panel having 256 or less lines and two for that having 257 to 512 lines. Table 15 lists the number of memory devices required for each mode.

Table 14 Memory Mode Summary

	Asynchronous With-Memory Mode	Synchronous With-Memory Mode	Synchronous Without Memory Mode
Centering/stretching	Possible	Possible	Impossible
Max number of gray levels	16	16	16
Max number of color levels	16	4096 (frame-based data thinning)	4096 (pulse width modulation)
Dual screen	Possible	Possible	Impossible
Max number of display lines	512	512	1024
Frame frequency conversion	Possible	Impossible	Impossible

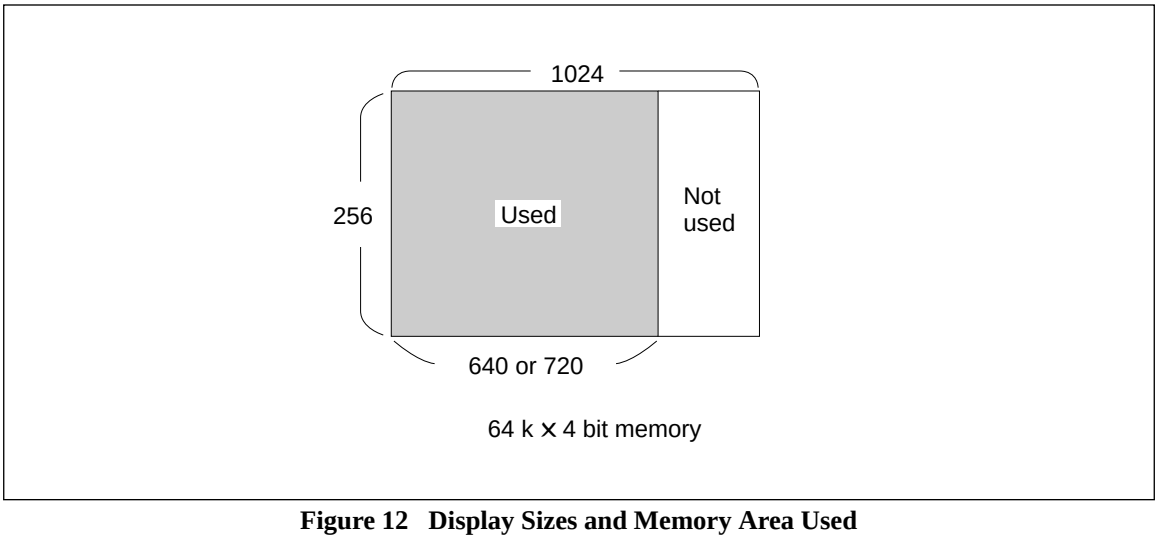


Figure 12 Display Sizes and Memory Area Used

Table 15 Number of Memory Devices for Different Display modes

	Number of Memory Devices Required					
	Asynchronous			Synchronous		
Display Mode	**64 k × 4**	**256 k × 4**	**128 k × 8**	**64 k × 4**	**256 k × 4**	**128 k × 8**
Monochrome Modes 1–4	2	1	1	2	1	1
16-level grayscale (frame-based) Modes 5–8	8	4	2	2	1	1
16-level grayscale (1/2 pulse width) Modes 9–12	8	4	2	4	2	1
8-color Mode 15	6	3	2	6	3	2
16-color Modes 13, 14	8	4	2	8	4	2
4096-color-scale (frame-based) Modes 16–18	—	—	—	6	3	2

Frame-based: Frame-based data thinning method
1/2 pulse width: 1/2 pulse width modulation method

Note: With-memory mode does not support color level display using the pulse width modulation method.

Display Timing Signal Fine Adjustment

When the display timing signal is supplied externally, a phase shift may appear between CRT data and the display timing signal, since each signal has its own peculiar lag. The CLINE can adjust the display timing signal with pins AJ3–AJ0 (in pin programming method) or with the input timing control register (R1) (in internal register programming method) to compensate the phase shift (table 1).

Figure 13 (a) shows an example of adjusting a display timing signal that is two dots ahead of the display start position. In this case, pins (AJ3, AJ2, AJ1, AJ0) or data bits (3, 2, 1, 0) of R1 must be set to (1, 0, 1, 0) to delay the signal for two dots. Conversely, they must be set to (0, 0, 1, 0) to advance the signal for two dots for the case of figure 13 (b), where the display timing signal is two dots behind.

When there is no need to adjust the signal, a setting of either (0, 0, 0, 0) or (1, 0, 0, 0) will work.

It should be noted that the VGA CRT system applies the BLANK signal, which includes the border area period, as the display timing signal, and that the CLINE removes the border area period. Consequently, the border area period must be considered for adjusting the display timing signal.

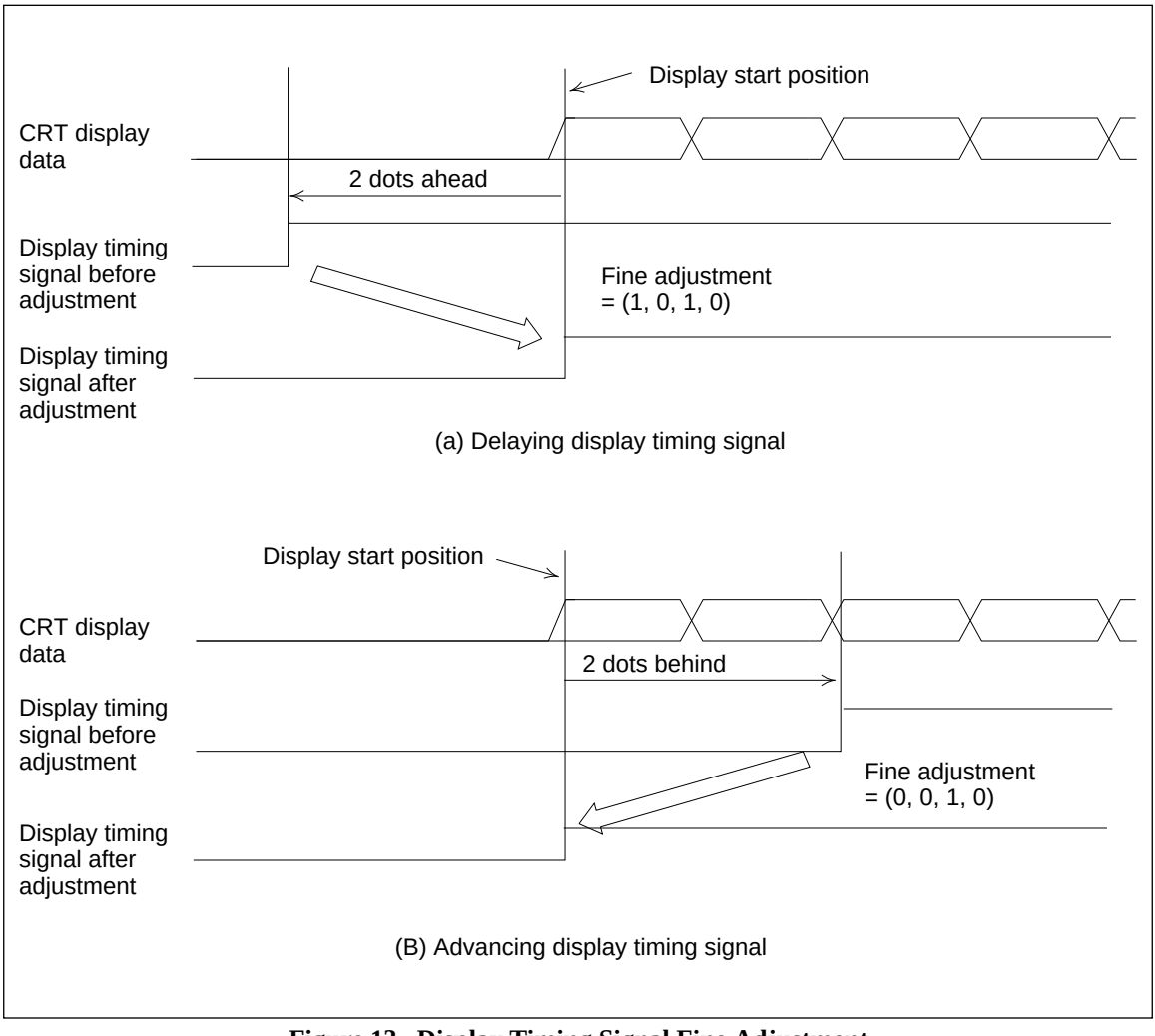


Figure 13 Display Timing Signal Fine Adjustment

Border Color Control

In the internal register programming method, the CLINE can specify the color of a blank area that is left on a centered display (figure 14). Any of 16 colors or the color of the dot immediately before the valid display data can be specified by the border color control register (R7). However, the desired color can be specified only in asynchronous mode.

In the pin programming method, the specified color is always the same color as the dot immediately before the valid display data.

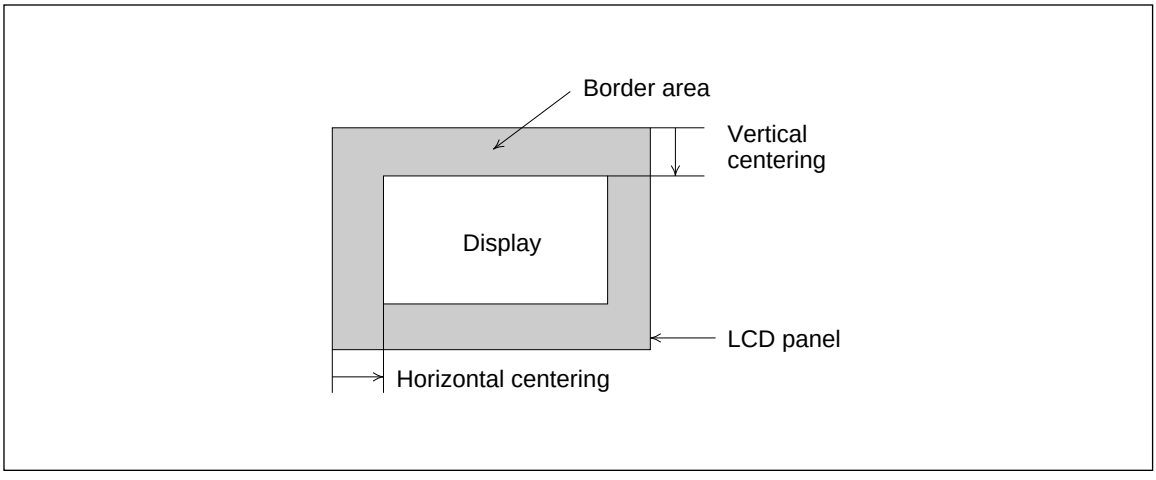


Figure 14 Border Area and an LCD Panel

Internal Registers

The CLINE has one index register (IR) and 15 data registers (R0–R14). In the MPU programming method, the desired register address must be written in one cycle into the index register before writing or reading data to/from the register in the following cycle. By contrast, in the ROM programming method, the index register is not used; the CLINE automatically reads data from the ROM, in which data has been written to the ROM addresses corresponding to the desired data registers, and writes it to the data register. Registers are valid only for the internal register programming method and are invalid (don't care) for the pin programming method. Since all data registers are reset to 0s, they must be rewritten after reset.

Register Access for MPU Programming Method

First write the desired data register address into the index register with $\overline{CS}$ = 0, RS = 0, and $\overline{WR}$ = 0, then write/read data to/from the register with $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 0 or $\overline{RD}$ = 0. Figure 15 shows the timing for writing data into an internal register.

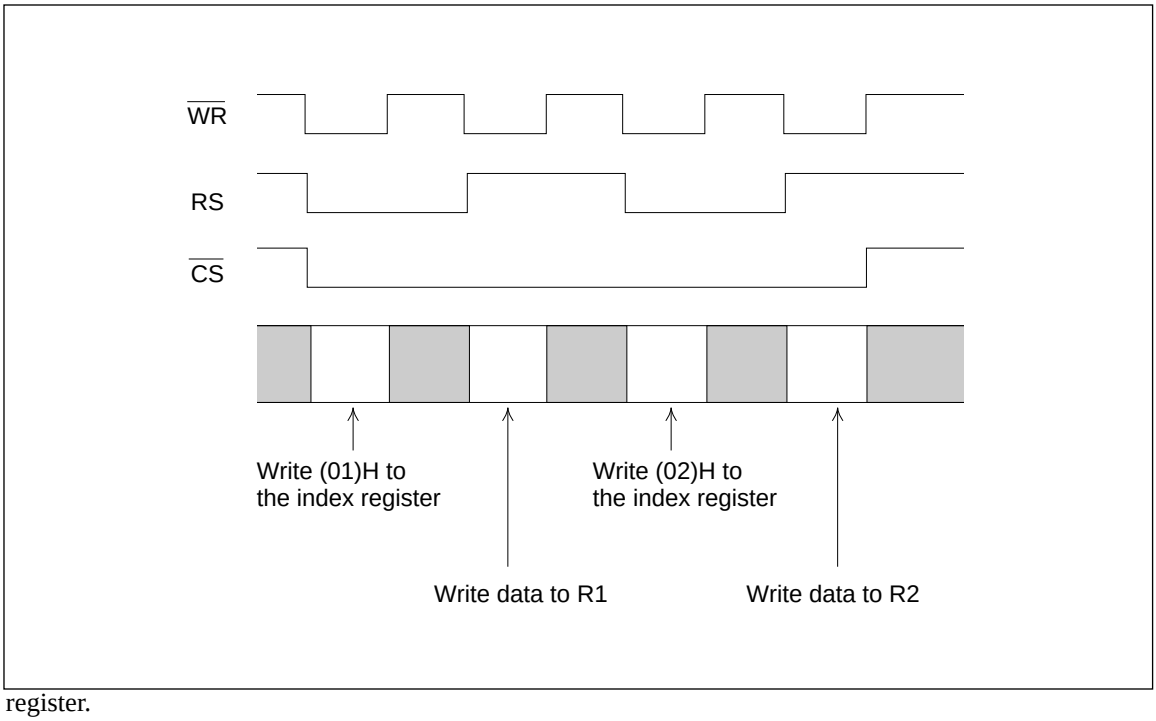


Figure 15 Internal Register Write by MPU

ROM Data Setting for ROM Programming Method

The desired data must have been previously written to the ROM addresses corresponding to the data register addresses; that is, to ROM addresses $0000–$000F. Data for the gradation level palettes must have been written to ROM addresses $0010–$003F. Consequently, data written for internal registers R11 and R12 are invalid. Figure 16 shows the ROM address map.

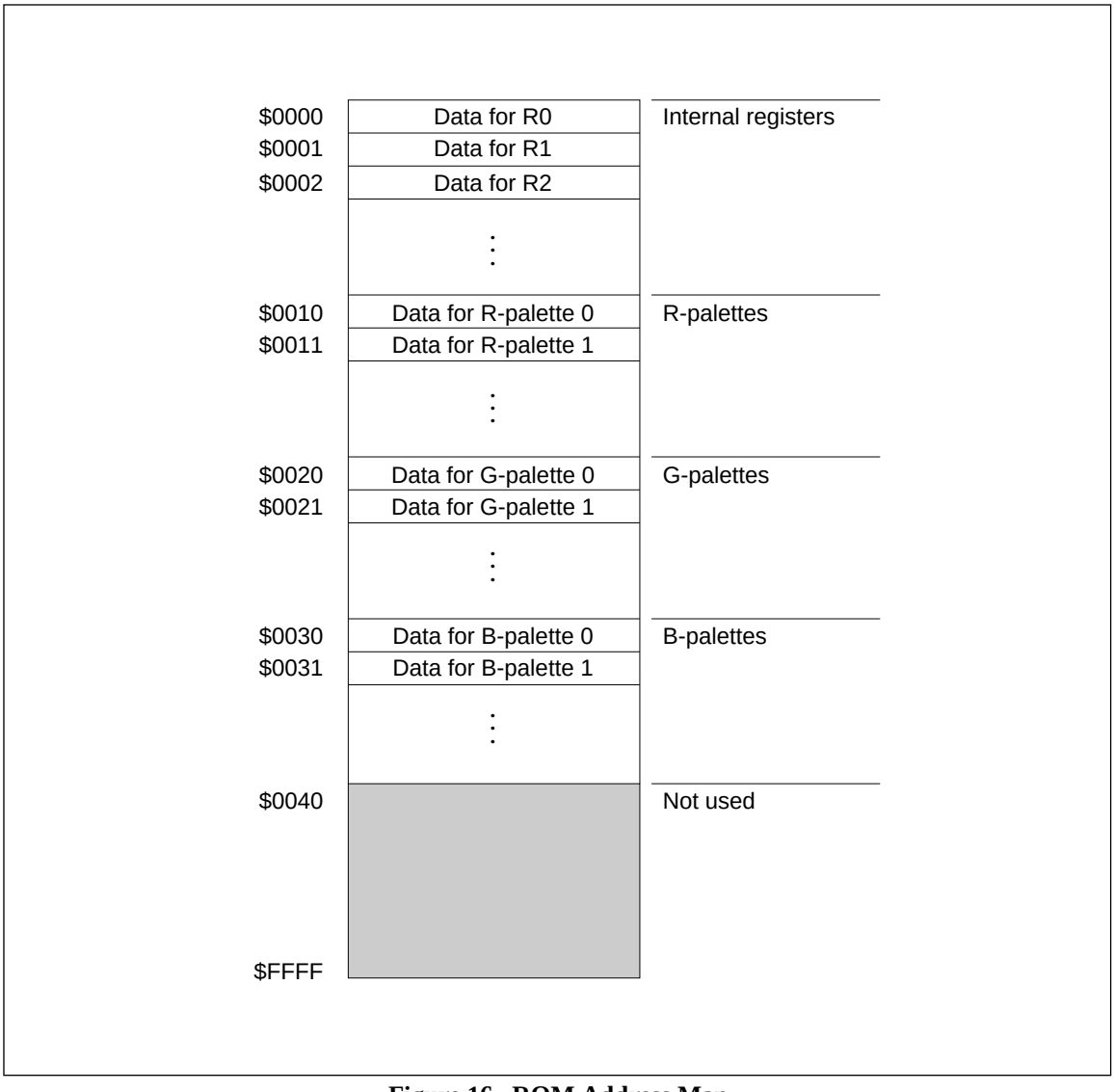


Figure 16 ROM Address Map

Register Function

Index Register (IR): The index register (figure 17), composed of four valid bits, selects one of the 15 data registers. The index register itself is selected by the MPU while the RS signal is low and selects a data register with the register address written.

Control Register (R0): The control register (figure 18) is composed of five valid bits, each with a particular function.

- STE bit
  - — STE = 1: Stretching function enabled
  - — STE = 0: Stretching function disabled
- CRE bit
  - — CRE = 1: Vertical centering function enabled
  - — CRE = 0: Vertical centering function disabled

Simultaneous use of stretching and vertical centering functions is impossible; if both the CRE and STE bits are set to 1 at the same time, correct display will be disabled.

- CCE bit
  - — CCE = 1: Horizontal centering function enabled
  - — CCE = 0: Horizontal entering function disabled
- SP bit
  - — SP = 1: Double-width display
  - — SP = 0: Normal display
- DISPON bit
  - — DISPON = 1: Display on
  - — DISPON = 0: Display off

DISPON is always cleared at reset. In the MPU programming method, rewriting this bit can always be rewritten. However, display will be off for four frames after reset, regardless of the status of this bit.

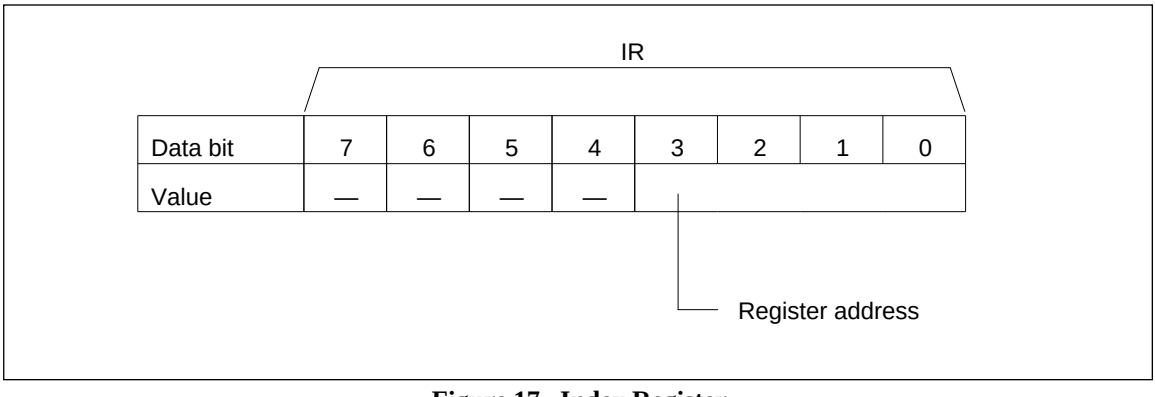


Figure 17 Index Register

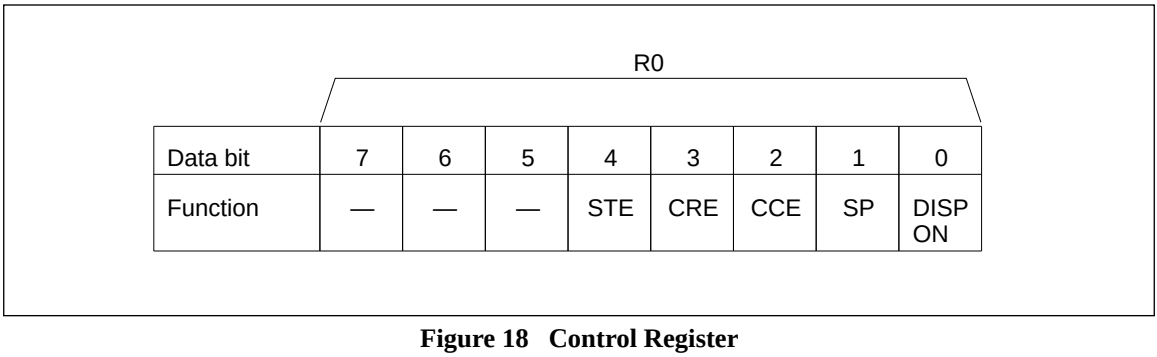


Figure 18 Control Register

Input Timing Control Register: The input timing control register (figure 19) has five valid bits, having two different functions.

- DOTE bit : Switches RGB data latch timing.
  - — DOTE = 1: Latches data at the rising edge of the dot clock pulses
  - — DOTE = 0: Latches data at the falling edge of the dot clock pulses
- AJ3-AJ0 bits: Adjust the externally supplied display timing signal to synchronize its phase with that of LCD data. Write the shift, represented in dots, between the display timing signal and the display start position to these bits. The absolute value of the number of dots to be shifted must be written to the AJ2-AJ0 bits and shift polarity to the AJ3 bit. If there is no need to adjust the display timing signal, these bits may be set to either (1, 0, 0, 0) or (0, 0, 0, 0).

R1

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	DOTE	AJ3	AJ2	AJ1	AJ0

3	2	1	0	Number of Dots Adjusted
0	0	0	0	0
	0	0	1	–1
	0	1	0	–2
1	0	0	0	0
	0	0	1	+1
	0	1	0	+2
	0	1	1	+3
	1	0	0	+4
	1	0	1	+5
	1	1	0	+6

Note: – (minus) and + (plus) in the Number of Dots Adjusted column indicate advancing and delaying the display timing signal, respectively.

Figure 19 Input Timing Control Register

Horizontal Display Size Register: The horizontal display size register (figure 20), composed of seven valid bits, specifies the horizontal display size in units of characters (eight dots). The value to write to this register is "number of characters displayed on one horizontal line – 1." A maximum of 90 characters (720 dots) can be specified.

This register is set automatically in VGA mode.

Vertical Display Size Register: The vertical display size register (figure 21), composed of nine valid bits, specifies the vertical display size in units of lines. The value to write to this register is "number of lines displayed from display screen top to bottom – 1." A maximum of 512 lines can be specified.

This register is set automatically in VGA mode.

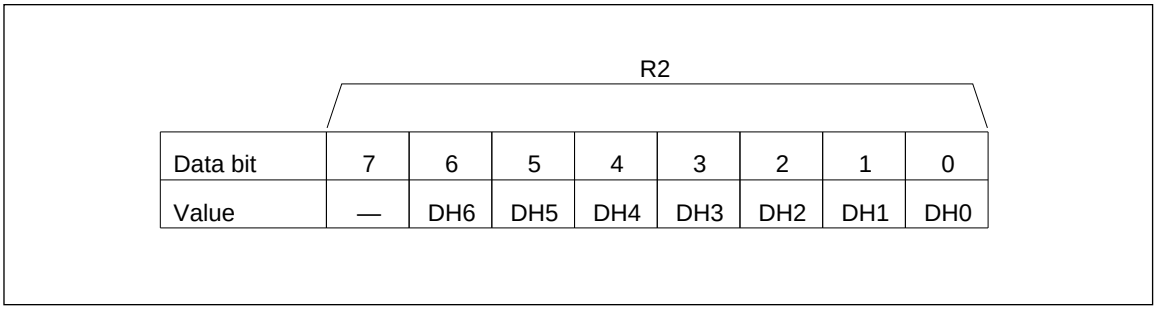


Figure 20 Horizontal Display Size Register

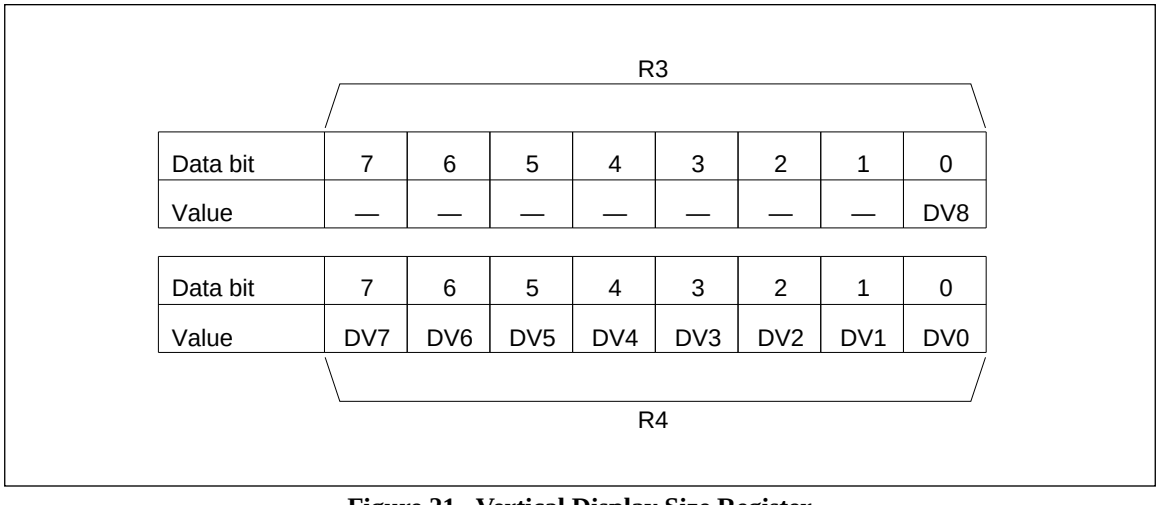


Figure 21 Vertical Display Size Register

Centering Raster Register: The centering raster register (figure 22), composed of eight bits, specifies the number of rasters for vertically centering the display within the range of 1 to 256. The value to write to this register is "number of rasters for centering – 1." As shown in figure 23, the number here indicates the number of rasters in either the upper border area or lower border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of rasters must be correctly written if the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled the control register's CRE bit is 1. This register is set automatically in VGA mode.

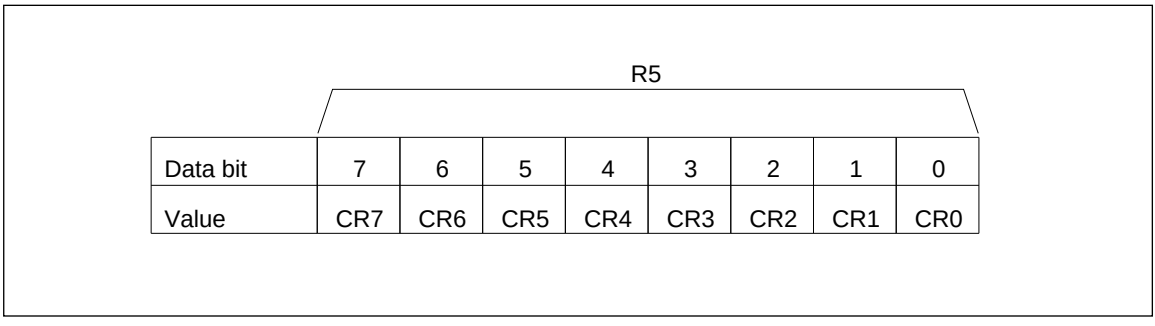


Figure 22 Centering Raster Register

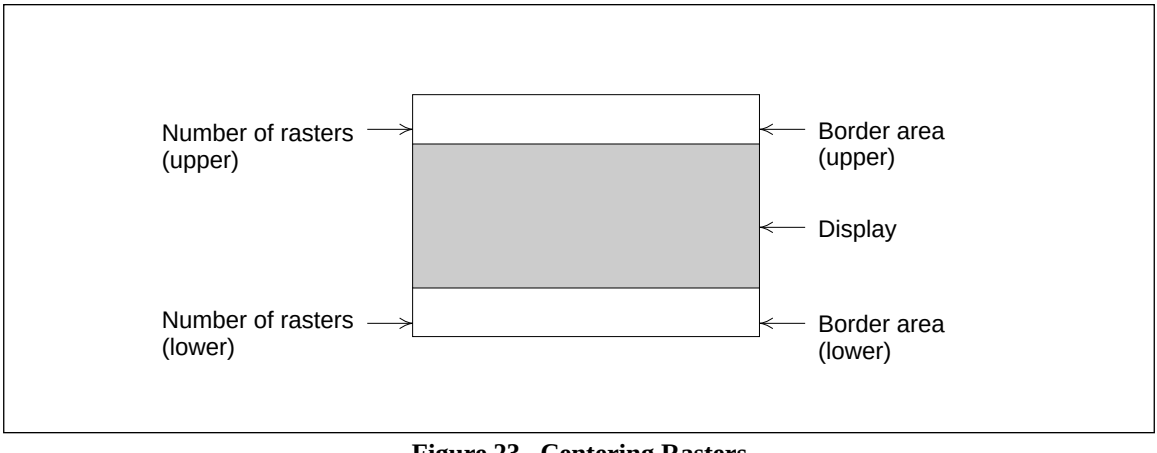


Figure 23 Centering Rasters

Centering Character Register: The centering character register (figure 24), composed of five valid bits, specifies the number of characters for horizontally centering the display within the range of 1 to 32. The value to write to this register is "number of characters for centering – 1." As shown in figure 25, the number here indicates the number of characters in either the left border area or right border area, not the total number. Since the LCD panel size is determined by this number and the display size, the number of characters must be correctly written when the display size differs from the LCD panel size. Incorrect setting disables correct display. This register is enabled when the control register's CCE bit is 1.

This register is set automatically in VGA mode.

R6

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	CC4	CC3	CC2	CC1	CC0

Figure 24 Centering Character Register

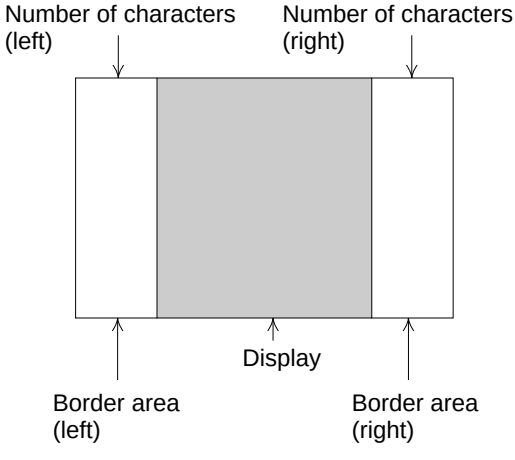


Figure 25 Centering Characters

Border Color Control Register: The border color control register (figure 26), has five valid bite having two different functions. These functions are available only in with-memory mode.

- BM bit: Specifies border control mode; reset to 0. This bit must be 1 in asynchronous mode.
  - — BM = 1: Displays the color specified by the BCI, BCR, BCG, and BCB bits in the border area (disabled in synchronous mode)
  - — BM = 0: Displays the color of the dot immediately before the display period on the border area
- BCI, BCR, BCG, and BCB bits: Specify the color to be displayed on the border area. These bits are enabled when the BM bit is 1; reset to 0s.

Stretching Control Register: The stretching control register (figure 27), composed of four valid bits, is used in combination with the stretching index register (R9 and R10). It specifies the period for stretching in units of lines. The value to write to this register is "number of lines –1." This register is enabled when the control register's STE bit is 1.

This register is set automatically in VGA mode.

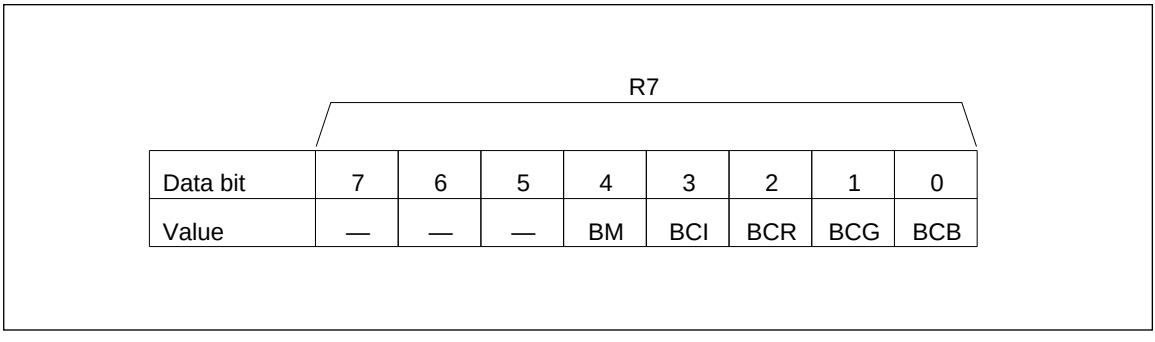


Figure 26 Border Color Control Register

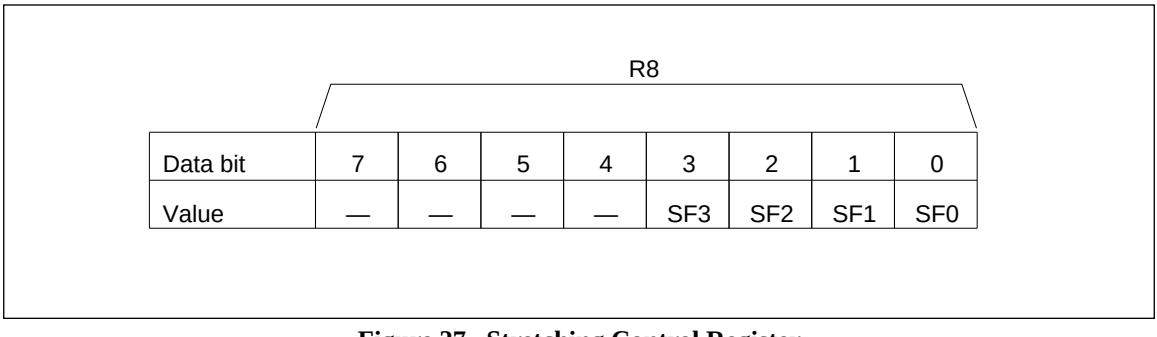


Figure 27 Stretching Control Register

Stretching Index Register: The stretching index register (figure 28), composed of 16 valid bits, is used in combination with the stretching control register (R8). It specifies the lines to be displayed twice among those specified by R8. The lines represented by the SI bits which are set to 1s will be displayed twice. Although this register has 16 bits, only the bits within the period specified by R8 are enabled. For example, when R8 is set to four, only five bits of SI0 to SI4 of this register are enabled (figure 29).

This register is set automatically in VGA mode.

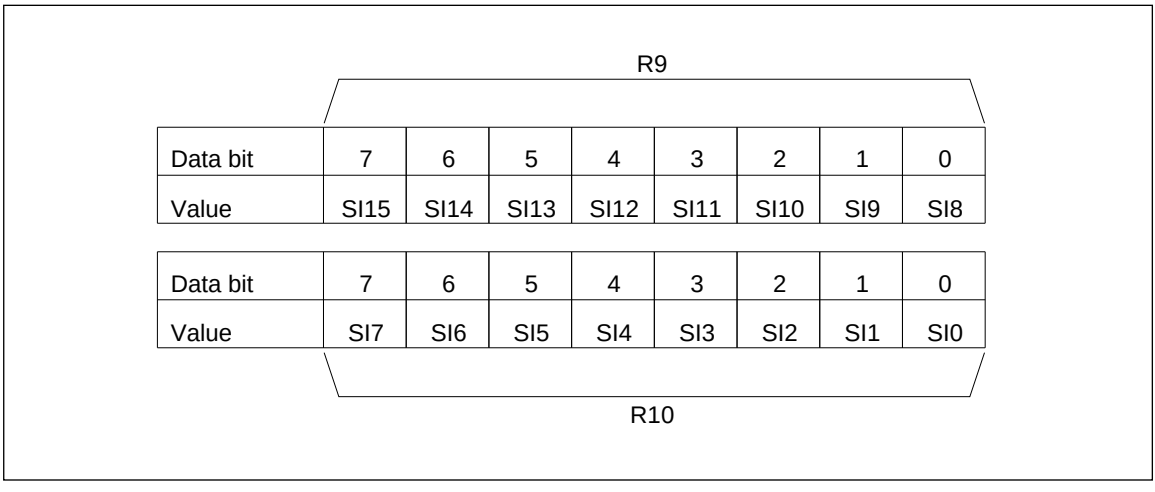


Figure 28 Stretching Index Register

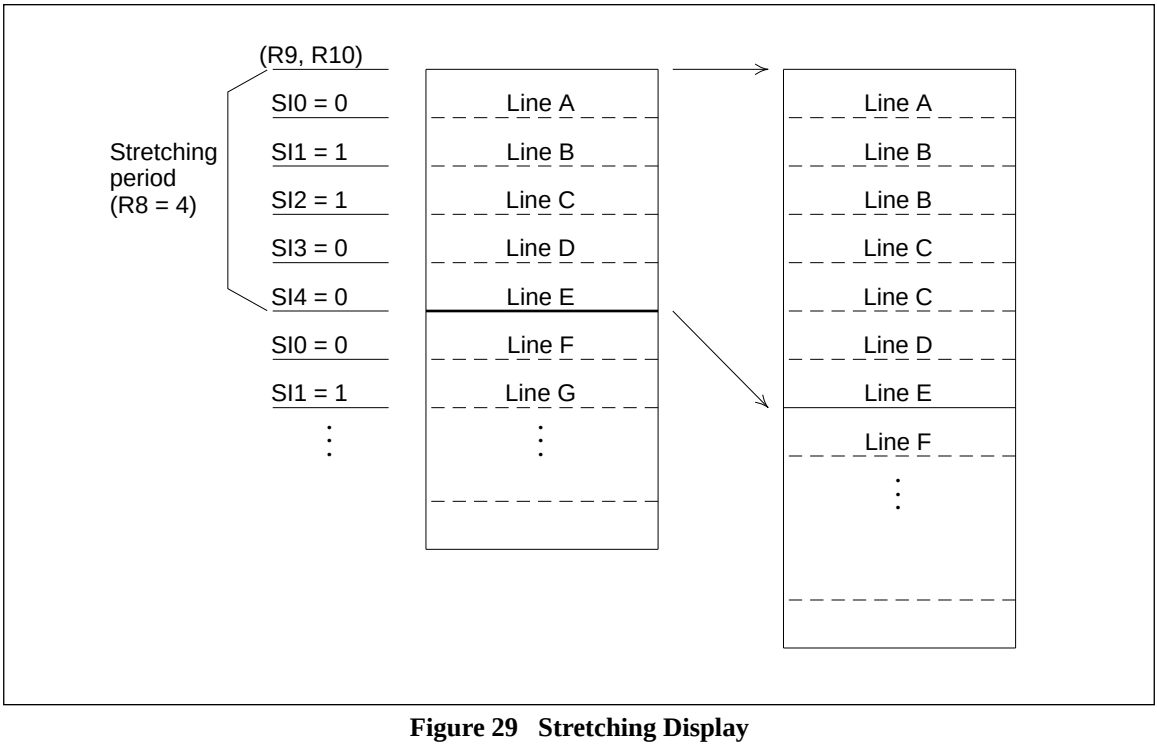


Figure 29 Stretching Display

Gradation Level Palette Address Register: The gradation level palette address register (figure 30) is composed of six valid bits with two different functions.

- PS1 and FS0 bits: Specify a method of selecting the plane of the gradation level palettes (R, G, or B).
  - — (PS1, PS0) = (0, 0): Every time the gradation level palette data register (R12) is read from or written to, either R-, G-, or B-palette is automatically selected, in that order
  - — (PS1, PS0) = (0, 1): R-palette is selected
  - — (PS1, PS0) = (1, 0): G-palette is selected
  - — (PS1, PS0) = (1, 1): B-palette is selected
- PA3–PA0 bits: Specify the desired gradation level palette using the address written to these bits. After palette address specification, data is read from or written to the specified palette and the address is automatically incremented by 1. The address increment manner depends on PS1 and PS0 settings.
  - — (PS1, PS0) = (0, 0): Gradation level palette address is automatically incremented by 1 after reading/writing data from/to R, G, and B gradation level palettes in that order, through the gradation level palette data register
  - — Other settings: Gradation level palette address is automatically incremented by 1 after reading/writing data from/to any one gradation level palette, through the gradation level palette data register

R11

Data bit	7	6	5	4	3	2	1	0
Value	—	—	PS1	PS0	PA3	PA2	PA1	PA0

Figure 30 Gradation Level Palette Address Register

Gradation Level Palette Data Register: The gradation level palette data register (figure 31), composed of six valid bits, contains data which is read from or written to the gradation level palette specified with the gradation level palette address register (R11).

Gradation level palettes must be set according to the display mode used (16-level grayscale display or 4096-color-scale display); the R-palette must be used for 16-level grayscale display, and R-, G-, and B-palettes for 4096-color-scale display. PD5 bit must be 1 and PD4 bit must be 0 in frame-based data thinning mode. PD4 bit must be 1 in 1/2 pulse width modulation mode. Show table 13.

In the MPU programming method, the gradation level palettes must be read/written after 100 ms have elapsed after reset. Note that display is scattered during palette read/write.

In the MPU programming method, gradation level palettes are not directly read from, but are read from via this register. Consequently, any data that happens to be in this register at that time is read out in the first read cycle, and then data corresponding to the specified address is transferred to this register and read from this register in the following read cycle. The address is incremented (or R-, G-, and B-palettes are switched) at the same time. In other words, after address setting, the first data read is incorrect, and the second data read is correct. Consequently, one dummy read is required after setting a gradation level palette address. Figure 32 shows the timing for reading a gradation level palette.

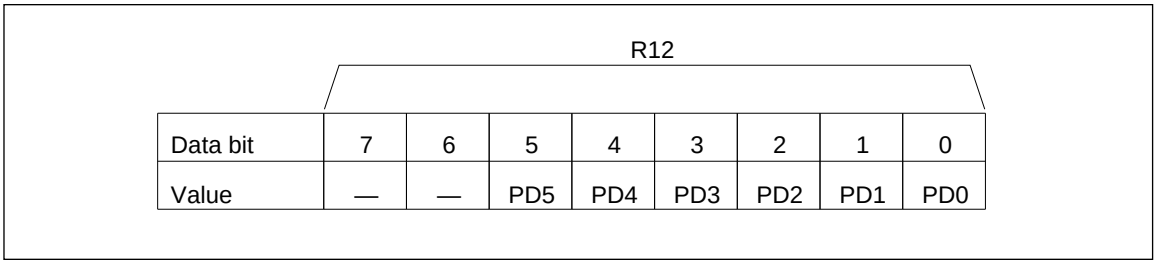


Figure 31 Gradation Level Palette Data Register

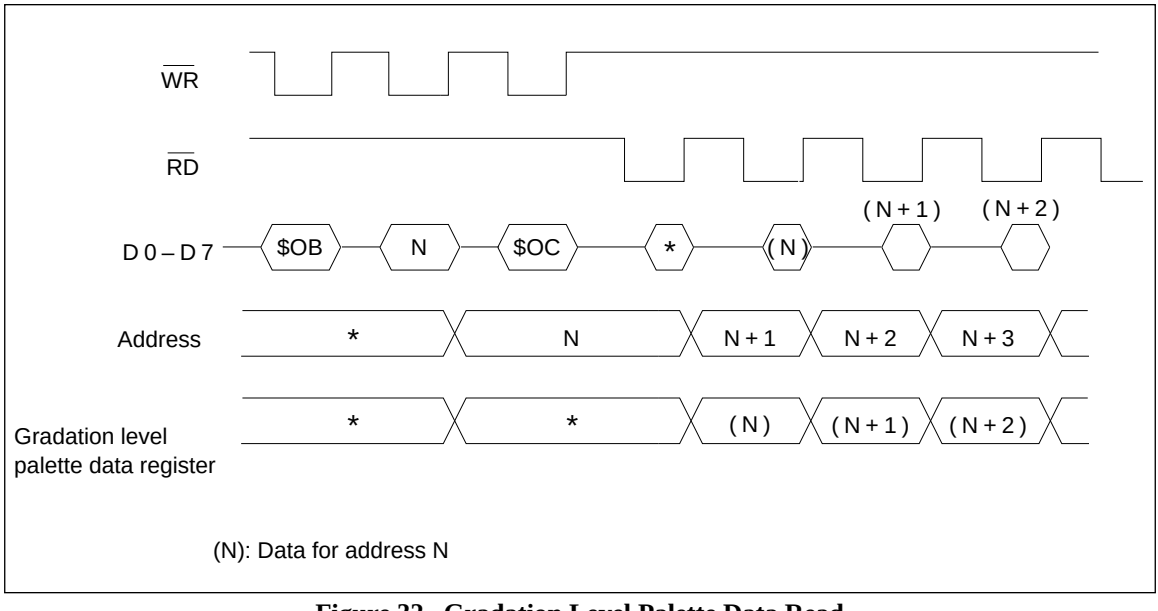


Figure 32 Gradation Level Palette Data Read

Gradation Display Clock Period Register: The gradation display clock period register (figure 33), composed of nine valid bits, specifies the period of XCL1, the LCD data latch clock, when pulse width modulation method is used for gradation display. The value to write to this register is "specified number – 1," in units of dots. Eight through 512 dots can be specified. Note that this register is invalid in with-memory mode.

This register is set automatically in VGA mode.

- GC8–GC0 bits: Specify the number of dots for T1; T1 is the period of XCL1 for 1/2 pulse width gradation display. When the total number of dots for one period of the YCL1 clock pulse cannot be divided by two for 1/2 pulse width gradation display, the remainder is added to T1 as T1', where T1' = T_L – T1 (figure 34).

R13

Data bit	7	6	5	4	3	2	1	0
Value	—	—	—	—	—	—	—	GC8

Data bit	7	6	5	4	3	2	1	0
Value	GC7	GC6	GC5	GC4	GC3	GC2	GC1	GC0

R14

Figure 33 Gradation Display Clock Period Register

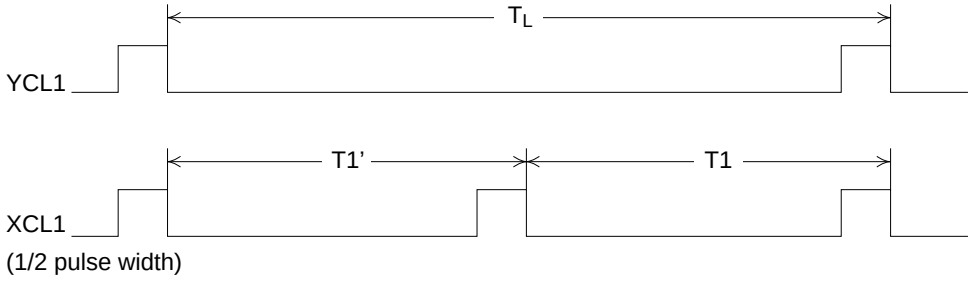


Figure 34 T_L, T1, and T'

Reset Description

The $\overline{RES}$ signal resets and starts the CLINE. The $\overline{RES}$ signal must be supplied at each power-on. Reset is defined as shown in figure 35.

Pin: In principle, the $\overline{RES}$ signal does not control output signals and it operates regardless of other input signals. The reset states of input/output pins are described below.

- D0–D7: Not affected by reset. These pins output data even during the reset state when $\overline{RD}$ = 0, $\overline{CS}$ = 0, RS = 1, and $\overline{WR}$ = 1, in the MPU programming method.
- A0–A5: Always output 0s during the reset state in the ROM programming method. Otherwise, these pins serve as input pins.

Registers: The contents of all internal registers are lost and cleared; the desired data must be rewritten after reset.

Palettes: Palettes are automatically loaded after reset with the appropriate data according to the display mode. When data different from the automatically set data is needed, the data must be overwritten 100 µs or more after reset. (100 µs is required for automatic data setting.)

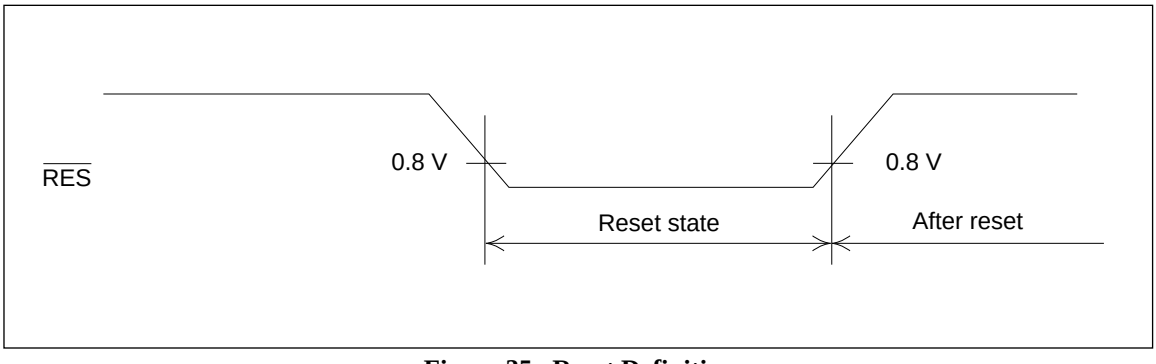


Figure 35 Reset Definition

There are some restrictions and notices in the HD66850F. Please check the following content, and use it.

Input Signal Timing

HSYNC, VSYNC Asserted Width: The HSYNC and VSYNC input signals have the minimum asserted width to operate correctly, please keep the asserted width with the below value or more.

HSYNC to VSYNC, HSYNC to $\overline{\text{BLANK}}$ Phase Shift: There are some restrictions between HSYNC and VSYNC, and HSYNC and $\overline{\text{BLANK}}$. Don't input them within the restricted phase shift.

Table 16 HSYNC, VSYNC Asserted Width

Condition	Item	Symbol	Minimum Dots
All mode	Asserted HSYNC	a	12 dots or more
	Asserted VSYNC	b	2 rasters or more

Table 17 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

Condition	Item	Symbol	Available Dots
All mode	VSYNC	c	3 dots or less, 16 dots or more
	BLANK	d	1 dot or more

Note: In VGA mode, the polarities of HSYNC and VSYNC depend on the display resolution on CRT, but we will explain them as the active-high input in this document.

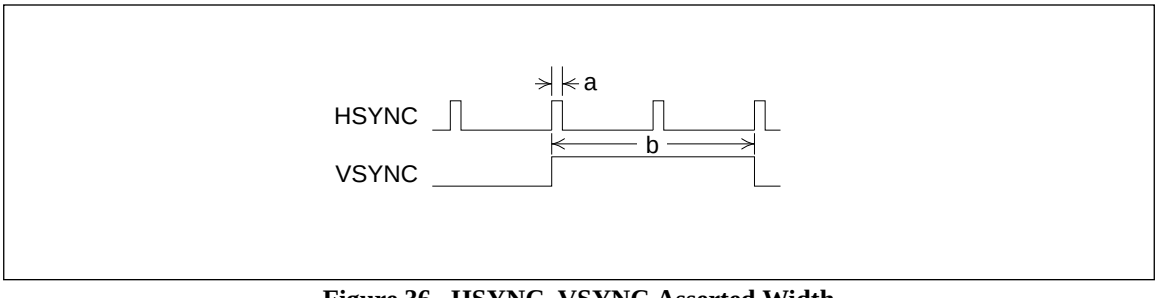


Figure 36 HSYNC, VSYNC Asserted Width

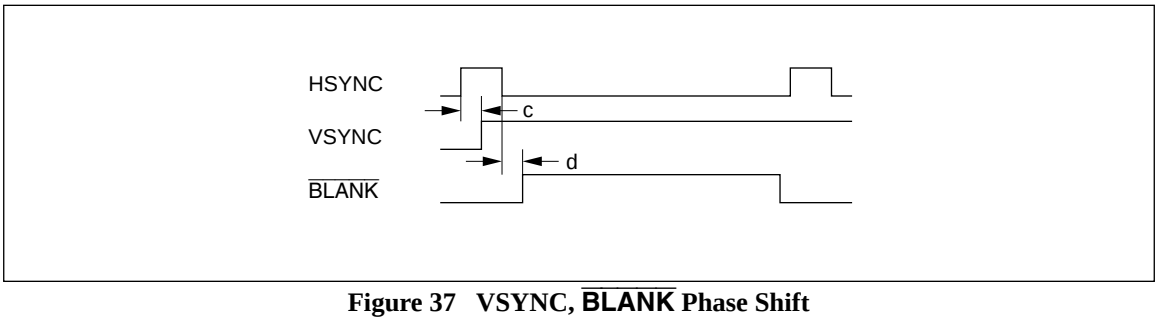


Figure 37 VSYNC, $\overline{\text{BLANK}}$ Phase Shift

Total Horizontal Dots: HD66850F needs 48 dots for the horizontal retrace period, and the HSYNC period must be 688 dots or more when 640 dots display, 768 dots or more when 720 dots display.

Horizontal Front Porch: There is a restriction about the horizontal front porch (from negated $\overline{\text{BLANK}}$ to asserted HSYNC) as the below in VGA mode. Please input them with the minimum value or more. Especially in 320 or 360 dots wide, period of the front porch is usually just 3 or 4 dots. Please delay HSYNC asserted timing, and hold the minimum value. Otherwise the first line on a panel will be incorrect.

Table 18 Total Horizontal Dots

Condition	Symbol	Minimum Dots
All mode	e	688 dots (when 640 dots display)
		768 dots (when 720 dots display)

Table 19 Horizontal Front Porch

			Dot Adjust								
Condition	Symbol	Item	–2	–1	±0	+1	+2	+3	+4	+5	+6
VGA mode	f	Horizontal 320 or 640 dots display	1 dot or more				3 dots or more				7 dots or more
		Horizontal 360 or 720 dots display	1 dot or more					5 dots or more			

Note: The BLANK 'High' width (g) must be 328 or 336 dots in 320 dots display, 376 dots in 360 dots display, 656 dots in 640 dots display, and 738 dots display in 720 dots display.

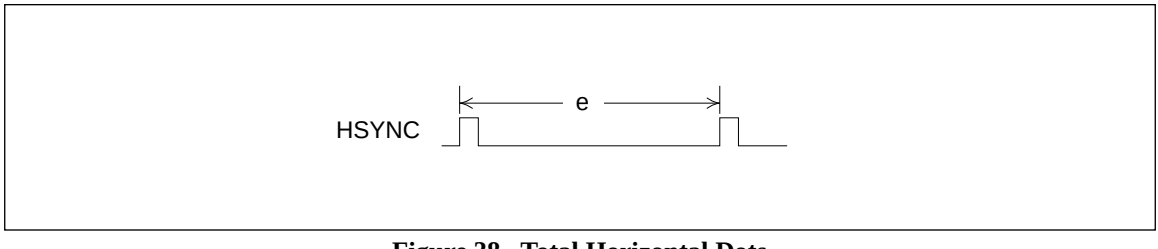


Figure 38 Total Horizontal Dots

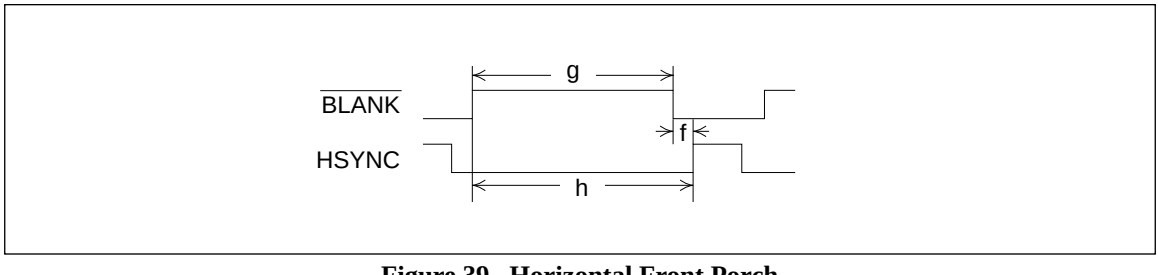


Figure 39 Horizontal Front Porch

When it displays 720 dots wide (text mode) on 640 dots panel in VGA mode, HD66850F removes 1 dot from each 9 dots. It may not display correctly according to the combination of the dot ajust and the period from negated $\overline{\text{BLANK}}$ to asserted HSYNC (h in figure 4). In this case, please change the dot adjust, or delay asserted timing of HSYNC.

This restriction causes trouble when the below equation is satisfied. When the total horizontal dot is 900 dots wide, and the period between negated $\overline{\text{BLANK}}$ to asserted HSYNC is 'h' dots,

$$4 \times [(h - 2)/4 \uparrow] = 9 \times M + A$$

($\uparrow$: revaluation, M and A: integer)

The 'A' which causes trouble depends on the dot ajust as below.

Table 20 Display Period + Horizontal Front Porch

Condition	Symbol	Item		Dot Adjust –2	–1	±0	+1	+2	+3	+4	+5	+6
VGA mode & with buffer memory mode, 720 dots display on 640 dots panel	h	Monochrome or 8/16 colors mode	743 to 746 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			747 to 750 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			751 to 754 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			755 to 758 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG
			759 to 762 dots	ok	ok	ok	NG	ok	ok	ok	NG	ok
			763 to 766 dots	ok	ok	NG	ok	ok	ok	ok	NG	ok
		64/512/4096 colors mode	743 to 764 dots	ok	NG	ok	ok	ok	ok	NG	ok	ok
			747 to 750 dots	ok	NG	ok	ok	ok	NG	ok	ok	ok
			751 to 754 dots	NG	ok	ok	ok	ok	NG	ok	ok	ok
			755 to 758 dots	NG	ok	ok	ok	NG	ok	ok	ok	ok
			759 to 762 dots	ok	ok	ok	ok	NG	ok	ok	ok	NG
			763 to 766 dots	ok	ok	ok	NG	ok	ok	ok	ok	NG

Note: The total horizontal dot must be 900 dots wide.

Parameter	Item	Dot Adjust –2	–1	±0	+1	+2	+3	+4	+5	+6
A	Monochrome or 8/16 colors mode	1	2	3	4	5	6	7	8	0
		6	7	8	0	1	2	3	4	5
	64/512/4096 colors mode	0	1	2	3	4	5	6	7	8
		5	6	7	8	0	1	2	3	4

Automatic Judgement of VGA Display Resolution: In VGA mode, HD66850 judges the current display resolution from the polarities of VSYNC, and HSYNC, and the width of $\overline{\text{BLANK}}$ 'H' automatically. Please input these signals as below to judge the correct resolution.

Table 21 $\overline{\text{BLANK}}$ 'High' Level Width

Condition	Symbol	VGA Mode No.	Horizontal Resolution	$\overline{\text{BLANK}}$ H Width
VGA mode	j	0/1	360 wide	378 dots
		2/3, 7	720 wide	738 dots
		4/5	320 wide	336 dots
		6, F, 10, 11, 12	640 wide	656 dots
		13 (256 col)	320 wide	328 dots

Table 22 Polarities of HSYNC and VSYNC

Condition	VGA Mode No.	Vertical Resolution	HSYNC	VSYNC
VGA mode	F, 10	350 raster high	Positive	Negative
	0/1, 2/3, 4/5, 6, 7, 13	400 raster high	Negative	Positive
	11, 12	480 raster high	Negative	Negative

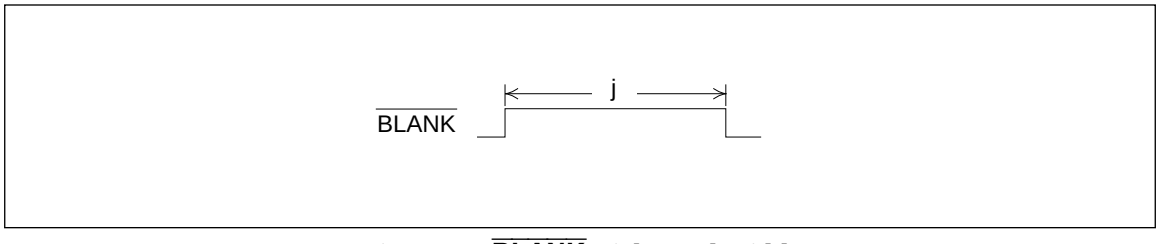


Figure 40 $\overline{\text{BLANK}}$ High Level Width

Border Area: In VGA mode, there is border area around display area. When the border and display area is scanned, $\overline{\text{BLANK}}$ is 'high' level. HD66850 internally generates the display timing which indicates just the display area from $\overline{\text{BLANK}}$ input. So, please input the $\overline{\text{BLANK}}$ with the horizontal border dot wide and vertical border high raster as below.

Table 23 Number of Horizontal Border Dot

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	k	0/1	360	9 dots
		2/3, 7	720	9 dots
		4/5	320	8 dots
		6, F, 10, 11, 12	640	8 dots
		13 (256 col)	320	4 dots

Table 24 Number of Vertical Border Raster

Condition	Symbol	VGA Mode No.	Resolution	Border
VGA mode	m	F, 10	350	6 rasters
		0/1, 2/3, 4/5, 6, 7, 13	400	7 rasters
		11, 12	480	8 rasters

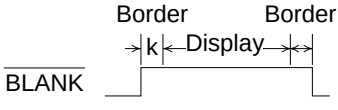


Figure 41 Number of Horizontal Border Dot

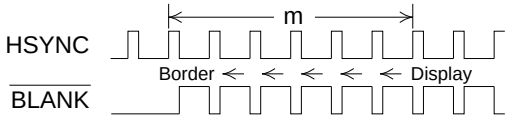


Figure 42 Number of Vertical Border Raster

When 64 k × 4 bit (256 k) or 128 k × 8 (1M) bit memory is attached for buffer memory, please satisfy the below relationship about vertical display and border raster.

$$\left[\begin{array}{l}\text{Vertical}\\ \text{display raster}\end{array}\right] + \left[\begin{array}{l}\text{Vertical border}\\ \text{raster after display}\end{array}\right] \leq \begin{array}{l}512\\ \text{raster}\end{array}$$

Usually, the vertical 480 rasters mode (VGA mode 11, 12) has 6 or 7 border rasters, so this limitation will be no problem.

Table 25 Vertical Display Raster + Vertical Border Raster After Display

Condition	Symbol	Vertical Display Raster + Vertical Border Raster after Display
VGA and with memory mode	n	512 rasters or less

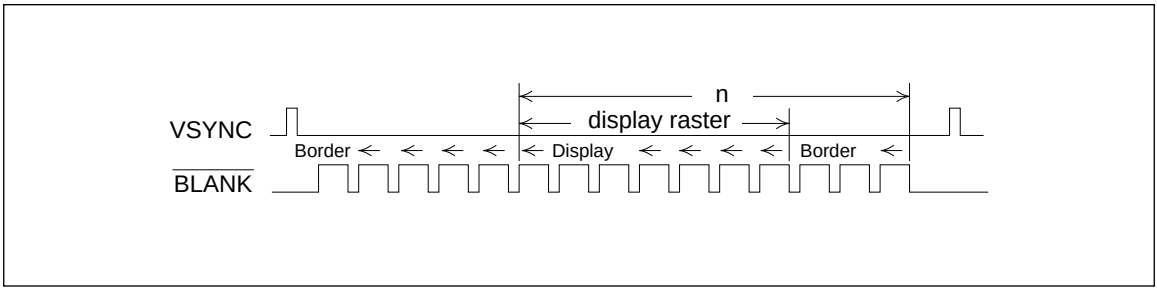


Figure 43 Vertical Display Raster

Asynchronous Mode

In asynchronous mode, the set data in the gradation palette is broken owing to the dot adjust during display. To avoid this problem, in MPU and ROM programming method, please write '1' to bit 4 (BM mode) of the border control register (R7), and all '0' to bit 3-0 (border color) of R7. The register R7 must be '10H'. In pin programming method, please adjust display timing with AJ3-AJ0 pins, and start to display just from left edge on an LCD panel without border dot, rise the $\overline{\text{BLANK}}$ input at same DOTCLK edge as change of the video data (R/G/B).

In 8/16 colors mode, this restriction is no problem in any mode because HD66850F does not access the gradation palette. In 64 / 512 / 4096 colors mode, it does not support asynchronous mode.

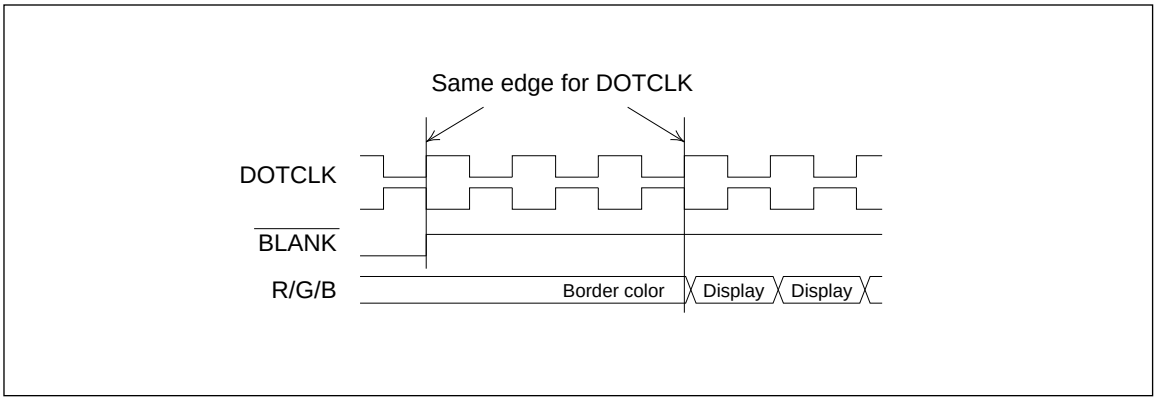


Figure 44 Countermeasure in the Pin Programming Method

Frame Period

In synchronous with-memory mode, DOTCLK and frame period for CRT are same as one for LCD. When it displays on a full screen with stretching or centering function, HD66850F needs to extend the frame period for displaying on LCD. If this frame period for LCD were longer than one for CRT, HD66850F can not work correctly.

HD66850F needs 48 dots period for the horizontal retrace, and number of the total horizontal dot for LCD is number of the horizontal display dot + 48 dots. This minimum frame period which is necessary to display on LCD is shown as below.

$$\text{Minimum frame period for LCD} = (\text{Number of horizontal display dot} + 48) \times \text{Vertical panel size [dots]}$$

The frame period for CRT must be longer than the above minimum one for LCD.

For example, when HD66850F stretchs CRT resolution with 640 × 350 dots to the LCD panel with 640 × 480 dots, the minimum frame period for LCD is (640 + 48) × 480 = 330, 240 dots.

On the other hand, when number of the total horizontal dot for CRT is 800 dots wide, 330, 240/800 = 412.8 rasters, so HD66850F needs 413 or more rasters high as the total vertical raster for CRT.

In asynchronous mode, HD66850F separates LCD clock (LDOTCK) from CRT clock (DOTCK), and the both frame period are different. So, this limitation is no problem.

LCD Alternating Signal M

When LCD alternating signal M is changed at same line in each frame, brightness of the line differs from one of another line. To avoid this problem, the signal M is ususally controlled to change at different line in each frame. But period of the signal M may synchronize with the frame period according to the total vertical raster. In this case, adjust period of the M, and don't synchronize them.

Especially, it is easy to synchronize them in VGA 720 × 400 dots mode. For example, when it displays 720 × 400 dots in synchronous with-memory mode, usaually number of the total horizontal dot for CRT is 900 dots wide, and number of the total vertical raster is 448 rasters high, so the frame period for CRT is 900 × 448 = 403,200 [dots]. On the other hand, number of the total horizontal dot for LCD is 720 + 48 = 768 dots wide, and the frame period (403,200 dots) divided by a total horizontal dot for LCD (768 dots) is 512 which is interger. So, when line number of period of the M equals to the following divisor of 512:

[1, 3, 5, 7, 15, 21, 25, 35, 75, 105, 175] (lines),

period of the M synchronizes with the frame period, and a horizontal bright line is appeared when the M is changed.

Vertical Centering

Number of vertical centering line depends on 'the value in register (R5) + 1' in non-VGA mode, or on the VSIZE pin and display resolution in VGA mode. But when '0' is written in the register (R5) and the vertical centering is enabled, HD66850F can not works correctly. Don't set '0' in the register (R5). And when number of vertical display raster is same as the vertical panel size (VSIZE), the vertical centering enable bit (bit 3 in R0) must be cleared. Especially in VGA mode, please update the enable bit according to selected VGA display mode.

When stretching function is selected, there is no restriction about setting '0' in the stretching registers (R8, R9, R10).

Table 26 Notes on VGA Mode Usage by LCD Panel Size

Horizontal Size (dots)	Vertical Size (lines)	Notes
640	—	• In VGA text modes (0/1, 2/3, 7), there is no space between characters.
720	—	• In VGA graphic modes (4/5, 6, F, 10, 11, 12, 13), horizontal centering is necessary. (Display is automatically centered horizontally in with-memory mode. See note below.)
—	400	• Data on line 401 through line 480 in VGA 640-by-480 graphic modes (11, 12) are not displayed. • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)
—	480	• Vertical centering or stretching is necessary for VGA text modes (0/1, 2/3, 7). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-200 or 320-by-200 graphic modes (4/5, 6, 13). (Display is automatically stretched in with-memory mode. See note below.) • Vertical centering or stretching is necessary for VGA 640-by-350 graphic modes (F, 10). (Display is automatically stretched in with-memory mode. See note below.)

Note: For without-memory mode, external circuits or BIOS tuning are required.

Table 27 Notes on Internal Register Settings

Register No.	Bits	Register or Bit Function	Notes	
			VGA	Non-VGA
R0	STE	Stretching enable	1	1
R0	CRE	Vertical centering enable	2	2
R0	CCE	Horizontal centering enable	3	4
R0	SP	Double-width display set	5	4
R0	DISPON	Display on	6	6
R1	DOTE	Dot clock phase select	4	4
R1	AJ3–AJ0	Display timing adjust	4	4
R2	DH6–DH0	Display horizontal size set	7	4
R3–R4	DV8–DV0	Display vertical size set	8	4
R5	CR7–CR0	Centering raster set	8	4
R6	CC4–CC0	Centering character set	3	4
R7	BM	Border control mode select	9	9
R7	BCI, BCR, BCG, BCB	Border color select	10	10
R8	SF3–SF0	Stretching period	8	4
R9–R10	SI15–SI0	Stretching index set	—	—
R11	PS1–PS0	Gradation display palette select	11	11
R11	PA3–PA0	Gradation display palette address set		
R12	PD5–PD0	Gradation level palette data set		
R13–R14	GC8–GC0	Gradation display clock period set	7	12

Notes:
1. Simultaneous use with vertical centering function is impossible.
2. Simultaneous use with stretching function is impossible.
3. Automatically set for a 640- or 320-dot-wide display on a 720-dot-wide LCD panel; cannot be rewritten.
4. Must be set after reset.
5. Automatically set for a middle-resolution display; cannot be rewritten.
6. Display will turn on four frames after reset. Display will not turn on during four frames after reset.
7. Automatically set according to the horizontal panel size and number of displayed horizontal dots; cannot be rewritten.
8. Automatically set according to the vertical panel size and polarity of HSYNC and VSYNC signals; cannot be rewritten.
9. Available only in with-memory mode.
10. Available only in asynchronous with-memory mode.
11. In the MPU programming method, automatically set for 16-level display after reset; can be rewritten 100 µs after reset. In ROM programming method, appropriate data must be written.
12. In with-memory mode, automatically set according to the horizontal panel size and number ofdisplayed horizontal dots; cannot be rewritten. For without-memory mode, appropriate data must be written after reset.

Table 28 Limits on Register Values

Register Function	Applied to	Limits
Horizontal display size control	R2	$4 \le Nchd \le (R2 + 1) \le 90$ (HSIZE = 1) $4 \le Nchd \le (R2 + 1) \le 80$ (HSIZE = 0)
Vertical display size control	R3, R4	$4 \le Ncvd \le (R3, R4 + 1) \le 512$
Vertical centering	R3, R4, R5	$2 \le (R5 + 1) \le 256$ $(R5 + 1) \times 2 + Ncvd = (R3, R4 + 1)$
Horizontal centering	R2, R6	$2 \le (R6 + 1) \le 32$ $(R6 + 1) \times 2 + Nchd = (R2 + 1)$
Gradation display clock period control	R13, R14	$(R13, R14 + 1) = (Ncht \times 8)/n$ (MMODE1 = 1) n: 2 for 1/2 pulse width gradation display $(R2 + 1) + 8 \le Ncht$ (NMODE1 = 0)
Miscellaneous	R2, R3, R4	$1/2f_{DOTCLK} \le \{(R + 1) + 6\} \times 8 \times (R3, R4 + 1) \times f_{FLM} \le 2f_{DOTCLK}$ (SYNC = 0)

Ncht: Total number of characters on a CRT horizontal line
(total number of dots on a CRT horizontal line × 1/8)

Nchd: Number of characters displayed on a CRT horizontal line
(number of dots displayed on a CRT horizontal line × 1/8)

Ncvd: Number of lines displayed from screen top to bottom on the CRT display

f_{LDOTCK}: LCD dot clock frequency

f_{DOTCLK}: CRT dot clock frequency

f_{FLM}: Frame frequency

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Power supply voltage	V_{CC}	–0.3 to 7.0	V
Input voltage	Vin	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}	–20 to +75	°C
Storage temperature	T_{stg}	–55 to +125	°C

Notes: 1. Permanent LSI damage may occur if maximum ratings are exceeded.
Normal operation should be under recommended operating conditions (V_{CC} = 5.0 ± 10%, GND = 0V, Ta = –20°C to +75°C. (If these conditions are exceeded, LSI reliability may be affected.
2. All voltages are referenced to GND = 0 V.

Electrical Characteristics

DC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Item		Symbol	Min	Max	Unit	Test Condition
Input high-level voltage	$\overline{RES}$ pin	V_{IH}	V_{CC} – 0.5	—	V	
	DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4		2.2	—	V	
	Other input pins*1		2.0	—	V	
Input low-level voltage		V_{IL}	—	0.8	V	
Output high-level voltage	TL interface pins*2	V_{OH}	2.4	—	V	I_{OH} = –200 µA
	CMOS interface pins*3		V_{CC} –0.8	—	V	I_{OH} = –200 µA
Output low-level voltage	TTL interface pins*2	V_{OL}	—	0.4	V	I_{OL} = 1.6 mA
	CMOS interface pins*3		—	0.8	V	I_{OL} = 200 µA
Input leakage current		I_{TL}	–2.5	+2.5	µA	
Three-state leakage current		I_{TSL}	–10.0	10.0	µA	
Current consumption		I_{CC}	—	100	mA	Output pins open

Notes: 1. Other input pins: DOTCLK, HSYNC, VSYNC, $\overline{BLANK}$, MS0–MS15, LDOTCK, D0–D7, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, R0–R3, G0–G3, B0–B3, PMODE1, PMODE0, LMODE0–LMODE4, MMODE1, MMODE0, SYNC, VMODE, VSIZE, HSIZE, TEST1, TEST0
2. TTL interface output pins: D0–D7, DOTE/$\overline{RD}$/A5, SP/$\overline{WR}$/A4, AJ3/$\overline{CS}$/A3, AJ2/RS/A2, AJ1/A1, AJ0/A0, MD0–MD15, MA0–MA7, MA8/$\overline{SOE1}$, $\overline{SOE0}$, $\overline{WE}$, DT/$\overline{OE}$, $\overline{RAS1}$, $\overline{RAS0}$, $\overline{CAS}$, $\overline{CASL}$, SC
3. CMOS interface output pins: UD0–UD7, LD0–LD7, XCL1, YCL1, CL2, FLM, M, SCLK, DISPON, DATAE

AC Characteristics (V_{CC} = 5.0 V ± 10%, GND = 0 V, Ta = –20 to +75°C, unless otherwise specified)

Video interface

No.	Item	Symbol	Min	Max	Unit	Reference
1	DOTCLK cycle time	T_{CYCD}	31.2	62.5	ns	Figure 45
2	DOTCLK low-level pulse width	t_{WDL}	15	—	ns	
3	DOTCLK high-level pulse width	t_{WDH}	15	—	ns	
4	DOTCLK rise time	t_{Dr}	—	5	ns	
5	DOTCLK fall time	t_{Df}	—	5	ns	
6	Video data setup time	t_{VDS}	10	—	ns	
7	Video data hold time	t_{VDH}	10	—	ns	
8	$\overline{\text{BLANK}}$ setup time	t_{BLS}	10	—	ns	
9	$\overline{\text{BLANK}}$ hold time	t_{BLH}	10	—	ns	
10	$\overline{\text{BLANK}}$ low-level pulse width	t_{BLW}	—	12	µs	
11	$\overline{\text{BLANK}}$ phase shift	t_{BLPD}	2Tc	—	ns	
12	Phase shift setup time	t_{PDS}	2Tc	—	ns	
13	Phase shift hold time	t_{PDH}	2Tc	—	ns	

Tc: DOTCLK cycle time

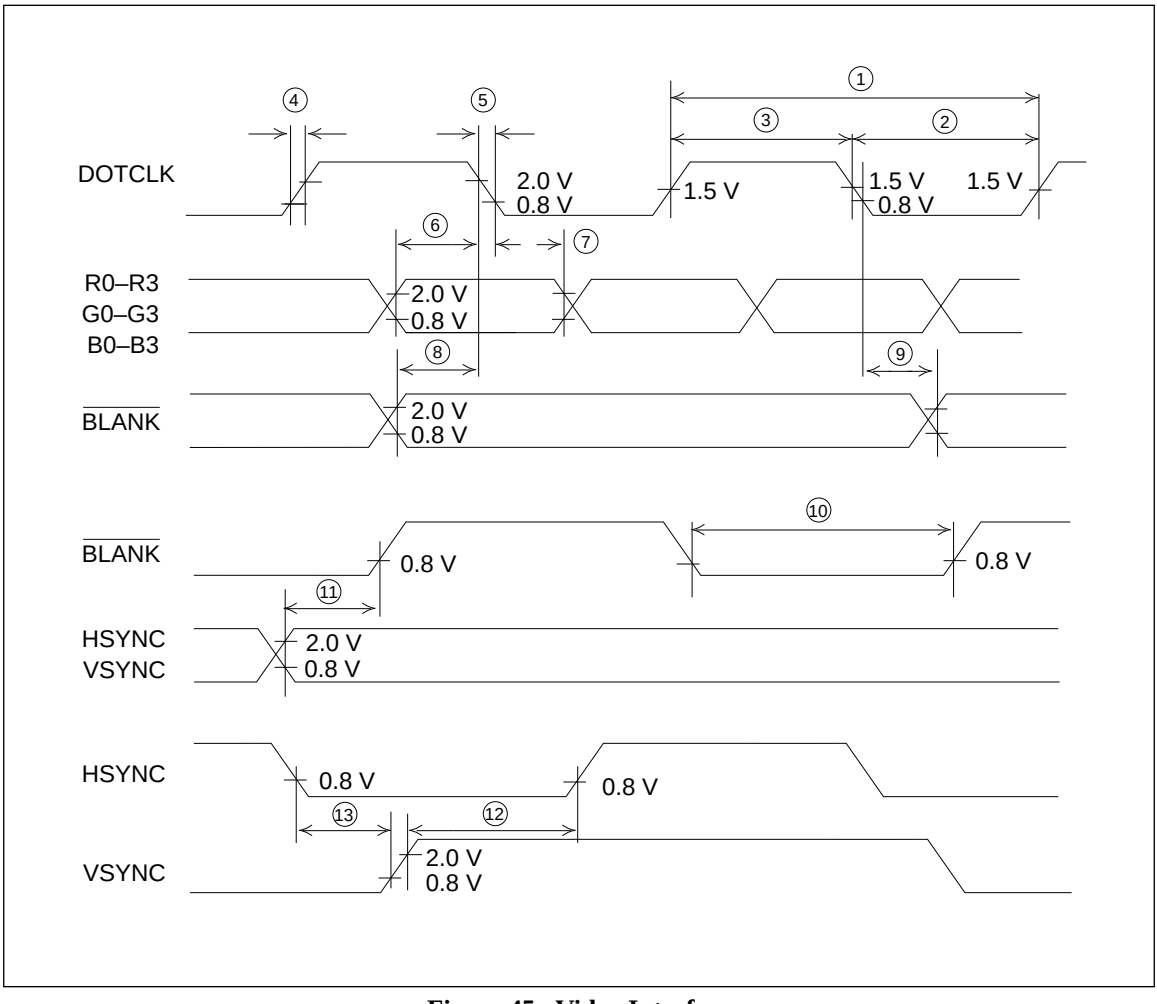


Figure 45 Video Interface

Memory Interface

No.	Item	Symbol	Min	Max	Unit	Reference
14	$\overline{RAS}$ cycle time	t_{RC}	12Tc – 10	—	ns	Figure 46
15	$\overline{RAS}$ low-level pulse width	t_{RAS}	5Tc	128Tc – 20	ns	
16	$\overline{RAS}$ high-level pulse width	t_{RP}	4Tc – 40	—	ns	
17	$\overline{CAS}$ hold time	t_{CSH}	6Tc – 50	—	ns	
18	$\overline{RAS}$, $\overline{CAS}$ delay time	t_{RCD}	3Tc – 40	—	ns	
19	$\overline{CAS}$ low-level pulse width	t_{CAS1}	3Tc – 35	—	ns	
20	$\overline{CASL}$ low-level pulse width	t_{CAS2}	2Tc – 30	—	ns	
21	$\overline{CAS}$ high-level pulse width	t_{CP1}	1Tc – 20	—	ns	
22	$\overline{CASL}$ high-level pulse width	t_{CP2}	2Tc – 20	—	ns	
23	$\overline{CAS}$ cycle time	t_{PC}	4Tc – 20	—	ns	
24	$\overline{RAS}$ hold time	t_{RSH}	4Tc – 40	—	ns	
25	Row address setup time	t_{ASR}	2Tc – 50	—	ns	
26	Row address hold time	t_{RAH}	2Tc – 30	—	ns	
27	Column address setup time	t_{ASC}	1Tc – 30	—	ns	
28	Column address hold time	t_{CAH}	2Tc – 40	—	ns	
29	$\overline{WE}$ setup time	t_{WS}	2Tc – 50	—	ns	
30	$\overline{WE}$ hold time	t_{WH}	2Tc – 40	—	ns	
31	Memory data setup time	t_{MDS}	1Tc – 30	—	ns	
32	Memory data hold time	t_{MDH}	2Tc – 35	—	ns	
33	Data transfer $\overline{DT}/\overline{OE}$ setup time	t_{DTS}	2Tc – 50	—	ns	Figure 47
34	Data transfer $\overline{DT}/\overline{OE}$ hold time	t_{DTH}	6Tc – 50	—	ns	
35	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{CDH}	2Tc – 40	—	ns	
36	Phase shift between $\overline{CAS}$ and $\overline{DT}/\overline{OE}$	t_{DTR}	2Tc – 50	—	ns	
37	$\overline{CAS}$ setup time	t_{CSR}	2Tc – 50	—	ns	Figure 48
38	$\overline{CAS}$ hold time	t_{CHR}	6Tc – 50	—	ns	
39	Phase shift between $\overline{RAS}$ and $\overline{CAS}$	t_{RPC}	2Tc – 50	—	ns	
40	SC cycle time	t_{SCC}	$4T_L$ – 10	—	ns	Figure 49
41	SC high-level pulse width	t_{SC}	$2T_L$ – 50	—	ns	
42	SC low-level pulse width	t_{SCP}	$2T_L$ – 50	—	ns	
43	Memory data read setup time	t_{RDS}	40	—	ns	
44	Memory data read hold time	t_{RDH}	5	—	ns	
45	Phase shift between $\overline{SOE}$ and SC	t_{DSE}	20	—	ns	

T_C: DOTCLK cycle time
T_L: LDOTCK cycle time (= T_C for synchronous mode)

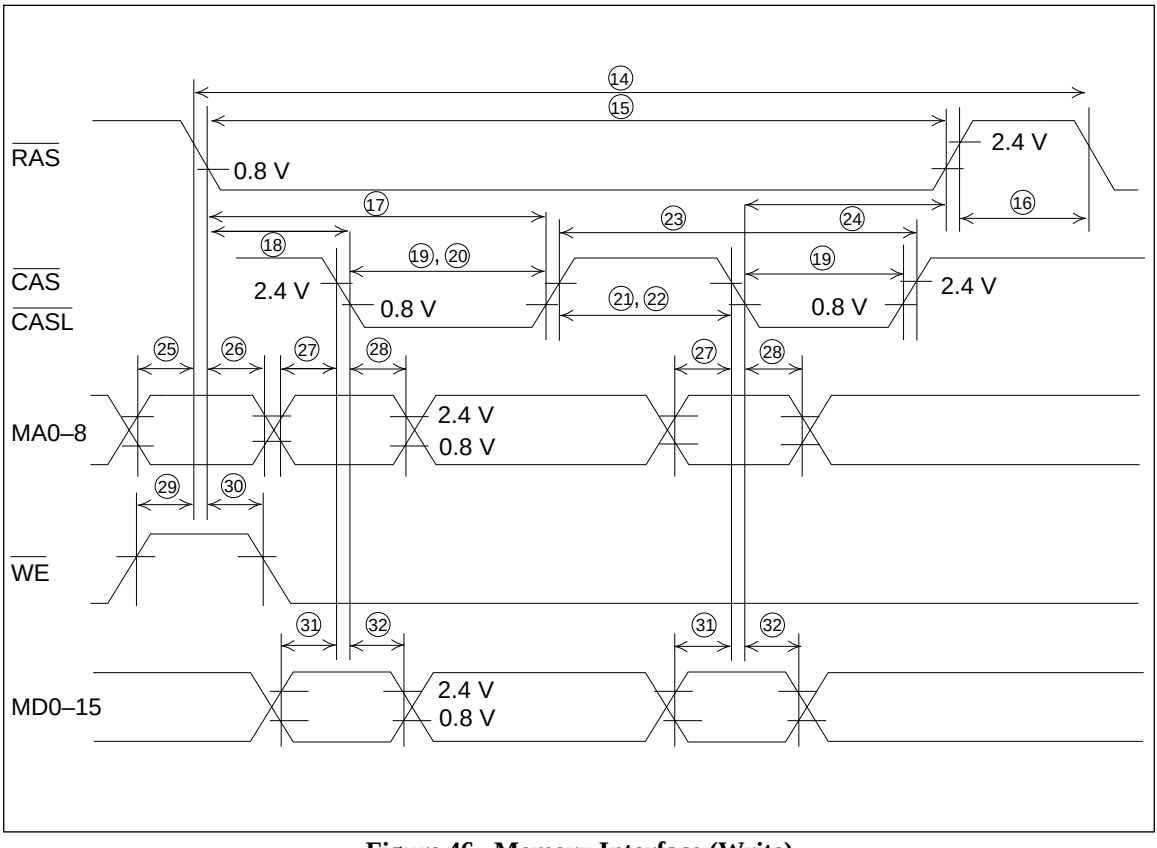


Figure 46 Memory Interface (Write)

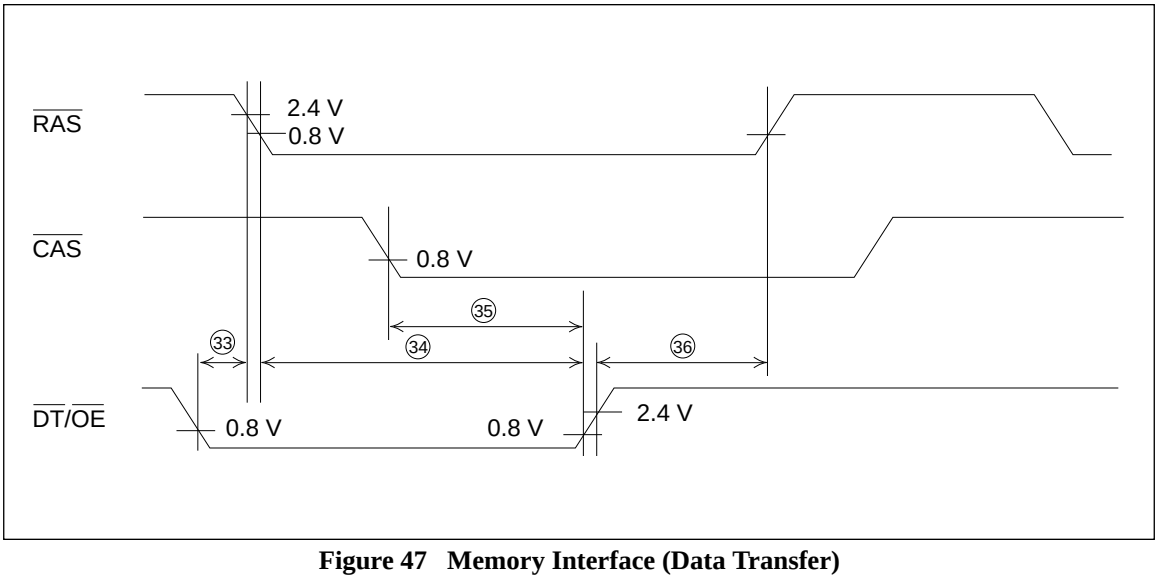


Figure 47 Memory Interface (Data Transfer)

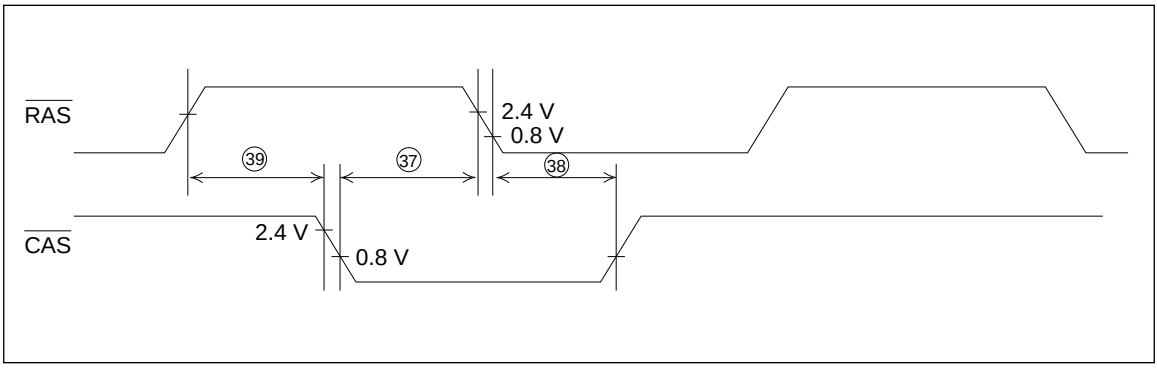


Figure 48 Memory Interface (Refresh)

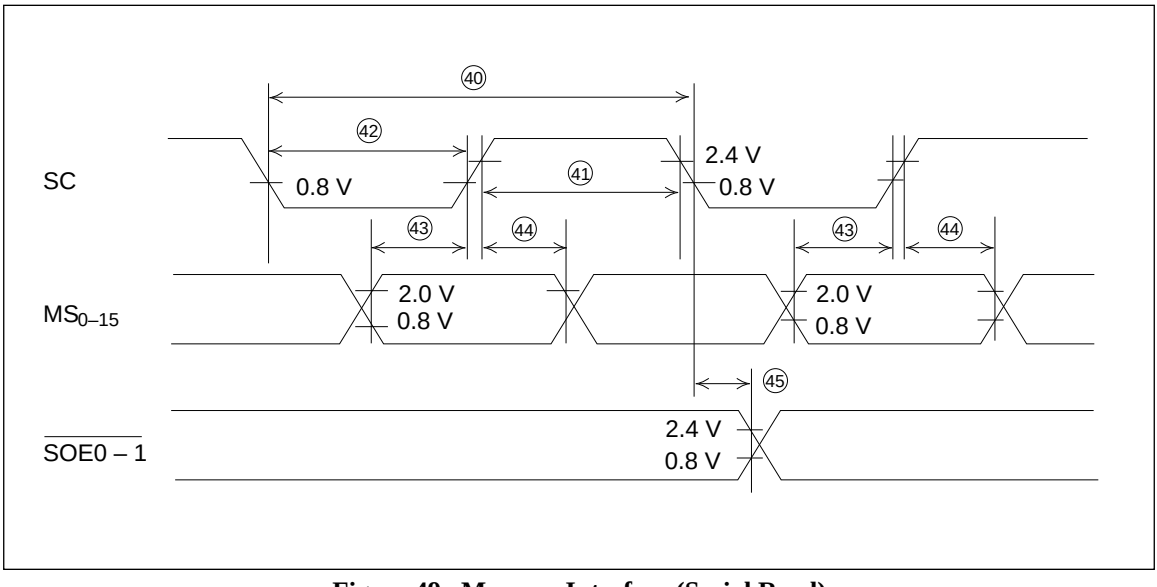


Figure 49 Memory Interface (Serial Read)

LCD Driver Interface

No.	Item	Symbol	Min	Max	Unit	Reference
46	CL2 cycle time	t_{WCL2}	$2T_L - 10$*1	—	ns	Figure 50
			$4T_L - 10$*2			
			$8T_L - 10$*3			
			$16T_L - 10$*4			
47	CL2 high-level pulse width	t_{WCL2H}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*2			
			$4T_L - 40$*3			
			$8T_L - 40$*4			
48	CL2 low-level pulse width	t_{WCL2L}	$1T_L - 40$*1	—	ns	
			$2T_L - 40$*1			
			$4T_L - 40$*2			
			$8T_L - 40$*4			
49	CL1 high-level pulse width	t_{WCL1h}	150	—	ns	
50	LCD data delay time	t_{DD}	—	30	ns	
51	CL1 setup time	t_{SCL1}	200	—	ns	
52	CL1 hold time	t_{HCL1}	200	—	ns	
53	M output delay time	t_{DM}	—	100	ns	
54	FLM setup time	t_{HF}	100	—	ns	
55	LDOTCK cycle time	t_{CYCL}	31.2	100	ns	
56	LDOTCK high-level pulse width	t_{WLH}	15	—	ns	
57	LDOTCK low-level pulse width	t_{WLL}	15	—	ns	
58	LDOTCK rise time	t_{Lr}	—	5	ns	
59	LDOTCK fall time	t_{Lf}	—	5	ns	

T_L: LDOTCK cycle time (= T_C for synchronous mode)

Notes: 1. For display modes 9, 13, 16, 19, and 20
2. For display modes 1, 5, 10, 11, 14, 15, 17, and 18
3. For display modes 2, 3, 6, 7, and 12
4. For display modes 4 and 8

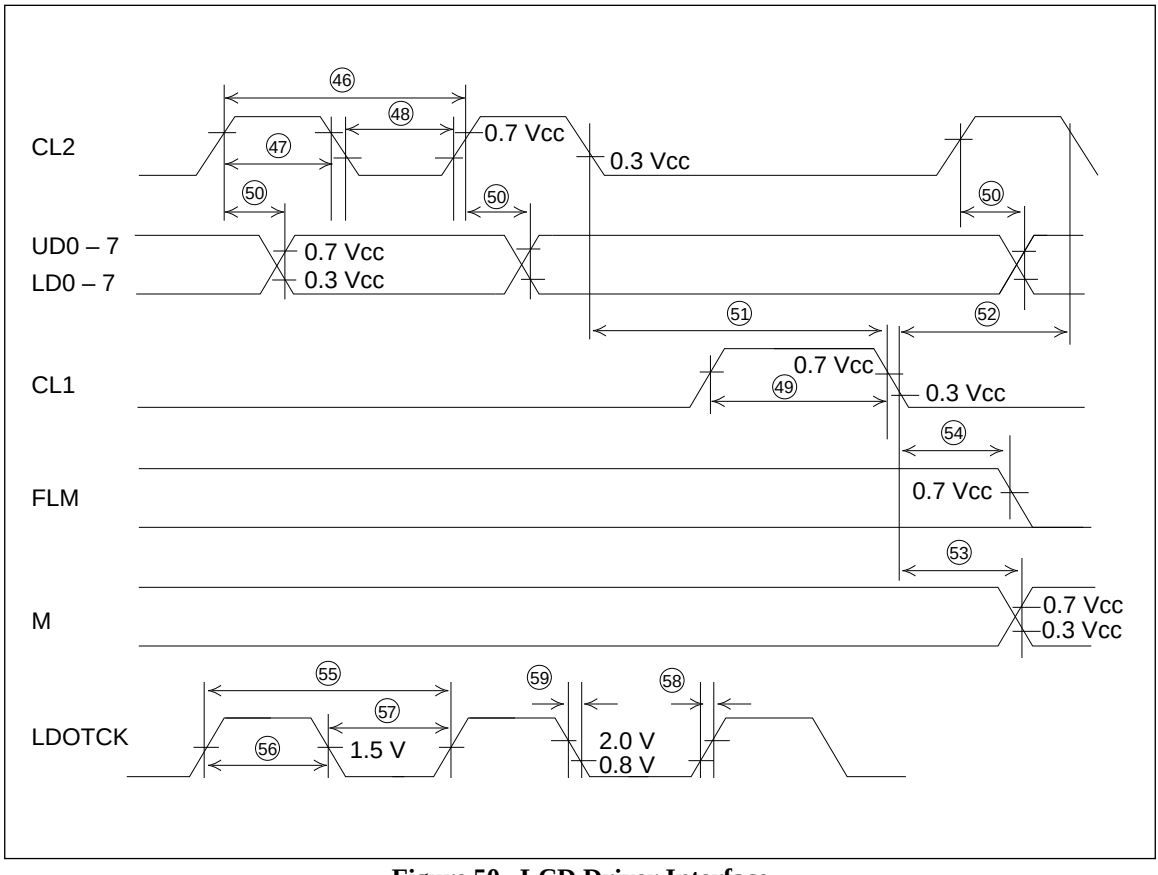


Figure 50 LCD Driver Interface

MPU Interface

No.	Item	Symbol	Min	Max	Unit	Reference
60	$\overline{RD}$ low-level pulse width	t_{WRDL}	$4T_C + 10$	—	ns	Figure 51
61	$\overline{RD}$ high-level pulse width	t_{WRDH}	$4T_C + 10$	—	ns	
62	$\overline{WR}$ low-level pulse width	t_{WWRL}	$4T_C + 10$	—	ns	
63	$\overline{WR}$ high-level pulse width	t_{WWRH}	$4T_C + 10$	—	ns	
64	$\overline{RD}$ input inhibited time	t_{RIH}	$4T_C + 10$	—	ns	
65	$\overline{WR}$ input inhibited time	t_{WIH}	$4T_C + 10$	—	ns	
66	Address setup time	t_{AS}	0	—	ns	
67	Address hold time	t_{AH}	0	—	ns	
68	Data delay time	t_{DDR}	—	100	ns	
69	Data output hold time	t_{DHR}	10	—	ns	
70	Data setup time	t_{DSW}	0	—	ns	
71	Data hold time	t_{DHW}	0	—	ns	

T_C: DOTCLK cycle time

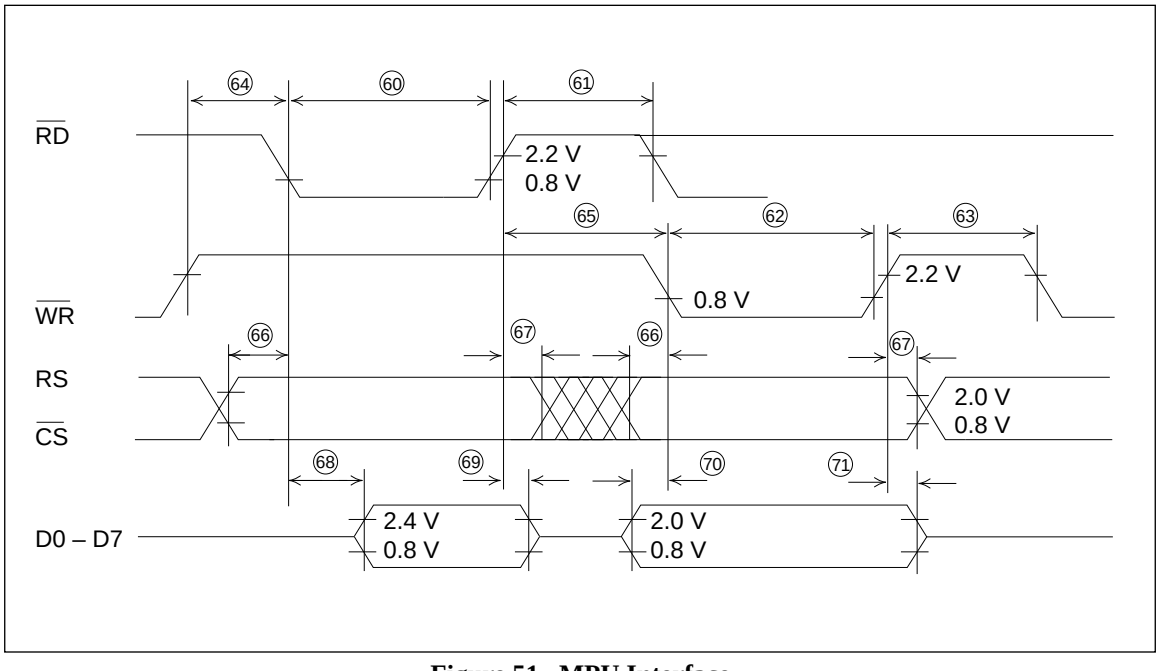


Figure 51 MPU Interface

ROM Interface

No.	Item	Symbol	Min	Max	Unit	Reference
72	ROM address cycle time	t_{CYCA}	$16T_C - 20$	—	ns	Figure 52
73	ROM data setup time	t_{DSWD}	150	—	ns	
74	ROM data hold time	t_{DHWD}	10	—	ns	

T_C: DOTCLK cycle time

RES Timing

No.	Item	Symbol	Min	Max	Unit	Reference
75	$\overline{RES}$ low-level pulse width	t_{RES}	1	—	µs	Figure 53

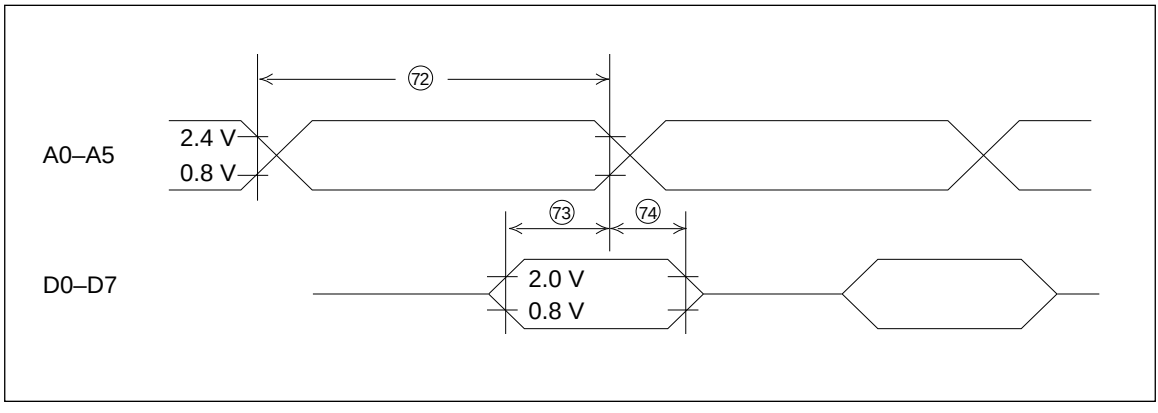


Figure 52 ROM Interface

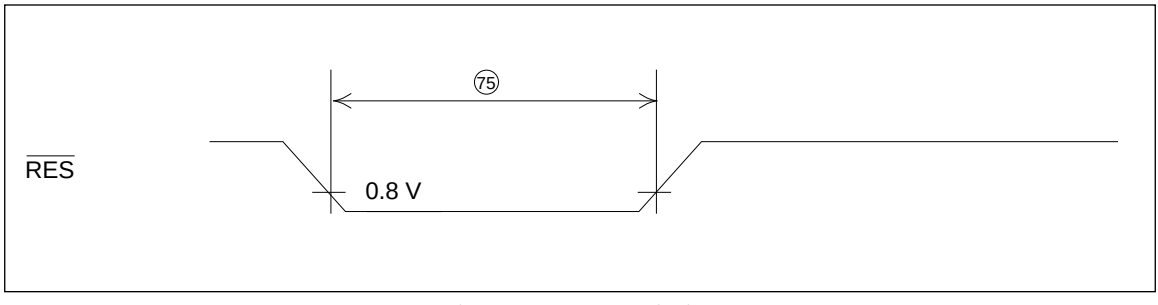
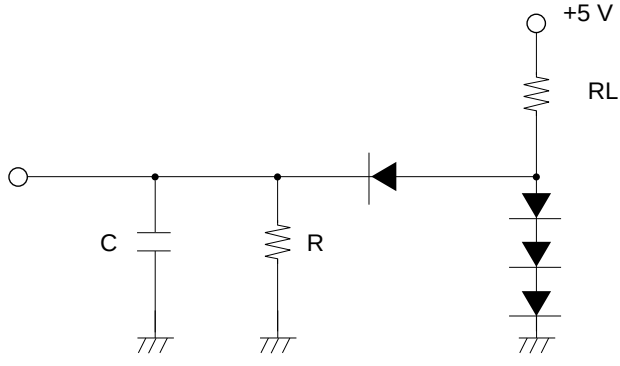


Figure 53 Reset Timing

Load Circuit

Pins	R_L	R	C	Reference
MA0 – MA7, MA8/$\overline{SOE1}$, $\overline{DT}$/$\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{CASL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{SOE0}$, MD0 – MD15, D0 – D7, A0/AJ0, A1/AJ1, A2/RS/AJ2, A3/$\overline{CS}$/AJ3, A4/$\overline{WR}$/SP, A5/$\overline{RD}$/DOTE	2.4 kΩ	11 kΩ	40 pF	Figure 54
DISPON, DATAE, SCLK, M, FLM, CL2, YCL1, XCL1, LD0 – LD7, UD0 – UD7	—	—	40 pF	Figure 55



C: 40 pF
R: 11 kΩ
RL: 2.4 kΩ

All diodes are 1S2074 (H)

Applicable pins: MA0–MA7, MA8/$\overline{SOE1}$, $\overline{DT}$/$\overline{OE}$, $\overline{WE}$, $\overline{CAS}$, $\overline{CASL}$, $\overline{RAS0}$, $\overline{RAS1}$, $\overline{SOE0}$, MD0–MD15, D0-D7, A0/AJ0, A1/AJ1, A2/RS/AJ2, A3/$\overline{CS}$/AJ3, A4/$\overline{WR}$/SP, A5/$\overline{RD}$/DOTE

Figure 54 TTL Load Circuit

Applicable pins: DISPON, DATAE, SCLK, M, FLM, CL2, YCL1, XCL1, LD0 – LD7, UD0 – UD7

Figure 55 Capacitive Load Circuit