HD74AC165

Parallel-Load 8-bit Shift Register

REJ03D0254–0200Z
(Previous ADE-205-374 (Z))
Rev.2.00
Jul.16.2004

Description

This 8-bit serial shift register shifts data from Q_A to Q_H when clocked, Parallel inputs to each stage are enabled by a low level at the Shift/Load Input. Also included is a gated clock input and a complementary output from the eighth bit.

Clocking is accomplished through a 2-input NOR gate permitting one input to be used as a clock inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the Shift/Load input high enables the other clock input. Data transfer occurs on the positive going edge of the clock. Parallel loading is inhibited as long as the Shift/Load input is high. When taken low, data at the parallel inputs is loaded directly into the register independent of the state of the clock.

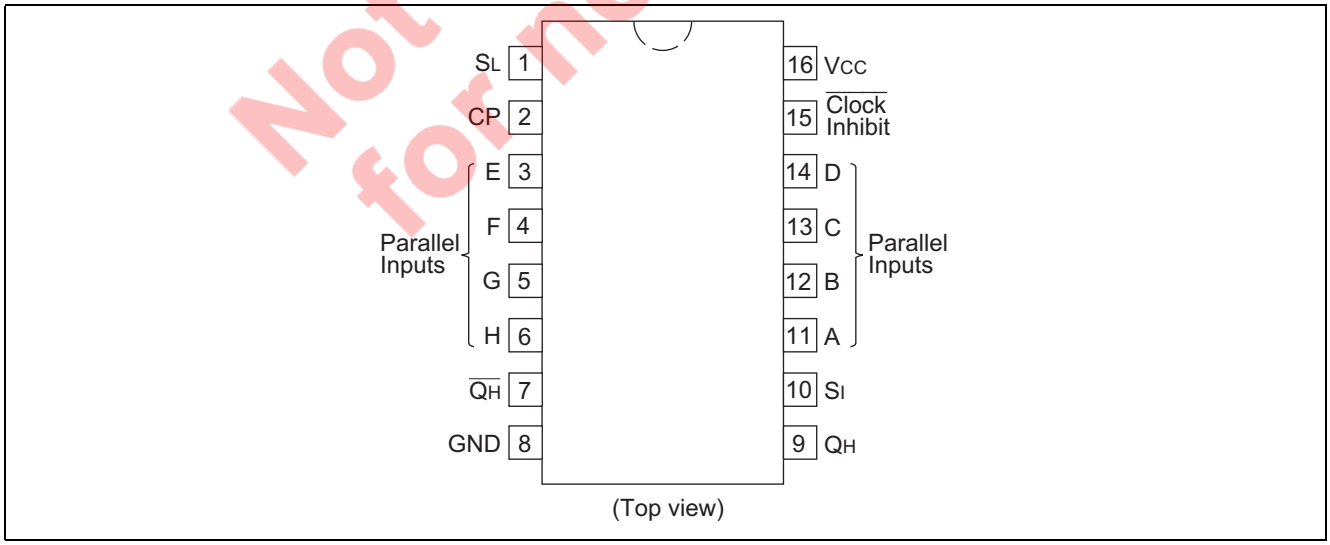
Features

- Outputs Source/Sink 24 mA
- Ordering Information

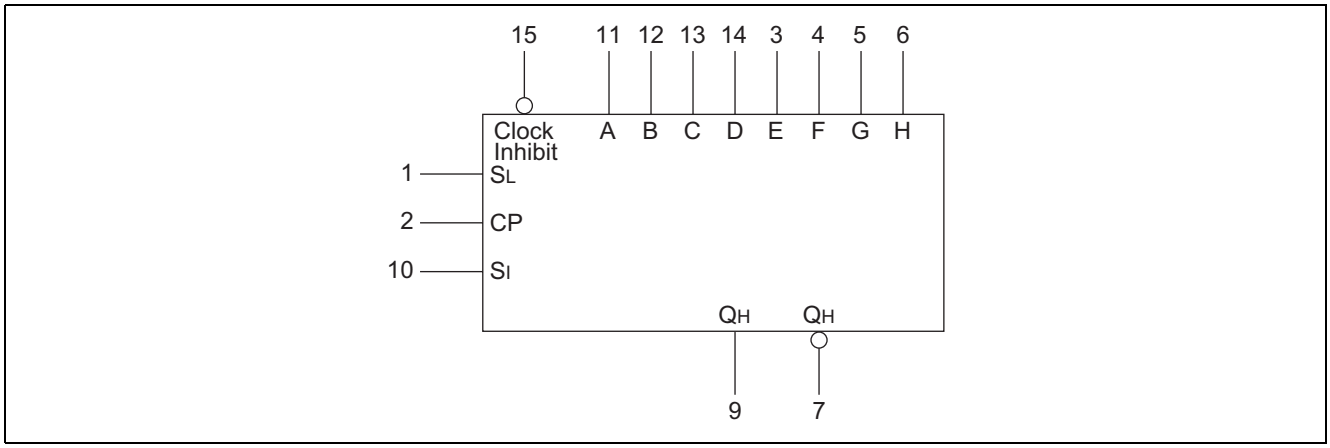
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC165FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC165RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

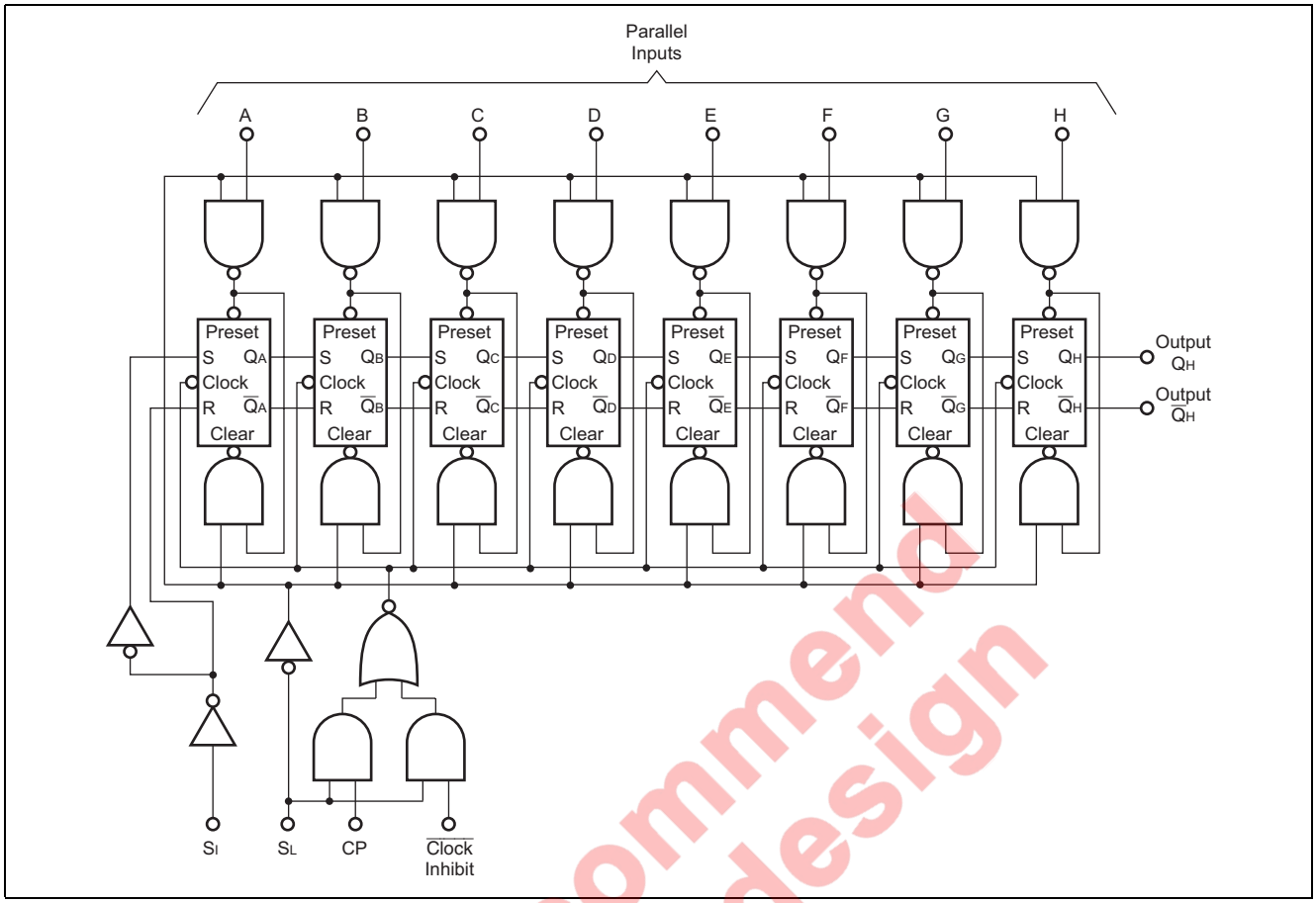
A to H	Parallel Inputs
S_I	Serial Input
CP	Clock Input
S_L	Shift Load
$\overline{\text{Clock}}$ Inhibit	Clock Inhibit
Q_H, $\overline{Q}_H$	Outputs

Truth Table

Inputs					Internal Outputs		Outputs
S_L	$\overline{\text{Clock}}$ Inhibit	CP	S_I	Parallel A ····· H	Q_A	Q_B	Q_H
L	X	X	X	a ····· h	a	b	h
H	L	L	X	X	$Q_{A\overline{D}}$	$Q_{B\overline{O}}$	Q_{HO}
H	L	⎍	H	X	H	Q_{An}	Q_{Gn}
H	L	⎍	L	X	L	Q_{An}	Q_{Cn}
H	H	X	X	X	$Q_{A\overline{D}}$	$Q_{B\overline{O}}$	Q_{HO}

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
⎍ : Low-to-High Clock Transition

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f_{max}	3.3	85	—	—	70	—	MHz
		5.0	100	—	—	90	—	
Propagation delay CP to Q_H or $\overline{Q}_H$	t_{PLH}	3.3	1.0	11.0	17.5	1.0	20.5	ns
		5.0	1.0	8.0	11.5	1.0	13.5	
Propagation delay CP to Q_H or $\overline{Q}_H$	t_{PHL}	3.3	1.0	12.0	18.0	1.0	21.5	ns
		5.0	1.0	8.5	12.5	1.0	14.5	
Propagation delay H to Q_H or $\overline{Q}_H$	t_{PLH}	3.3	1.0	13.5	19.5	1.0	22.5	ns
		5.0	1.0	9.5	13.5	1.0	15.5	
Propagation delay H to Q_H or $\overline{Q}_H$	t_{PHL}	3.3	1.0	9.0	14.0	1.0	16.5	ns
		5.0	1.0	6.5	9.5	1.0	11.0	
Propagation delay S_L to Q_H or $\overline{Q}_H$	t_{PLH}	3.3	1.0	11.5	20.5	1.0	23.5	ns
		5.0	1.0	8.5	14.0	1.0	16.0	
Propagation delay S_L to Q_H or $\overline{Q}_H$	t_{PHL}	3.3	1.0	10.0	16.5	1.0	19.5	ns
		5.0	1.0	7.5	11.0	1.0	12.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW H to S_L	t_{su}	3.3	3.5	5.0	6.0	ns
		5.0	2.5	4.0	4.5	
Hold time, HIGH or LOW H to S_L	t_h	3.3	–1.0	0.5	0.5	ns
		5.0	–0.5	0.5	0.5	
Setup time, HIGH or LOW S_{in} to CP	t_{su}	3.3	1.0	3.5	4.0	ns
		5.0	0.5	3.0	3.5	
Hold time, HIGH or LOW S_{in} to CP	t_h	3.3	1.5	2.0	2.0	ns
		5.0	1.0	2.0	2.0	
Setup time, HIGH or LOW S_L to CP	t_{su}	3.3	3.0	5.0	6.0	ns
		5.0	2.0	4.0	4.5	
Hold time, HIGH or LOW S_L to CP	t_h	3.3	–2.0	0.0	0.0	ns
		5.0	–1.0	0.0	0.0	
Recovery time clock inhibit to CP	t_{rec}	3.3	2.5	3.5	3.5	ns
		5.0	2.0	3.0	3.0	
Clock pulse width	t_w	3.3	3.0	5.5	7.0	ns
		5.0	3.0	4.5	5.0	

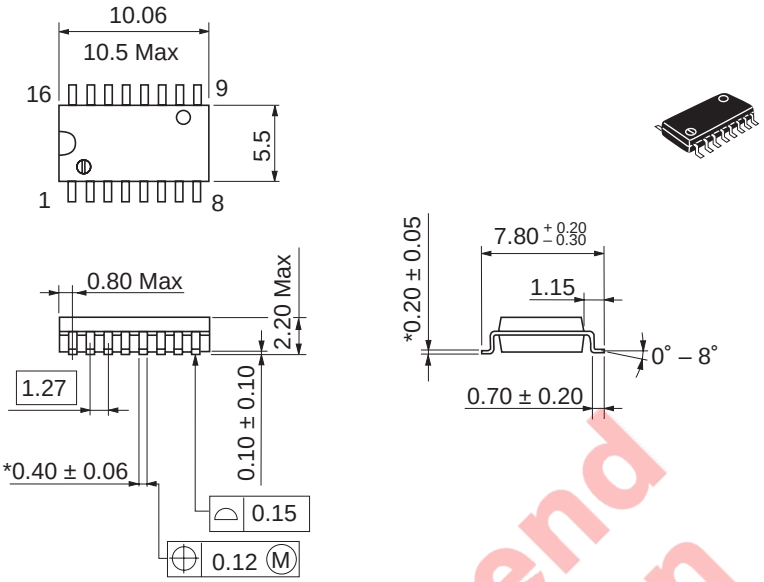
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	50	pF	V_{CC} = 5.0 V

Package Dimensions

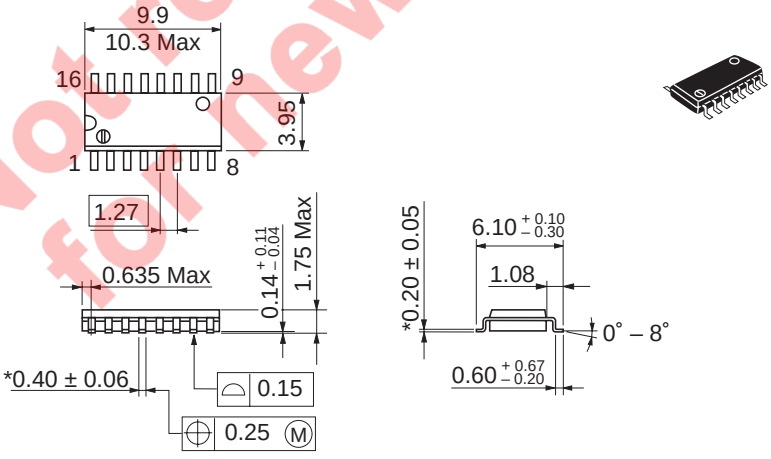
As of January, 2003
Unit: mm



Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003
Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS SALES OFFICES

http://www.renesas.com

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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