HD74AC166/HD74ACT166

8-bit Shift Register

REJ03D0255–0200Z
(Previous ADE-205-375 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC166/HD74ACT166 is an 8-bit, serial or parallel-in, serial-out shift register using edge triggered D-type flip-flops. Serial and parallel entry are synchronous, with state changes initiated by the rising edge of the clock. An asynchronous Master Reset overrides other inputs and clears all flip-flops. The circuit can be clocked from two sources or one CP input can be used to trigger the other.

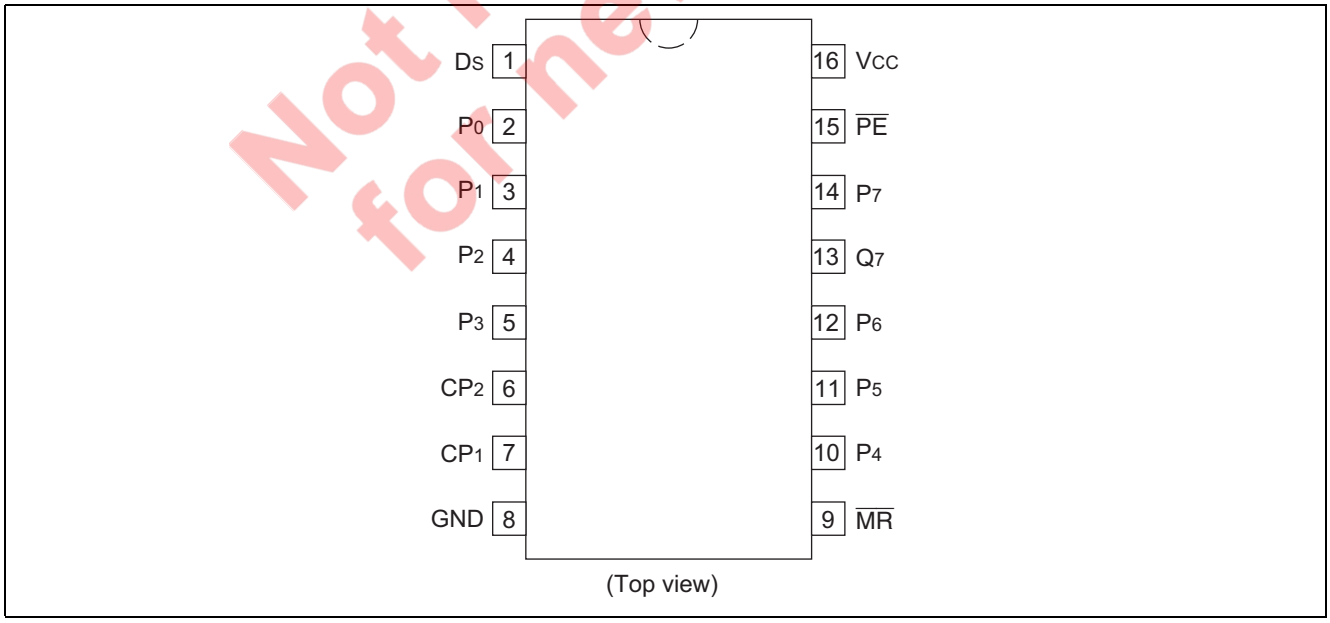
Features

- Outputs Source/Sink 24 mA
- HD74ACT166 has TTL-Compatible Inputs
- Ordering Information: Ex. HD74AC166

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC166AFPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC166ARPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)
HD74AC166TELL	TSSOP-16 pin	TTP-16DAV	T	ELL(2,000 pcs/reel)

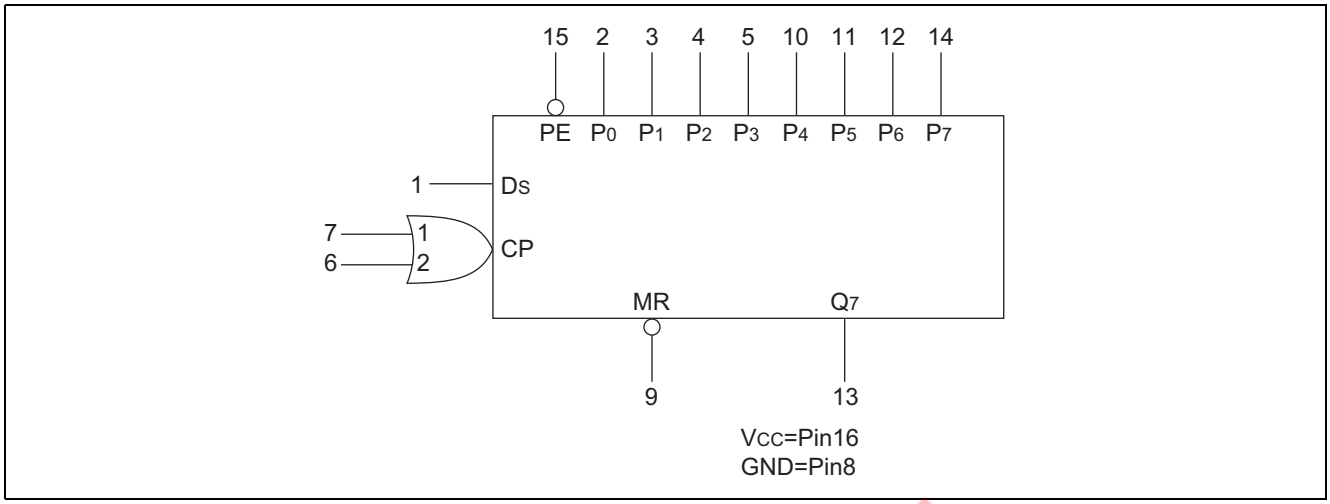
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

CP_1, CP_2	Clock Pulse Inputs (Active Rising Edge)
D_S	Serial Data Input
$\overline{PE}$	Parallel Enable Input (Active Low)
P_0 to P_7	Parallel Data Inputs
$\overline{MR}$	Asynchronous Master Reset Input (Active Low)
Q_7	Last Stage Output

Functional Description

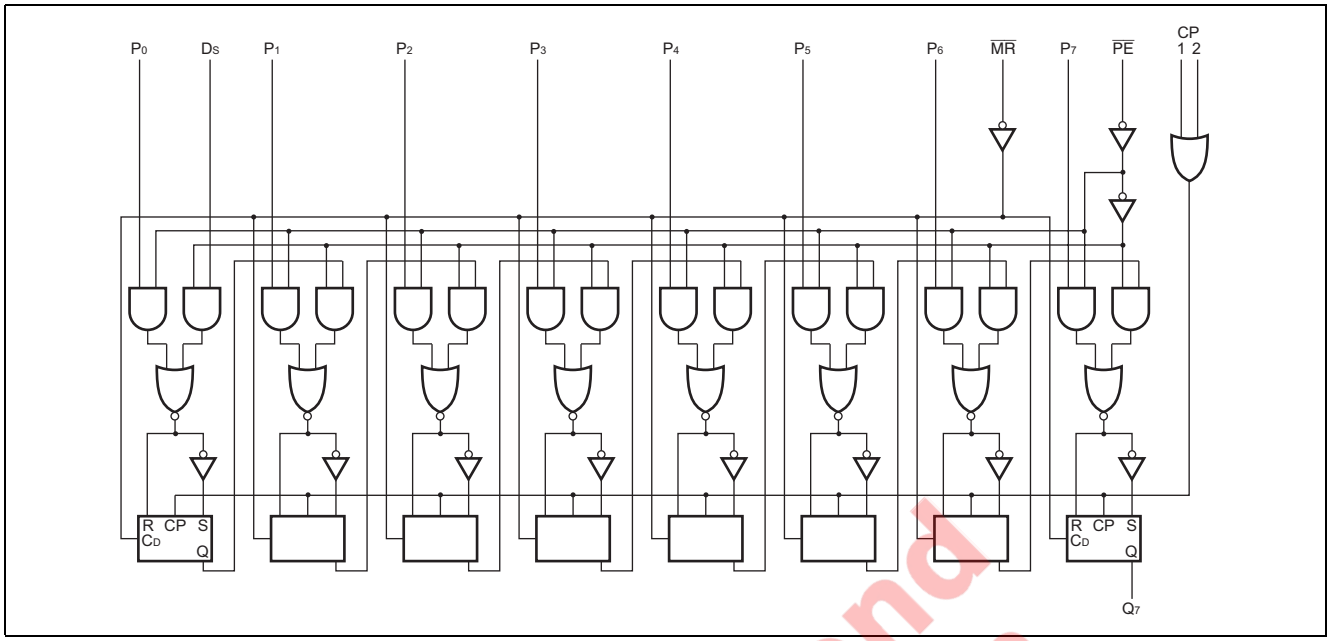
Operation is synchronous (except for Master Reset) and state changes are initiated by the rising edge of either clock input if the other clock input is Low. When one of the clock inputs is used as an active High clock inhibt, it should attain the High state while the other clock is still in the High state following the previous operation. When the Parallel Enable ($\overline{PE}$) input is Low, data is loaded into the register from the Parallel Data (P_0 to P_7) inputs on the next rising edge of the clock. When $\overline{PE}$ is High, information is shifted from the Serial Data (D_S) input to Q_0 and all data in the register is shifted one bit position (i.e., $Q_0 \rightarrow Q_1$, $Q_1 \rightarrow Q_2$, etc.) on the rising edge of the clock.

Truth Table

Inputs						Internal Outputs		Output
					Parallel			
$\overline{MR}$	$\overline{PE}$	CP_2	CP_1	D_S	P_0 to P_7	Q_0	Q_6	Q_7
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	⎍	X	a ··· h	a	b	h
H	H	L	⎍	H	X	H	Q_{An}	Q_{Gn}
H	H	L	⎍	L	X	L	Q_{An}	Q_{Gn}
H	X	H	⎍	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
⎍ : Low-to-High Clock Transition

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions: HD74AC166

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics: HD74AC166

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

Recommended Operating Conditions: HD74ACT166

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	tr, tf	8	ns/V	V_{CC} = 4.5V V_{CC} = 5.5V

DC Characteristics: HD74ACT166

Item	Sym-bol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	2.0	1.5	—	2.0	—			
	V_{IL}	4.5	—	1.5	0.8	—	0.8		V_{OUT} = 0.1 V or Vcc–0.1 V	
		5.5	—	1.5	0.8	—	0.8			
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		5.5	5.4	5.49	—	5.4	—			
		4.5	3.94	—	—	3.80	—		V_{IN} = V_{IL}	I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	4.5	—	0.001	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		5.5	—	0.001	0.1	—	0.1			
		4.5	—	—	0.32	—	0.37		V_{IN} = V_{IL}	I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
I_{CC}/input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	V_{IN} = V_{CC}–2.1 V	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC166

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	75	—	—	65	—	MHz
		5.0	100	—	—	80	—	
Propagation delay CP_1 or CP_2 to Q_7	t_{PLH}	3.3	1.0	11.0	14.5	1.0	15.5	ns
		5.0	1.0	9.5	11.5	1.0	12.5	
Propagation delay CP_1 or CP_2 to Q_7	t_{PHL}	3.3	1.0	10.5	14.0	1.0	15.0	
		5.0	1.0	9.0	11.0	1.0	12.0	
Propagation delay $\overline{MR}$ to Q_7	t_{PHL}	3.3	1.0	9.5	12.0	1.0	13.0	
		5.0	1.0	6.5	9.0	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC166

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time $\overline{PE}$ or P_n or D_S to CP_n	t_{su}	3.3	3.0	5.5	6.0	ns
		5.0	2.0	4.0	4.5	
Hold time CP_n to $\overline{PE}$ or P_n or D_S	t_h	3.3	–1.5	3.0	3.0	
		5.0	–0.5	3.0	3.0	
Pulse width CP_n or $\overline{MR}$	t_w	3.3	2.0	5.5	7.0	
		5.0	2.0	4.5	5.0	
Recovery time $\overline{MR}$ to CP_n	t_{rec}	3.3	–2.5	0.0	0.0	
		5.0	–1.5	0.0	0.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT166

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	5.0	100	—	—	80	—	MHz
Propagation delay CP_n to Q_7	t_{PLH}	5.0	1.0	10.0	12.5	1.0	13.5	ns
Propagation delay CP_n to Q_7	t_{PHL}	5.0	1.0	9.5	12.0	1.0	13.0	
Propagation delay $\overline{MR}$ to Q_7	t_{PHL}	5.0	1.0	8.5	11.0	1.0	12.0	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT166

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time $\overline{PE}$ or P_n or D_S to CP_n	t_{su}	5.0	2.5	7.0	8.0	ns
Hold time CP_n to $\overline{PE}$ or P_n or D_S	t_h	5.0	0.0	1.5	1.5	
Pulse width CP_n or $\overline{MR}$	t_w	5.0	4.5	7.0	8.0	
Recovery time $\overline{MR}$ to CP_n	t_{rec}	5.0	–2.5	0.5	0.5	

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

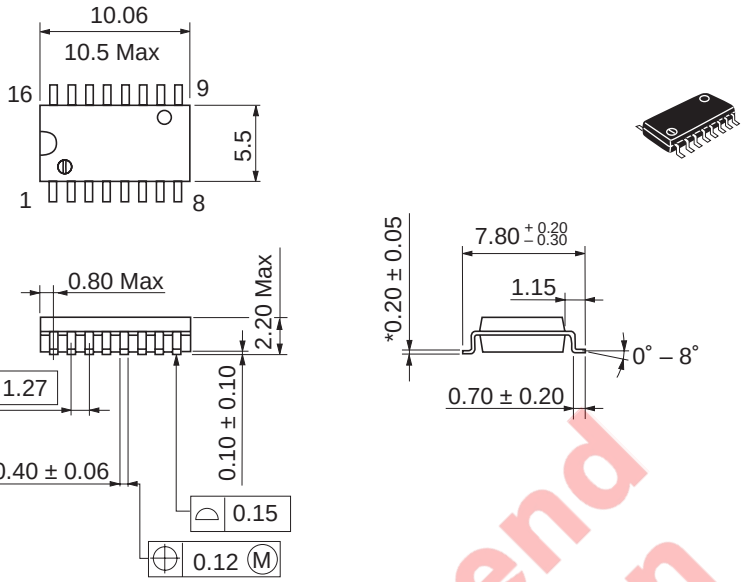
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	35.0	pF	V_{CC} = 5.0 V

Package Dimensions

As of January, 2003

Unit: mm

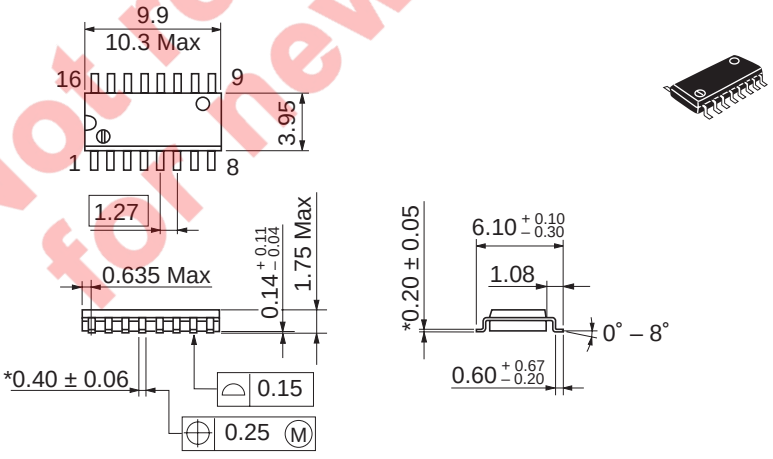


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm

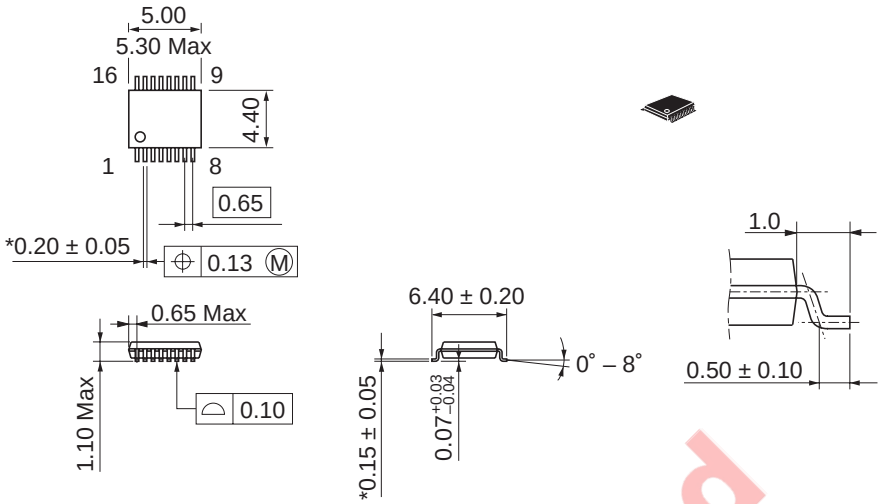


Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

*Ni/Pd/Au plating

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