HD74AC174

Hex D-Type Flip-Flop with Master Reset

REJ03D0256–0200Z
(Previous ADE-205-376 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC174 is a high-speed hex D flip-flop. The device is used primarily as a 6-bit edge-triggered storage register. The information on the D inputs is transferred to storage during the Low-to-High clock transition. The device has a Master Reset to simultaneously clear all flip-flops.

Features

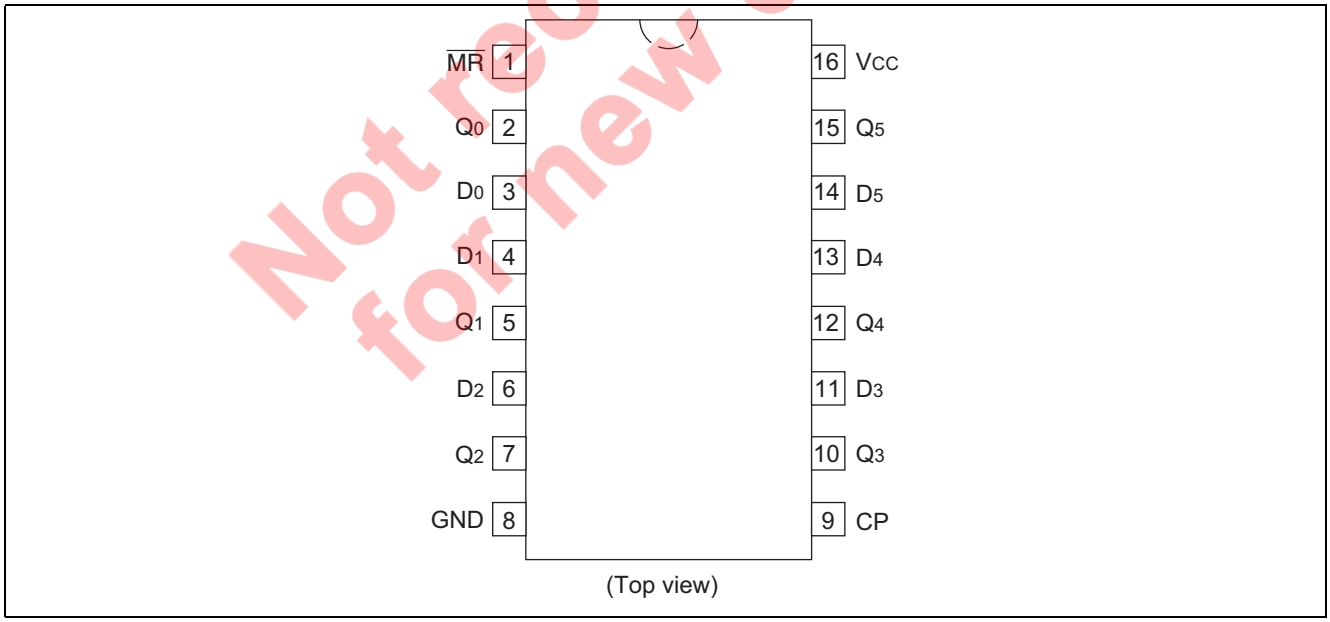
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC174FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC174RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

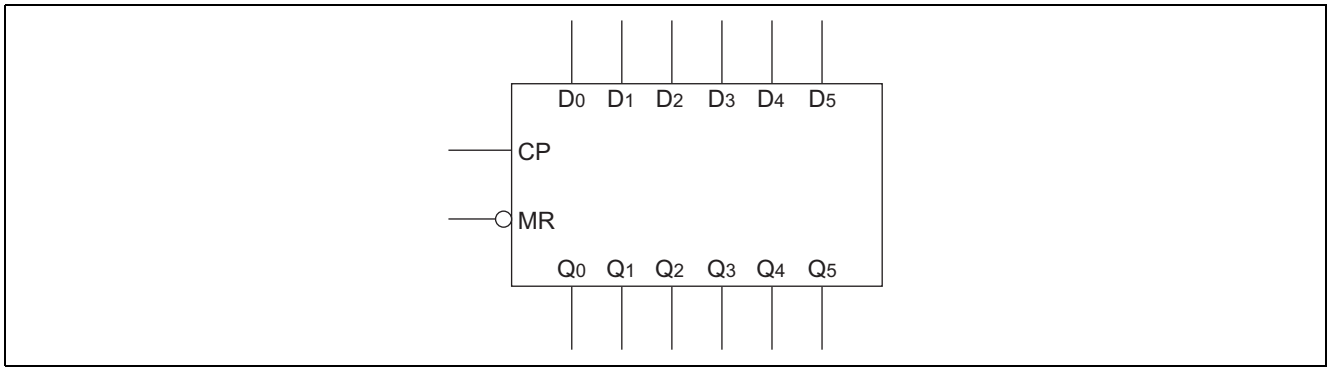
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Not recommend for new design

Pin Arrangement



Logic Symbol



Pin Names

D_0 to D_5	Data Inputs
CP	Clock Pulse Input
$\overline{MR}$	Master Reset Input
Q_0 to Q_5	Outputs

Functional Description

The HD74AC174 consists of six edge-triggered D flip-flops with individual D inputs and Q outputs. The Clock (CP) and Master Reset ($\overline{MR}$) are common to all flip-flops. Each D input's state is transferred to the corresponding flip-flops's output following the Low-to-High Clock (CP) transition. A Low input to the Master Reset ($\overline{MR}$) will force all outputs Low independent of Clock or Data inputs. The HD74AC174 is useful for applications where the true output only is required and the Clock and Master Reset are common to all storage elements.

Truth Table

Inputs			Output
$\overline{MR}$	CP	D	Q
L	X	X	L
H	⎍	H	H
H	⎍	L	L
H	L	X	Q

H : High Voltage Level
L : Low Voltage Level
X : Immaterial
⎍ : Low-to-High Transition of Clock

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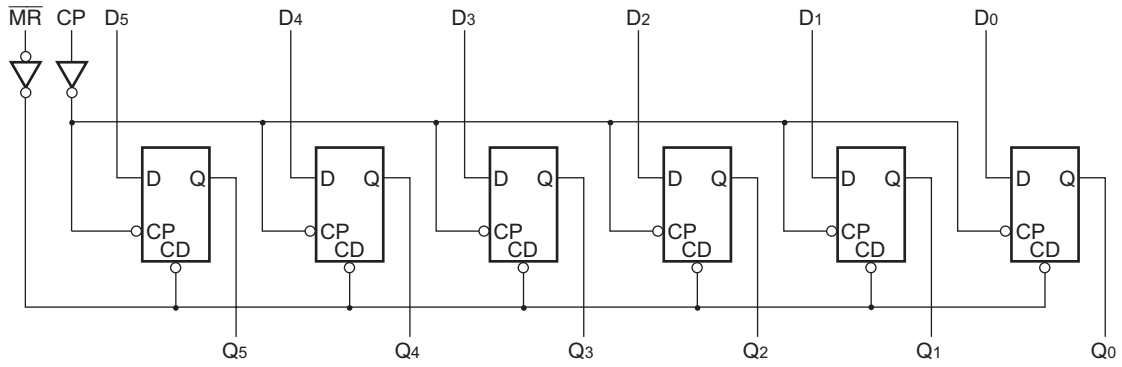
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

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DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74AC174

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	90	100	—	70	—	MHz
		5.0	100	125	—	100	—	
Propagation delay CP to Q_n	t_{PLH}	3.3	1.0	9.0	11.5	1.0	12.5	ns
		5.0	1.0	6.0	8.5	1.0	9.5	
Propagation delay CP to Q_n	t_{PHL}	3.3	1.0	8.5	11.0	1.0	12.0	ns
		5.0	1.0	6.0	8.0	1.0	9.0	
Propagation delay $\overline{MR}$ to Q_n	t_{PHL}	3.3	1.0	9.0	11.5	1.0	12.5	ns
		5.0	1.0	7.0	9.0	1.0	10.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Not recommend for new design

AC Operating Requirements: HD74AC174

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW	t_{su}	3.3	2.5	6.5	7.0	ns
D_n to CP		5.0	2.0	5.0	5.5	
Hold time, HIGH or LOW	t_h	3.3	1.0	3.0	3.0	ns
D_n to CP		5.0	0.5	3.0	3.0	
$\overline{MR}$ pulse width, LOW	t_w	3.3	1.0	5.5	7.0	ns
		5.0	1.0	5.0	5.0	
CP pulse width	t_w	3.3	1.0	5.5	7.0	ns
		5.0	1.0	5.0	5.0	
Recovery time	t_{rec}	3.3	0	2.5	2.5	ns
$\overline{MR}$ to CP		5.0	0	2.0	2.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	85.0	pF	V_{CC} = 5.0 V

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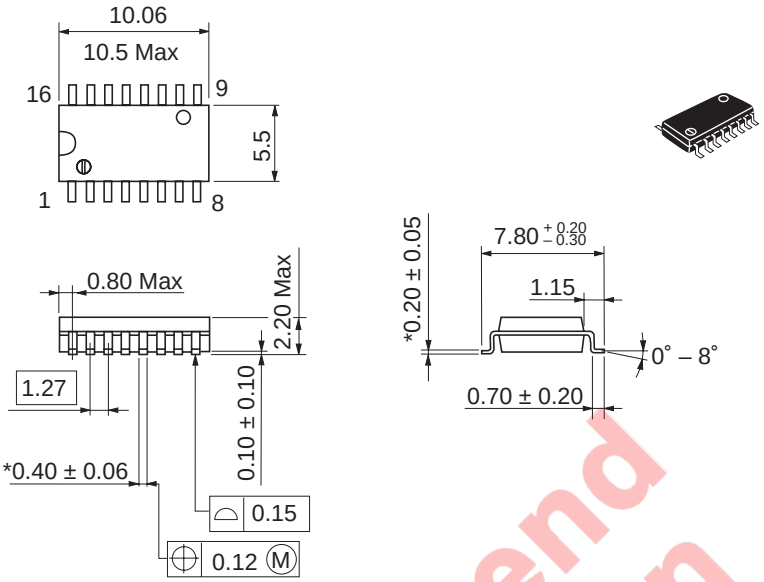
Package Dimensions

As of January, 2003

Unit: mm

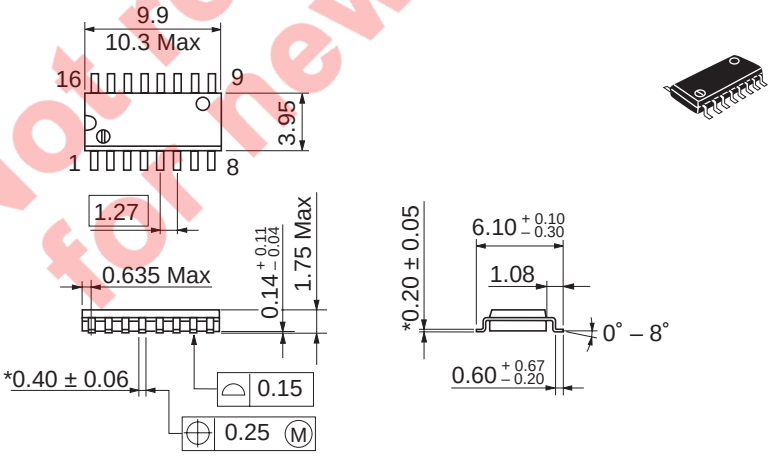


Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

*Ni/Pd/Au plating

As of January, 2003

Unit: mm



Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

*Ni/Pd/Au plating

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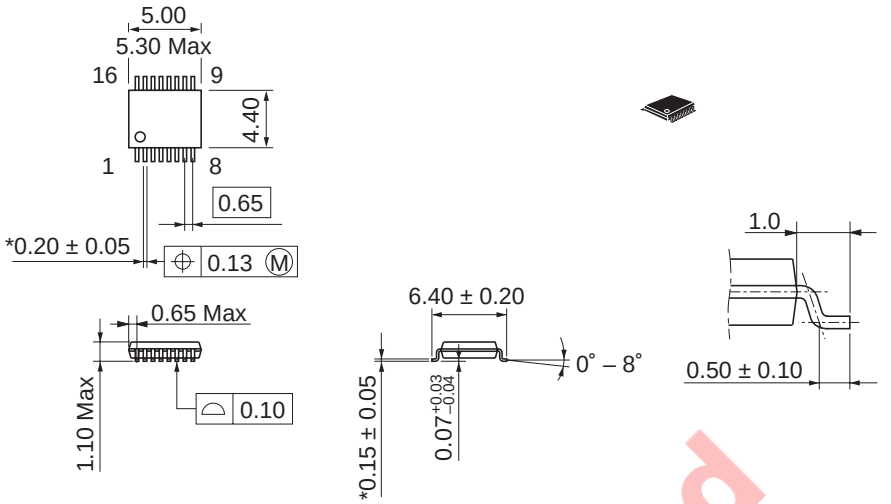
As of January, 2003

Unit: mm



Package Code	TTP-16DAV
JEDEC	—
JEITA	—
Mass (reference value)	0.05 g

*Ni/Pd/Au plating

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