
HD74AC182/HD74ACT182

Carry Lookahead Generator

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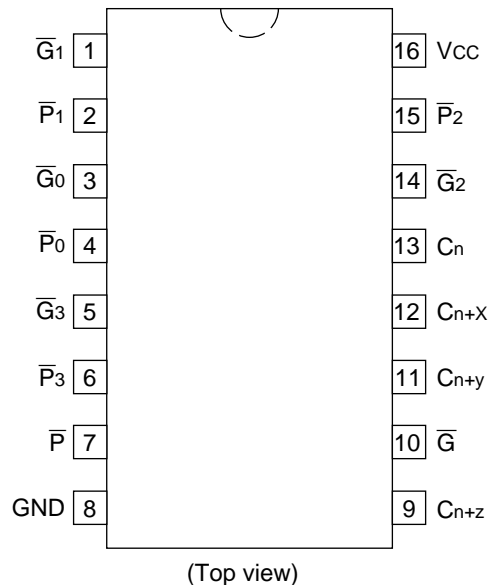
Description

The HD74AC182/HD74ACT182 is a high-speed carry lookahead generator. It is generally used with the HD74AC181 or HD74AC381 4-bit arithmetic logic unit to provide high-speed lookahead over word lengths of more than four bits.

Features

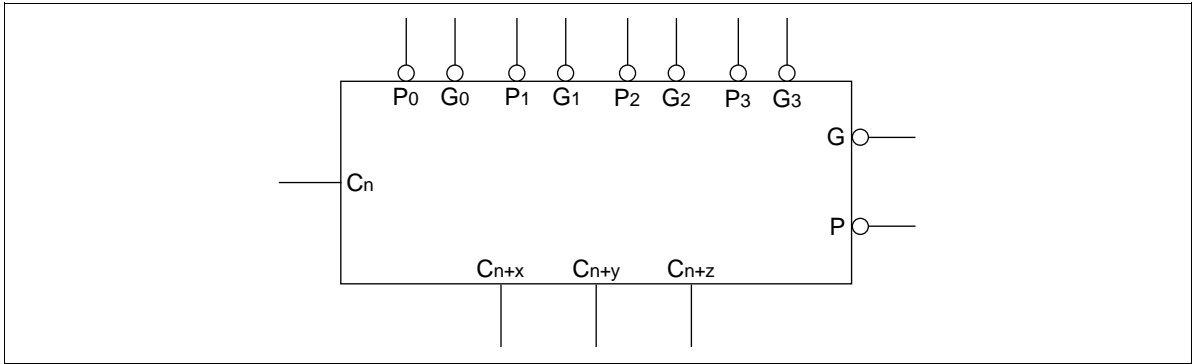
- Outputs Source/Sink 24 mA
- HD74ACT182 has TTL-Compatible Inputs

Pin Arrangement



HD74AC182/HD74ACT182

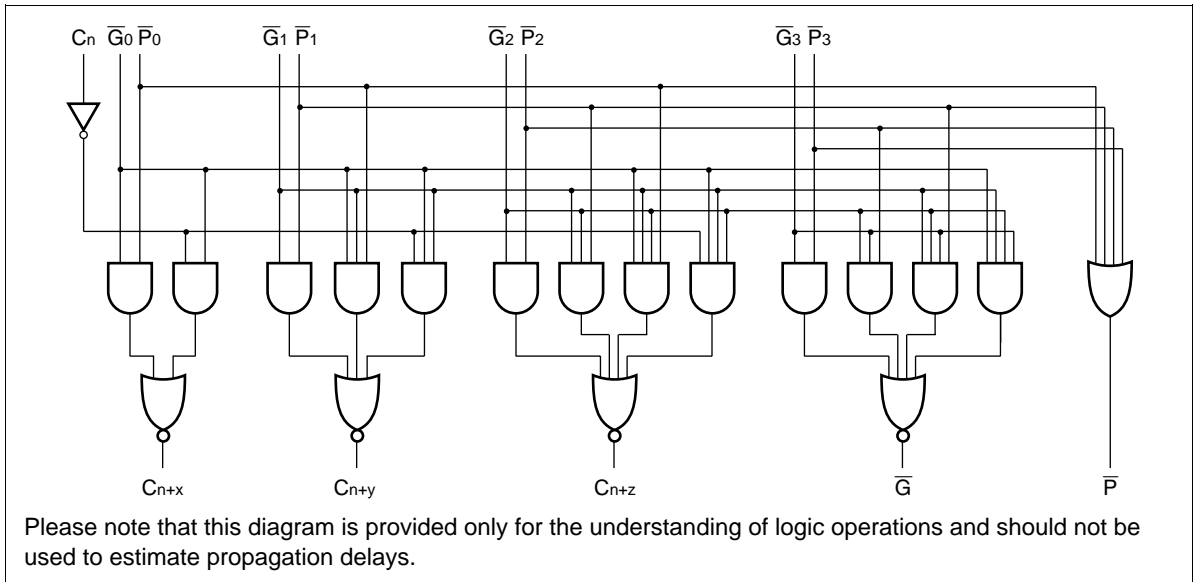
Logic Symbol



Pin Names

C_n	Carry Input
$\overline{G}_0, \overline{G}_2$	Carry Generate Inputs (Active Low)
\overline{G}_1	Carry Generate Input (Active Low)
\overline{G}_3	Carry Generate Input (Active Low)
$\overline{P}_0, \overline{P}_1$	Carry Propagate Inputs (Active Low)
\overline{P}_2	Carry Propagate Input (Active Low)
\overline{P}_3	Carry Propagate Input (Active Low)
C_{n+x} to C_{n+z}	Carry Outputs
\overline{G}	Carry Generate Output (Active Low)
\overline{P}	Carry Propagate Output (Active Low)

Logic Diagram



Functional Description

The HD74AC182/HD74ACT182 carry lookahead generator accepts up to four pairs of Active Low Carry Propagate (\bar{P}_0 to \bar{P}_3) and Carry Generate (\bar{G}_0 to \bar{G}_3) signals and an Active High Carry input (C_n) and provides anticipated Active High carries (C_{n+x} , C_{n+y} , C_{n+z}) across four groups of binary adders. The HD74AC182/HD74ACT182 also has Active Low Carry Propagate (\bar{P}) and Carry Generate (\bar{G}) outputs which may be used for further level of lookahead. The logic equations provided at the outputs are:

$$\begin{aligned}
 C_{n+x} &= G_0 + P_0 C_n \\
 C_{n+y} &= G_1 + P_1 G_0 + P_1 P_0 C_n \\
 C_{n+z} &= G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 C_n \\
 \bar{G} &= \bar{G}_3 + P_3 \bar{G}_2 + P_3 P_2 \bar{G}_1 + P_3 P_2 P_1 \bar{G}_0 \\
 \bar{P} &= \bar{P}_3 \bar{P}_2 \bar{P}_1 \bar{P}_0
 \end{aligned}$$

Also, the HD74AC182/HD74ACT182 can be used with binary ALUs in an active Low or active High input operand mode. The connections (Figure a) to and from the ALU to the carry lookahead generator are identical in both cases. Carries are rippled between lookahead blocks. The critical speed path follows the circled numbers. There are several possible arrangements for the carry interconnects, but all achieve about the same speed. A 28-bit ALU is formed by dropping the last HD74AC182/HD74ACT182.

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Truth Table

Inputs									Outputs				
C_n	\overline{G}_0	\overline{P}_0	\overline{G}_1	\overline{P}_1	\overline{G}_2	\overline{P}_2	\overline{G}_3	\overline{P}_3	C_{n+x}	C_{n+y}	C_{n+z}	\overline{G}	\overline{P}
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	X	H	H					L		
X	X	X	H	H	H	X					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	X	X	L	X					H		
X	X	X	L	X	X	L					H		
X	L	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	H	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		L	X	X	L	X	L				L	
	L		X	L	X	L	X	L				L	
		H		X		X		X					H
		X		H		X		X					H
		X		X		H		X					H
		X		X		X		H					H
		L		L		L		L					L

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

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DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = 25^\circ\text{C}$
Maximum I_{CC} /input (HD74ACT182)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1\text{ V}$, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$

AC Characteristics: HD74AC182

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t_{PLH}	3.3	1.0	8.0	10.5	1.0	11.5	ns
P_n to P		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay	t_{PHL}	3.3	1.0	8.0	10.5	1.0	11.5	ns
P_n to P		5.0	1.0	5.5	8.0	1.0	9.0	
Propagation delay	t_{PLH}	3.3	1.0	9.5	12.0	1.0	13.0	ns
C_n to $C_{n+x,y,z}$		5.0	1.0	7.5	10.0	1.0	11.0	
Propagation delay	t_{PHL}	3.3	1.0	9.0	12.0	1.0	13.0	ns
C_n to $C_{n+x,y,z}$		5.0	1.0	7.0	10.0	1.0	11.0	
Propagation delay	t_{PLH}	3.3	1.0	10.5	13.0	1.0	14.0	ns
P_n or G_n to $C_{n+x,y,z}$		5.0	1.0	8.0	10.5	1.0	11.5	
Propagation delay	t_{PHL}	3.3	1.0	11.5	14.0	1.0	15.5	ns
P_n or G_n to $C_{n+x,y,z}$		5.0	1.0	9.0	11.5	1.0	12.5	

Note: 1. Voltage Range 3.3 is $3.3\text{ V} \pm 0.3\text{ V}$
Voltage Range 5.0 is $5.0\text{ V} \pm 0.5\text{ V}$

HD74AC182/HD74ACT182

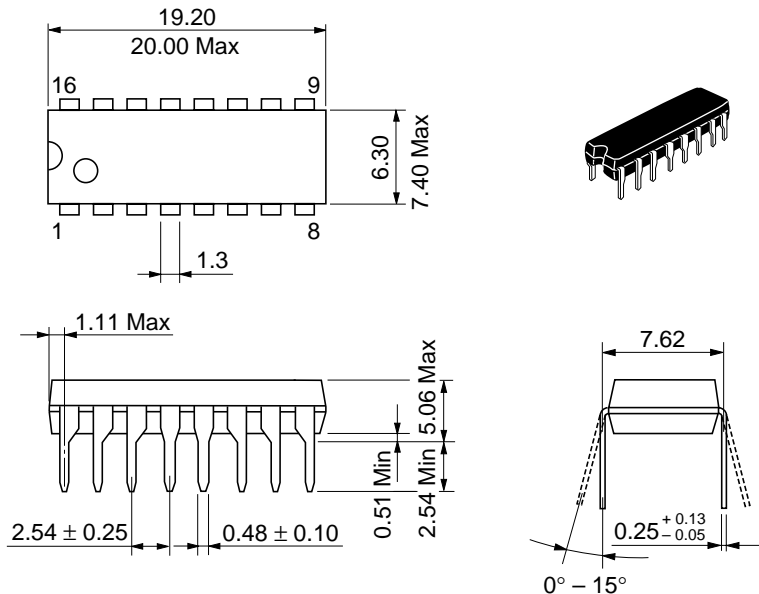
AC Characteristics: HD74ACT182

Item	Symbol	V_{CC} (V)* ¹	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay P _n to P	t _{PLH}	5.0	1.0	7.0	9.0	1.0	10.0	ns
Propagation delay P _n to P	t _{PHL}	5.0	1.0	8.0	10.0	1.0	11.0	ns
Propagation delay C _n to C _{n+x,y,z}	t _{PLH}	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay C _n to C _{n+x,y,z}	t _{PHL}	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay P _n or G _n to C _{n+x,y,z}	t _{PLH}	5.0	1.0	9.0	11.0	1.0	12.0	ns
Propagation delay P _n or G _n to C _{n+x,y,z}	t _{PHL}	5.0	1.0	10.0	12.5	1.0	13.5	ns

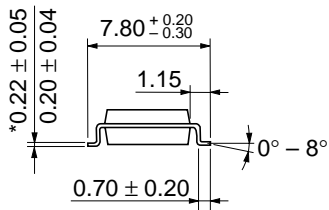
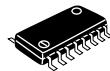
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	50.0	pF	V _{CC} = 5.0 V



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



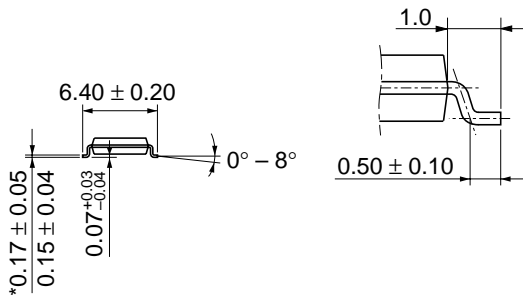
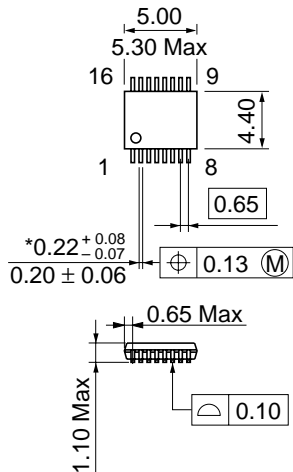
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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