HD74AC195

4-bit Parallel-Access Shift Register

HITACHI

Description

This shift register features parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; Shift from Q_0 towards Q_3.

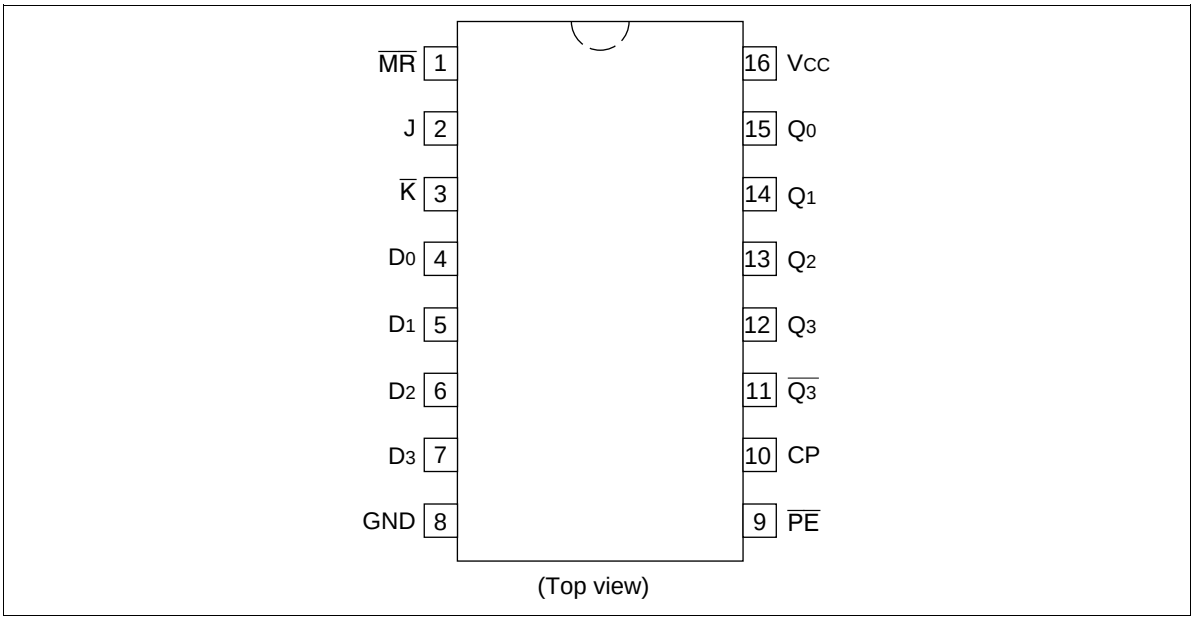
Parallel loading is accomplished by applying the four bits of data, and taking the $\overline{PE}$ Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the CP input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the $\overline{PE}$ input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs allow the first stage to perform as a J-$\overline{K}$ or toggle flip-flop as shown in the function table.

Features

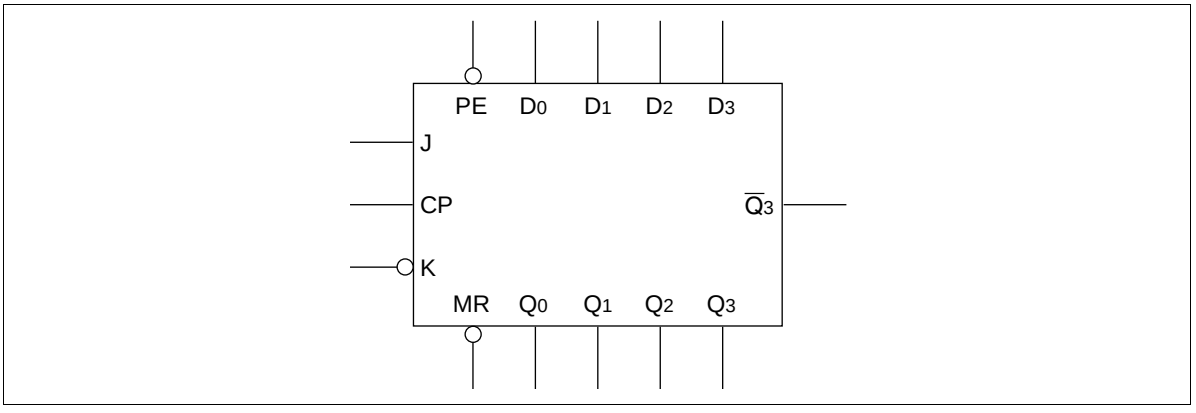
- Shift Right and Parallel Load Capability
- J-$\overline{K}$ (D-Type) Inputs to First Stage
- Complement Output from Last Stage
- Asynchronous Master Reset
- Outputs Source/Sink 24 mA

Hitachi semiconductor

Pin Arrangement



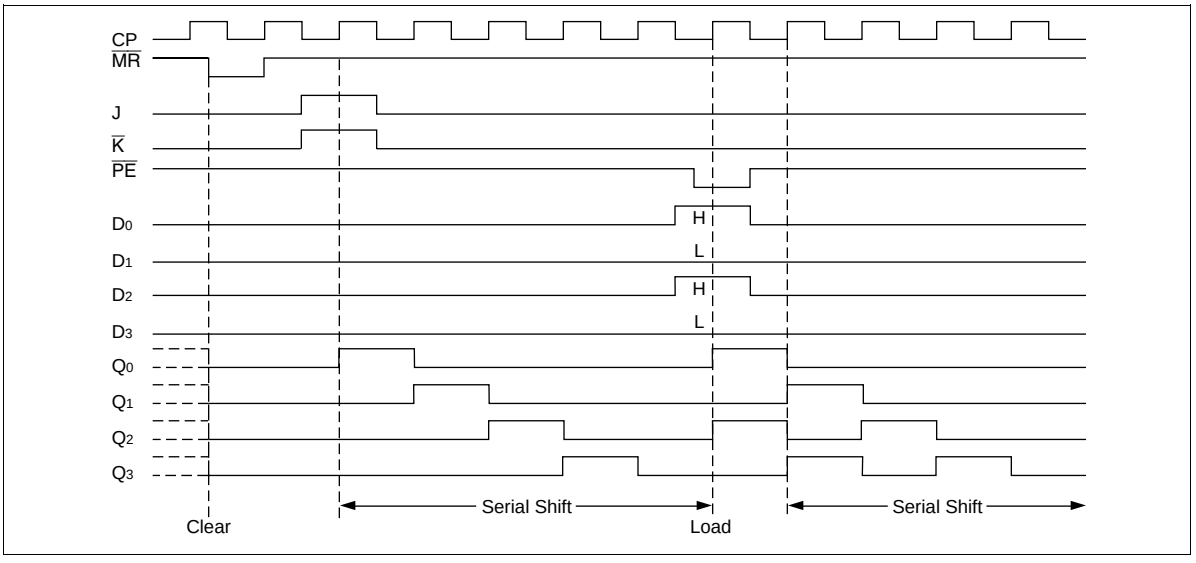
Logic Symbol



Pin Names

CP	Clock Pulse Input (Active Rising Edge)
D_0 to D_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
$\overline{MR}$	Asynchronous Master Reset
J, $\overline{K}$	J-$\overline{K}$ or D Type Serial Inputs
Q_0 to Q_3, $\overline{Q}_3$	Outputs

Timing Diagram



Mode Select-Function Table

	Inputs						Outputs				
Operating Modes	$\overline{MR}$	CP	$\overline{PE}$	J	$\overline{K}$	D_n	Q_0	Q_1	Q_2	Q_3	$\overline{Q}_3$
Asynchronous Reset	L	X	X	X	X	X	L	L	L	L	H
Shift, Set First Stage	H	⎍	H	H	H	X	H	q_0	q_1	q_2	$\overline{q}_2$
Shift, Reset First Stage	H	⎍	H	L	L	X	L	q_0	q_1	q_2	$\overline{q}_2$
Shift, Toggle First Stage	H	⎍	H	H	L	X	$\overline{q}_0$	q_0	q_1	q_2	$\overline{q}_2$
Shift, Retain First Stage	H	⎍	H	L	H	X	q_0	q_0	q_1	q_2	$\overline{q}_2$
Parallel Load	H	⎍	L	X	X	d_n	d_0	d_1	d_2	d_3	$\overline{d}_3$

H : HIGH Voltage Level

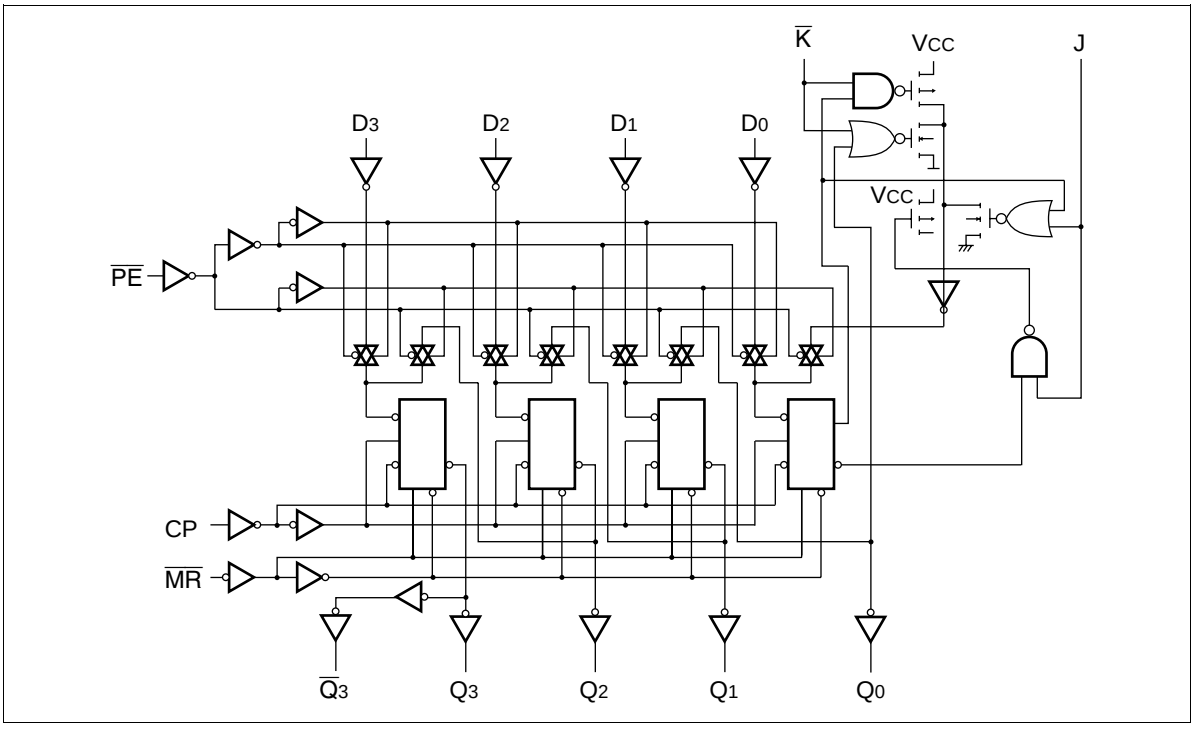
L : LOW Voltage Level

X : Immaterial

Lower case letters indicate the state of the referenced input (or output) one setup time prior to the LOW-to-HIGH transition.

⎍ : LOW-to-HIGH clock transition.

Logic Diagram



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = Worst case
Maximum quiescent supply current	I_{CC}	8.0	µA	V_{IN} = V_{CC} or ground, V_{CC} = 5.5 V, Ta = 25°C

AC Characteristics: HD74AC195

Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF			Ta = –40°C to +85°C, C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock	f_{max}	3.3	75	—	—	65	—	MHz
frequency		5.0	100	—	—	85	—	
Propagation delay	t_{PLH}	3.3	1.0	9.0	13.0	1.0	15.0	ns
CP to Q_n or $\overline{Q}_3$		5.0	1.0	5.5	10.0	1.0	11.5	
Propagation delay	t_{PHL}	3.3	1.0	9.0	13.0	1.0	15.0	ns
CP to Q_n or $\overline{Q}_2$		5.0	1.0	6.5	10.0	1.0	11.5	
Propagation delay	t_{PLH}	3.3	1.0	7.5	10.5	1.0	12.0	ns
$\overline{MR}$ to $\overline{Q}_2$		5.0	1.0	5.5	8.0	1.0	9.5	
Propagaion delay	t_{PHL}	3.3	1.0	6.0	9.0	1.0	10.5	ns
$\overline{MR}$ to $\overline{Q}_n$		5.0	1.0	5.0	7.0	1.0	8.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74AC195

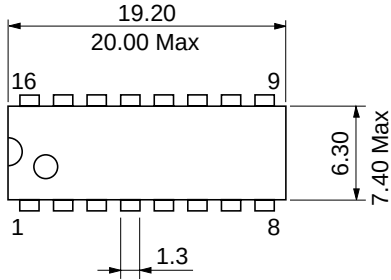
Item	Symbol	V_{CC} (V)*[1]	Ta = +25°C, C_L = 50 pF		Ta = –40°C to +85°C, C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW	t_{su}	3.3	3.0	5.5	7.0	ns
J, $\overline{K}$ or $\overline{D}_n$ to CP		5.0	2.0	4.0	5.0	
Hold time, HIGH or LOW	t_h	3.3	–0.5	2.0	3.6	ns
J, $\overline{K}$ or $\overline{D}_n$ to CP		5.0	0.5	1.5	2.0	
Setup time, HIGH or LOW	t_{su}	3.3	3.5	5.0	7.0	ns
$\overline{PE}$ to CP		5.0	2.5	4.0	5.0	
Hold time, HIGH or LOW	t_h	3.3	–2.0	0.0	0.0	ns
$\overline{PE}$ to CP		5.0	–1.5	0.0	0.0	
Recovery time	t_{rec}	3.3	–1.5	0.5	0.5	ns
$\overline{MR}$ to CP		5.0	–1.0	0.5	0.5	
Pulse width	t_w	3.3	–3.0	5.5	7.0	ns
		5.0	–3.0	4.5	5.0	

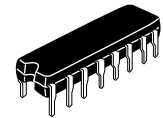
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

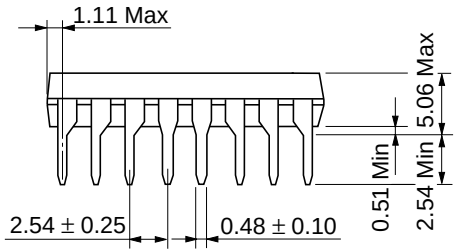
Capacitance

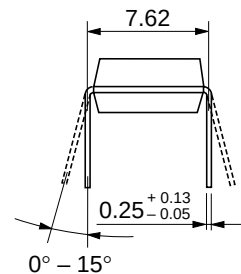
Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	125	pF	V_{CC} = 5.0 V

Unit: mm



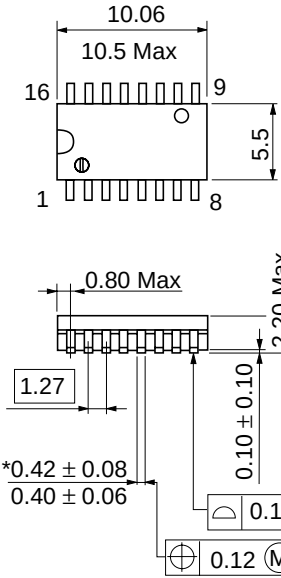


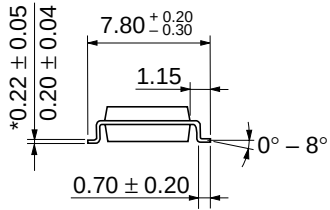


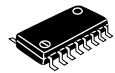


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

Unit: mm



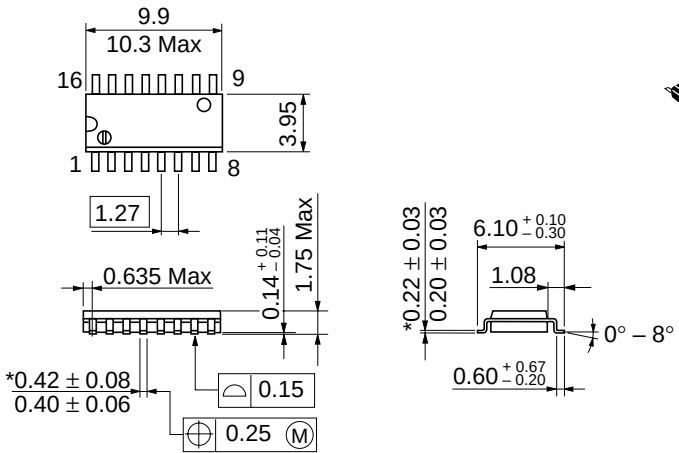




*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

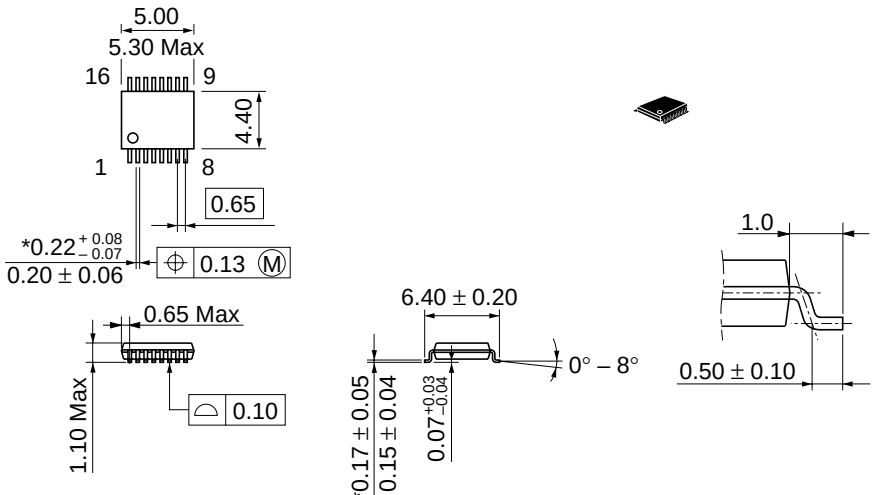
Unit: mm



Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

*Dimension including the plating thickness
Base material dimension

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL
NorthAmerica : http:semiconductor.hitachi.com/
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX