
HD74AC240/HD74ACT240

Octal Buffer/Line Driver with 3-State Output

HITACHI

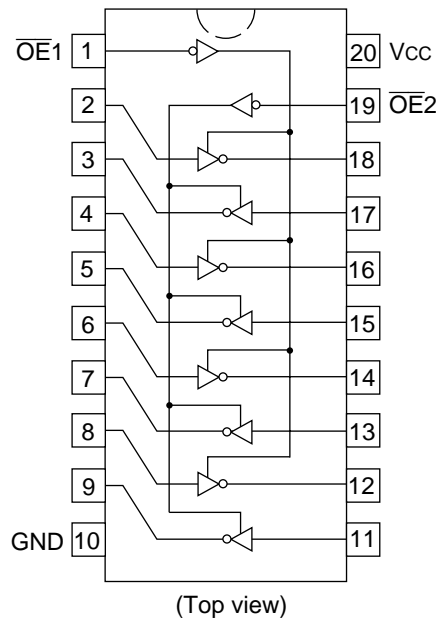
Description

The HD74AC240/HD74ACT240 is an octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

Features

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- Outputs Source/Sink 24 mA
- HD74ACT240 has TTL-Compatible Inputs

Pin Arrangement



HD74AC240/HD74ACT240

Truth Tables

Inputs

\overline{OE}_1	D	Outputs (Pins 12, 14, 16, 18)
L	L	H
L	H	L
H	X	Z

Inputs

\overline{OE}_2	D	Outputs (Pins 3, 5, 7, 9)
L	L	H
L	H	L
H	X	Z

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

Z : High Impedance

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$
Maximum additional I_{CC}/input (HD74ACT240)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1 V$, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$

AC Characteristics: HD74AC240

Item	Symbol	V _{CC} (V) ^{*1}	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay	t _{PLH}	3.3	1.0	6.0	8.0	1.0	9.0	ns
Data to output		5.0	1.0	4.5	6.5	1.0	7.0	
Propagation delay	t _{PHL}	3.3	1.0	5.0	8.0	1.0	8.5	ns
Data to output		5.0	1.0	4.5	6.0	1.0	6.5	
Output enable time	t _{PZH}	3.3	1.0	6.0	10.5	1.0	11.0	ns
		5.0	1.0	5.0	7.0	1.0	8.0	
Output enable time	t _{PZL}	3.3	1.0	7.0	10.0	1.0	11.0	ns
		5.0	1.0	5.5	8.0	1.0	8.5	
Output disable time	t _{PHZ}	3.3	1.0	7.0	10.0	1.0	10.5	ns
		5.0	1.0	6.5	9.0	1.0	9.5	
Output disable time	t _{PLZ}	3.3	1.0	7.5	10.5	1.0	11.5	ns
		5.0	1.0	6.5	9.0	1.0	9.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT240

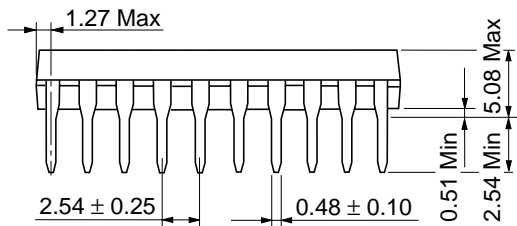
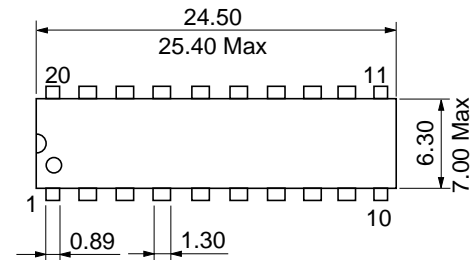
Item	Symbol	V _{CC} (V) ^{*1}	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay Data to output	t _{PLH}	5.0	1.0	6.0	8.5	1.0	9.5	ns
Propagation delay Data to output	t _{PHL}	5.0	1.0	5.5	7.5	1.0	8.5	ns
Output enable time	t _{PZH}	5.0	1.0	7.0	8.5	1.0	9.5	ns
Output enable time	t _{PZL}	5.0	1.0	7.0	9.5	1.0	10.5	ns
Output disable time	t _{PHZ}	5.0	1.0	8.0	9.5	1.0	10.5	ns
Output disable time	t _{PLZ}	5.0	1.0	6.5	10.0	1.0	10.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

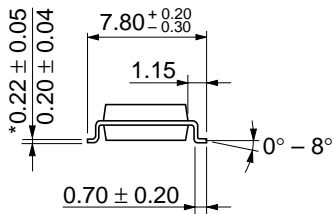
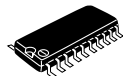
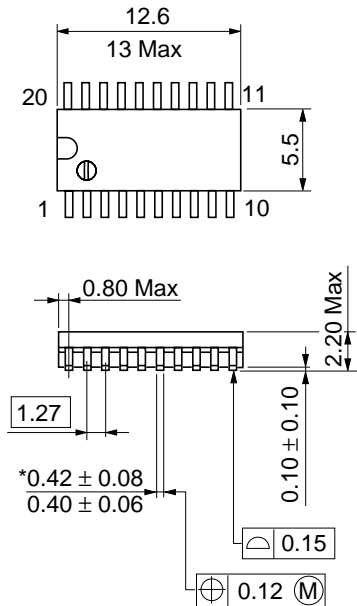
HD74AC240/HD74ACT240

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	45.0	pF	$V_{CC} = 5.0 \text{ V}$

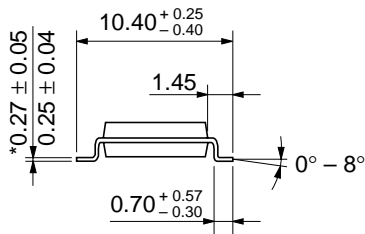
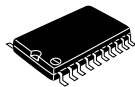
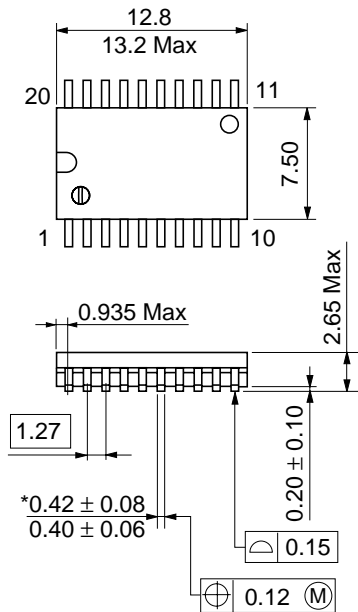


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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