

HD74AC259

8-bit Addressable Latch

REJ03D0264-0200Z
 (Previous ADE-205-385 (Z))
 Rev.2.00
 Jul.16.2004

Description

The HD74AC259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable.

Features

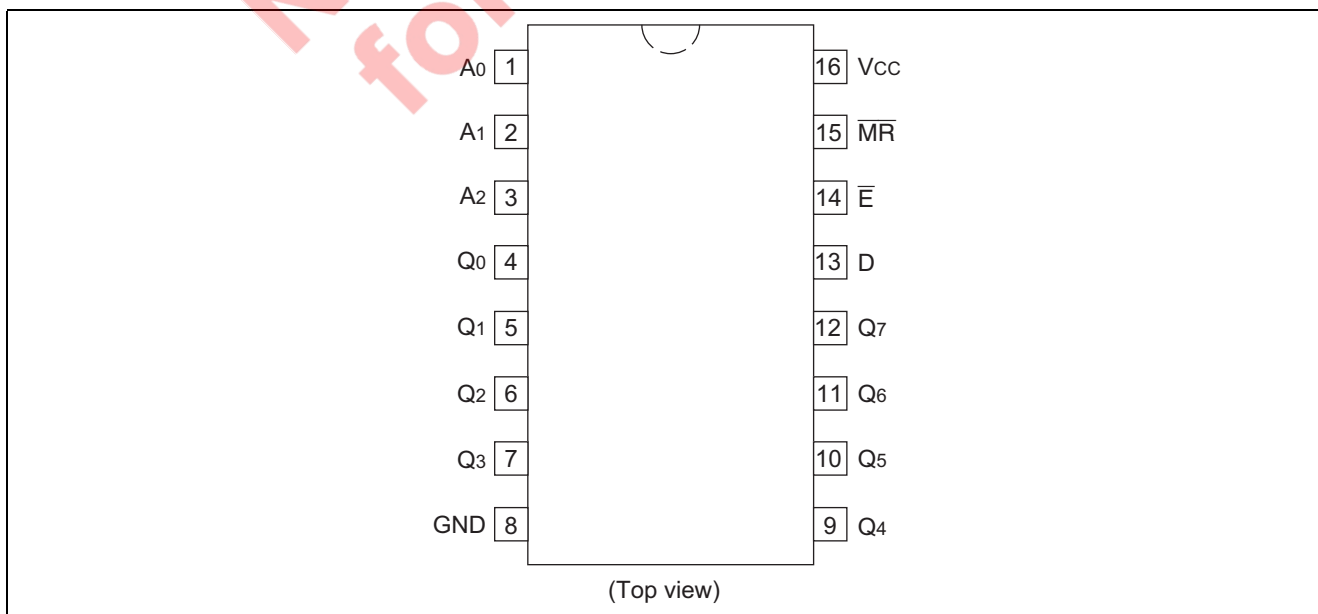
- Serial-to-Parallel Conversion
- Eight Bits of Storage with Output of Each Bit Available
- Random (Addressable) Data Entry
- Active High Demultiplexing or Decoding Capability
- Easily Expandable
- Common Clear
- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC259FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74AC259RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

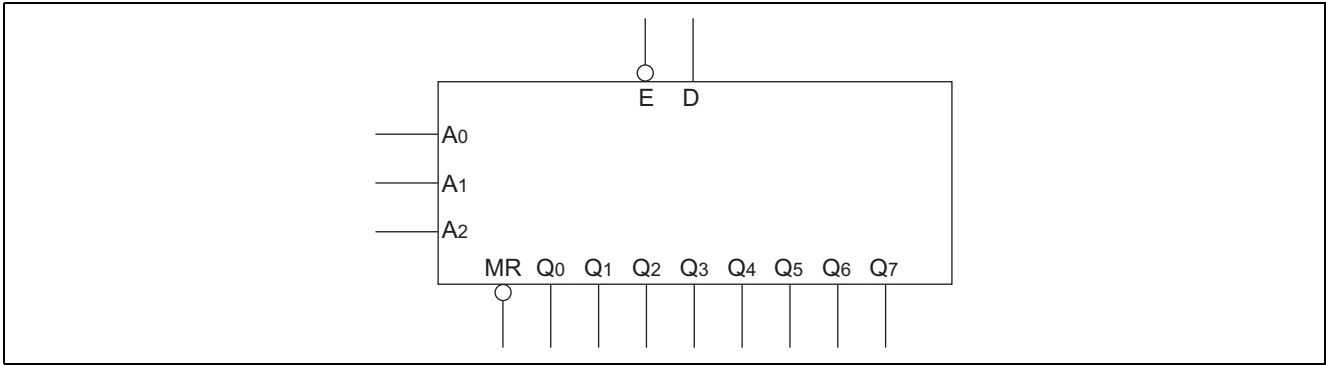
Notes: 1. Please consult the sales office for the above package availability.

2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol

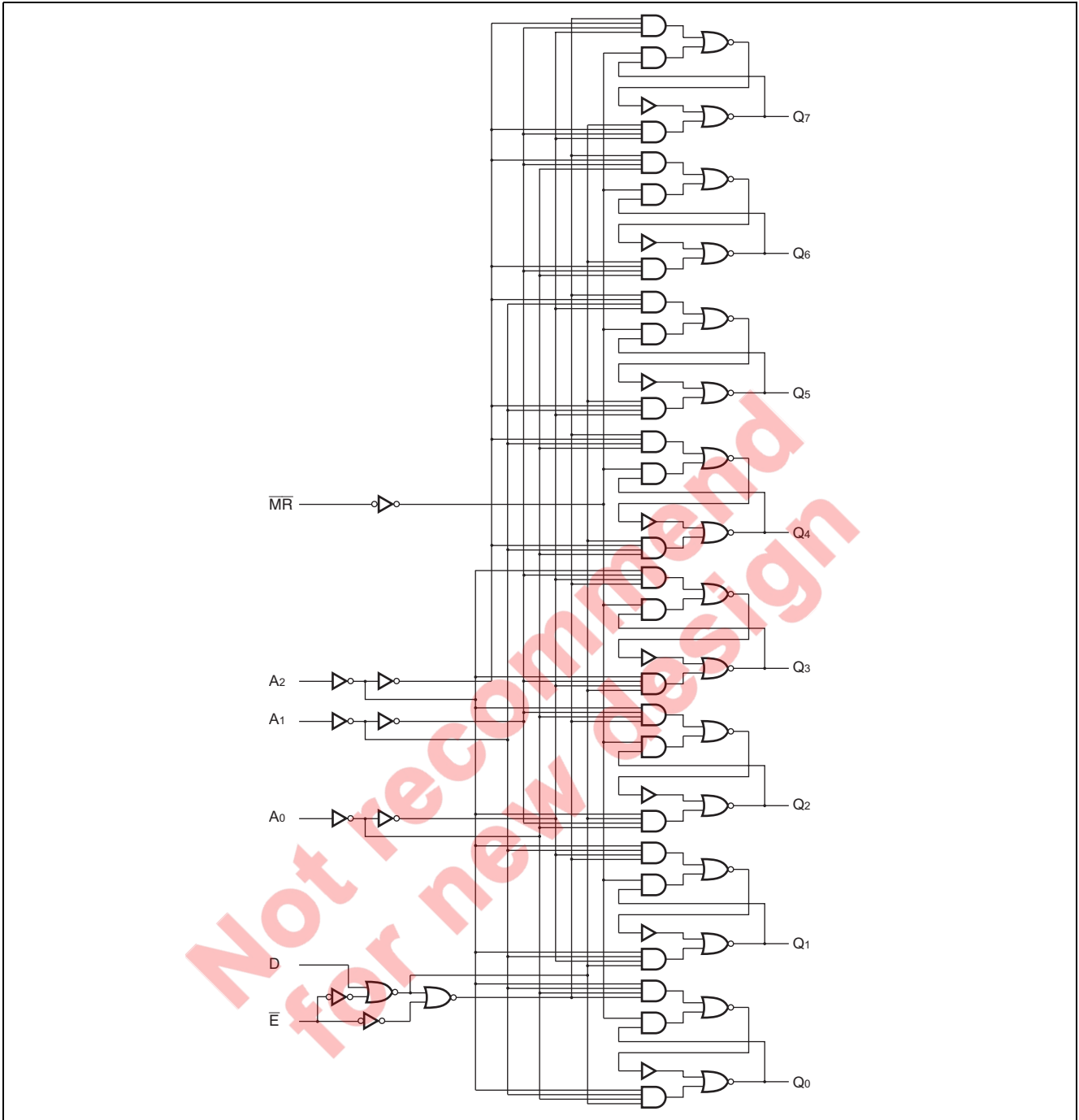


Pin Names

- A₀ – A₂ Address Inputs
- D Data Inputs
- \overline{E} Enable Input (Active LOW)
- \overline{MR} Master Reset (Active LOW)
- Q₀ – Q₇ Latch Outputs

Not recommend
for new design

Logic Diagram



Function Table

Operating Mode	Inputs						Outputs							
	MR	\bar{E}	D	A ₀	A ₁	A ₂	Q ₀	Q ₁	Q ₂	Q ₃	Q ₄	Q ₅	Q ₆	Q ₇
Master reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D = H)	L	L	d	L	L	L	Q = d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q = d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q = d	L	L	L	L	L
	L	L	d	H	H	L	L	L	L	Q = d	L	L	L	L
	L	L	d	L	L	H	L	L	L	L	Q = d	L	L	L
	L	L	d	H	L	H	L	L	L	L	L	Q = d	L	L
	L	L	d	L	H	H	L	L	L	L	L	L	Q = d	L
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q = d
Store (Do nothing)	H	H	X	X	X	X	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
Addressable latch	H	L	d	L	L	L	Q = d	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	L	L	q ₀	Q = d	q ₂	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	H	L	q ₀	q ₁	Q = d	q ₃	q ₄	q ₅	q ₆	q ₇
	H	L	d	H	H	L	q ₀	q ₁	q ₂	Q = d	q ₄	q ₅	q ₆	q ₇
	H	L	d	L	L	H	q ₀	q ₁	q ₂	q ₃	Q = d	q ₅	q ₆	q ₇
	H	L	d	H	L	H	q ₀	q ₁	q ₂	q ₃	q ₄	Q = d	q ₆	q ₇
	H	L	d	L	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	Q = d	q ₇
	H	L	d	H	H	H	q ₀	q ₁	q ₂	q ₃	q ₄	q ₅	q ₆	Q = d

H : High Voltage Level

L : Low Voltage Level

X : Immaterial

d : High or Low data one setup time prior to the Low-to-High Enable transition.

q : Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V _{CC}	-0.5 to 7	V	
DC input diode current	I _{IK}	-20	mA	V _I = -0.5V
		20	mA	V _I = V _{CC} +0.5V
DC input voltage	V _I	-0.5 to V _{CC} +0.5	V	
DC output diode current	I _{OK}	-50	mA	V _O = -0.5V
		50	mA	V _O = V _{CC} +0.5V
DC output voltage	V _O	-0.5 to V _{CC} +0.5	V	
DC output source or sink current	I _O	±50	mA	
DC V _{CC} or ground current per output pin	I _{CC} , I _{GND}	±50	mA	
Storage temperature	T _{stg}	-65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V _{CC}	2 to 6	V	
Input and output voltage	V _I , V _O	0 to V _{CC}	V	
Operating temperature	T _a	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V _{IN} 30% to 70% V _{CC}	tr, tf	8	ns/V	V _{CC} = 3.0V
				V _{CC} = 4.5 V
				V _{CC} = 5.5 V

DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Condition		
			min.	typ.	max.	min.	max.				
Input Voltage	V _{IH}	3.0	2.1	1.5	—	2.1	—	V	V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	3.15	2.25	—	3.15	—				
		5.5	3.85	2.75	—	3.85	—				
	V _{IL}	3.0	—	1.50	0.9	—	0.9		V _{OUT} = 0.1 V or V _{CC} -0.1 V		
		4.5	—	2.25	1.35	—	1.35				
		5.5	—	2.75	1.65	—	1.65				
Output voltage	V _{OH}	3.0	2.9	2.99	—	2.9	—	V	V _{IN} = V _{IL} or V _{IH} I _{OUT} = -50 μA		
		4.5	4.4	4.49	—	4.4	—				
		5.5	5.4	5.49	—	5.4	—				
		3.0	2.58	—	—	2.48	—			V _{IN} = V _{IL} or V _{IH} I _{OH} = -12 mA	
		4.5	3.94	—	—	3.80	—				I _{OH} = -24 mA
		5.5	4.94	—	—	4.80	—				I _{OH} = -24 mA
	V _{OL}	3.0	—	0.002	0.1	—	0.1	V _{IN} = V _{IL} or V _{IH} I _{OUT} = 50 μA			
		4.5	—	0.001	0.1	—	0.1				
		5.5	—	0.001	0.1	—	0.1				
		3.0	—	—	0.32	—	0.37		V _{IN} = V _{IL} or V _{IH} I _{OL} = 12 mA		
		4.5	—	—	0.32	—	0.37			I _{OL} = 24 mA	
		5.5	—	—	0.32	—	0.37			I _{OL} = 24 mA	
Input leakage current	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} = V _{CC} or GND		
Dynamic output current*	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} = 1.1 V		
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85 V		
Quiescent supply current	I _{CC}	5.5	—	—	8.0	—	80	μA	V _{IN} = V _{CC} or ground		

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	3.3	65	—	—	60	—	MHz
		5.0	110	—	—	95	—	
Propagation delay MR to Q _n	t _{PHL}	3.3	1.0	8.5	14.5	1.0	16.5	ns
		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay D _n to Q _n	t _{PLH}	3.3	1.0	7.0	10.5	1.0	12.0	ns
		5.0	1.0	5.5	7.5	1.0	8.5	
Propagation delay D _n to Q _n	t _{PHL}	3.3	1.0	7.0	10.5	1.0	12.0	ns
		5.0	1.0	5.5	7.5	1.0	8.5	
Propagaion delay A _n to Q _n	t _{PLH}	3.3	1.0	11.5	18.5	1.0	21.5	ns
		5.0	1.0	8.0	11.5	1.0	14.0	
Propagation delay A _n to Q _n	t _{PHL}	3.3	1.0	11.5	18.5	1.0	21.0	ns
		5.0	1.0	8.0	11.5	1.0	13.5	
Propagation delay E̅ to Q	t _{PLH}	3.3	1.0	9.0	15.0	1.0	17.0	ns
		5.0	1.0	6.5	9.0	1.0	10.5	
Propagation delay E̅ to Q _n	t _{PHL}	3.3	1.0	9.0	14.0	1.0	16.0	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW D to \bar{E}	t _{SU}	3.3	1.0	3.5	3.5	ns
		5.0	0.0	3.0	3.0	
Hold time, HIGH or LOW D to \bar{E}	t _H	3.3	0.5	2.0	2.0	ns
		5.0	0.5	2.0	2.0	
Setup time, HIGH or LOW A _n to \bar{E}	t _{SU}	3.3	1.0	6.0	7.0	ns
		5.0	0.0	4.5	5.0	
Hold time, HIGH or LOW A _n to \bar{E}	t _H	3.3	-3.0	0.0	0.0	ns
		5.0	-1.0	0.0	0.0	
Pulse width	t _w	3.3	3.0	5.5	7.0	ns
		5.0	3.0	4.5	5.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

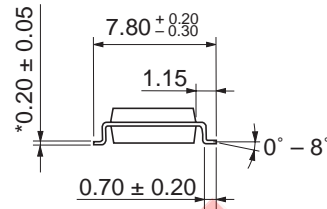
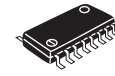
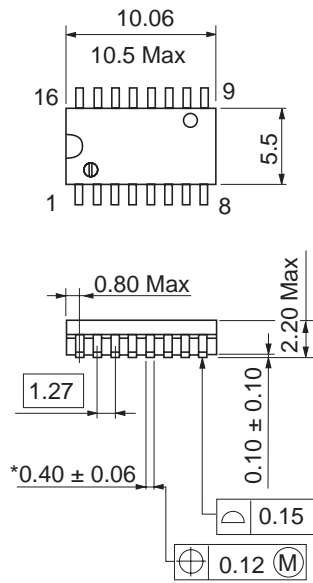
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	35	pF	V _{CC} = 5.0 V

Not recommended
for new designs

Package Dimensions

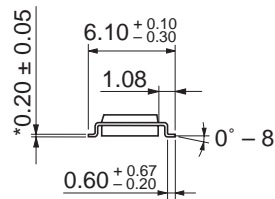
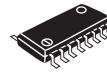
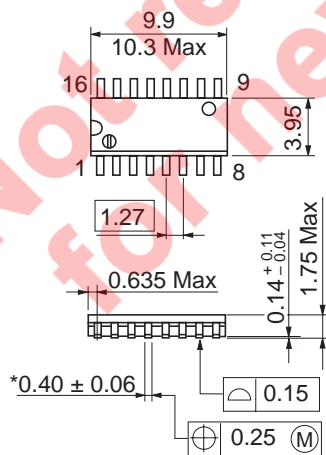
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

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