HD74AC393

Dual Modulo-16-Counter

REJ03D0275–0200Z
(Previous ADE-205-396 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74AC393 contains a pair of high speed 4-stage ripple counters. Each half of the HD74AC393 operates as a modulo-16 binary divider, with the last three stages triggered in a ripple fashion. The flip-flops are triggered by a High-to-Low transition of their $\overline{CP}$ inputs. Each half of each circuit type has a Master Reset input which responds to a High signal by forcing all four outputs to the Low state.

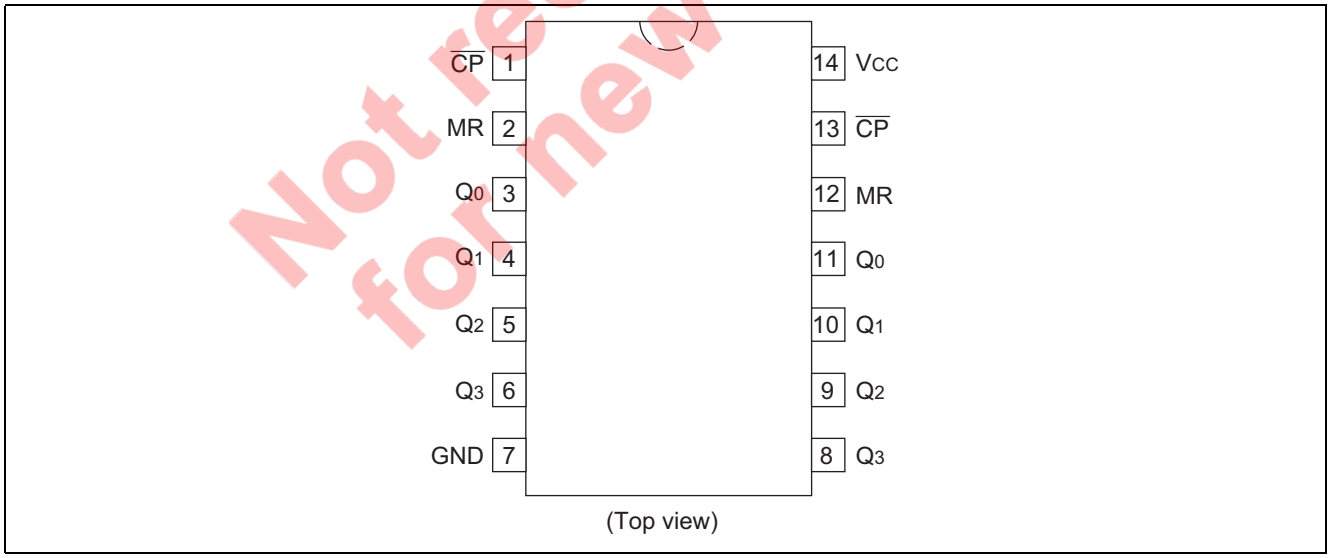
Features

- Outputs Source/Sink 24 mA
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74AC393FPEL	SOP-14 pin (JEITA)	FP-14DAV	FP	EL (2,000 pcs/reel)
HD74AC393RPEL	SOP-14 pin (JEDEC)	FP-14DNV	RP	EL (2,500 pcs/reel)

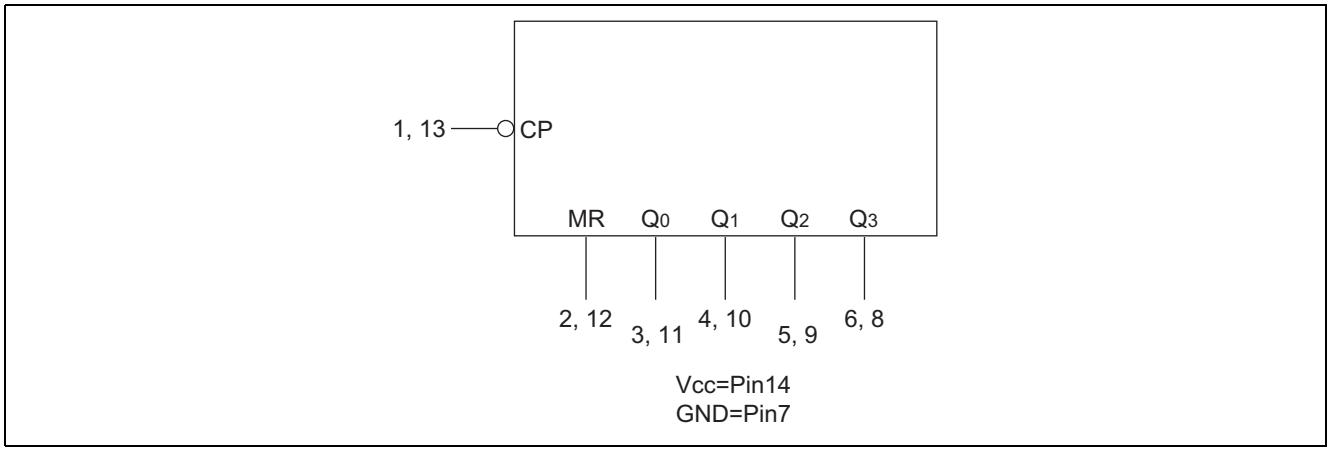
Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



(Top view)

Logic Symbol



Pin Names

$\overline{CP}$	Clock Pulse Input (Active Falling Edge)
MR	Asynchronous Master Reset Input (Active High)
$Q_0 - Q_3$	Flip-flop Outputs

Functional Description

Each half of the HD74AC393 operates in the modulo-16 binary sequence, as indicated in the + 16 Truth Table. The first flip-flop is triggered by High-to-Low transitions of the $\overline{CP}$ input signal. Each of the other flip-flops is triggered by a High-to-Low transition of the Q output of the preceding flip-flop. Thus state changes of the Q outputs do not occur simultaneously. This means that logic signals derived from combinations of these outputs will be subject to decoding spikes and, therefore, should not be used as clocks for other counters, registers or flip-flops. A High signal on MR forces all outputs to the Low state and prevents counting.

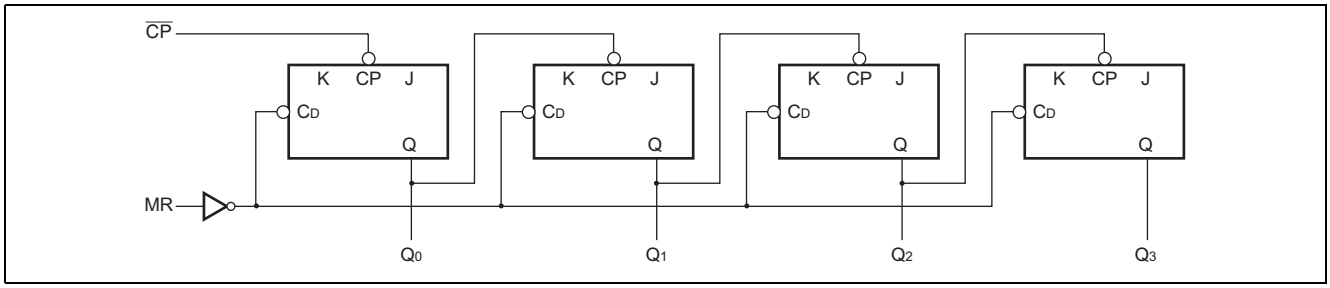
Truth Table

Count	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H : High Voltage Level

L : Low Voltage Level

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	–0.5 to 7	V	
DC input diode current	I_{IK}	–20	mA	V_I = –0.5V
		20	mA	V_I = Vcc+0.5V
DC input voltage	V_I	–0.5 to Vcc+0.5	V	
DC output diode current	I_{OK}	–50	mA	V_O = –0.5V
		50	mA	V_O = Vcc+0.5V
DC output voltage	V_O	–0.5 to Vcc+0.5	V	
DC output source or sink current	I_O	±50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	±50	mA	
Storage temperature	Tstg	–65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 30% to 70% V_{CC}	tr, tf	8	ns/V	V_{CC} = 3.0V
				V_{CC} = 4.5 V
				V_{CC} = 5.5 V

DC Characteristics

Item	Sym-bol	Vcc (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Condition	
			min.	typ.	max.	min.	max.			
Input Voltage	V_{IH}	3.0	2.1	1.5	—	2.1	—	V	V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	3.15	2.25	—	3.15	—			
		5.5	3.85	2.75	—	3.85	—			
	V_{IL}	3.0	—	1.50	0.9	—	0.9		V_{OUT} = 0.1 V or V_{CC} –0.1 V	
		4.5	—	2.25	1.35	—	1.35			
		5.5	—	2.75	1.65	—	1.65			
Output voltage	V_{OH}	3.0	2.9	2.99	—	2.9	—	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = –50 µA	
		4.5	4.4	4.49	—	4.4	—			
		5.5	5.4	5.49	—	5.4	—			
		3.0	2.58	—	—	2.48	—		V_{IN} = V_{IL} or V_{IH}	I_{OH} = –12 mA
		4.5	3.94	—	—	3.80	—			I_{OH} = –24 mA
		5.5	4.94	—	—	4.80	—			I_{OH} = –24 mA
	V_{OL}	3.0	—	0.002	0.1	—	0.1		V_{IN} = V_{IL} or V_{IH} I_{OUT} = 50 µA	
		4.5	—	0.001	0.1	—	0.1			
		5.5	—	0.001	0.1	—	0.1			
		3.0	—	—	0.32	—	0.37		V_{IN} = V_{IL} or V_{IH}	I_{OL} = 12 mA
		4.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
		5.5	—	—	0.32	—	0.37			I_{OL} = 24 mA
Input leakage current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	V_{OLD} = 1.1 V	
	I_{OHD}	5.5	—	—	—	–75	—	mA	V_{OHD} = 3.85 V	
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	µA	V_{IN} = V_{CC} or ground	

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C_L = 50 pF			Ta = –40°C to +85°C C_L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	125	—	—	100	—	MHz
		5.0	150	—	—	125	—	
Propagation delay $\overline{CP}$ to Q_0	t_{PLH}	3.3	1.0	8.5	12.0	1.0	13.0	ns
		5.0	1.0	6.5	9.0	1.0	10.0	
Propagation delay $\overline{CP}$ to Q_0	t_{PHL}	3.3	1.0	8.0	11.5	1.0	12.5	ns
		5.0	1.0	6.0	8.5	1.0	9.5	
Propagation delay $\overline{CP}$ to Q_1	t_{PLH}	3.3	1.0	12.0	15.0	1.0	16.0	ns
		5.0	1.0	9.5	12.0	1.0	13.0	
Propagation delay $\overline{CP}$ to Q_1	t_{PHL}	3.3	1.0	11.5	14.5	1.0	15.5	ns
		5.0	1.0	9.0	11.5	1.0	12.5	
Propagation delay $\overline{CP}$ to Q_2	t_{PLH}	3.3	1.0	15.0	18.0	1.0	19.5	ns
		5.0	1.0	12.0	14.5	1.0	16.0	
Propagation delay $\overline{CP}$ to Q_2	t_{PHL}	3.3	1.0	14.5	17.5	1.0	19.0	ns
		5.0	1.0	11.5	14.0	1.0	15.5	
Propagation delay $\overline{CP}$ to Q_3	t_{PLH}	3.3	1.0	18.0	20.5	1.0	22.0	ns
		5.0	1.0	14.5	17.0	1.0	18.5	
Propagation delay $\overline{CP}$ to Q_3	t_{PHL}	3.3	1.0	17.5	20.5	1.0	21.5	ns
		5.0	1.0	14.0	16.5	1.0	17.5	
Propagation delay MR to Q_0, Q_1, Q_2 or Q_3	t_{PHL}	3.3	1.0	10.5	14.0	1.0	15.0	ns
		5.0	1.0	8.5	11.0	1.0	12.0	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements

Item	Symbol	V_{CC} (V)*1	Ta = +25°C C_L = 50 pF		Ta = –40°C to +85°C C_L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Pulse width $\overline{CP}$	t_w	3.3	3.5	5.5	7.0	ns
		5.0	2.5	4.5	5.0	
Recovery time MR to $\overline{CP}$	t_{rec}	3.3	–2.5	0.0	0.0	ns
		5.0	–2.5	0.0	0.0	

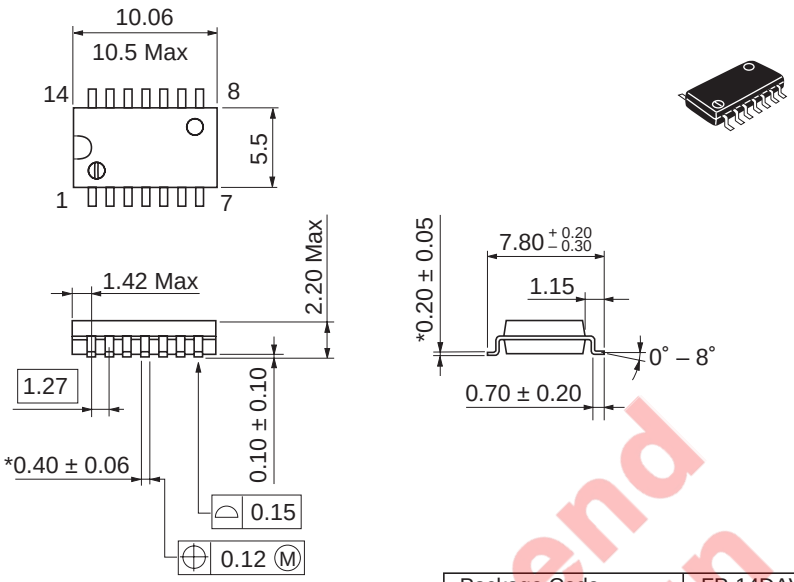
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	V_{CC} = 5.5 V
Power dissipation capacitance	C_{PD}	50	pF	V_{CC} = 5.0 V

Package Dimensions

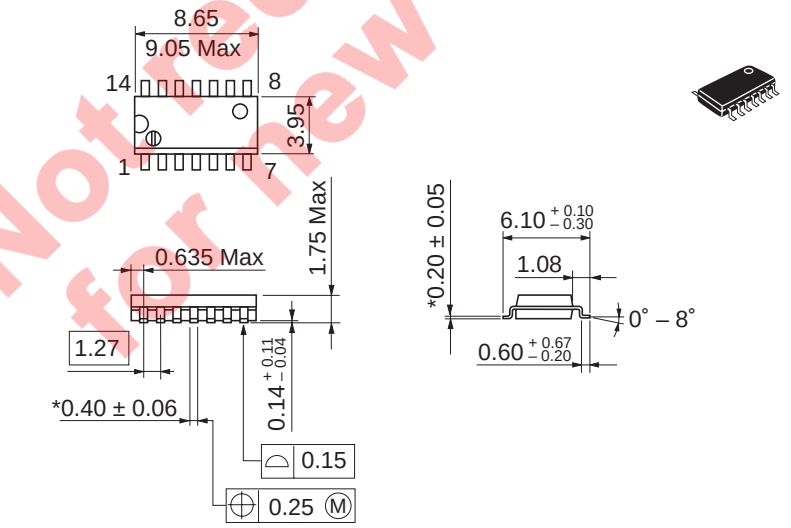
As of January, 2003
Unit: mm



Package Code	FP-14DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.23 g

*Ni/Pd/Au plating

As of January, 2003
Unit: mm



Package Code	FP-14DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.13 g

*Ni/Pd/Au plating

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