
HD74AC539

Dual 1-of-4 Decoder with 3-State Output

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Description

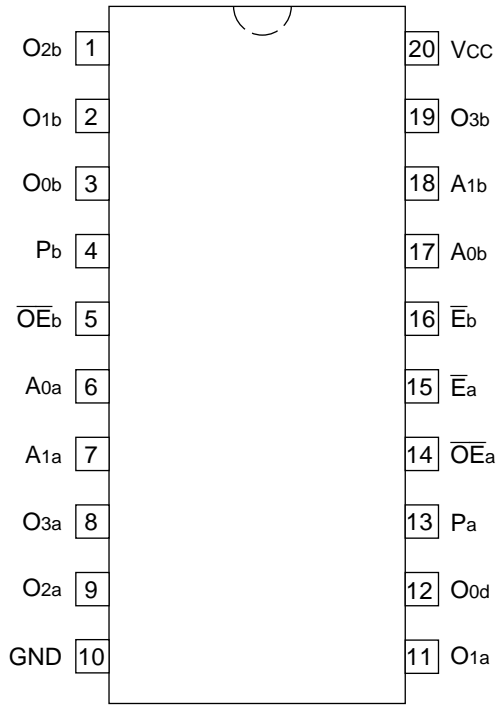
The HD74AC539 contains two independent decoders. Each accepts two Address (A_0 , A_1) input signals and decodes them to select one of four mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active HIGH ($P = L$) or active LOW ($P = H$). An active LOW input Enable (\overline{E}) is available for data demultiplexing; data is routed to the selected output in non-inverted form in the active LOW mode or in inverted form in the active HIGH mode. A HIGH signal on the active LOW Output Enable (\overline{OE}) input forces the 3-state outputs to the high impedance state.

Feature

- Outputs Source/Sink 24 mA

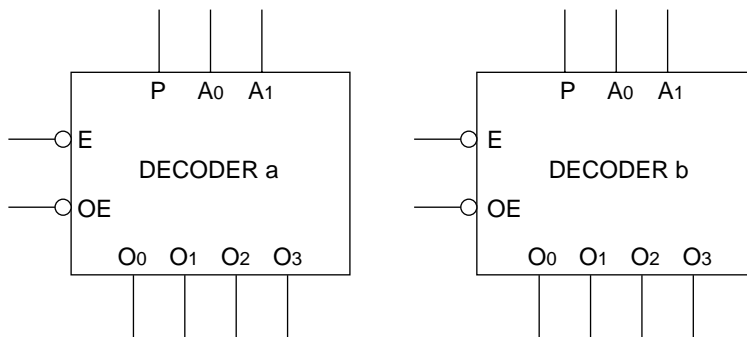
HD74AC539

Pin Arrangement



(Top view)

Logic Symbol



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Pin Names

- A_{0a} to A_{1a} Side A Address Inputs
- A_{0b} to A_{1b} Side B Address Inputs
- \overline{E}_a – \overline{E}_b Enable Inputs (Active LOW)
- \overline{OE}_a , \overline{OE}_b Output Enable Inputs (Active LOW)
- P_a , P_b Polarity Control Inputs
- O_{0a} to O_{3a} Side A 3-State Outputs
- O_{0b} to O_{3b} Side B 3-State Outputs

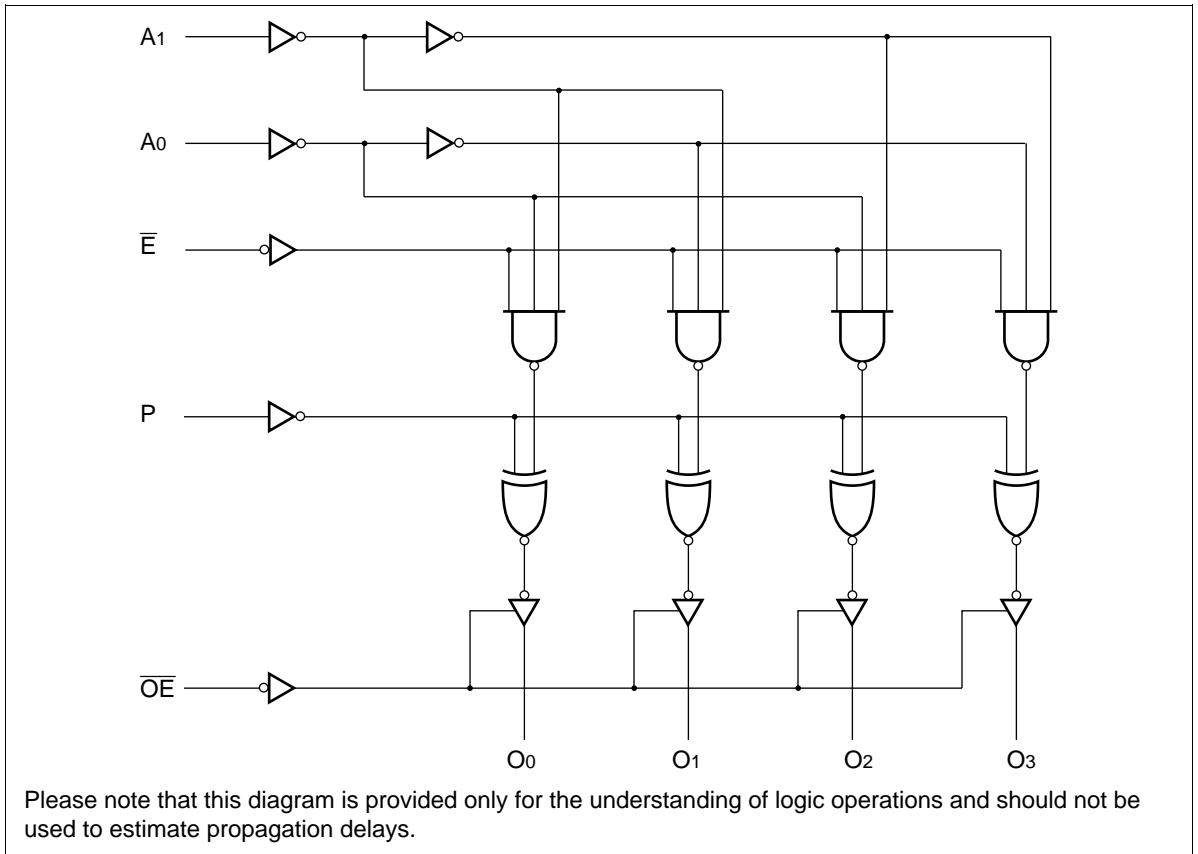
Truth Table

Function	Inputs				Outputs			
	\overline{OE}	\overline{E}	A_1	A_0	O_0	O_1	O_2	O_3
High impedance	H	X	X	X	Z	Z	Z	Z
Disable	L	H	X	X	$O_n = P$			
Active HIGH output ($P = L$)	L	L	L	L	H	L	L	L
	L	L	L	H	L	H	L	L
	L	L	H	L	L	L	H	L
	L	L	H	H	L	L	L	H
Active LOW output ($P = H$)	L	L	L	L	L	H	H	H
	L	L	L	H	H	L	H	H
	L	L	H	L	H	H	L	H
	L	L	H	H	H	H	H	L

- H : High Voltage Level
- L : Low Voltage Level
- X : Immaterial
- Z : High Impedance

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Logic Diagram (one half shown)



DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5 V$, $T_a = 25^\circ C$

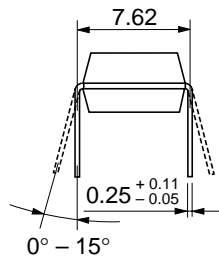
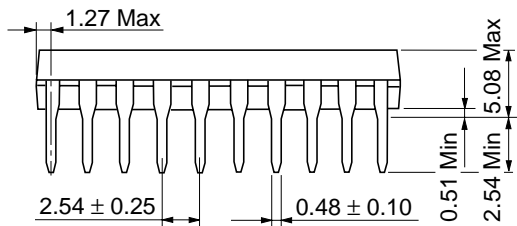
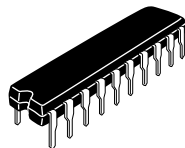
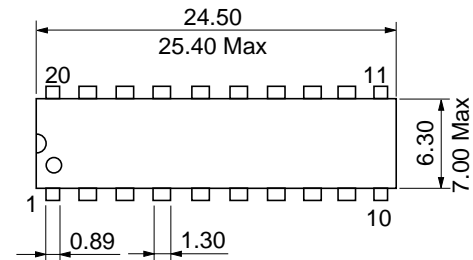
AC Characteristics: HD74AC539

Item	Symbol	V _{CC} (V)* ¹	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Propagation delay A _n to O _n	t _{PLH}	3.3	1.0	—	15.0	1.0	18.0	ns
		5.0	1.0	—	10.0	1.0	12.0	
Propagation delay A _n to O _n	t _{PHL}	3.3	1.0	—	15.0	1.0	18.0	ns
		5.0	1.0	—	10.0	1.0	12.0	
Propagation delay E̅ to O _n	t _{PLH}	3.3	1.0	—	14.5	1.0	16.5	ns
		5.0	1.0	—	9.5	1.0	11.0	
Propagation delay E̅ to O _n	t _{PHL}	3.3	1.0	—	13.5	1.0	15.5	ns
		5.0	1.0	—	9.0	1.0	11.5	
Propagation delay P to O _n	t _{PLH}	3.3	1.0	—	16.0	1.0	19.0	ns
		5.0	1.0	—	11.5	1.0	12.5	
Propagation delay P to O _n	t _{PHL}	3.3	1.0	—	16.0	1.0	19.0	ns
		5.0	1.0	—	11.5	1.0	12.5	
Propagation delay OE̅ to O _n	t _{ZH}	3.3	1.0	—	10.0	1.0	11.5	ns
		5.0	1.0	—	8.0	1.0	9.0	
Propagation delay OE̅ to O _n	t _{ZL}	3.3	1.0	—	9.5	1.0	11.0	ns
		5.0	1.0	—	7.5	1.0	8.5	
Propagation delay OE̅ to O _n	t _{HZ}	3.3	1.0	—	11.5	1.0	13.0	ns
		5.0	1.0	—	9.5	1.0	10.5	
Propagation delay OE̅ to O _n	t _{LZ}	3.3	1.0	—	10.5	1.0	12.0	ns
		5.0	1.0	—	8.5	1.0	9.5	

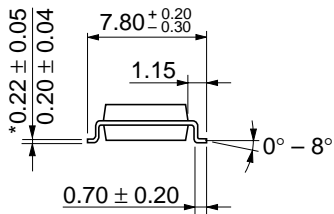
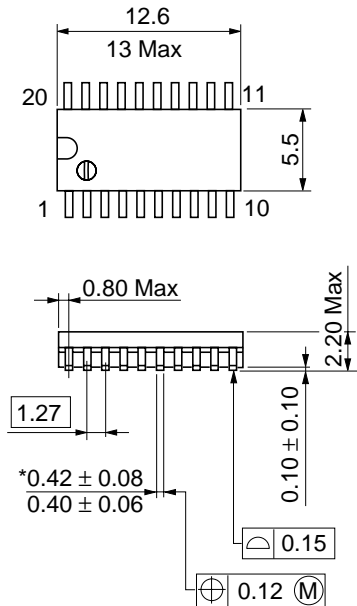
Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	60	pF	V _{CC} = 5.0 V

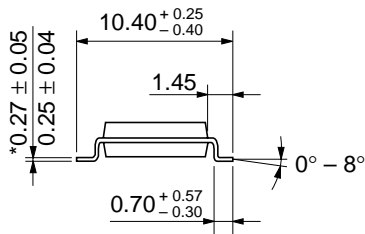
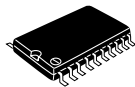
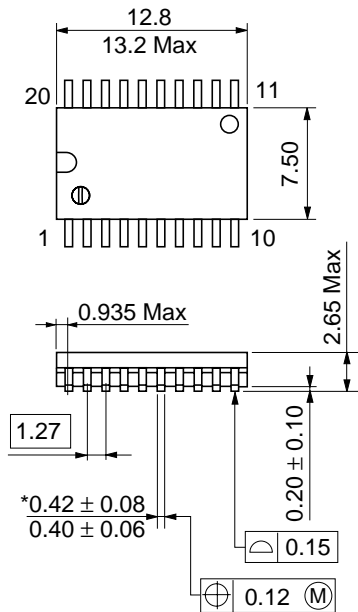


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



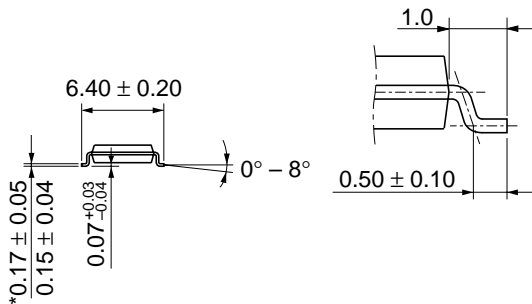
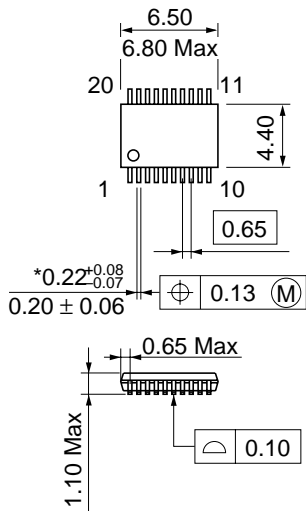
*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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