
HD74AC374/HD74ACT374

Octal D-Type Flip-Flops with 3-State Output

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Description

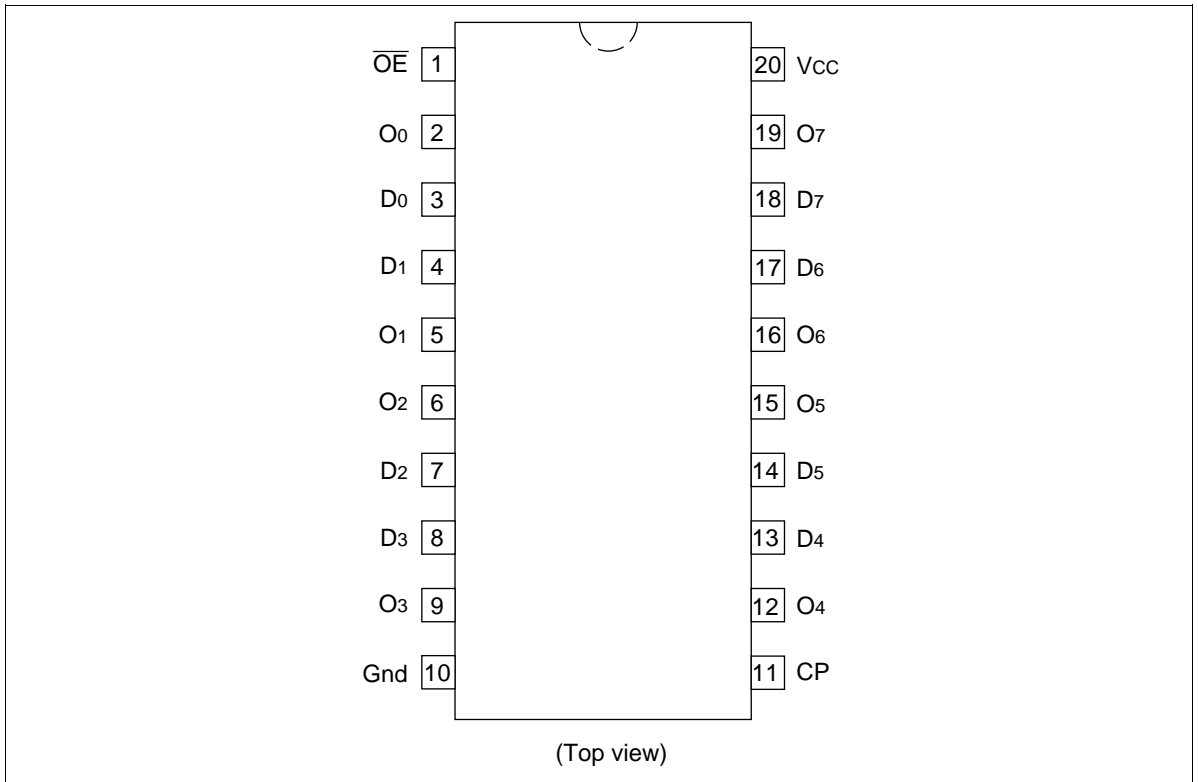
The HD74AC374/HD74ACT374 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable (\overline{OE}) are common to all flip-flops.

Features

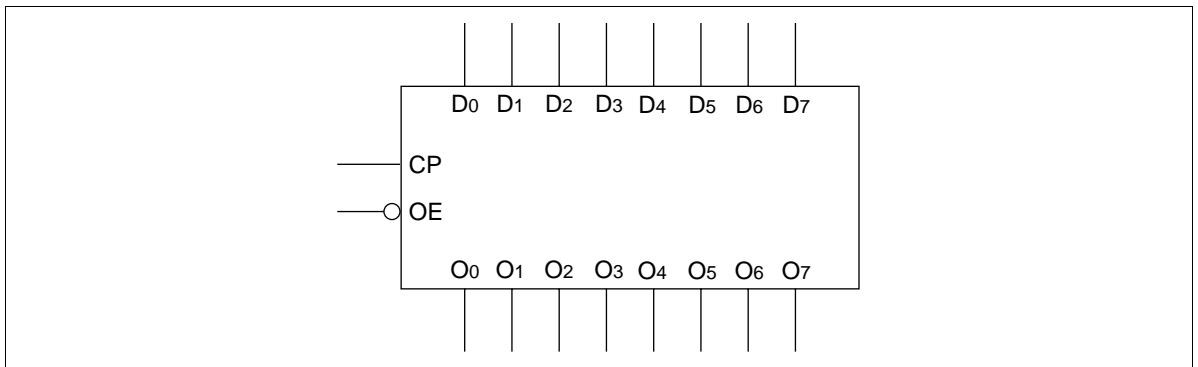
- Buffered Positive Edge-Triggered Clock
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- See HD74AC273/HD74ACT273 for Reset Version
- See HD74AC373/HD74ACT373 for Transparent Latch Version
- See HD74AC574/HD74ACT574 for Broadside Pinout Version
- See HD74AC564/HD74ACT564 for Broadside
- Pinout Version with Inverted Outputs
- HD74ACT374 has TTL-Compatible Inputs

HD74AC374/HD74ACT374

Pin Arrangement



Logic Symbol



Pin Names



- $D_0 - D_7$ Data Inputs
- CP Clock Pulse Input
- \overline{OE} 3-State Output Enable Input
- $O_0 - O_7$ 3-State Outputs

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Functional Description

The HD74AC374/HD74ACT374 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the Low-to-High Clock (CP) transition. With the Output Enable (\overline{OE}) Low, the contents of the eight flip-flops are available at the outputs. When the \overline{OE} is High, the outputs go to the high impedance state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

Truth Table


Inputs			Outputs
D_n	CP	\overline{OE}	O_n
H		L	H
L		L	L
X	X	H	Z

H : High Voltage Level

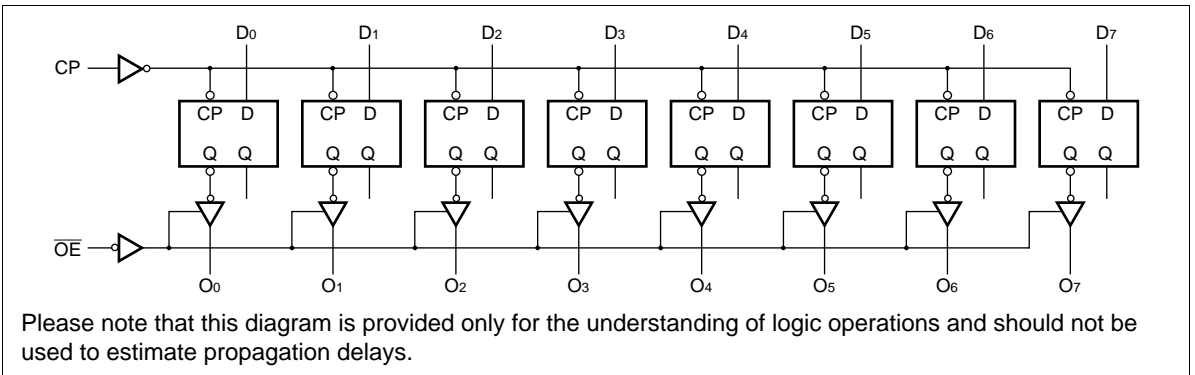
L : Low Voltage Level

X : Immaterial

Z : High Impedance

 : Low-to-High Transition

Logic Diagram



HD74AC374/HD74ACT374

DC Characteristics (unless otherwise specified)

Item	Symbol	Max	Unit	Condition
Maximum quiescent supply current	I_{CC}	80	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$
Maximum quiescent supply current	I_{CC}	8.0	μA	$V_{IN} = V_{CC}$ or ground, $V_{CC} = 5.5\text{ V}$, $T_a = 25^\circ\text{C}$
Maximum I_{CC}/input (HD74ACT374)	I_{CCT}	1.5	mA	$V_{IN} = V_{CC} - 2.1\text{ V}$, $V_{CC} = 5.5\text{ V}$, $T_a = \text{Worst case}$

AC Characteristics: HD74AC374

Item	Symbol	$V_{CC} (\text{V})^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50\text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50\text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f_{max}	3.3	60	110	—	60	—	MHz
		5.0	100	155	—	100	—	
Propagation delay CP to O_n	t_{PLH}	3.3	1.0	11.0	13.5	1.0	15.5	ns
		5.0	1.0	8.0	9.5	1.0	10.5	
Propagation delay CP to O_n	t_{PHL}	3.3	1.0	10.0	12.5	1.0	14.0	ns
		5.0	1.0	7.0	9.0	1.0	10.0	
Output enable time	t_{PZH}	3.3	1.0	9.5	11.5	1.0	13.0	ns
		5.0	1.0	7.0	8.5	1.0	9.5	
Output enable time	t_{PZL}	3.3	1.0	9.0	11.5	1.0	13.0	ns
		5.0	1.0	6.5	8.5	1.0	9.5	
Output disable time	t_{PHZ}	3.3	1.0	10.5	12.5	1.0	14.5	ns
		5.0	1.0	8.0	11.0	1.0	12.5	
Output disable time	t_{PLZ}	3.3	1.0	8.0	11.5	1.0	12.5	ns
		5.0	1.0	6.5	8.5	1.0	10.0	

Note: 1. Voltage Range 3.3 is $3.3\text{ V} \pm 0.3\text{ V}$
Voltage Range 5.0 is $5.0\text{ V} \pm 0.5\text{ V}$

AC Operating Requirements: HD74AC374

Item	Symbol	V _{CC} (V)*1	Ta = +25°C	Ta = -40°C		Unit
			C _L = 50 pF	to +85°C	C _L = 50 pF	
			Typ	Guaranteed Minimum		
Setup time, HIGH or LOW	t _{su}	3.3	2.0	5.5	6.0	ns
D _n to CP		5.0	1.0	4.0	4.5	
Hold time, HIGH or LOW	t _h	3.3	-1.0	1.0	1.0	ns
D _n to CP		5.0	-4.0	1.5	1.5	
CP pulse width, HIGH or LOW	t _w	3.3	4.0	5.5	6.0	ns
		5.0	2.5	4.0	4.5	

Note: 1. Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Characteristics: HD74ACT374

Item	Symbol	V _{CC} (V)*1	Ta = +25°C			Ta = -40°C to +85°C		Unit
			C _L = 50 pF			C _L = 50 pF		
			Min	Typ	Max	Min	Max	
Maximum clock frequency	f _{max}	5.0	100	160	—	90	—	MHz
Propagation delay CP to O _n	t _{PLH}	5.0	1.0	8.5	10.0	1.0	11.5	ns
Propagation delay CP to O _n	t _{PHL}	5.0	1.0	8.0	9.5	1.0	11.0	ns
Output enable time	t _{PZH}	5.0	1.0	8.0	9.5	1.0	10.5	ns
Output enable time	t _{PZL}	5.0	1.0	8.0	9.0	1.0	10.5	ns
Output disable time	t _{PHZ}	5.0	1.0	8.5	11.5	1.0	12.5	ns
Output disable time	t _{PLZ}	5.0	1.0	7.0	8.5	1.0	10.0	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

HD74AC374/HD74ACT374

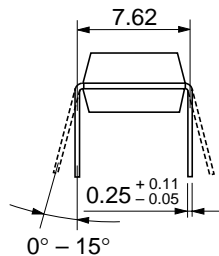
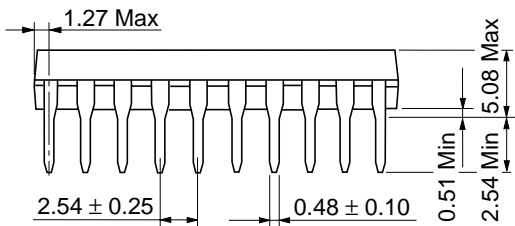
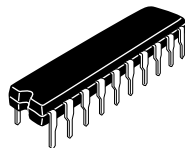
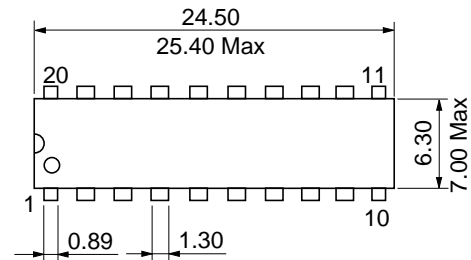
AC Operating Requirements: HD74ACT374

Item	Symbol	V_{CC} (V)*1	Ta = +25°C CL = 50 pF		Ta = -40°C to +85°C CL = 50 pF		Unit
			Typ	Guaranteed Minimum	Guaranteed Minimum	Guaranteed Minimum	
Setup time, HIGH or LOW D _n to CP	t _{su}	5.0	1.0	7.0	5.5	ns	
Hold time, HIGH or LOW D _n to CP	t _h	5.0	0.0	1.5	1.5	ns	
CP pulse width, HIGH or LOW	t _w	5.0	2.0	7.0	5.0	ns	

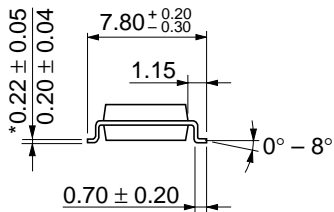
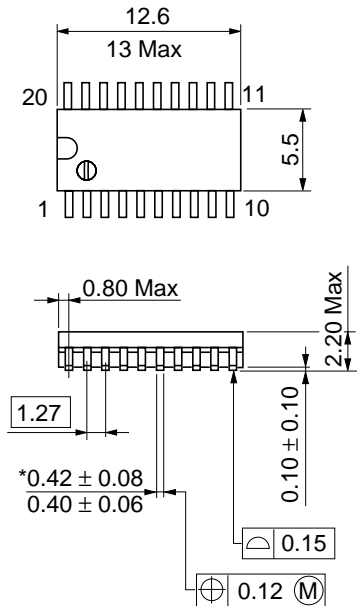
Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C _{IN}	4.5	pF	V _{CC} = 5.5 V
Power dissipation capacitance	C _{PD}	80.0	pF	V _{CC} = 5.0 V

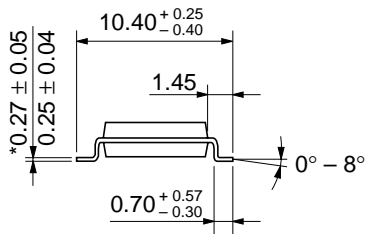
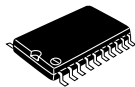
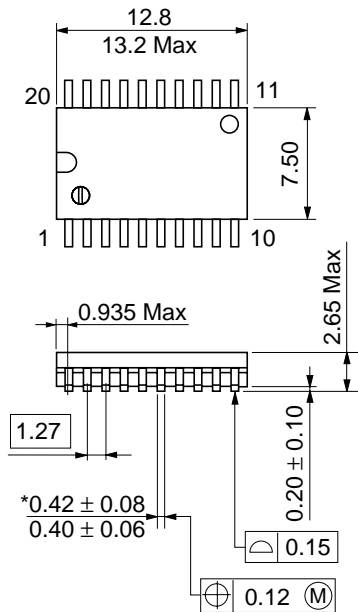


Hitachi Code	DP-20N
JEDEC	—
EIAJ	Conforms
Weight (reference value)	1.26 g



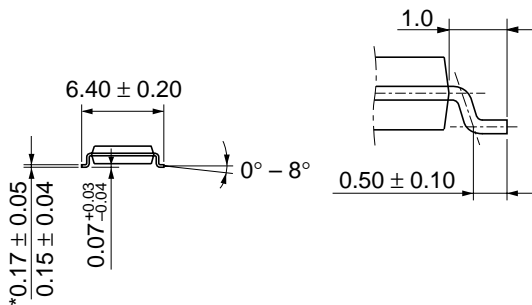
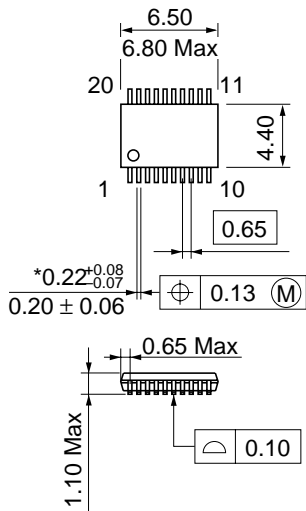
Hitachi Code	FP-20DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.31 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-20DB
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.52 g

*Dimension including the plating thickness
 Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-20DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.07 g

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