

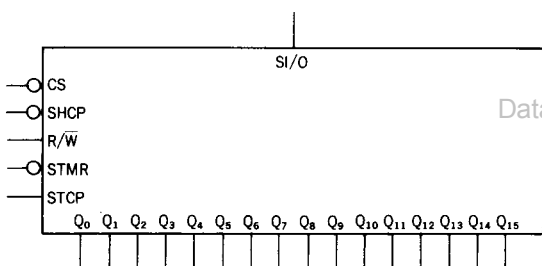
# HD74AC673/HD74ACT673 • 16-Bit Serial-In Serial/Parallel-Out Shift Register

## Description

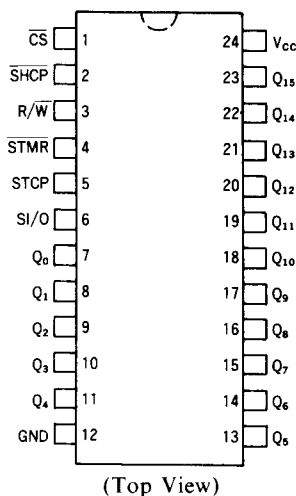
The 'AC673 contains a 16-bit serial-out shift register and a 16-bit parallel-out storage register. A single pin serves either as an input for serial entry or as a 3-state serial output. In the Serial-out mode, the data recirculates in the shift register. By means of a separate clock, The contents of the shift register are transferred to the storage register for parallel outputting. The contents of the storage register can also be parallel loaded back into the shift register. A HIGH signal on the Chip Select input prevents both shifting and parallel transfer. The storage register may be cleared via STMR.

- Serial-to-Parallel Converter
- 16-Bit Serial I/O Shift Register
- 16-Bit Parallel-Out Storage Register
- Recirculating Serial Shifting
- Recirculating Parallel Transfer
- Common Serial Data I/O Pin
- Outputs Source/sink 24mA
- HD74ACT673 has TTL Compatible Outputs

## Logic Symbol



## Pin Assignment



## Pin Names

- CS Chip Select Input (Active LOW)
- SHCP Shift Clock Pulse Input (Active Falling Edge)
- STMR Store Master Reset Input (Active LOW)
- STCP Store Clock Pulse Input
- R/W Read/Write Input
- SI/O Serial Data input or  
3-State Serial Output
- Q<sub>0</sub>-Q<sub>15</sub> Parallel Data Outputs

## Functional Description

The 16-bit shift register operates in one of four modes, as indicated in the Shift Register Operations Table. A HIGH signal on the Chip Select ( $\overline{CS}$ ) input prevents clocking and forces the Serial Input/Output (SI/O) 3-state buffer into the high impedance state. During serial shift-out operations, the SI/O buffer is active (i.e., enabled) and the output data is also recirculated back into the shift register. When parallel loading the shift register from the storage register, serial shifting is inhibited.

The storage register has an asynchronous master reset ( $\overline{STMR}$ ) input that overrides all other inputs and forces the Q<sub>0</sub>-Q<sub>15</sub> outputs LOW. The storage register is in the Hold mode when either  $\overline{CS}$  or the Read/Write (R/W) input is HIGH. With  $\overline{CS}$  and R/W both LOW, the storage register is parallel loaded from the shift register.

Shift Register Operations Table

Control Inputs				SI/O Status	Operating Mode
$\overline{CS}$	$R/\overline{W}$	$\overline{SHCP}$	STCP		
H	X	X	X	High Z	Hold
L	L	X	X	Data In	Serial Load
L	H	↓	L	Data Out	Serial Output with Recirculation
L	H	↓	H	Active	Parallel Load; No Shifting

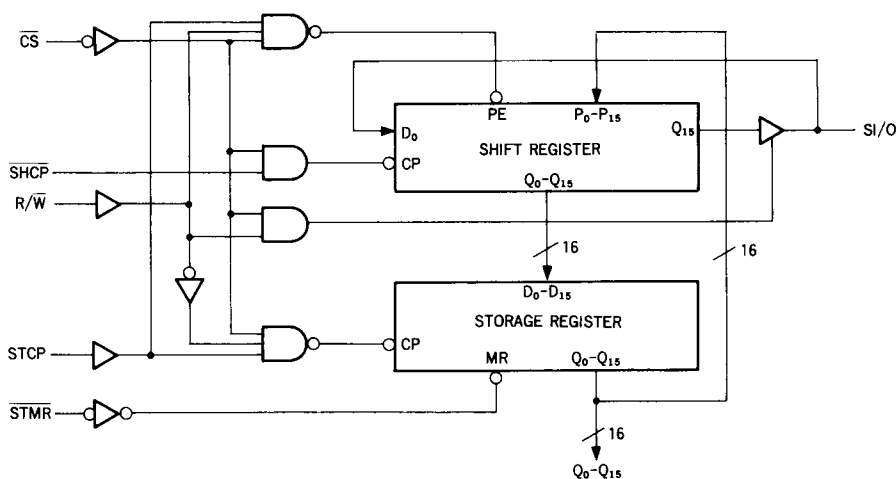
H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↓ = HIGH-to-LOW Transition

Storage Register Operations Table

Control Inputs				Operating Mode
STMR	$\overline{CS}$	$R/\overline{W}$	STCP	
L	X	X	X	Reset; Output
H	H	X	X	Hold
H	X	H	X	Hold
H	L	L	↑	Parallel Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↑ = LOW-to-HIGH Transition

Block Diagram



DC Characteristics (unless otherwise specified)

Symbol	Parameter	Max	Unit	Condition
$I_{CC}$	Maximum Quiescent Supply Current	80	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$ , $T_a = \text{Worst Case}$
$I_{CC}$	Maximum Quiescent Supply Current	8.0	$\mu A$	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5V$ , $T_a = 25^\circ C$
$I_{CC7}$	Maximum Additional $I_{CC}$ /Input (HD74ACT673)	1.5	mA	$V_{IN} = V_{CC} - 2.1V$ , $V_{CC} = 5.5V$ , $T_a = \text{Worst Case}$

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## AC Characteristics: HD74AC673

Symbol	Parameter	V <sub>cc</sub> * (V)	Ta = +25°C C <sub>L</sub> = 50pF			Ta = -40°C to +85°C C <sub>L</sub> = 50pF		Unit
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	3.3 5.0	1.0 1.0			1.0 1.0		ns
t <sub>PHL</sub>	Propagation Delay STMR to Qn	3.3 5.0	1.0 1.0		16.0 11.5	1.0 1.0	18.0 13.0	ns
t <sub>PLH</sub>	Propagation Delay STCP to Qn	3.3 5.0	1.0 1.0		19.0 13.5	1.0 1.0	21.5 15.5	ns
t <sub>PHL</sub>	Propagation Delay STCP to Qn	3.3 5.0	1.0 1.0		19.0 13.5	1.0 1.0	21.5 15.5	ns
t <sub>PLH</sub>	Propagation Delay SHCP to SI/O	3.3 5.0	1.0 1.0		21.5 15.5	1.0 1.0	24.5 17.5	ns
t <sub>PHL</sub>	Propagation Delay SHCP to SI/O	3.3 5.0	1.0 1.0		21.5 15.5	1.0 1.0	24.5 17.5	ns
t <sub>PZH</sub>	Enable Time CS or R/W to SI/O	3.3 5.0	1.0 1.0		14.0 10.0	1.0 1.0	15.5 11.0	ns
t <sub>PZL</sub>	Enable Time CS or R/W to SI/O	3.3 5.0	1.0 1.0		12.0 8.5	1.0 1.0	13.5 9.5	ns
t <sub>PHZ</sub>	Disable Time CS or R/W to SI/O	3.3 5.0	1.0 1.0		17.0 12.0	1.0 1.0	19.0 13.5	ns
t <sub>PLZ</sub>	Disable Time CS or R/W to SI/O	3.3 5.0	1.0 1.0		16.0 11.5	1.0 1.0	18.0 13.0	ns

\* Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

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## AC Operating Requirements: HD74AC673

Symbol	Parameter	V <sub>cc</sub> * (V)	Ta +25°C C <sub>L</sub> = 50pF		Ta = -40°C +85°C C <sub>L</sub> = 50pF		Unit
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW CS or R/W to STCP	3.3 5.0		4.5 4.0	5.0 4.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW CS or R/W to STCP	3.3 5.0		2.0 2.0	2.0 2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW SI/O to SHCP	3.3 5.0		4.5 4.0	5.0 4.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW SI/O to SHCP	3.3 5.0		2.0 2.0	2.0 2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW R/W or CS to SHCP	3.3 5.0		4.5 4.0	5.0 4.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW R/W or CS to SHCP	3.3 5.0		2.0 2.0	2.0 2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW STCP to SHCP	3.3 5.0		4.5 4.0	5.0 4.5		ns
t <sub>h</sub>	Hold Time, HIGH or LOW STCP to SHCP	3.3 5.0		2.0 2.0	2.0 2.0		ns
t <sub>w</sub>	Pulse Width, HIGH or LOW	3.3 5.0		5.5 4.5	6.0 5.0		ns
t <sub>rec</sub>	Recovery Time, STMR to STCP	3.3 5.0		2.0 2.0	2.0 2.0		ns

\* Voltage Range 3.3 is 3.0V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

## AC Characteristics: HD74ACT673

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50pF			Ta = -40°C to +85°C CL = 50pF		Unit
			Min	Typ	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	5.0	70			60		ns
t <sub>PHL</sub>	Propagation Delay STMR to Qn	5.0	1.0		13.0	1.0	14.5	ns
t <sub>PLH</sub>	Propagation Delay STCP to Qn	5.0	1.0		14.5	1.0	16.5	ns
t <sub>PHL</sub>	Propagation Delay STCP to Qn	5.0	1.0		14.5	1.0	16.5	ns
t <sub>PLH</sub>	Propagation Delay SHCP to SI/O	5.0	1.0		16.5	1.0	19.0	ns
t <sub>PHL</sub>	Propagation Delay SHCP to SI/O	5.0	1.0		16.5	1.0	19.0	ns
t <sub>PZH</sub>	Enable Time CS or R/W to SI/O	5.0	1.0		11.5	1.0	13.0	ns
t <sub>PZL</sub>	Enable Time CS or R/W to SI/O	5.0	1.0		10.0	1.0	11.5	ns
t <sub>PHZ</sub>	Disable Time CS or R/W to SI/O	5.0	1.0		14.0	1.0	16.0	ns
t <sub>PLZ</sub>	Disable Time CS or R/W to SI/O	5.0	1.0		13.5	1.0	15.5	ns

\* Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements: HD74ACT673

Symbol	Parameter	Vcc* (V)	Ta = +25°C CL = 50 pF		Ta = -55°C to 125°C CL = 50 pF		Unit
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW CS or R/W to STCP	5.0		6.0	7.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW CS or R/W to STCP	5.0		2.0	2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW SI/O to SHCP	5.0		6.0	7.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW SI/O to SHCP	5.0		2.0	2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW R/W or CS to SHCP	5.0		6.0	7.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW R/W or CS to SHCP	5.0		2.0	2.0		ns
t <sub>s</sub>	Setup Time, HIGH or LOW STCP to SHCP	5.0		6.0	7.0		ns
t <sub>h</sub>	Hold Time, HIGH or LOW STCP to SHCP	5.0		2.0	2.0		ns
t <sub>w</sub>	Pulse Width, HIGH or LOW	5.0		7.0	8.0		ns
t <sub>rec</sub>	Recovery Time, STMR to STCP	5.0		2.0	2.0		ns

\* Voltage Range 5.0 is 5.0V ± 0.5V

## HD74AC673/HD74ACT673

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### Capacitance

Symbol	Parameter	Typ	Unit	Condition
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC}=5.5V$
$C_{PD}$	Power Dissipation Capacitance		pF	$V_{CC}=5.5V$
$C_{I/O}$	Input/Output Capacitance	15.0	pF	$V_{CC}=5.0V$

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