
HD74ALVCH162270

12-bit to 24-bit Registered Bus Exchanger with 3-state Outputs

REJ03D0051-0300Z
(Previous ADE-205-178A(Z))
Rev.3.00
Oct.02.2003

Description

The HD74ALVCH162270 is used in applications where data must be transferred from a narrow high speed bus to a wide lower frequency bus. The device provides synchronous data exchange between the two ports. Data is stored in the internal registers on the low to high transition of the clock (CLK) input when the appropriate CLKEN inputs are low. The select (\overline{SEL}) line selects 1B or 2B data for the A outputs. For data transfer in the A to B direction, a two stage pipeline is provided in the A to 1B path, with a single storage register in the A to 2B path. Proper control of the \overline{CLKENA} inputs allows two sequential 12-bit words to be presented synchronously as a 24-bit word on the B port. Data flow is controlled by the active low output enables (\overline{OEA} , \overline{OEB}). The control terminals are registered to synchronize the bus direction changes with CLK. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26 Ω resistors to reduce overshoot and undershoot.

Features

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 12 \text{ mA}$ (@ $V_{CC} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26 Ω series resistors, so no external resistors are required.

Function Table

Inputs			Outputs	
CLK	\overline{OEA}	\overline{OEB}	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

Output enable

Inputs			Outputs		
CLKENA1	CLKENA2	CLK	A	1B	2B
X	H	↑	L	1B ₀ ^{*1,2}	2B ₀ ^{*1}
X	H	↑	H	1B ₀ ^{*1,2}	2B ₀ ^{*1}
L	L	↑	L	L ^{*2}	L
L	L	↑	H	H ^{*2}	H
H	L	↑	L	1B ₀ ^{*1}	L
H	L	↑	H	1B ₀ ^{*1}	H
H	H	X	X	1B ₀ ^{*1}	2B ₀ ^{*1}

A- to-B storage ($\overline{OEB} = L$)

Note: This functional table describes the case of transferring the same data for A to 1B path. For the case of transferring different data, see logic diagrams.

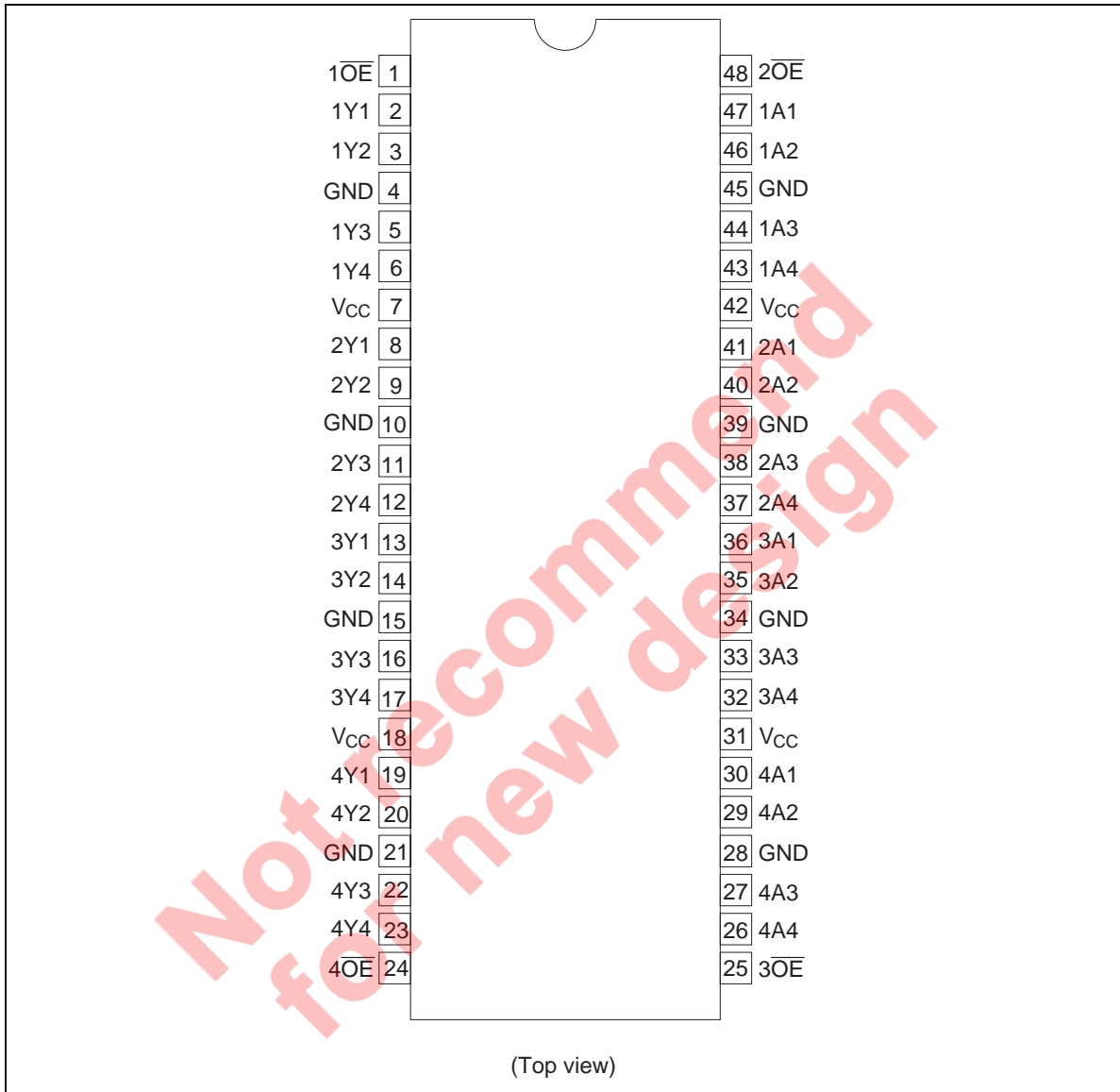
Inputs						Output A
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	
H	X	X	H	X	X	A ₀ ^{*1}
X	H	X	L	X	X	A ₀ ^{*1}
L	X	↑	H	L	X	L
L	X	↑	H	H	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

B-to-A storage ($\overline{OEA} = L$)

- H : High level
- L : Low level
- X : Immaterial
- Z : High impedance
- ↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.
 2. Two CLK edges are needed to propagate data.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 4.6	V	
Input voltage ^{*1, 2}	V_I	-0.5 to 4.6	V	Except I/O ports
		-0.5 to $V_{CC} + 0.5$		I/O ports
Output voltage ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 50	mA	$V_O = 0$ to V_{CC}
V_{CC} , GND current / pin	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3}	P_T	1	W	TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

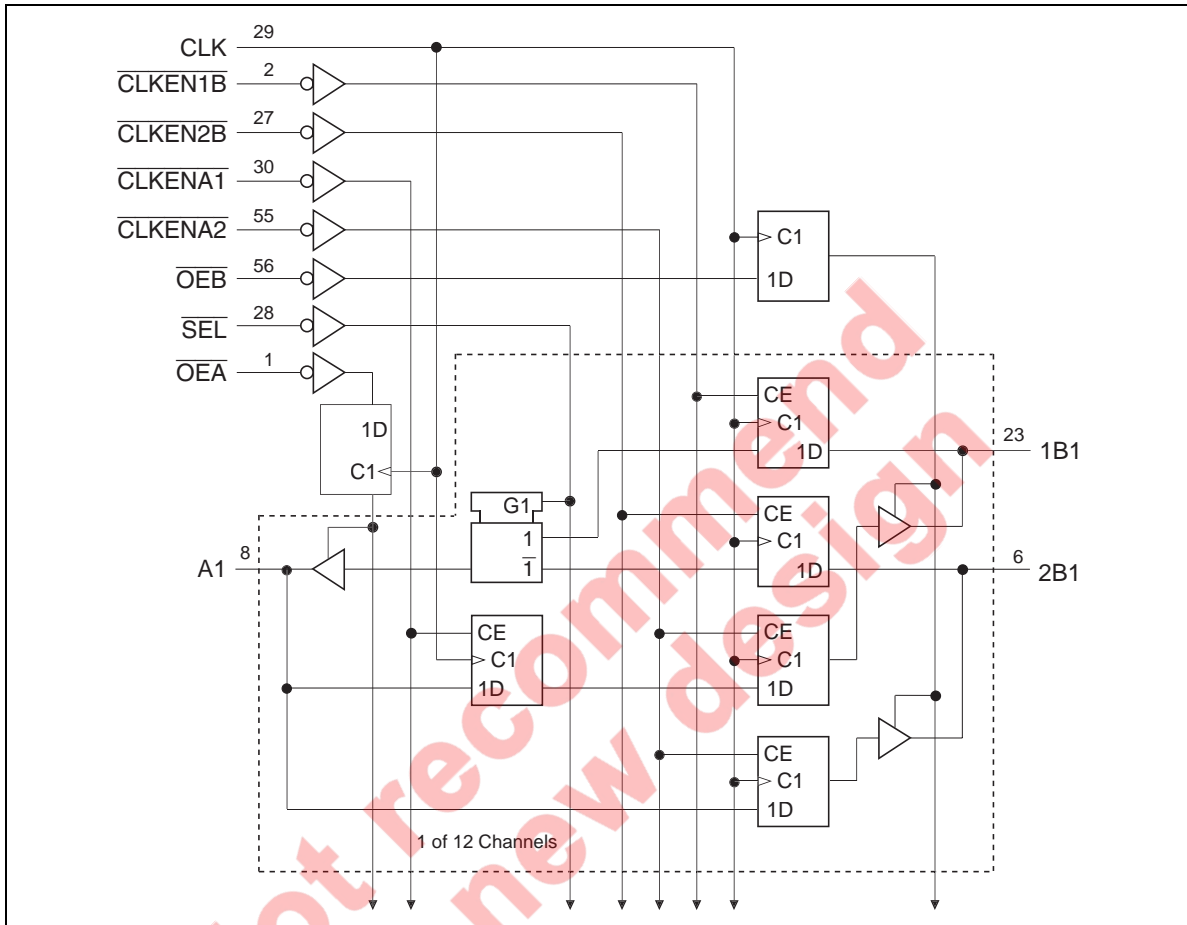
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	-6	mA	$V_{CC} = 2.3\text{ V}$
			-8		$V_{CC} = 2.7\text{ V}$
			-12		$V_{CC} = 3.0\text{ V}$
Low level output current	I_{OL}	—	6	mA	$V_{CC} = 2.3\text{ V}$
			8		$V_{CC} = 2.7\text{ V}$
			12		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Max	Unit	Test Conditions			
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	V _{IL}	2.3 to 2.7	—	0.7					
		2.7 to 3.6	—	0.8					
Output voltage	V _{OH}	2.3 to 3.6	V _{CC} -0.2	—	V	I _{OH} = -100 μA			
		2.3	1.9	—		I _{OH} = -4 mA, V _{IH} = 1.7 V			
		2.3	1.7	—		I _{OH} = -6 mA, V _{IH} = 1.7 V			
		3.0	2.4	—		I _{OH} = -6 mA, V _{IH} = 2.0 V			
		2.7	2.0	—		I _{OH} = -8 mA, V _{IH} = 2.0 V			
		3.0	2.0	—		I _{OH} = -12 mA, V _{IH} = 2.0 V			
	V _{OL}	2.3 to 3.6	—	0.2		I _{OL} = 100 μA			
		2.3	—	0.4		I _{OL} = 4 mA, V _{IL} = 0.7 V			
		2.3	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.7 V			
		3.0	—	0.55		I _{OL} = 6 mA, V _{IL} = 0.8 V			
		2.7	—	0.6		I _{OL} = 8 mA, V _{IL} = 0.8 V			
		3.0	—	0.8		I _{OL} = 12 mA, V _{IL} = 0.8 V			
		Input current	I _{IN}	3.6		—	±5	μA	V _{IN} = V _{CC} or GND
			I _{IN (hold)}	2.3		45	—		V _{IN} = 0.7 V
2.3	-45			—	V _{IN} = 1.7 V				
3.0	75			—	V _{IN} = 0.8 V				
3.0	-75			—	V _{IN} = 2.0 V				
3.6	—			±500	V _{IN} = 0 to 3.6 V ^{*1}				
Off state output current	I _{OZ}			3.6	—	±10	μA		V _{OUT} = V _{CC} or GND
Quiescent supply current	I _{CC}	3.6	—	40	μA	V _{IN} = V _{CC} or GND			

Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

Switching Characteristics

(Ta = 0 to +70°C)

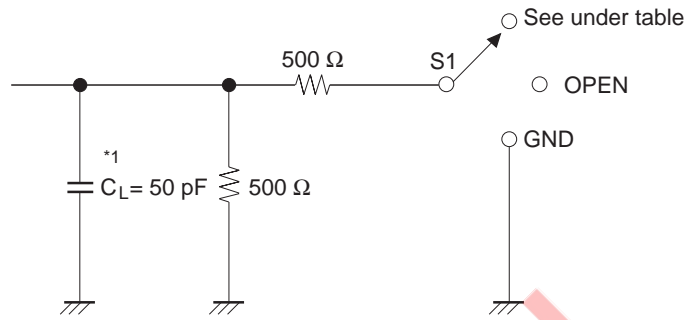
Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	2.5±0.2	135	—	—	MHz		
		2.7	135	—	—			
		3.3±0.3	135	—	—			
Propagation delay time	t _{PLH}	2.5±0.2	2.5	—	6.9	ns	CLK	B
		2.7	—	—	6.4			
		3.3±0.3	1.7	—	5.6			
	t _{PHL}	2.5±0.2	2.2	—	6.4	ns	CLK	A
		2.7	—	—	6.0			
		3.3±0.3	1.6	—	5.2			
		2.5±0.2	2.4	—	7.2	ns	SEL	A
		2.7	—	—	7.0			
		3.3±0.3	1.6	—	6.0			
Output enable time	t _{ZH}	2.5±0.2	2.1	—	7.9	ns	CLK	A or B
		2.7	—	—	7.4			
		3.3±0.3	1.6	—	6.5			
Output disable time	t _{ZL}	2.5±0.2	3.0	—	7.8	ns	CLK	A or B
		2.7	—	—	7.1			
		3.3±0.3	1.7	—	6.2			
Input capacitance	C _{IN}	3.3	—	3.5	pF	Control inputs		
Output capacitance	C _{IN/O}	3.3	—	9.0	pF	A or B ports		

Switching Characteristics (cont.)

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)
Setup time	t _{su}	2.5±0.2	4.1	—	—	ns	A data before CLK↑
		2.7	3.8	—	—		
		3.3±0.3	3.1	—	—		
		2.5±0.2	0.9	—	—		B data before CLK↑
		2.7	1.2	—	—		
		3.3±0.3	0.9	—	—		
		2.5±0.2	3.5	—	—		CLKENA1 or CLKENA2 before CLK↑
		2.7	3.2	—	—		
		3.3±0.3	2.7	—	—		
		2.5±0.2	3.4	—	—		CLKEN1B or CLKEN2B before CLK↑
		2.7	3.0	—	—		
		3.3±0.3	2.6	—	—		
		2.5±0.2	4.4	—	—		OE before CLK↑
		2.7	3.9	—	—		
		3.3±0.3	3.2	—	—		
Hold time	t _h	2.5±0.2	0	—	—	ns	A data after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.2	—	—		
		2.5±0.2	1.4	—	—		B data after CLK↑
		2.7	1.0	—	—		
		3.3±0.3	1.7	—	—		
		2.5±0.2	0	—	—		CLKENA1 or CLKENA2 after CLK↑
		2.7	0.1	—	—		
		3.3±0.3	0.3	—	—		
		2.5±0.2	0	—	—		CLKEN1B or CLKEN2B after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.6	—	—		
		2.5±0.2	0	—	—		OE after CLK↑
		2.7	0	—	—		
		3.3±0.3	0.1	—	—		
Pulse width	t _w	2.5±0.2	3.3	—	—	ns	CLK "H" or "L"
		2.7	3.3	—	—		
		3.3±0.3	3.3	—	—		

• Test Circuit

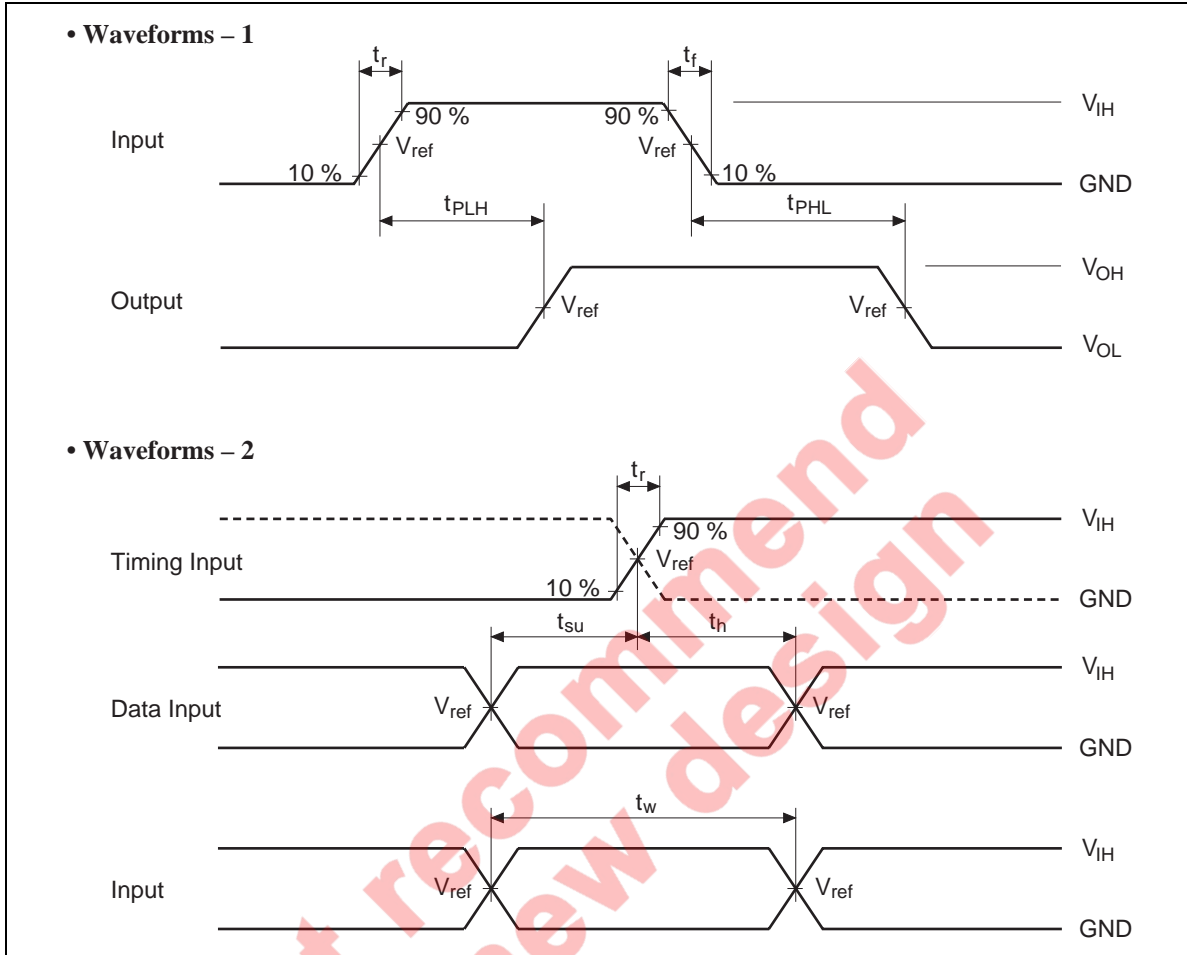


Load Circuit for Outputs

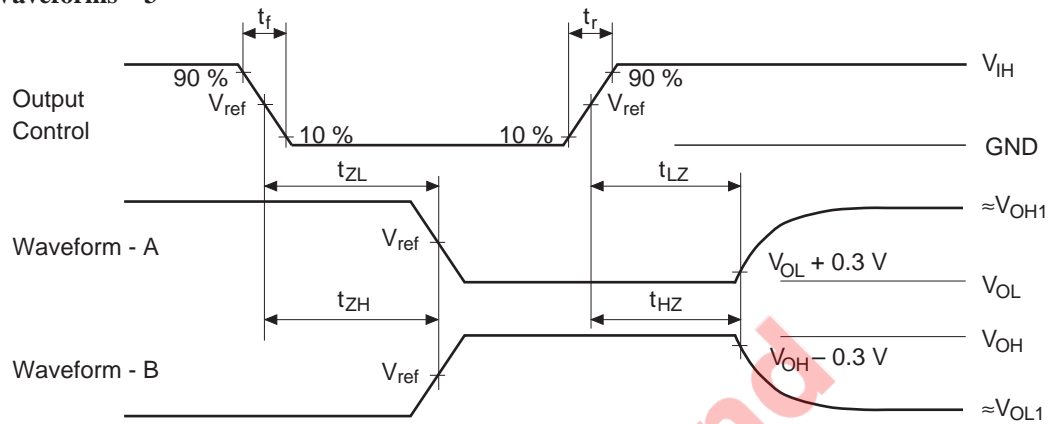
Symbol	$V_{CC}=2.5\pm 0.2\text{ V}$	$V_{CC}=2.7\text{ V},$ $3.3\pm 0.3\text{ V}$
t_{PLH}/t_{PHL}	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	4.6 V	6.0 V

Note: 1. C_L includes probe and jig capacitance.

Not recommended for new design



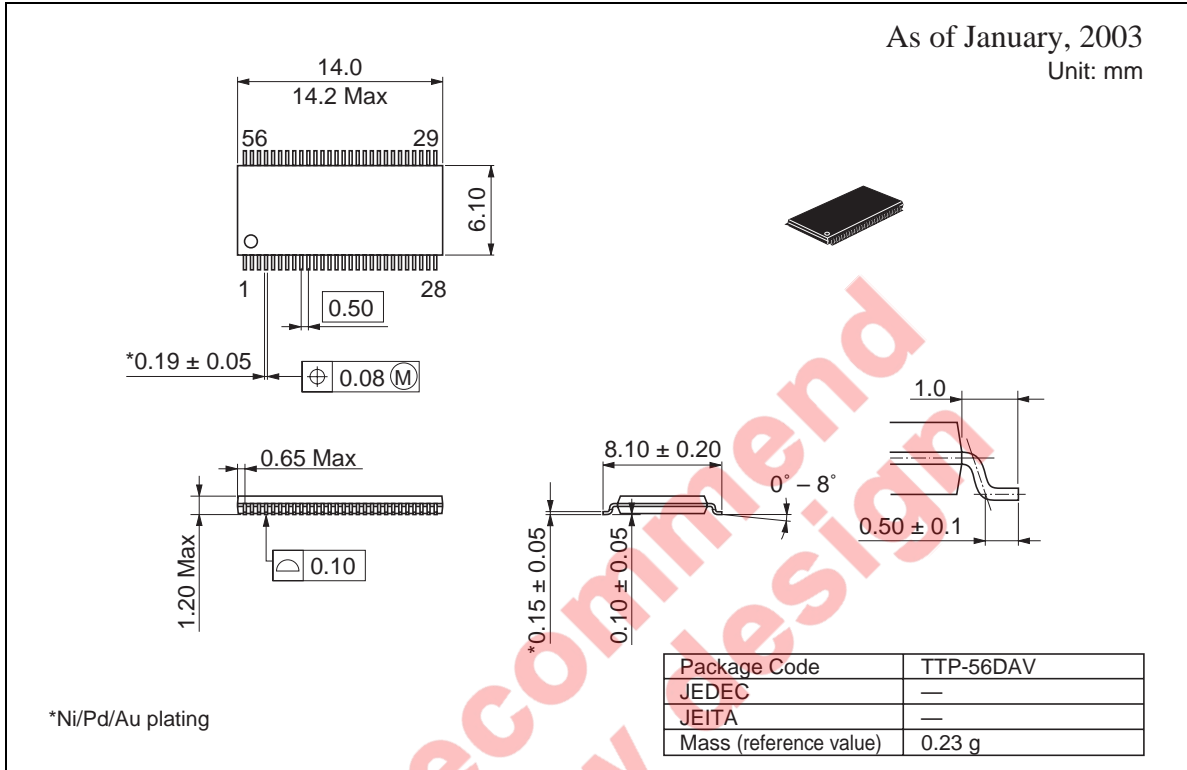
• Waveforms – 3



TEST	$V_{CC}=2.5\pm 0.2 V$	$V_{CC}=2.7 V, 3.3\pm 0.3 V$
V_{IH}	2.3 V	2.7 V
V_{ref}	1.2 V	1.5 V
V_{OH1}	2.3 V	3.0 V
V_{OL1}	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001