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# HD74ALVCH162543

16-bit Registered Transceivers with 3-state Outputs

## HITACHI

ADE-205-183 (Z)  
Preliminary  
1st. Edition  
December 1996

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### Description

The HD74ALVCH162543 can be used as two 8-bit transceivers or one 16-bit transceiver. Separate latch enable ( $\overline{\text{LEAB}}$  or  $\overline{\text{LEBA}}$ ) and output enable ( $\overline{\text{OEAB}}$  or  $\overline{\text{OEBA}}$ ) inputs are provided for each register to permit independent control in either direction of data flow. The A to B enable ( $\overline{\text{CEAB}}$ ) input must be low in order to enter data from A or to output data from B. If  $\overline{\text{CEAB}}$  is low and  $\overline{\text{LEAB}}$  is low, the A to B latches are transparent; a subsequent low to high transition of  $\overline{\text{LEAB}}$  puts the A latches in the storage mode. With  $\overline{\text{CEAB}}$  and  $\overline{\text{OEAB}}$  both low, the 3-state B outputs are active and reflect the data present at the output of the A latches. Data flow from B to A is similar but requires using  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$ , and  $\overline{\text{OEBA}}$ . Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level. All outputs, which are designed to sink up to 12 mA, include 26  $\Omega$  resistors to reduce overshoot and undershoot.

### Features

- $V_{\text{CC}} = 2.3 \text{ V}$  to 3.6 V
- Typical  $V_{\text{OL}}$  ground bounce  $< 0.8 \text{ V}$  (@ $V_{\text{CC}} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- Typical  $V_{\text{OH}}$  undershoot  $> 2.0 \text{ V}$  (@ $V_{\text{CC}} = 3.3 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ )
- High output current  $\pm 12 \text{ mA}$  (@ $V_{\text{CC}} = 3.0 \text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors
- All outputs have equivalent 26  $\Omega$  series resistors, so no external resistors are required.

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## Function Table <sup>\*2</sup>

Inputs				Output B
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B <sub>0</sub> <sup>*1</sup>
L	L	L	L	L
L	L	L	H	H

H : High level

L : Low level

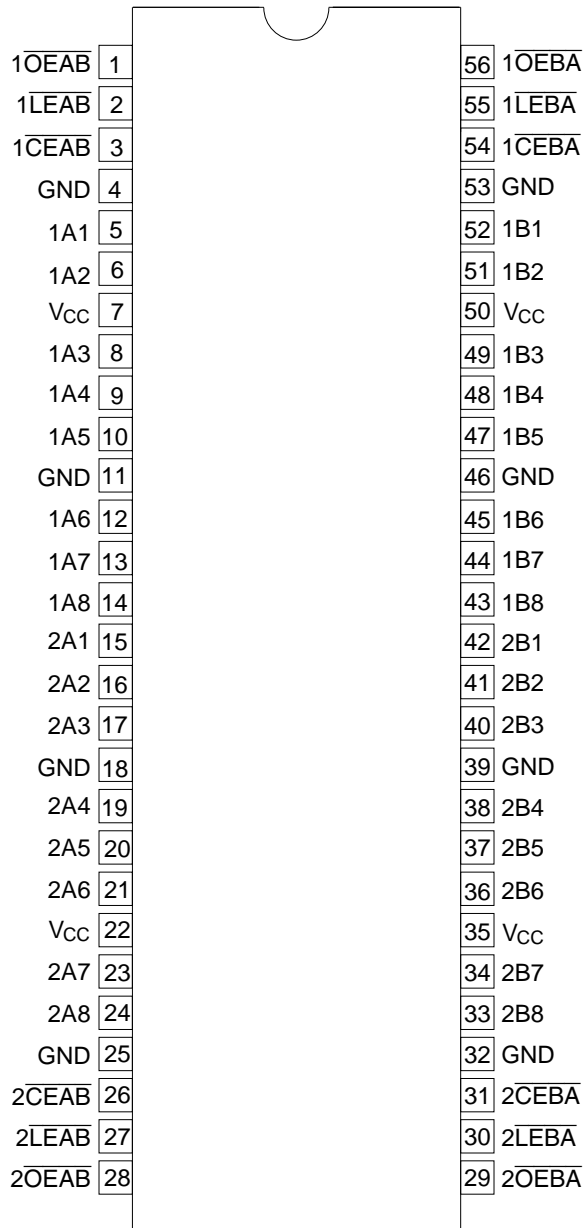
X : Immaterial

Z : High impedance

Notes: 1. Output level before the indicated steady state input conditions were established.

2. A to B data flow is shown; B to A flow control is the same except that it uses  $\overline{CEBA}$ ,  $\overline{LEBA}$ , and  $\overline{OEBA}$ .

Pin Arrangement



(Top view)

## Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1,2</sup>	$V_I$	-0.5 to 4.6 -0.5 to $V_{CC} + 0.5$	V	Except I/O ports I/O ports
Output voltage <sup>*1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	
Output clamp current	$I_{OK}$	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	±50 ±100	mA	$V_O = 0$ to $V_{CC}$
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

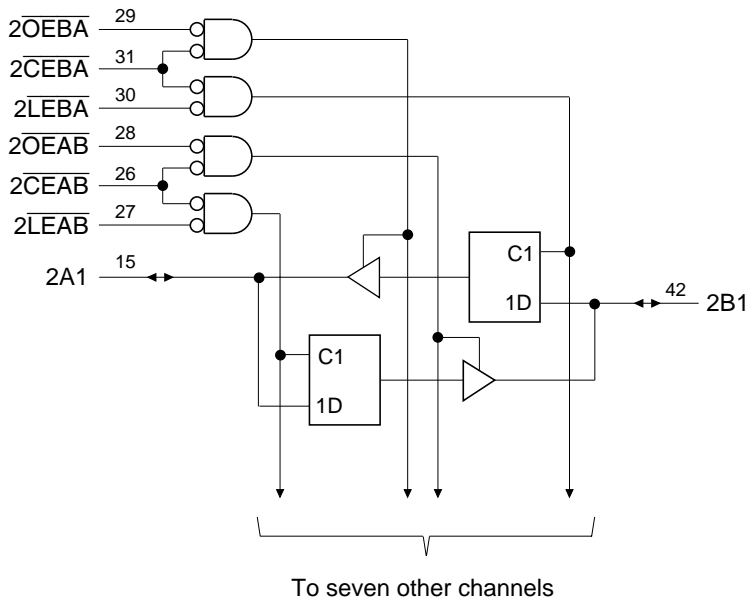
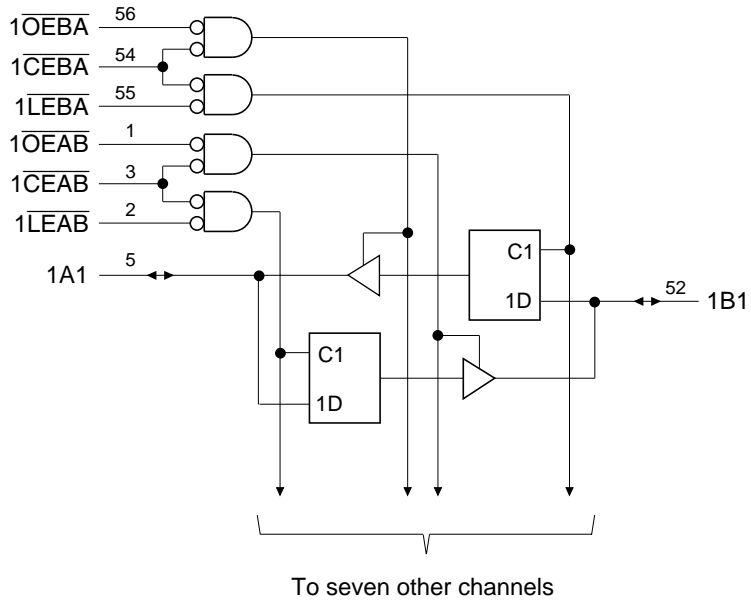
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

## Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	-6 -8 -12	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	6 8 12	mA	$V_{CC} = 2.3\text{ V}$ $V_{CC} = 2.7\text{ V}$ $V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



# HD74ALVCH162543

## Electrical Characteristics (Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V) <sup>1</sup>	Min	Max	Unit	Test Conditions			
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	V <sub>IL</sub>	2.3 to 2.7	—	0.7					
		2.7 to 3.6	—	0.8					
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA			
		2.3	1.9	—		I <sub>OH</sub> = -4 mA, V <sub>IH</sub> = 1.7 V			
		2.3	1.7	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V			
		3.0	2.4	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 2.0 V			
		2.7	2.0	—		I <sub>OH</sub> = -8 mA, V <sub>IH</sub> = 2.0 V			
		3.0	2.0	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V			
	V <sub>OL</sub>	Min to Max	—	0.2		I <sub>OL</sub> = 100 μA			
		2.3	—	0.4		I <sub>OL</sub> = 4 mA, V <sub>IL</sub> = 0.7 V			
		2.3	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V			
		3.0	—	0.55		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.8 V			
		2.7	—	0.6		I <sub>OL</sub> = 8 mA, V <sub>IL</sub> = 0.8 V			
		3.0	—	0.8		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V			
		Input current	I <sub>IN</sub>	3.6		—	±5	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
				I <sub>IN (hold)</sub>		2.3	45		—
2.3	-45		—		V <sub>IN</sub> = 1.7 V				
3.0	75		—		V <sub>IN</sub> = 0.8 V				
3.0	-75		—		V <sub>IN</sub> = 2.0 V				
3.6	—		±500	V <sub>IN</sub> = 0 to 3.6 V					
Off state output current <sup>2</sup>	I <sub>OZ</sub>	3.6	—	±10	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND			
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND			
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND			

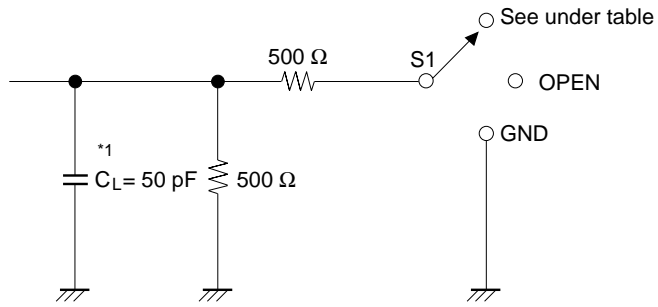
Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

Switching Characteristics (Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)		
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	—	6.2	ns	A or B	B or A		
		2.7	—	—	5.5					
	t <sub>PHL</sub>	3.3±0.3	1.0	—	4.9					
		2.5±0.2	1.1	—	7.6				$\overline{LE}$	A or B
		2.7	—	—	6.9					
		3.3±0.3	1.1	—	5.6					
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.0	—	8.2	ns	$\overline{CE}$	A or B		
		2.7	—	—	7.6					
	t <sub>ZL</sub>	3.3±0.3	1.0	—	6.2					
		2.5±0.2	1.0	—	7.8				$\overline{OE}$	A or B
		2.7	—	—	7.0					
		3.3±0.3	1.0	—	5.9					
Output disable time	t <sub>HZ</sub>	2.5±0.2	2.0	—	6.8	ns	$\overline{CE}$	A or B		
		2.7	—	—	6.7					
	t <sub>LZ</sub>	3.3±0.3	1.5	—	5.6					
		2.5±0.2	1.6	—	6.4				$\overline{OE}$	A or B
		2.7	—	—	5.3					
		3.3±0.3	1.1	—	5.1					
Setup time	t <sub>SU</sub>	2.5±0.2	1.2	—	—	ns	Data before $\overline{CE}\uparrow$			
		2.7	1.5	—	—					
		3.3±0.3	1.2	—	—					
		2.5±0.2	1.2	—	—		Data before $\overline{LE}\uparrow$			
		2.7	1.5	—	—		$\overline{CE}$ "L"			
		3.3±0.3	1.2	—	—					
Hold time	t <sub>H</sub>	2.5±0.2	1.2	—	—	ns	Data after $\overline{CE}\uparrow$			
		2.7	0.8	—	—					
		3.3±0.3	1.3	—	—					
		2.5±0.2	1.2	—	—		Data after $\overline{LE}\uparrow$			
		2.7	0.8	—	—		$\overline{CE}$ "L"			
		3.3±0.3	1.3	—	—					
Pulse width	t <sub>W</sub>	2.5±0.2	3.3	—	—	ns	$\overline{CE}$ or $\overline{LE}$ "L"			
		2.7	3.3	—	—					
		3.3±0.3	3.3	—	—					
Input capacitance	C <sub>IN</sub>	3.3	—	3.5	—	pF	Control inputs			
Output capacitance	C <sub>IN/O</sub>	3.3	—	7.0	—	pF	A or B ports			

## • Test Circuit



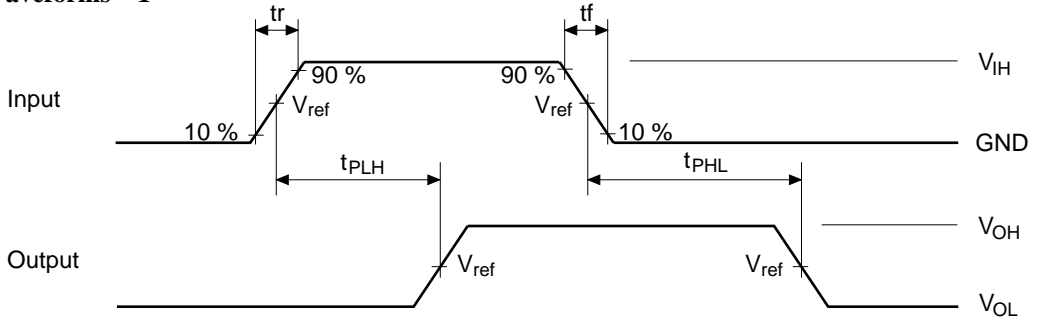
Load Circuit for Outputs

Symbol	V <sub>CC</sub> =2.5±0.2V	V <sub>CC</sub> =2.7V, 3.3±0.3V
t <sub>PLH</sub> /t <sub>PHL</sub>	OPEN	OPEN
t <sub>su</sub> /t <sub>h</sub> /t <sub>w</sub>	OPEN	OPEN
t <sub>ZH</sub> /t <sub>HZ</sub>	GND	GND
t <sub>ZL</sub> /t <sub>LZ</sub>	4.6 V	6.0 V

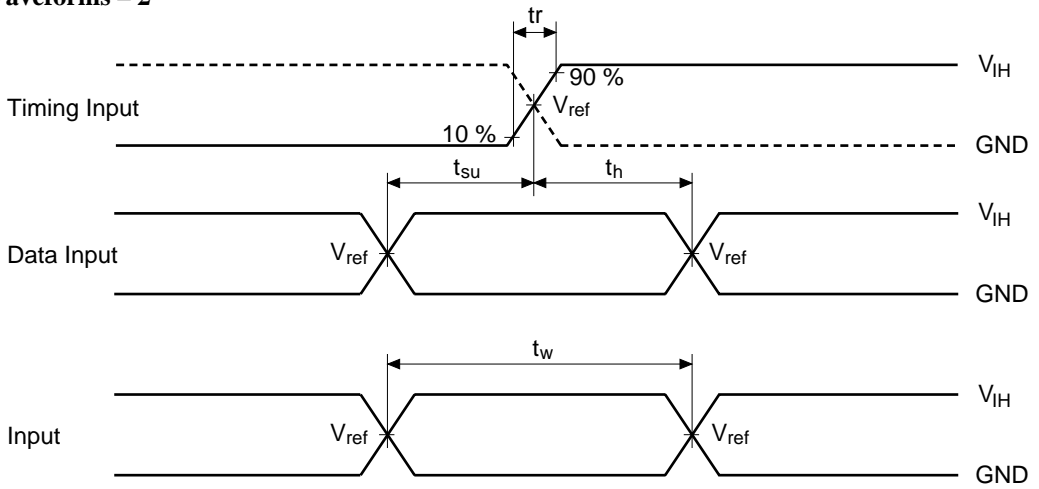
Note: 1. C<sub>L</sub> includes probe and jig capacitance.



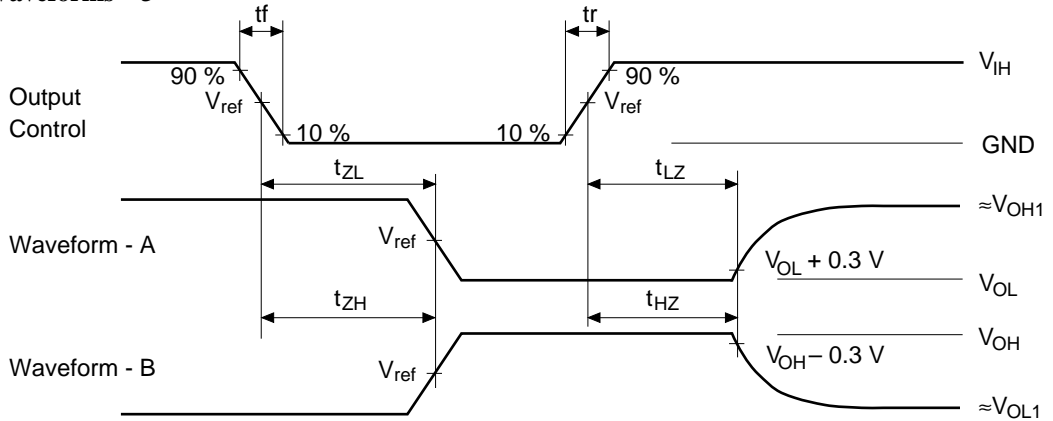
• Waveforms – 1



• Waveforms – 2



• Waveforms – 3

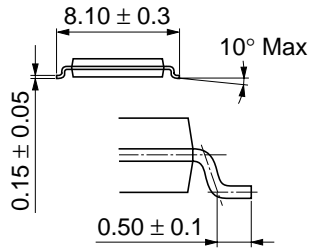
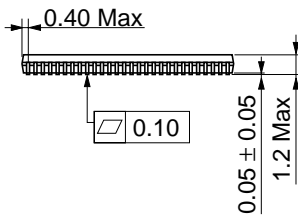
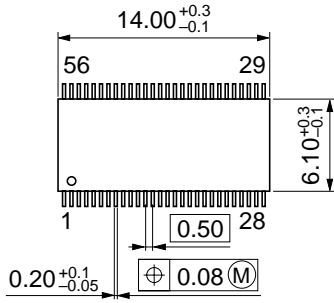


TEST	$V_{CC}=2.5\pm 0.2V$	$V_{CC}=2.7V, 3.3\pm 0.3V$
$V_{IH}$	2.3 V	2.7 V
$V_{ref}$	1.2 V	1.5 V
$V_{OH1}$	2.3 V	3.0 V
$V_{OL1}$	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10$  MHz,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns.
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

Package Dimensions

Unit : mm



Hitachi code	TTP-56D
EIAJ code	—
JEDEC code	—

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