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# HD74ALVCH16820

## 3.3-V 10-bit Flip Flops with Dual Outputs

REJ03D0034-0400Z  
(Previous ADE-205-170B(Z))  
Rev.4.00  
Oct.02.2003

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### Description

The flip flops of the HD74ALVCH16820 are edge triggered D-type flip flops. On the positive transition of the clock (CLK) input, the device provides true data at the Q outputs. A buffered output enable ( $\overline{OE}$ ) input can be used to place the ten outputs in either a normal logic state (high or low logic level) or a high impedance state. In the high impedance state, the outputs neither load nor drive the bus lines significantly. The high impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.  $\overline{OE}$  input does not affect the internal operation of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

### Features

- $V_{CC} = 2.3\text{ V to }3.6\text{ V}$
- Typical  $V_{OL}$  ground bounce  $< 0.8\text{ V}$  ( $@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C}$ )
- Typical  $V_{OH}$  undershoot  $> 2.0\text{ V}$  ( $@V_{CC} = 3.3\text{ V}, T_a = 25^\circ\text{C}$ )
- High output current  $\pm 24\text{ mA}$  ( $@V_{CC} = 3.0\text{ V}$ )
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

**Function Table**

Inputs			Output Qn <sup>*1</sup>
$\overline{OEn}^{*2}$	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q <sub>0</sub> <sup>*1</sup>
H	X	X	Z

H : High level

L : Low level

X : Immaterial

Z : High impedance

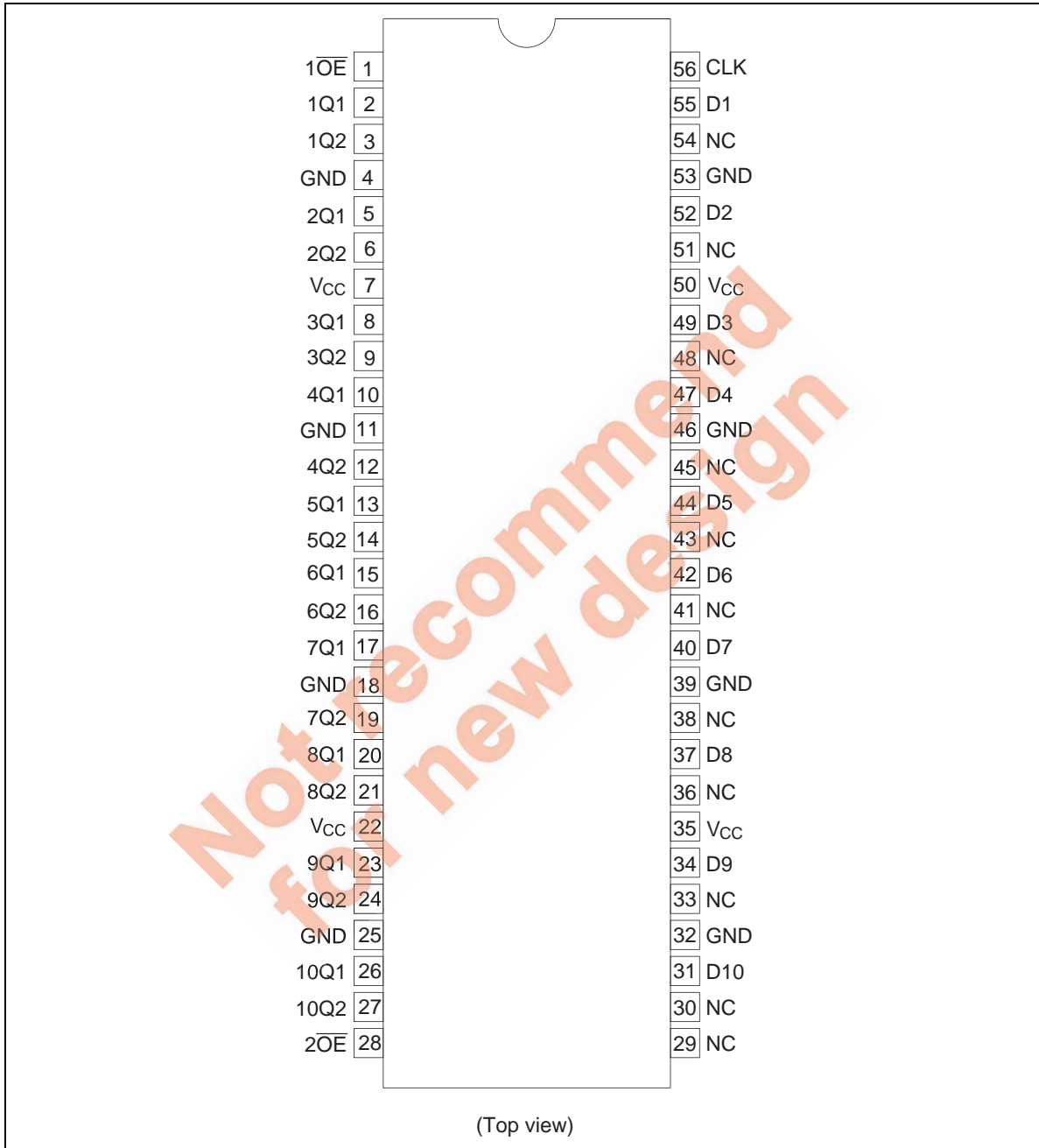
↑ : Low to high transition

Notes: 1. Output level before the indicated steady state input conditions were established.

2. n = 1, 2

Not recommend  
for new design

Pin Arrangement



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1</sup>	$V_I$	-0.5 to 4.6	V	
Output voltage <sup>*1, 2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 50$	mA	$V_O = 0$ to $V_{CC}$
$V_{CC}$ , GND current / pin	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	1	W	TSSOP
Storage temperature	$T_{stg}$	-65 to 150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

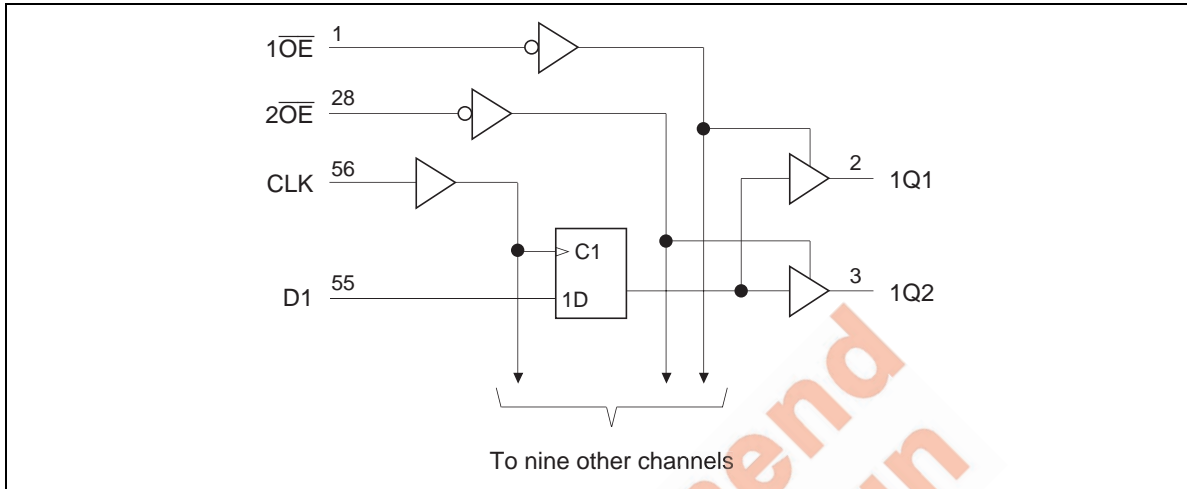
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.

**Recommended operating conditions**

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	$V_{CC}$	2.3	3.6	V	
Input voltage	$V_I$	0	$V_{CC}$	V	
Output voltage	$V_O$	0	$V_{CC}$	V	
High level output current	$I_{OH}$	—	-12	mA	$V_{CC} = 2.3\text{ V}$
		—	-12		$V_{CC} = 2.7\text{ V}$
		—	-24		$V_{CC} = 3.0\text{ V}$
Low level output current	$I_{OL}$	—	12	mA	$V_{CC} = 2.3\text{ V}$
		—	12		$V_{CC} = 2.7\text{ V}$
		—	24		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	$T_a$	-40	85	$^\circ\text{C}$	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic Diagram



Not recommended  
for new design

**Electrical Characteristics**

(Ta = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V) <sup>*1</sup>	Min	Max	Unit	Test Conditions			
Input voltage	V <sub>IH</sub>	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	V <sub>IL</sub>	2.3 to 2.7	—	0.7					
		2.7 to 3.6	—	0.8					
Output voltage	V <sub>OH</sub>	Min to Max	V <sub>CC</sub> -0.2	—	V	I <sub>OH</sub> = -100 μA			
		2.3	2.0	—		I <sub>OH</sub> = -6 mA, V <sub>IH</sub> = 1.7 V			
		2.3	1.7	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 1.7 V			
		2.7	2.2	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V			
		3.0	2.4	—		I <sub>OH</sub> = -12 mA, V <sub>IH</sub> = 2.0 V			
		3.0	2.0	—		I <sub>OH</sub> = -24 mA, V <sub>IH</sub> = 2.0 V			
	V <sub>OL</sub>	Min to Max	—	0.2	μA	I <sub>OL</sub> = 100 μA			
		2.3	—	0.4		I <sub>OL</sub> = 6 mA, V <sub>IL</sub> = 0.7 V			
		2.3	—	0.7		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.7 V			
		2.7	—	0.4		I <sub>OL</sub> = 12 mA, V <sub>IL</sub> = 0.8 V			
		3.0	—	0.55		I <sub>OL</sub> = 24 mA, V <sub>IL</sub> = 0.8 V			
		Input current	I <sub>IN</sub>	3.6		—	±5	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
				2.3		45	—		V <sub>IN</sub> = 0.7 V
						-45	—		V <sub>IN</sub> = 1.7 V
3.0	75			—	V <sub>IN</sub> = 0.8 V				
	-75			—	V <sub>IN</sub> = 2.0 V				
3.6	—			±500	V <sub>IN</sub> = 0 to 3.6 V				
Off state output current <sup>*2</sup>	I <sub>OZ</sub>	3.6	—	±10	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND			
Quiescent supply current	I <sub>CC</sub>	3.6	—	40	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND			
	ΔI <sub>CC</sub>	3.0 to 3.6	—	750	μA	V <sub>IN</sub> = one input at (V <sub>CC</sub> -0.6) V, other inputs at V <sub>CC</sub> or GND			

Notes: 1. For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

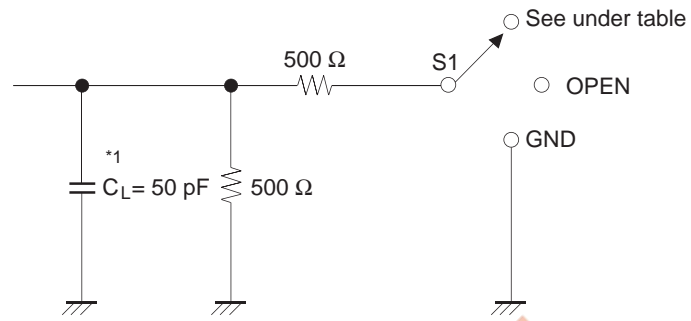
2. For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current.

**Switching Characteristics**

(T<sub>a</sub> = -40 to 85°C)

Item	Symbol	V <sub>CC</sub> (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f <sub>max</sub>	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t <sub>PLH</sub>	2.5±0.2	1.0	—	5.9	ns	CLK	Q
	t <sub>PHL</sub>	2.7	—	—	5.5			
	3.3±0.3	1.0	—	4.8				
Output enable time	t <sub>ZH</sub>	2.5±0.2	1.0	—	6.4	ns	OE	Q
	t <sub>ZL</sub>	2.7	—	—	6.1			
	3.3±0.3	1.0	—	5.0				
Output disable time	t <sub>HZ</sub>	2.5±0.2	1.3	—	5.7	ns	OE	Q
	t <sub>LZ</sub>	2.7	—	—	5.0			
	3.3±0.3	1.0	—	4.5				
Setup time	t <sub>su</sub>	2.5±0.2	1.7	—	—	ns		
		2.7	1.8	—	—			
		3.3±0.3	1.4	—	—			
Hold time	t <sub>h</sub>	2.5±0.2	1.1	—	—	ns		
		2.7	1.1	—	—			
		3.3±0.3	1.0	—	—			
Pulse width	t <sub>w</sub>	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C <sub>IN</sub>	3.3	—	3.5	—	pF	Control inputs	
		3.3	—	6.0	—		Data inputs	
Output capacitance	C <sub>O</sub>	3.3	—	7.0	—	pF	Outputs	

• Test Circuit



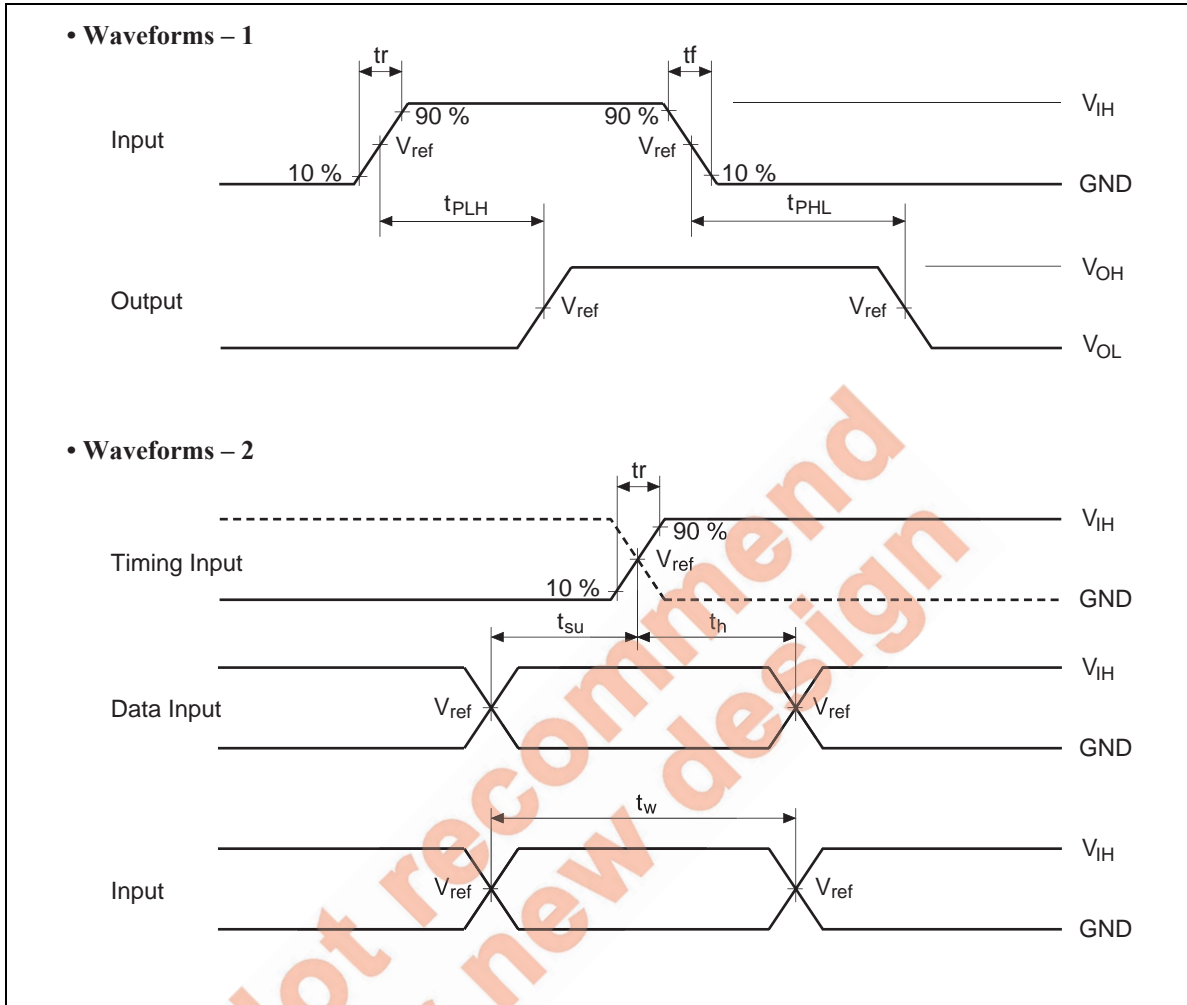
Load Circuit for Outputs

Symbol	V <sub>CC</sub> =2.5±0.2 V	V <sub>CC</sub> = 2.7 V, 3.3±0.3 V
t <sub>PLH</sub> /t <sub>PHL</sub>	OPEN	OPEN
t <sub>su</sub> /t <sub>h</sub> /t <sub>w</sub>	OPEN	OPEN
t <sub>ZH</sub> /t <sub>HZ</sub>	GND	GND
t <sub>ZL</sub> /t <sub>LZ</sub>	4.6 V	6.0 V

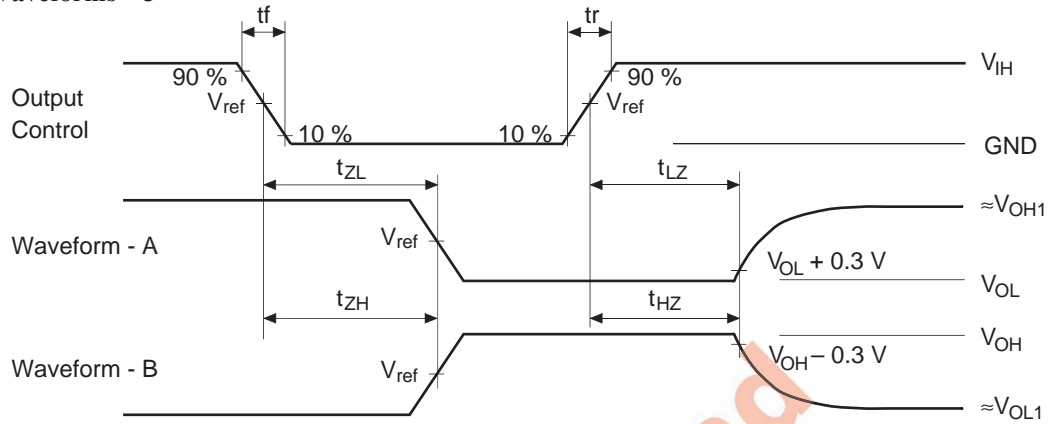
Note: 1. C<sub>L</sub> includes probe and jig capacitance.

Not recommended for new design





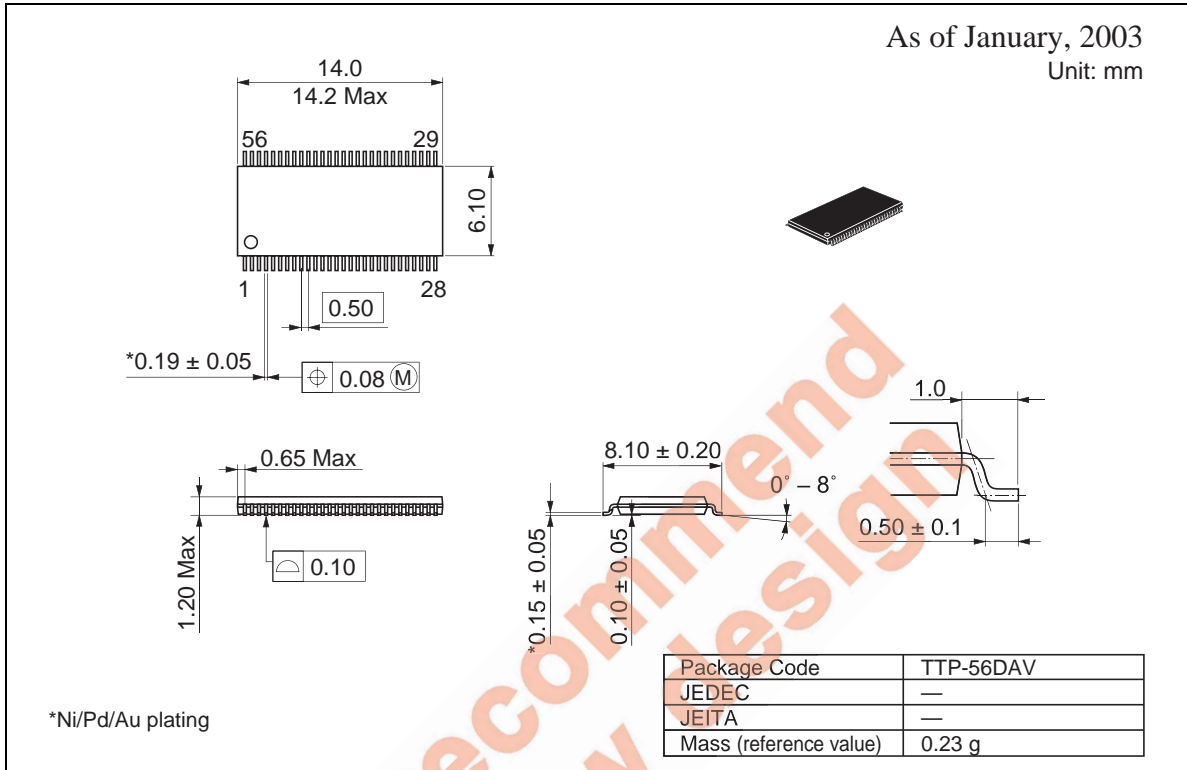
• Waveforms – 3



TEST	$V_{CC}=2.5\pm 0.2 V$	$V_{CC} = 2.7 V, 3.3\pm 0.3 V$
$V_{IH}$	2.3 V	2.7 V
$V_{ref}$	1.2 V	1.5 V
$V_{OH1}$	2.3 V	3.0 V
$V_{OL1}$	GND	GND

- Notes:
1. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_o = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  2. Waveform – A is for an output with internal conditions such that the output is low except when disabled by the output control.
  3. Waveform – B is for an output with internal conditions such that the output is high except when disabled by the output control.
  4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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