

HD74ALVCH16831

1-to 4 Address Register / Driver with 3-state Outputs

REJ03D0031-0200Z
(Previous ADE-205-194(Z))
Rev. 2.00
Oct.02.2003

Description

This 1-bit to 4-bit address register / driver is designed for 2.3 V to 3.6 V V_{CC} operation. The device is ideal for use in applications in which a single address bus is driving four separate memory locations. The HD74ALVCH16831 can be used as a buffer or a register, depending on the logic level of the select (\overline{SEL}) input. When \overline{SEL} is logic high, the device is in the buffer mode. The outputs follow the inputs and are controlled by the two output enable (\overline{OE}) controls. Each \overline{OE} controls two groups of nine outputs. When \overline{SEL} is logic low, the device is in the register mode. The register is an edge triggered D-type flip flop. On the positive transition of the clock (CLK) input, data set up at the A inputs is stored in the internal registers. \overline{OE} controls operate the same as in buffer mode. When \overline{OE} is logic low, the outputs are in a normal logic state (high or low logic level). When \overline{OE} is logic high, the outputs are in the high impedance state. To ensure the high impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current sinking capability of the driver. \overline{SEL} and \overline{OE} do not affect the internal operation of the flip flops. Old data can be retained or new data can be entered while the outputs are in the high impedance state. Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

Features

- $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$
- Typical V_{OL} ground bounce $< 0.8 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.0 \text{ V}$ (@ $V_{CC} = 3.3 \text{ V}$, $T_a = 25^\circ\text{C}$)
- High output current $\pm 24 \text{ mA}$ (@ $V_{CC} = 3.0 \text{ V}$)
- Bus hold on data inputs eliminates the need for external pullup / pulldown resistors

Function Table

Inputs				Output Y
\overline{OE}	\overline{SEL}	CLK	A	
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

H : High level

L : Low level

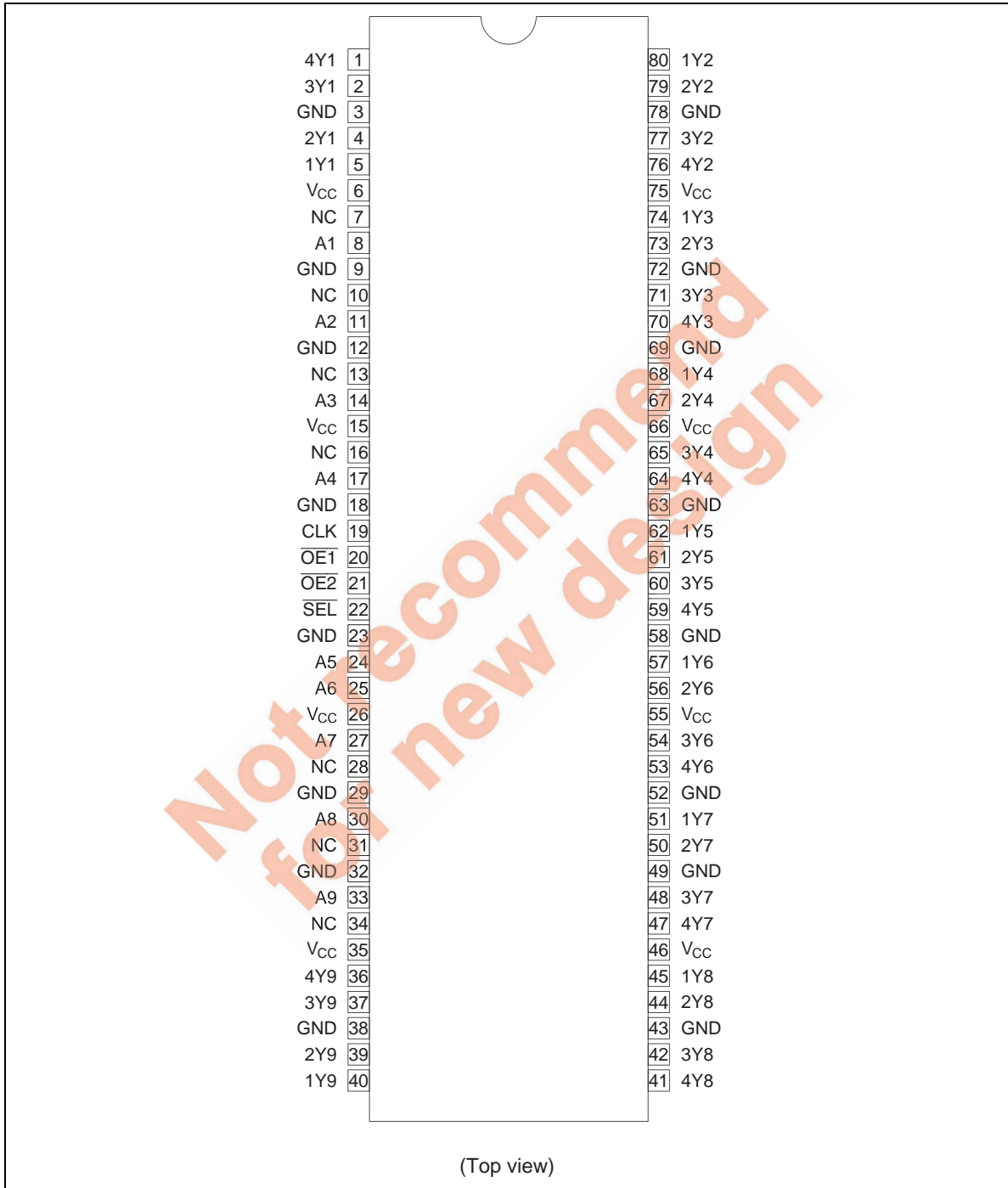
X : Immaterial

Z : High impedance

↑ : Low to high transition

**Not recommend
for new design**

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	-0.5 to 4.6	V	
Input voltage ^{*1}	V_I	-0.5 to 4.6	V	
Output voltage ^{*1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	±50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{CC}
V_{CC} , GND current / pin	I_{CC} or I_{GND}	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3}	P_T	1	W	TVSOP
Storage temperature	T_{stg}	-65 to 150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

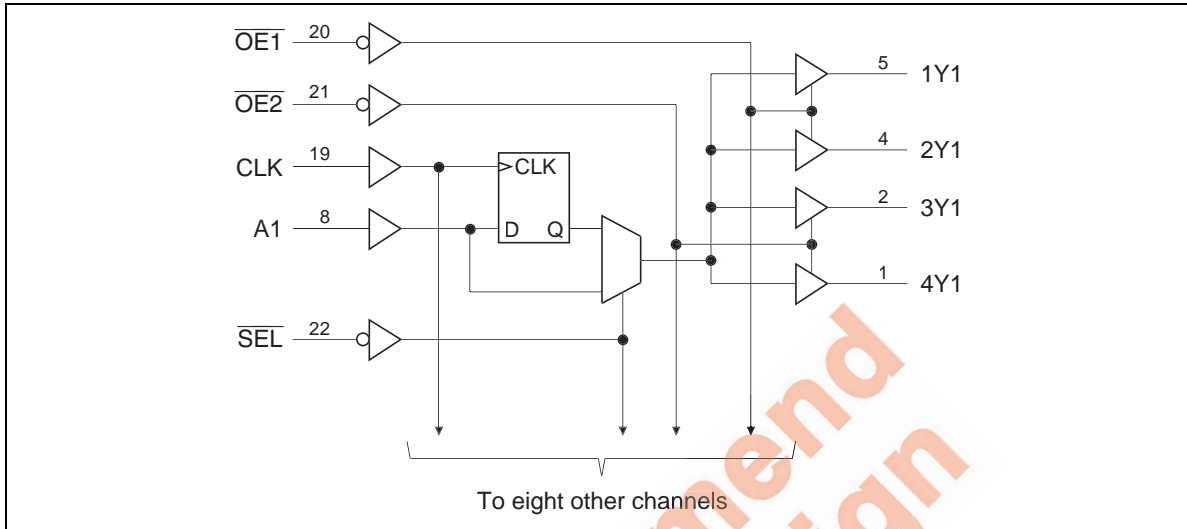
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage	V_{CC}	2.3	3.6	V	
Input voltage	V_I	0	V_{CC}	V	
Output voltage	V_O	0	V_{CC}	V	
High level output current	I_{OH}	—	-12	mA	$V_{CC} = 2.3\text{ V}$
		—	-12		$V_{CC} = 2.7\text{ V}$
		—	-24		$V_{CC} = 3.0\text{ V}$
Low level output current	I_{OL}	—	12	mA	$V_{CC} = 2.3\text{ V}$
		—	12		$V_{CC} = 2.7\text{ V}$
		—	24		$V_{CC} = 3.0\text{ V}$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	10	ns / V	
Operating temperature	T_a	-40	85	°C	

Note: Unused control inputs must be held high or low to prevent them from floating.

Logic diagram



Not recommended for new design

Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Max	Unit	Test Conditions			
Input voltage	V _{IH}	2.3 to 2.7	1.7	—	V				
		2.7 to 3.6	2.0	—					
	V _{IL}	2.3 to 2.7	—	0.7					
		2.7 to 3.6	—	0.8					
Output voltage	V _{OH}	2.3 to 3.6	V _{CC} -0.2	—	V	I _{OH} = -100 μA			
		2.3	2.0	—		I _{OH} = -6 mA, V _{IH} = 1.7 V			
		2.3	1.7	—		I _{OH} = -12 mA, V _{IH} = 1.7 V			
		2.7	2.2	—		I _{OH} = -12 mA, V _{IH} = 2.0 V			
		3.0	2.4	—		I _{OH} = -12 mA, V _{IH} = 2.0 V			
		3.0	2.0	—		I _{OH} = -24 mA, V _{IH} = 2.0 V			
	V _{OL}	2.3 to 3.6	—	0.2	μA	I _{OL} = 100 μA			
		2.3	—	0.4		I _{OL} = 6 mA, V _{IL} = 0.7 V			
		2.3	—	0.7		I _{OL} = 12 mA, V _{IL} = 0.7 V			
		2.7	—	0.4		I _{OL} = 12 mA, V _{IL} = 0.8 V			
		3.0	—	0.55		I _{OL} = 24 mA, V _{IL} = 0.8 V			
		Input current	I _{IN}	3.6		—	±5	μA	V _{IN} = V _{CC} or GND
				I _{IN (hold)}		2.3	45		—
2.3	-45				—	V _{IN} = 1.7 V			
Off state output current	I _{OZ}	3.0	75	—	μA	V _{IN} = 0.8 V			
		3.0	-75	—		V _{IN} = 2.0 V			
		3.6	—	±500		V _{IN} = 0 to 3.6 V ^{*1}			
		3.6	—	±10		V _{OUT} = V _{CC} or GND			
Quiescent supply current	I _{CC}	3.6	—	40	μA	V _{IN} = V _{CC} or GND			
		ΔI _{CC}	3.0 to 3.6	—		750	V _{IN} = one input at (V _{CC} -0.6) V, other inputs at V _{CC} or GND		

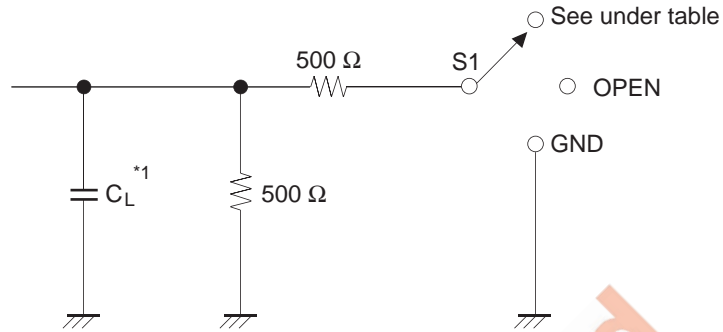
Note: 1. This is the bus hold maximum dynamic current required to switch the input from one state to another.

Switching Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	FROM (Input)	TO (Output)
Maximum clock frequency	f _{max}	2.5±0.2	150	—	—	MHz		
		2.7	150	—	—			
		3.3±0.3	150	—	—			
Propagation delay time	t _{PLH}	2.5±0.2	1.2	—	4.0	ns	A	Y
		2.7	—	—	4.1			
		3.3±0.3	1.6	—	3.6			
	t _{PHL}	2.5±0.2	1.1	—	4.5	ns	CLK	Y
		2.7	—	—	4.4			
		3.3±0.3	1.5	—	3.9			
		2.5±0.2	1.3	—	5.2		SEL	Y
		2.7	—	—	5.2			
		3.3±0.3	1.7	—	4.4			
Output enable time	t _{ZH}	2.5±0.2	1.1	—	5.1	ns	OE	Y
		2.7	—	—	5.0			
		3.3±0.3	1.2	—	4.3			
Output disable time	t _{ZL}	2.5±0.2	1.4	—	5.5	ns	OE	Y
		2.7	—	—	4.7			
		3.3±0.3	1.6	—	4.5			
Setup time	t _{su}	2.5±0.2	2.0	—	—	ns		
		2.7	2.0	—	—			
		3.3±0.3	1.6	—	—			
Hold time	t _h	2.5±0.2	0.7	—	—	ns		
		2.7	0.5	—	—			
		3.3±0.3	1.1	—	—			
Pulse width	t _w	2.5±0.2	3.3	—	—	ns		
		2.7	3.3	—	—			
		3.3±0.3	3.3	—	—			
Input capacitance	C _{IN}	3.3	—	4.5	—	pF	Control inputs	
		3.3	—	5.0	—		Data inputs	
Output capacitance	C _O	3.3	—	7.5	—	pF		

Test Circuit



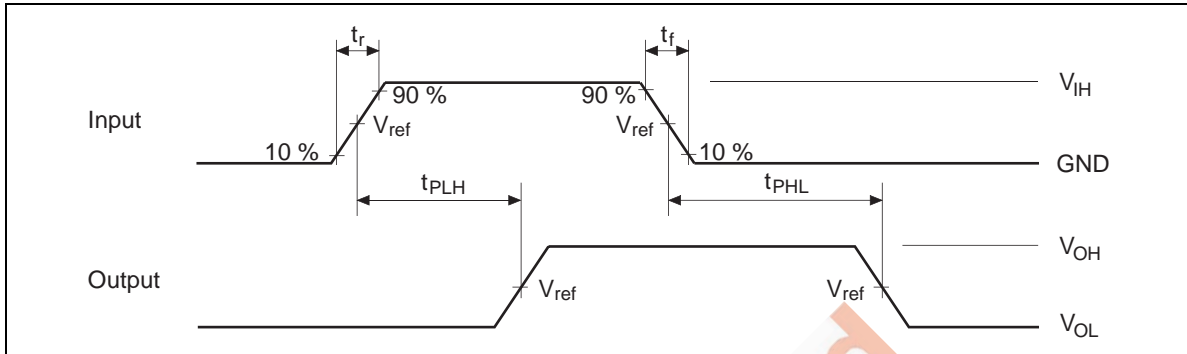
Load Circuit for Outputs

Symbol	$V_{CC}=2.5\pm 0.2V$	$V_{CC} = 2.7 V,$ $3.3\pm 0.3 V$
t_{PLH}/t_{PHL}	OPEN	OPEN
$t_{su}/t_h/t_w$	OPEN	OPEN
t_{ZH}/t_{HZ}	GND	GND
t_{ZL}/t_{LZ}	$2 \times V_{CC}$	6.0 V
C_L	30 pF	50 pF

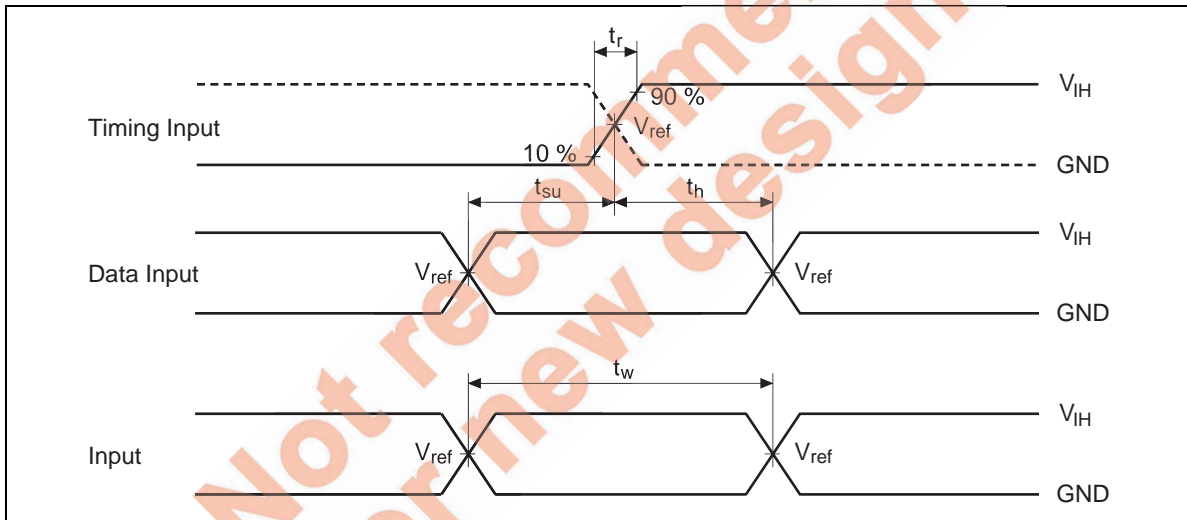
Note: 1. C_L includes probe and lig capacitance.

Not recommended for new design

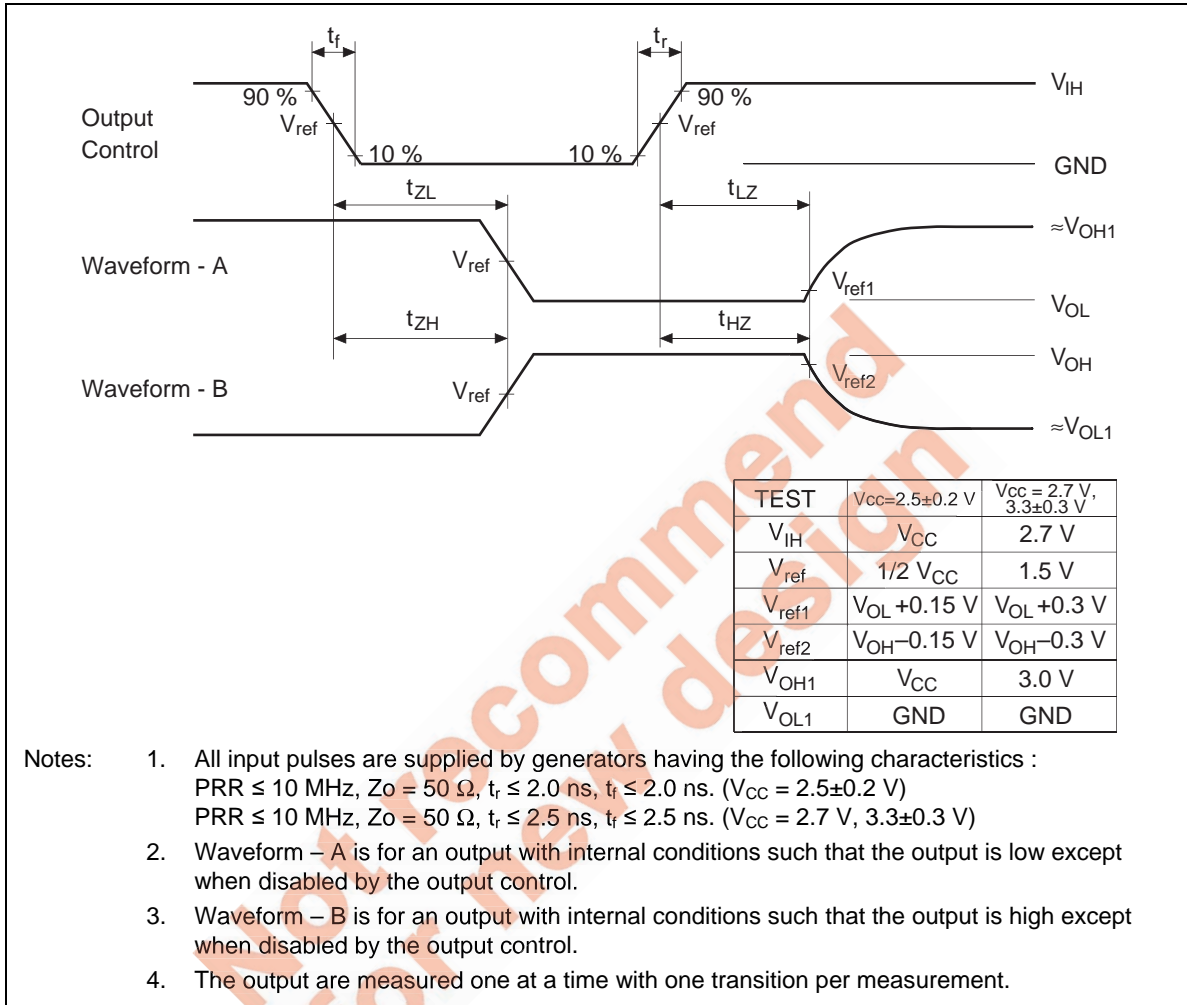
Waveforms – 1



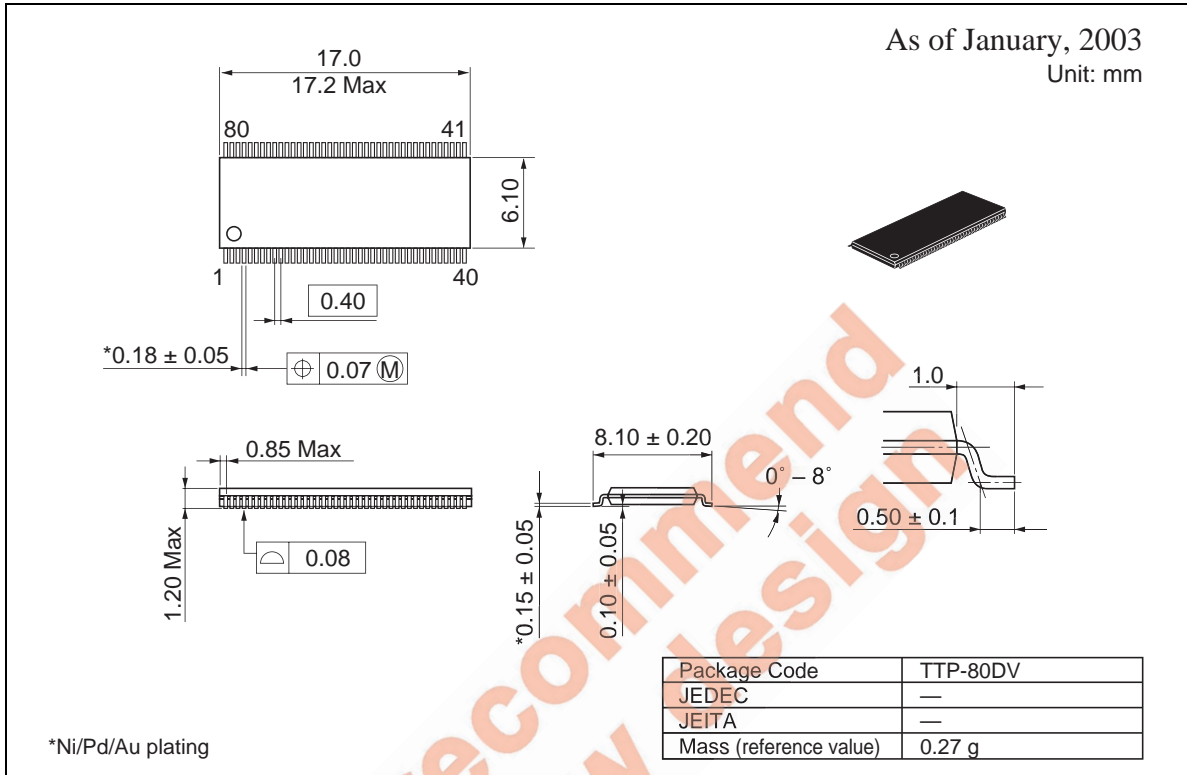
Waveforms – 2



Waveforms – 3



Package Dimensions



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