HD74BC574A

Octal D Type Flip Flops With 3 State Outputs

REJ03D0288–0300Z
(Previous ADE-205-042A (Z))
Rev.3.00
Jul.16.2004

Description

The HD74BC574A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight edge triger D type flip flops with three state outputs in a 20 pin package. Data at the D inputs meeting set up requirements, are transferred to the Q outputs on positive going transitions of the clock input. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the strage elements.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range
  Ta = –40 to + 85°C
- Ordering Information

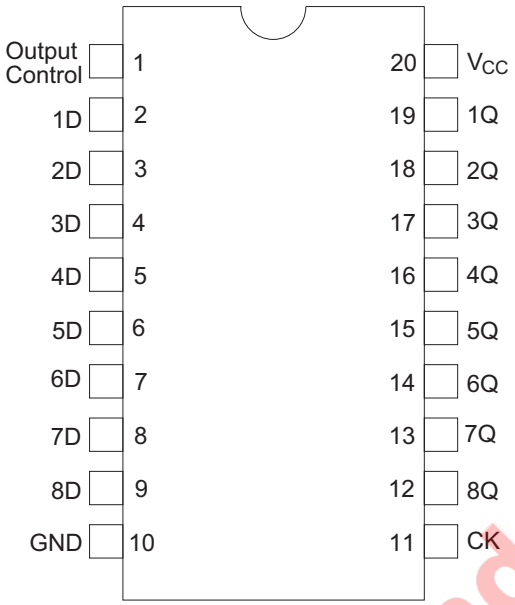
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74BC574AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)

Function Table

Inputs			Output Q
Output Control	CK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance
↑ : Low to high transition
Q_0 : Level of Q before the indicated steady state input conditions were established.

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input diode current	I_{IK}	±30	mA
Input voltage	V_{IN}	–0.5 to +7.5	V
Output voltage	V_{OUT}	–0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	–0.5 to +5.5	V
Storage temperature	Tstg	–65 to +150	°C

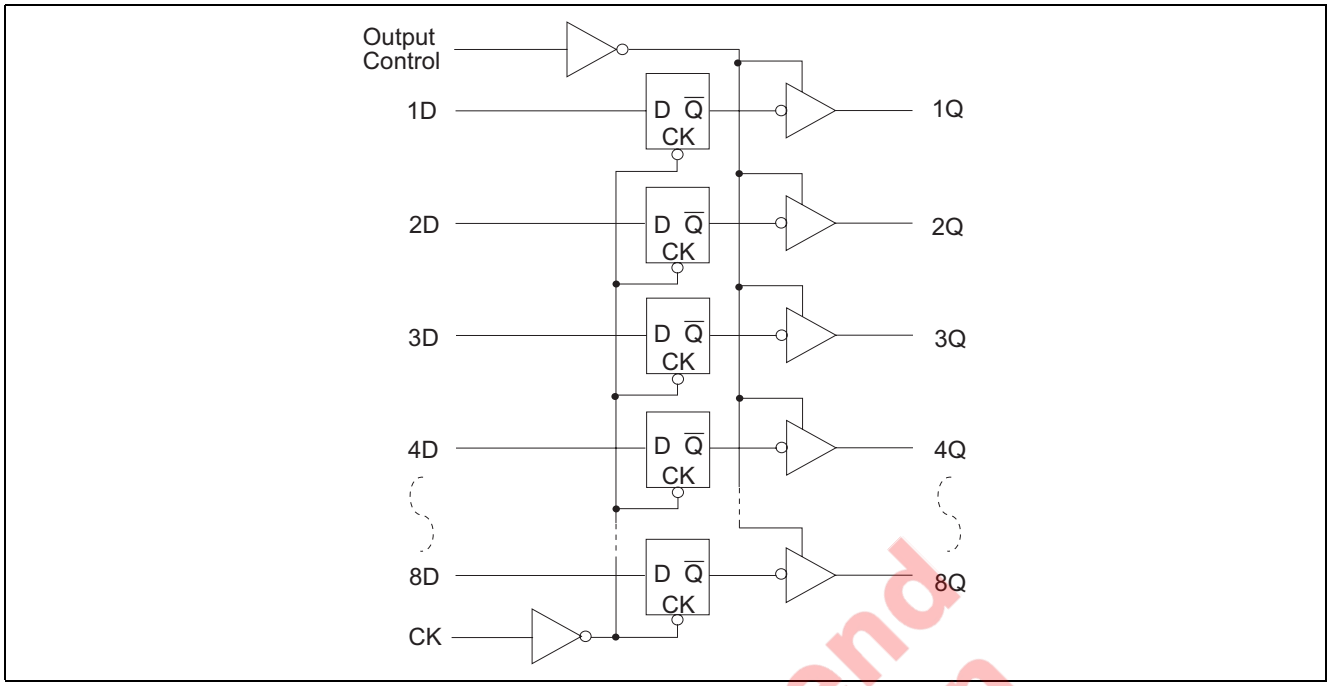
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	—	V_{CC}	V
Output voltage	V_{OUT}	0	—	V_{CC}	V
Operating temperature	Topr	–40	—	85	°C
Input rise/fall time*[1]	t_r, t_f	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics (Ta = –40°C to +85°C)

Item	Symbol	V_{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}		2.0	—	V	
	V_{IL}		—	0.8	V	
Output voltage	V_{OH}	4.5	2.4	—	V	I_{OH} = –3 mA
		4.5	2.0	—	V	I_{OH} = –15 mA
	V_{OL}	4.5	—	0.4	V	I_{OL} = 24 mA
		4.5	—	0.5	V	I_{OL} = 48 mA
Input diode voltage	V_{IK}	4.5	—	–1.2	V	I_{IN} = –18 mA
Input current	I_I	5.5	—	–250	µA	V_{IN} = 0 V
		5.5	—	1.0	µA	V_{IN} = 5.5 V
		5.5	—	100	µA	V_{IN} = 7.0 V
Short circuit output current*1	I_{OS}	5.5	–100	–225	mA	V_{IN} = 0 or 5.5 V
Off state output current	I_{OZH}	5.5	—	50	µA	V_O = 2.7 V
	I_{OZL}	5.5	—	–50	µA	V_O = 0.5 V
Supply current	I_{CCL}	5.5	—	29.5	mA	V_{IN} = 0 or 5.5 V All outputs is “L”
	I_{CCH}	5.5	—	2.5	mA	V_{IN} = 0 or 5.5 V All outputs is “H”
	I_{CCZ}	5.5	—	2.5	mA	V_{IN} = 0 or 5.5 V All outputs is “Z”
	I_{CCT}*2	5.5	—	1.5	mA	V_{IN} = 3.4 or 0.5 V

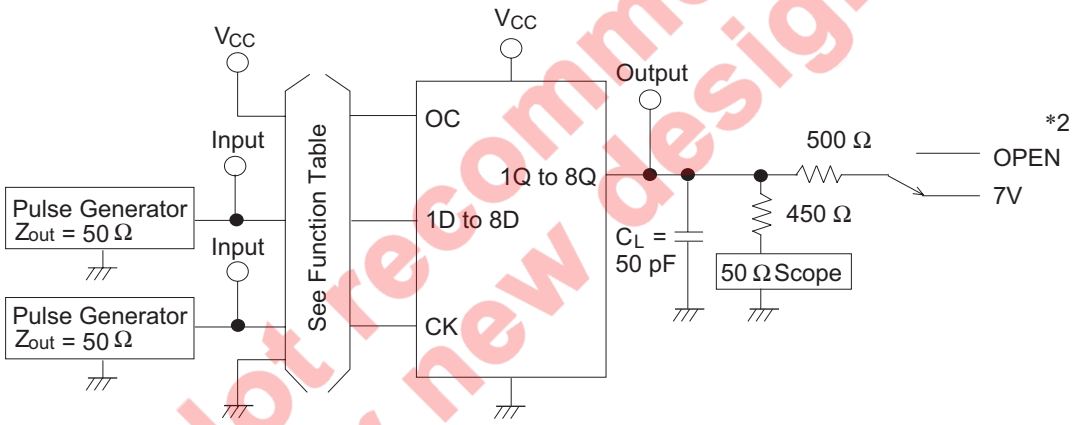
Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2. When input by the TTL level, it shows I_{CC} increase at per one input pin.

Switching Test Method (C_L = 50 pF)

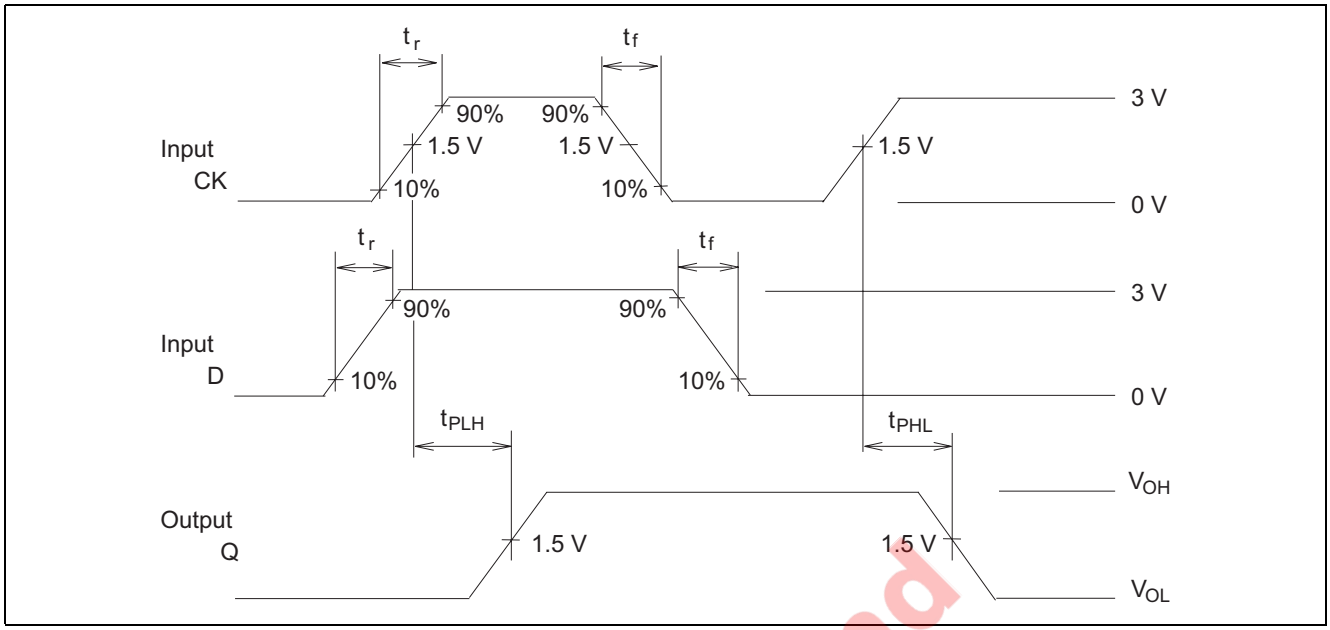
Item		Symbol	Ta = 25°C V_{CC} = 5.0 V		Ta = –40 to 85°C V_{CC} = 5.0 V ±10%		Unit	Test conditions
			Min	Max	Min	Max		
Propagation delay time	CK → Q	t_{PLH}	3.0	8.0	3.0	10.0	ns	See under figure
		t_{PHL}	3.0	8.0	3.0	10.0		
Output enable time		t_{ZH}	3.0	9.0	3.0	11.0	ns	
		t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time		t_{HZ}	3.0	8.0	3.0	10.0	ns	
		t_{LZ}	3.0	8.0	3.0	10.0		
Setup time		t_s(H)	2.0	—	2.0	—	ns	
		t_s(L)	2.0	—	2.0	—		
Hold time		t_h(H)	2.0	—	2.0	—	ns	
		t_h(L)	2.0	—	2.0	—		
Pulse width		t_W(H)	6.0	—	6.0	—	ns	
		t_W(L)	6.0	—	6.0	—		
Input capacitance		C_{IN}	3.0 (Typ)	—	—		pF	V_{IN} = V_{CC} or GND
Output capacitance		C_O	15.0 (Typ)		—		pF	V_O = V_{CC} or GND

Test Circuit

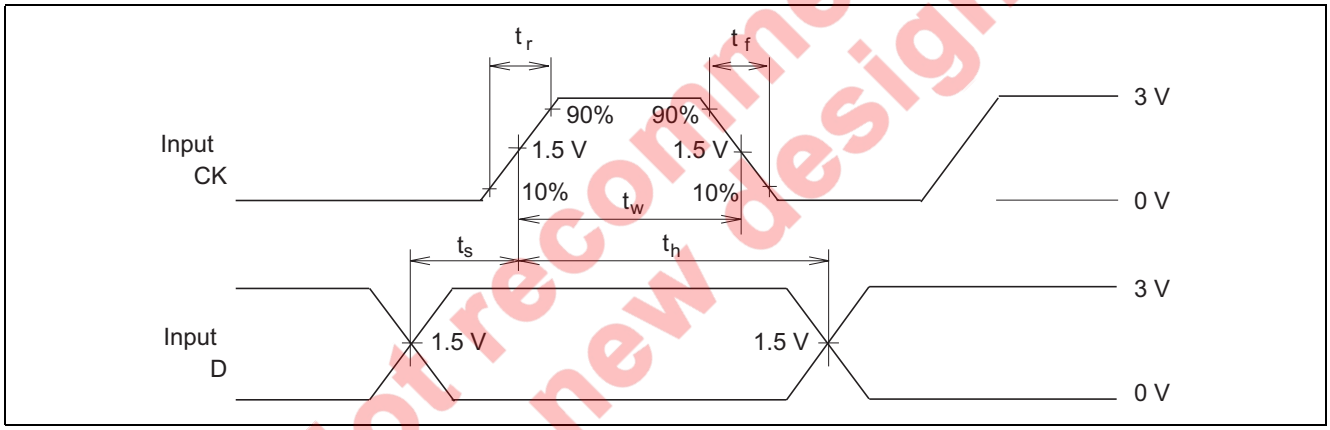


Notes: 1. C_L includes probe and jig capacitance.
2. OPEN: t_{PLH}, t_{PHL}, t_{ZH}, t_{HZ}, t_h, t_s t_w
7 V: t_{ZL}, t_{LZ}

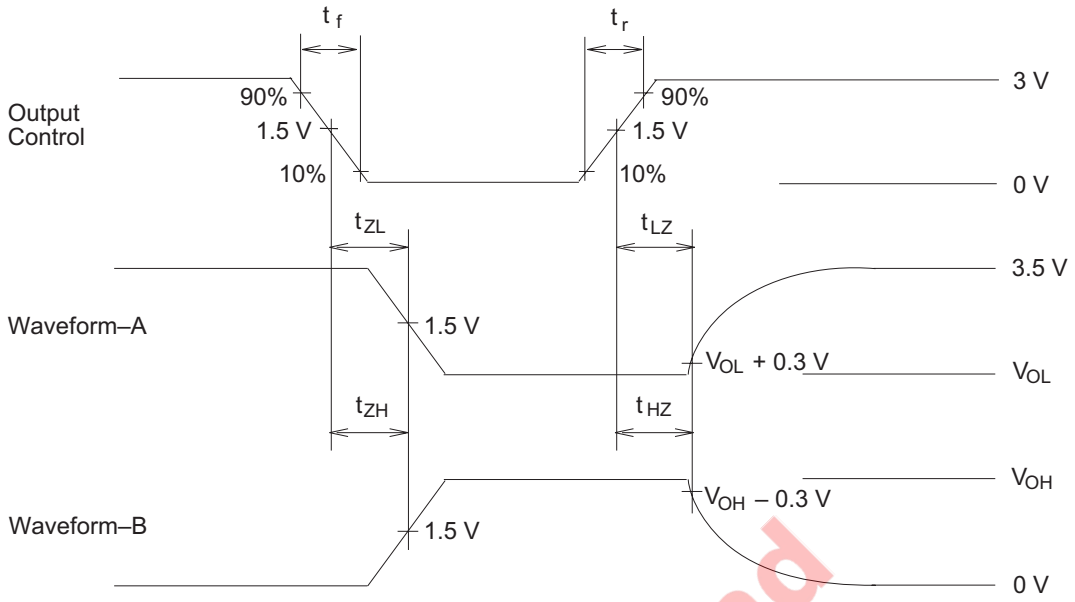
Waveforms-1



Waveforms-2



Waveforms-3

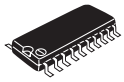


Notes:
1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveform: PRR = 1 MHz, duty cycle 50%
3. Waveform-A shows input conditions such that the output is “L” level when enable by the output control.
4. Waveform-B shows input conditions such that the output is “H” level when enable by the output control.

Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g

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