HD74BC645A

Octal Bus Transceivers With 3 State Outputs

REJ03D0291–0200Z
(Previous ADE-205-027 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74BC645A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC. When the frequency is 10 MHz. The device has eight bus transceivers with three state outputs in a 20 pin package. Each device has an active low enable input ($\overline{G}$) and a direction control input, DiR. When DiR is high, data flows from the A inputs to the B outputs. When DiR is high, data flows from the B inputs to the A outputs. When enable inputs ($\overline{G}$) is high, disables both A and B ports by placing then in a high impedance.

Features

- Input/Output are at high impedance state when power supply is off.
- Input pins can be open, when not used, owing to built in input pull up circuit.
- Input is TTL level.
- Wide operating temperature range
  Ta = –40 to +85°C.
- Ordering Information

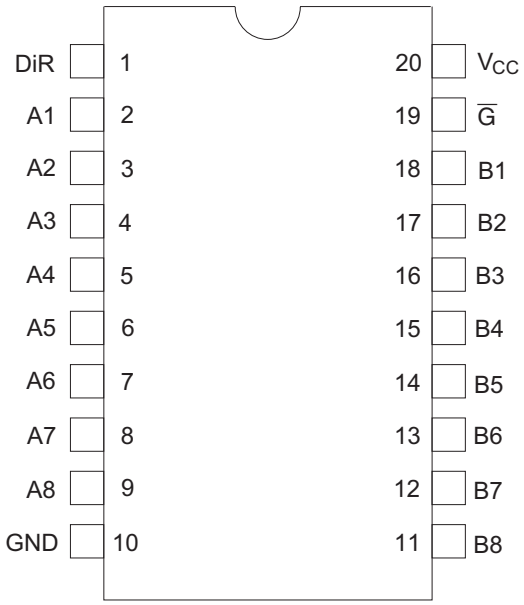
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74BC645AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)

Function Table

Control Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Z

H : High level
L : Low level
X : Immaterial
Z : High impedance

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7.0	V
Input diode current	I_{IK}	±30	mA
Input voltage	V_{IN}	–0.5 to +7.5	V
Output voltage	V_{OUT}	–0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	–0.5 to +5.5	V
Storage temperature	Tstg	–65 to +150	°C

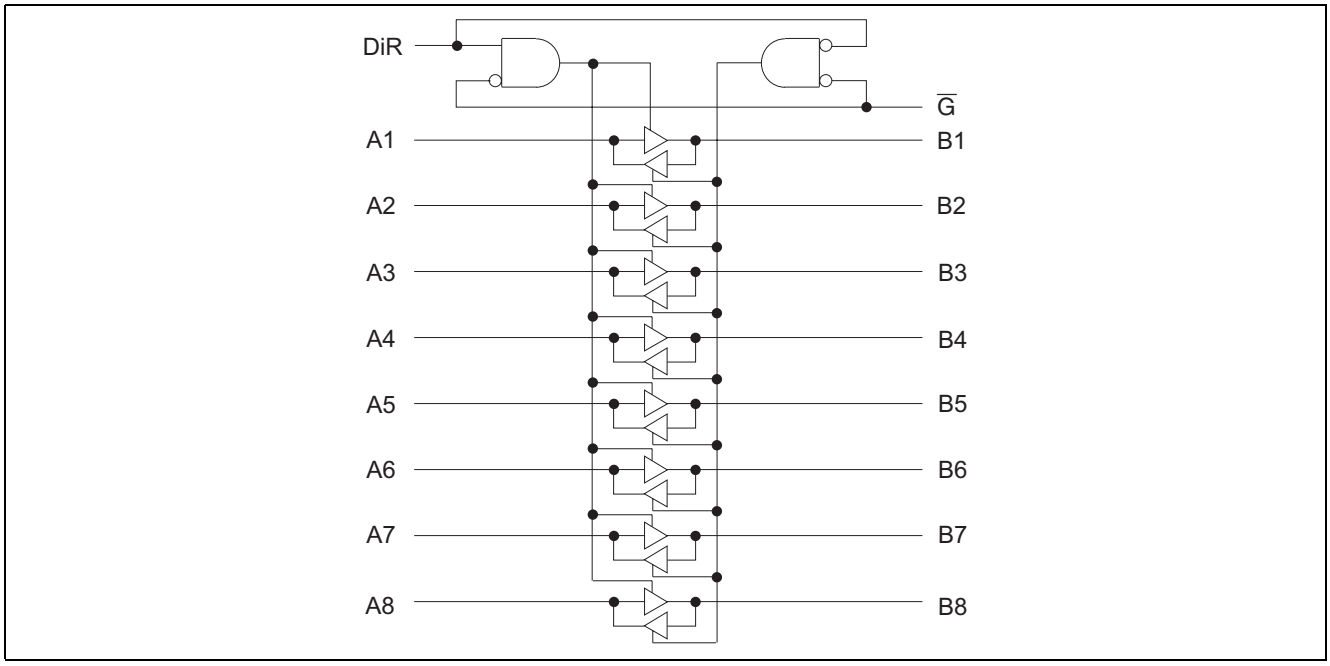
Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IN}	0	—	V_{CC}	V
Ouput voltage	V_{OUT}	0	—	V_{CC}	V
Operating temperature	Topr	–40	—	85	°C
Input rise/fall time*[1]	t_r, t_f	0	—	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics (Ta = –40 to +85°C)

Item	Symbol	V_{CC} (V)	Min	Max	Unit	Test Conditions
Input voltage	V_{IH}		2.0	—	V	
	V_{IL}		—	0.8	V	
Output voltage	V_{OH}	4.5	2.4	—	V	I_{OH} = –3 mA
		4.5	2.0	—	V	I_{OH} = –15 mA
	V_{OL}	4.5	—	0.5	V	I_{OL} = 48 mA
		4.5	—	0.55	V	I_{OL} = 64 mA
Input diode voltage	V_{IK}	4.5	—	–1.2	V	I_{IN} = –18 mA
Input current	I_I	5.5	—	–250	µA	V_{IN} = 0 V
		5.5	—	100	µA	An or Bn, V_{IN} = 5.5 V
		5.5	—	1.0	µA	DiR or $\overline{G}$, V_{IN} = 5.5 V
		5.5	—	100	µA	DiR or $\overline{G}$, V_{IN} = 7 V
Output short circuit current*[1]	I_{OS}	5.5	–100	–225	mA	V_O = 0 V, V_{IN} = 0 or 5.5 V
Off state output current	I_{OZH}	5.5	—	–100	µA	V_O = 2.7 V
	I_{OZL}	5.5	—	–250	µA	V_O = 0.5 V
Supply current	I_{CCL}	5.5	—	31.5	mA	V_{IN} = 0 or 5.5 V All outputs is “L”
	I_{CCH}	5.5	—	0.5	mA	V_{IN} = 0 or 5.5 V All outputs is “H”
	I_{CCZ}	5.5	—	4.5	mA	V_{IN} = 0 or 5.5 V All outputs is “Z”
	I_{CCT}*[2]	5.5	—	1.5	mA	V_{IN} = 3.4 or 0.5 V

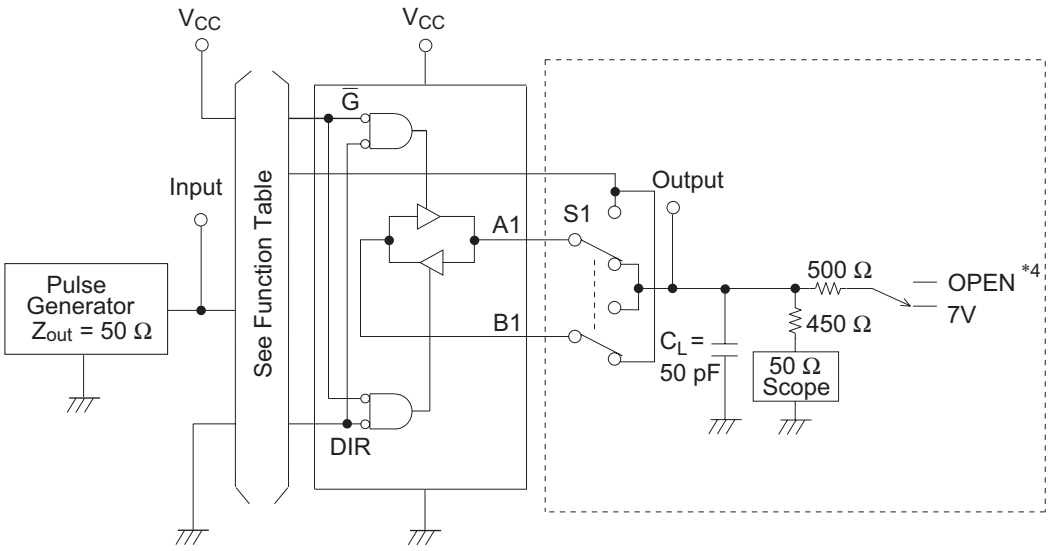
Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

2. When input by the TTL level, it shows I_{CC} increase at per one input pin.

Switching Characteristics (C_L = 50 pF)

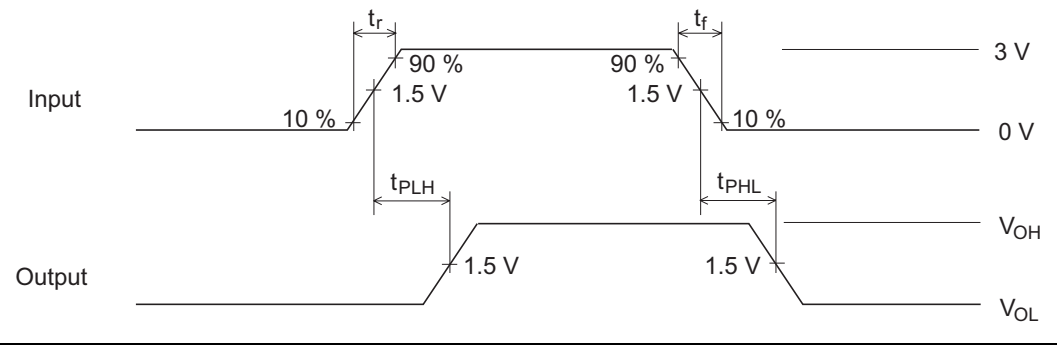
Item	Symbol	Ta = 25°C V_{CC} = 5.0 V		Ta = –40 to +85°C V_{CC} = 5.0 V ±10%		Unit	Test Conditions
		Min	Max	Min	Max		
Propagation delay time	t_{PLH}	3.0	6.0	3.0	7.0	ns	An to Bn
	t_{PHL}	3.0	6.0	3.0	7.0		
	t_{PLH}	3.0	6.0	3.0	7.0	ns	Bn to An
	t_{PHL}	3.0	6.0	3.0	7.0		
Output enable time	t_{ZH}	3.0	9.0	3.0	11.0	ns	$\overline{G}$ to Bn
	t_{ZL}	3.0	9.0	3.0	11.0		
	t_{ZH}	3.0	9.0	3.0	11.0	ns	$\overline{G}$ to An
	t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time	t_{HZ}	3.0	8.0	3.0	10.0	ns	$\overline{G}$ to Bn
	t_{LZ}	3.0	8.0	3.0	10.0		
	t_{HZ}	3.0	8.0	3.0	10.0	ns	$\overline{G}$ to An
	t_{LZ}	3.0	8.0	3.0	10.0		
Input capacitance	C_{IN}	3.0 (Typ)		—		pF	V_{IN} = V_{CC} or GND
Output capacitance	$C_{I/O}$	15.0 (Typ)		—		pF	$V_{I/O}$ = V_{CC} or GND

Test Circuit

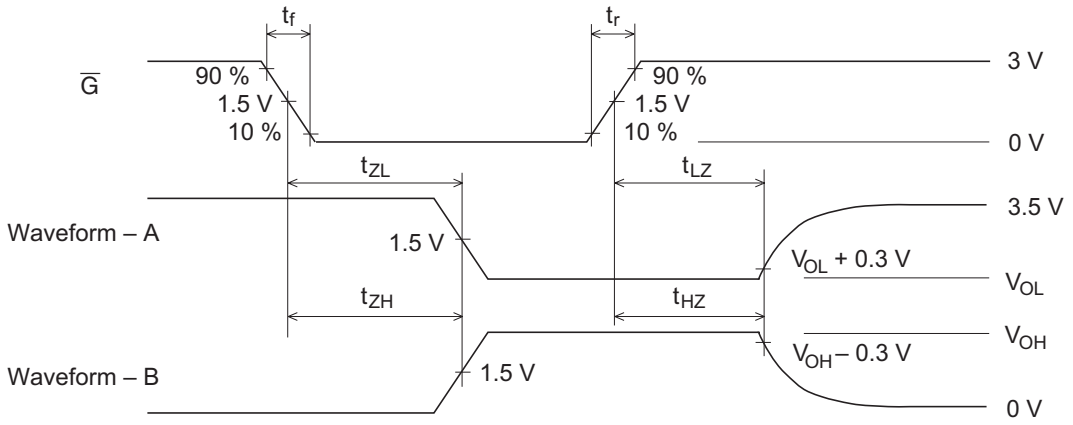


Notes:
1. C_L includes probe and jig capacitance.
2. A2-B2 to A8-B8 are identical to above load circuit.
3. S1: Input-Output change switch.
4. Open: t_{PLH}, t_{PHL}, t_{ZH} t_{HZ}
   7 V: t_{ZL}, t_{LZ}

Waveforms-1



Waveforms-2

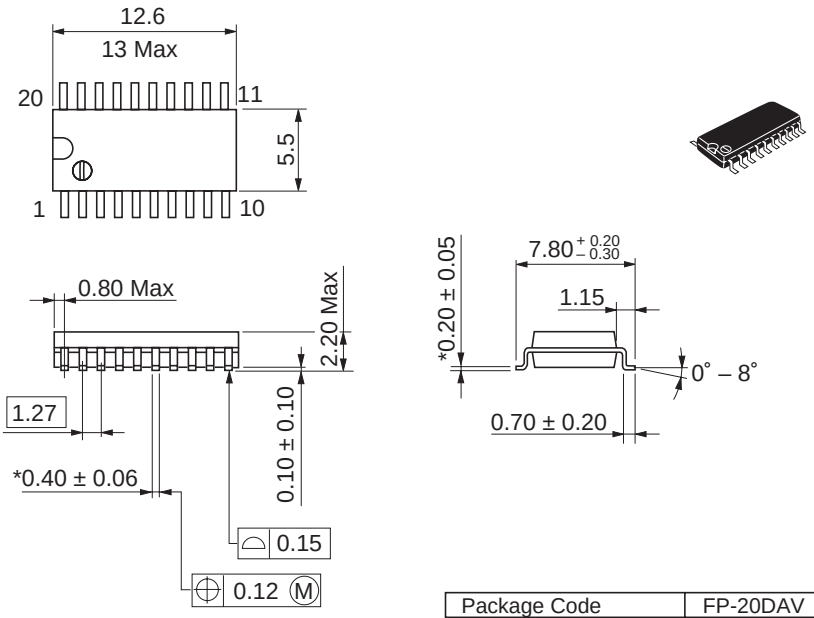


Notes:
1. t_r = 2.5 ns, t_f = 2.5 ns
2. Input waveforms: PRR = 1 MHz, duty cycle 50%
3. Waveform-A shows input conditions such that the output is “L” level when enable by the output control.
4. Waveform-B shows input conditions such that the output is “H” level when enable by the output control.

Package Dimensions

As of January, 2003

Unit: mm



*Ni/Pd/Au plating

Package Code	FP-20DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.31 g