

# HD74CDCF2510B

140 MHz, 0 to 85°C Operation  
3.3-V Phase-lock Loop Clock Driver

REJ03D0828-1000  
(Previous: ADE-205-225H)  
Rev.10.00  
Apr 07, 2006

## Description

The HD74CDCF2510B is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The HD74CDCF2510B operates at 3.3 V  $V_{CC}$  and is designed to drive up to five clock loads per output.

Bank of outputs provide ten low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent independent of the duty cycle at the input clock. Bank of outputs can be enabled or disabled via the control (G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the HD74CDCF2510B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, HD74CDCF2510B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals.

## Features

- Supports PC133 and meets “PC SDRAM registered DIMM specification, Rev. 1.1”
- Phase-lock loop clock distribution for synchronous DRAM applications
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input
- No external RC network required
- Support spread spectrum clock (SSC) synthesizers
- Supports frequencies up to 140 MHz
- 0 to 85°C operating range
- Ordering Information

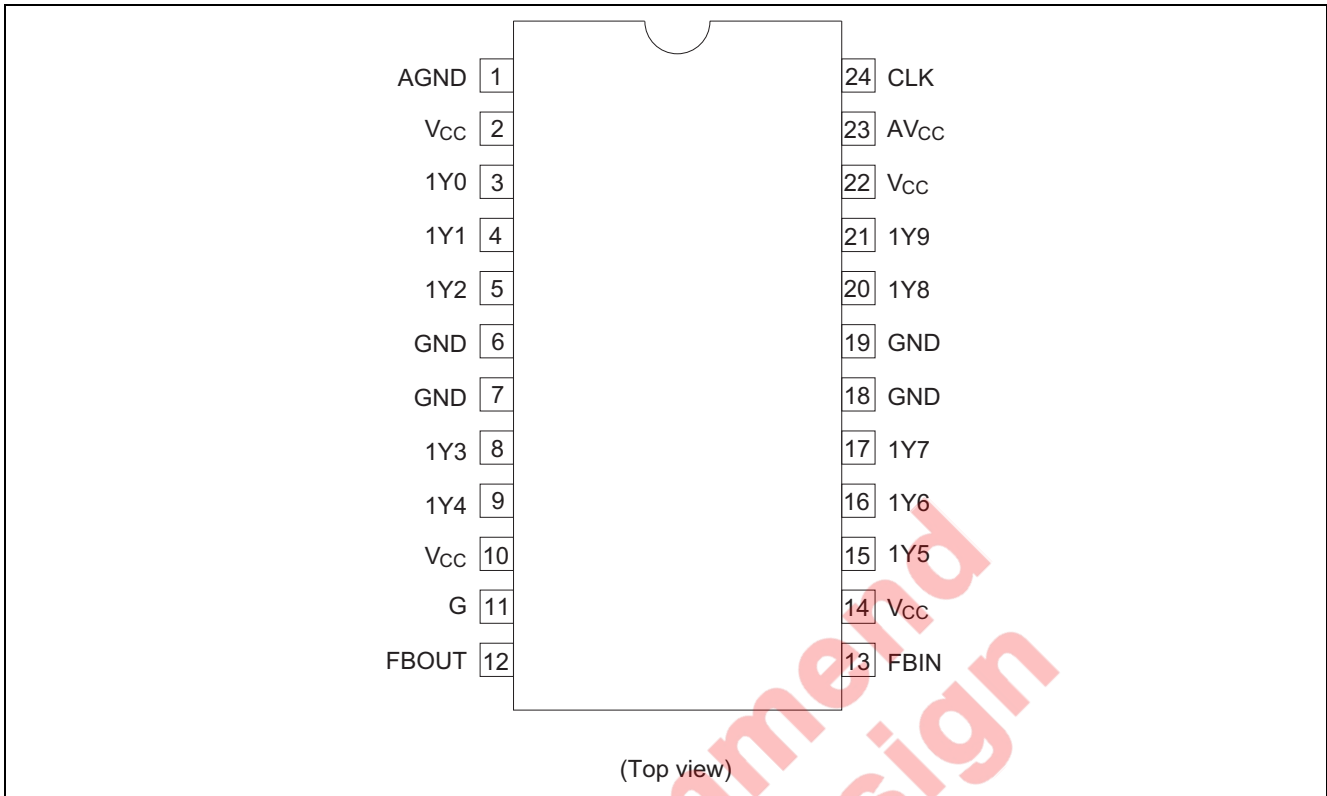
Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74CDCF2510BTEL	TSSOP-24 pin	PTSP0024JB-A (TTP-24DBV)	T	EL (1,000 pcs / Reel)

## Function Table

Inputs		Outputs	
G	CLK	1Y (0:9)	FBOUT
X	L	L	L
L	H	L	H
H	H	H	H

H : High level  
L : Low level  
X : Immaterial

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	-0.5 to 4.6	V	
Input voltage <sup>*1</sup>	$V_I$	-0.5 to 6.5	V	
Output voltage <sup>*1,2</sup>	$V_O$	-0.5 to $V_{CC} + 0.5$	V	
Input clamp current	$I_{IK}$	-50	mA	$V_I < 0$
Output clamp current	$I_{OK}$	$\pm 50$	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	$I_O$	$\pm 50$	mA	$V_O = 0$ to $V_{CC}$
Supply current	$I_{CC}$ or $I_{GND}$	$\pm 100$	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) <sup>*3</sup>	$P_T$	0.7	W	
Storage temperature	$T_{stg}$	-65 to +150	$^\circ\text{C}$	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

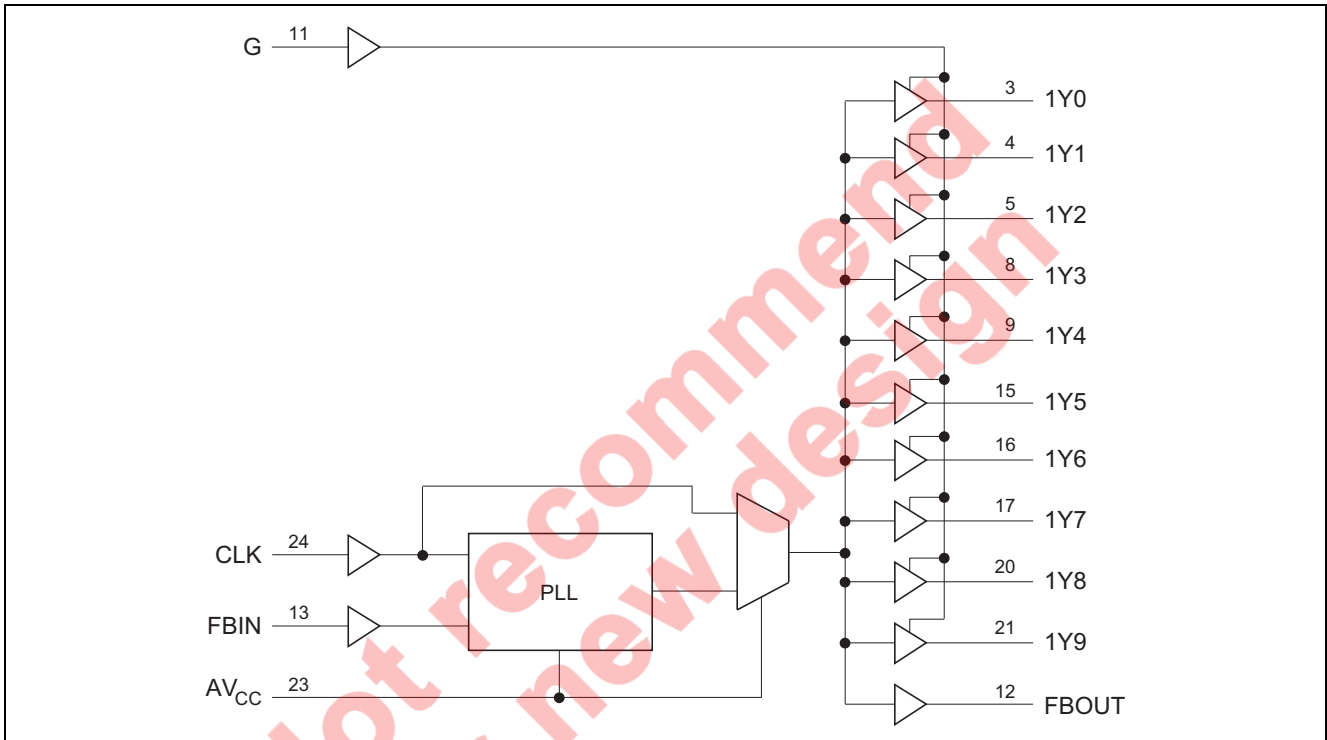
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150 $^\circ\text{C}$  and a board trace length of 750 mils.

### Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions
Supply voltage	$V_{CC}$	3.0	—	3.6	V	
Input voltage	$V_{IH}$	2.0	—	—	V	
	$V_{IL}$	—	—	0.8		
	$V_I$	0	—	$V_{CC}$		
Output current	$I_{OH}$	—	—	-12	mA	
	$I_{OL}$	—	—	12		
Operating temperature	$T_a$	0	—	85	°C	

Note: Unused inputs must be held high or low to prevent them from floating.

### Logic Diagram



**Pin Function**

Pin name	No.	Type	Description
CLK	24	I	Clock input. CLK provides the clock signal to be distributed by the HD74CDCF2510B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN	13	I	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
G	11	I	Output bank enable. G is the output enable for outputs 1Y(0:9). When G is low, outputs 1Y(0:9) are disabled to a logic-low state. When G is high, all outputs 1Y(0:9) are enabled and switch at the same frequency as CLK.
FBOUT	12	O	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
1Y(0:9)	3, 4, 5, 8, 9, 15, 16, 17, 20, 21	O	Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:9) is enabled via the G input. These outputs can be disabled to a logic low state by deasserting the G control input.
AV <sub>CC</sub>	23	Power	Analog power supply. AV <sub>CC</sub> provides the power reference for the analog circuitry. In addition, AV <sub>CC</sub> can be used to bypass the PLL for test purposes. When AV <sub>CC</sub> is strapped to ground, PLL is bypassed. This bypass mode is used for Hitachi test.
AGND	1	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
V <sub>CC</sub>	2, 10, 14, 22	Power	Power supply
GND	6, 7, 18, 19	Ground	Ground

**Electrical Characteristics**

Item	Symbol	Min	Typ <sup>*1</sup>	Max	Unit	Test Conditions
Input clamp voltage	V <sub>IK</sub>	—	—	-1.2	V	V <sub>CC</sub> = 3 V, I <sub>I</sub> = -18 mA
Output voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.2	—	—	V	V <sub>CC</sub> = Min to Max, I <sub>OH</sub> = -100 μA
		2.1	—	—		V <sub>CC</sub> = 3 V, I <sub>OH</sub> = -12 mA
		2.4	—	—		V <sub>CC</sub> = 3 V, I <sub>OH</sub> = -6 mA
	V <sub>OL</sub>	—	—	0.2	V	V <sub>CC</sub> = Min to Max, I <sub>OL</sub> = 100 μA
		—	—	0.8		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 12 mA
		—	—	0.55		V <sub>CC</sub> = 3 V, I <sub>OL</sub> = 6 mA
Input current	I <sub>IN</sub>	—	—	±5	μA	V <sub>CC</sub> = 3.6 V, V <sub>IN</sub> = V <sub>CC</sub> or GND
Quiescent supply current	I <sub>CC</sub>	—	—	10	μA	AV <sub>CC</sub> = GND, V <sub>CC</sub> = 3.6 V, V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0
	ΔI <sub>CC</sub>	—	—	500	μA	AV <sub>CC</sub> = GND, V <sub>CC</sub> = 3.3 to 3.6 V One input at V <sub>CC</sub> -0.6 V, Other inputs at V <sub>CC</sub> or GND
Input capacitance	C <sub>IN</sub>	—	4	—	pF	V <sub>CC</sub> = 3.3 V, V <sub>I</sub> = V <sub>CC</sub> or GND
Output capacitance	C <sub>O</sub>	—	6	—	pF	V <sub>CC</sub> = 3.3 V, V <sub>O</sub> = V <sub>CC</sub> or GND

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Switching Characteristics

( $C_L = 25 \text{ pF}$ ,  $T_a = 0 \text{ to } 85^\circ\text{C}$ )

Item	Symbol	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$			Unit	From (Input)	To (Output)
		Min	Typ	Max			
Phase error time	$t_{pe}$	-125	—	125	ps	CLKIN $\uparrow$ = 133 MHz	FBIN $\uparrow$
Between output pins skew <sup>*1</sup>	$t_{sk(O)}$	—	—	150	ps	Any Y or FBOUT, F (clkin = 133 MHz)	Any Y or FBOUT
Cycle to cycle jitter		-75	—	75	ps	F (clkin = 133 MHz)	Any Y or FBOUT
Duty cycle		45	—	55	%	F (clkin = 133 MHz)	Any Y or FBOUT
Slew rate		5.0	—	1.0	volts/ns		Any Y or FBOUT
Analog power supply rejection (DC to 10 MHz)	$V_{apsr}$ <sup>*2</sup>	100	—	—	mV <sub>P-P</sub>		$AV_{CC}$

Notes: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

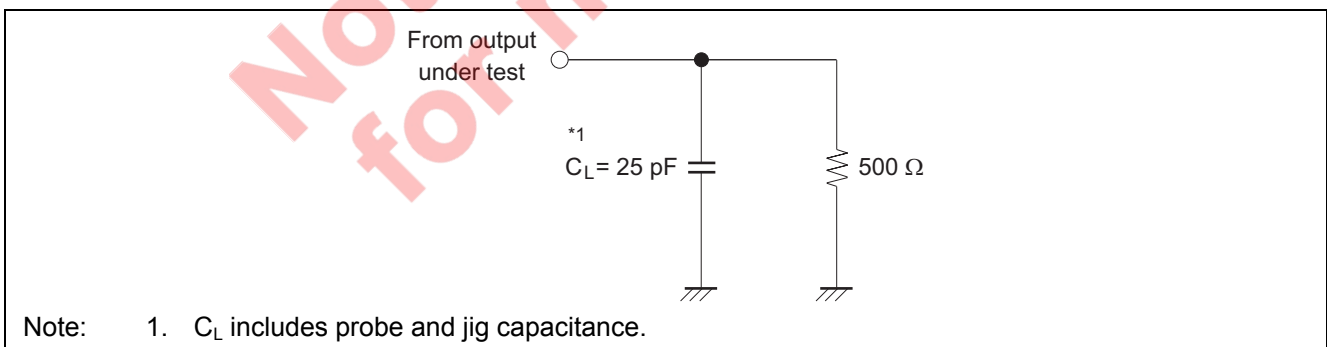
1. The  $t_{sk(O)}$  specification is only valid for equal loading of all outputs.
2. This parameter is characterized but not tested.

Timing Requirements

Item	Symbol	Min	Max	Unit	Test Conditions
Input clock frequency	$f_{clock}$	50	140	MHz	
Input clock duty cycle		40	60	%	
Stabilization time <sup>*1</sup>		—	1	ms	After power up

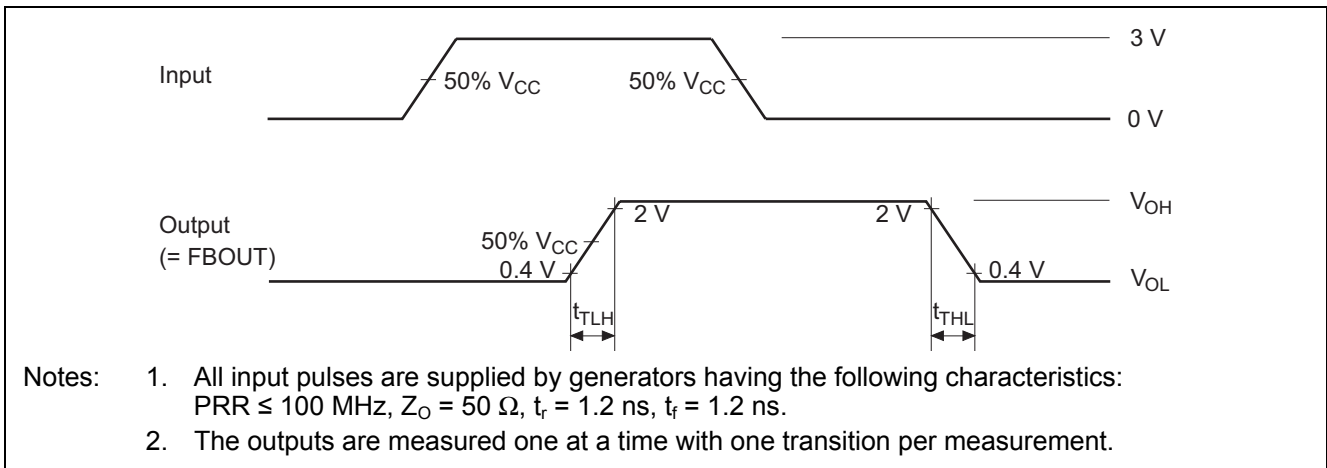
Note: 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

Test Circuit

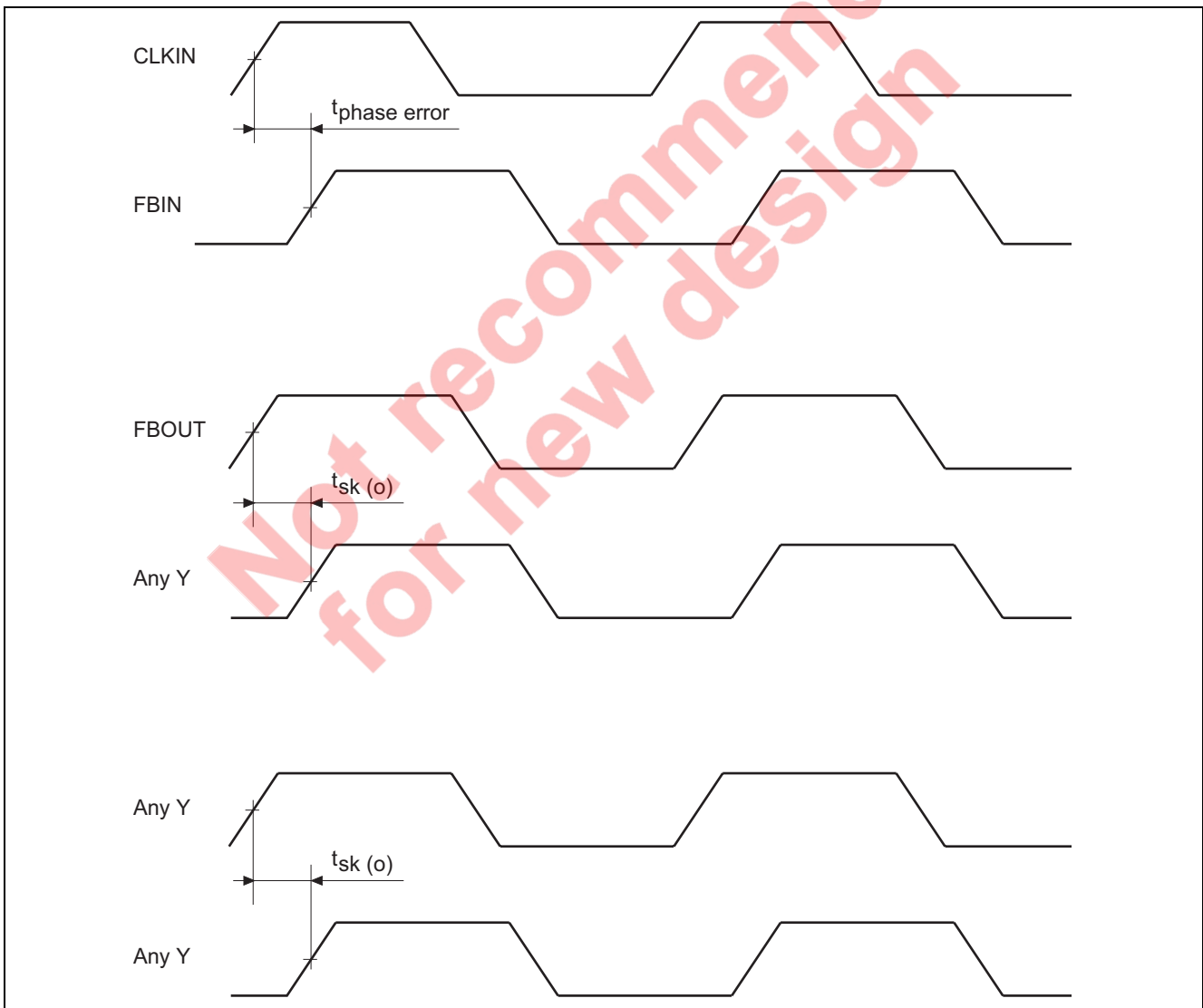


Note: 1.  $C_L$  includes probe and jig capacitance.

Waveforms – 1

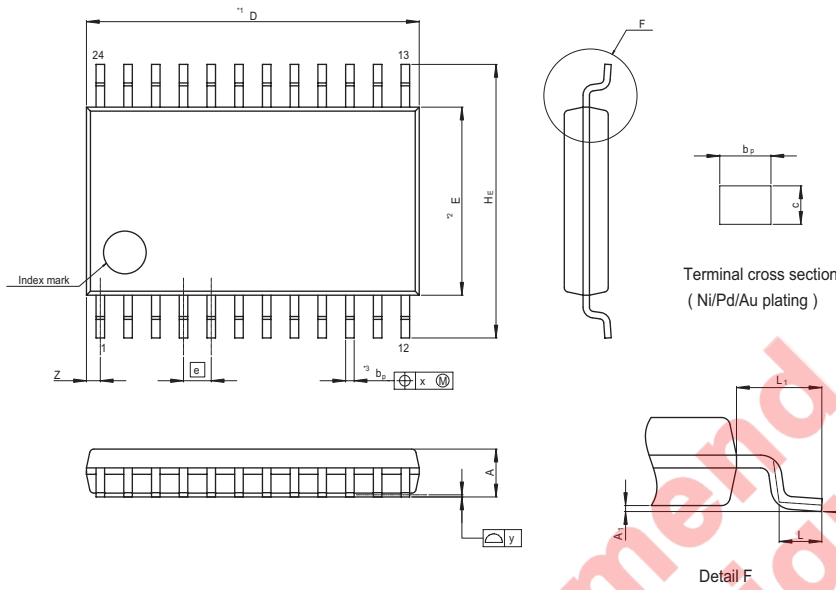


Waveforms – 2



Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP24-4.4x7.8-0.65	PTSP0024JB-A	TTP-24DBV	0.08g



NOTE)  
 1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2"  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION\*\*3\*\*DOES NOT  
 INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.80	8.10
E	—	4.40	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.03	0.07	0.10
A	—	—	1.10
b <sub>p</sub>	0.15	0.20	0.25
b <sub>1</sub>	—	—	—
c	0.10	0.15	0.20
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	6.20	6.40	6.60
Ⓜ	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L <sub>1</sub>	—	1.0	—

Not recommended for new design

**Keep safety first in your circuit designs!**

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

**Notes regarding these materials**

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.  
The information described here may contain technical inaccuracies or typographical errors.  
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.  
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.  
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



**RENESAS SALES OFFICES**

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

**Renesas Technology America, Inc.**

450 Holger Way, San Jose, CA 95134-1368, U.S.A  
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

**Renesas Technology Europe Limited**

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

**Renesas Technology (Shanghai) Co., Ltd.**

Unit 204, 205, AZIAcenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120  
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

**Renesas Technology Hong Kong Ltd.**

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong  
Tel: <852> 2265-6688, Fax: <852> 2730-6071

**Renesas Technology Taiwan Co., Ltd.**

10th Floor, No.99, Fushing North Road, Taipei, Taiwan  
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

**Renesas Technology Singapore Pte. Ltd.**

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632  
Tel: <65> 6213-0200, Fax: <65> 6278-8001

**Renesas Technology Korea Co., Ltd.**

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea  
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510