

HD74CDCV857A

2.5-V Phase-lock Loop Clock Driver

REJ03D0136–0300Z
 (Previous ADE-205-693B (Z))
 Rev.3.00
 Oct.09.2003

Description

The HD74CDCV857A is a high-performance, low-skew, low-jitter, phase locked loop clock driver. It is specifically designed for use with DDR (Double Data Rate) synchronous DRAMs.

Features

- DDR333 / PC2700-Compliant, also meets DDR266 / PC2100 requirement.
- Supports 60 MHz to 170 MHz operation range
- Distributes one differential clock input pair to ten differential clock outputs pairs
- Supports spread spectrum clock requirements meeting the PC100 SDRAM registered DIMM specification
- External feedback pins (FBIN, $\overline{\text{FBIN}}$) are used to synchronize the outputs to the clock input
- Supports 2.5V analog supply voltage (AV_{CC}), and 2.5 V V_{DDQ}
- No external RC network required
- Sleep mode detection
- 48pin TSSOP (Thin Shrink Small Outline Package)

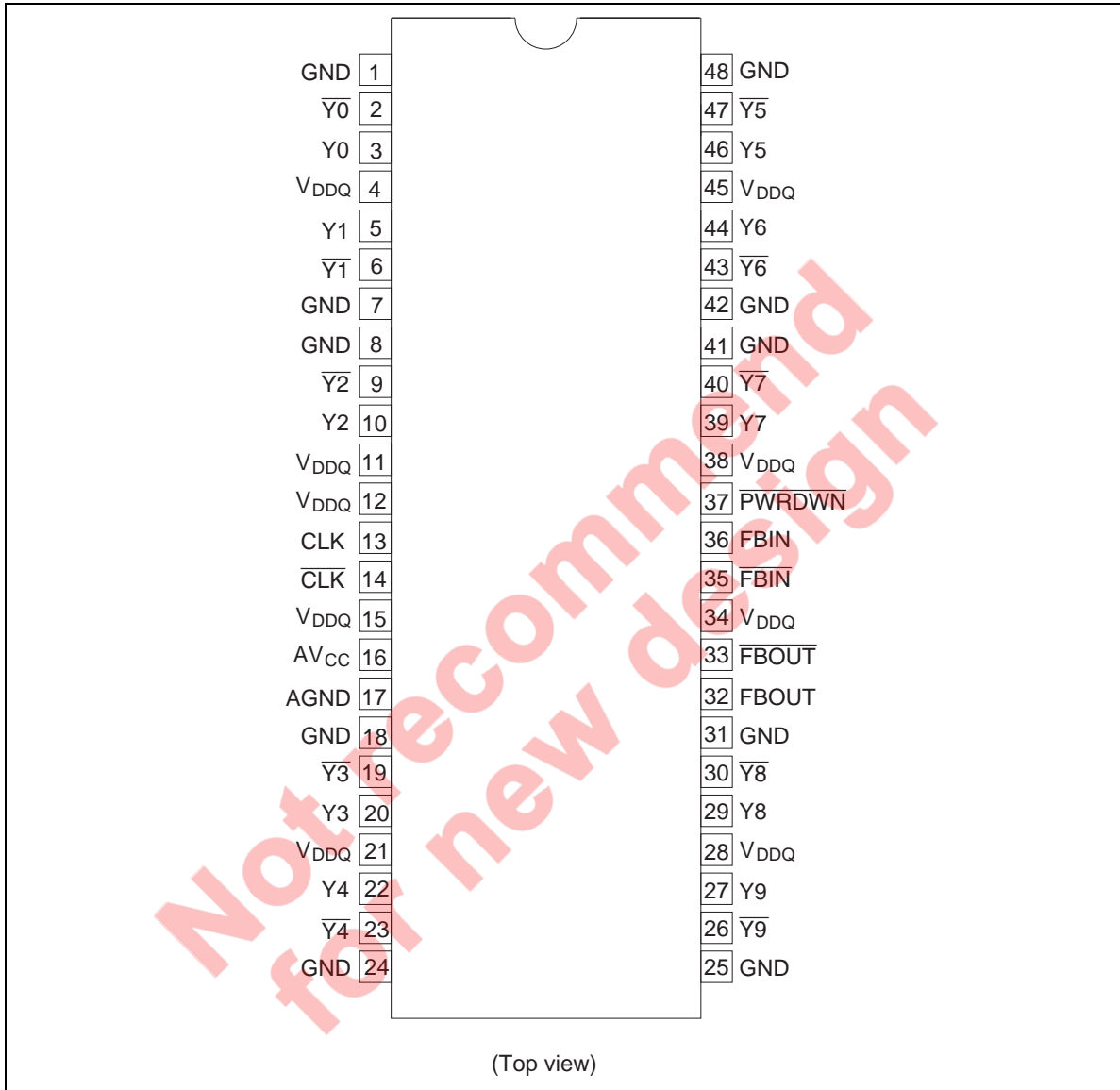
Function Table

Inputs				: Outputs					
AVCC	PWRDWN	CLK	$\overline{\text{CLK}}$: Y	$\overline{\text{Y}}$	FBOUT	$\overline{\text{FBOUT}}$: PLL	
GND	H	L	H	: L	H	L	H	: Bypassed / off ^{*1}	
GND	H	H	L	: H	L	H	L	: Bypassed / off ^{*1}	
X	L	L	H	: Z	Z	Z	Z	: off	
X	L	H	L	: Z	Z	Z	Z	: off	
2.5 V	H	L	H	: L	H	L	H	: on	
2.5 V	H	H	L	: H	L	H	L	: on	
2.5 V	X	Input clock frequency 60 to 170 MHz → 0 MHz		: Z	Z	Z	Z	: off	

H : High level
 L : Low level
 X : Don't care
 Z : High impedance

Notes: 1. Bypassed mode is used for RENESAS test mode.

Pin Arrangement

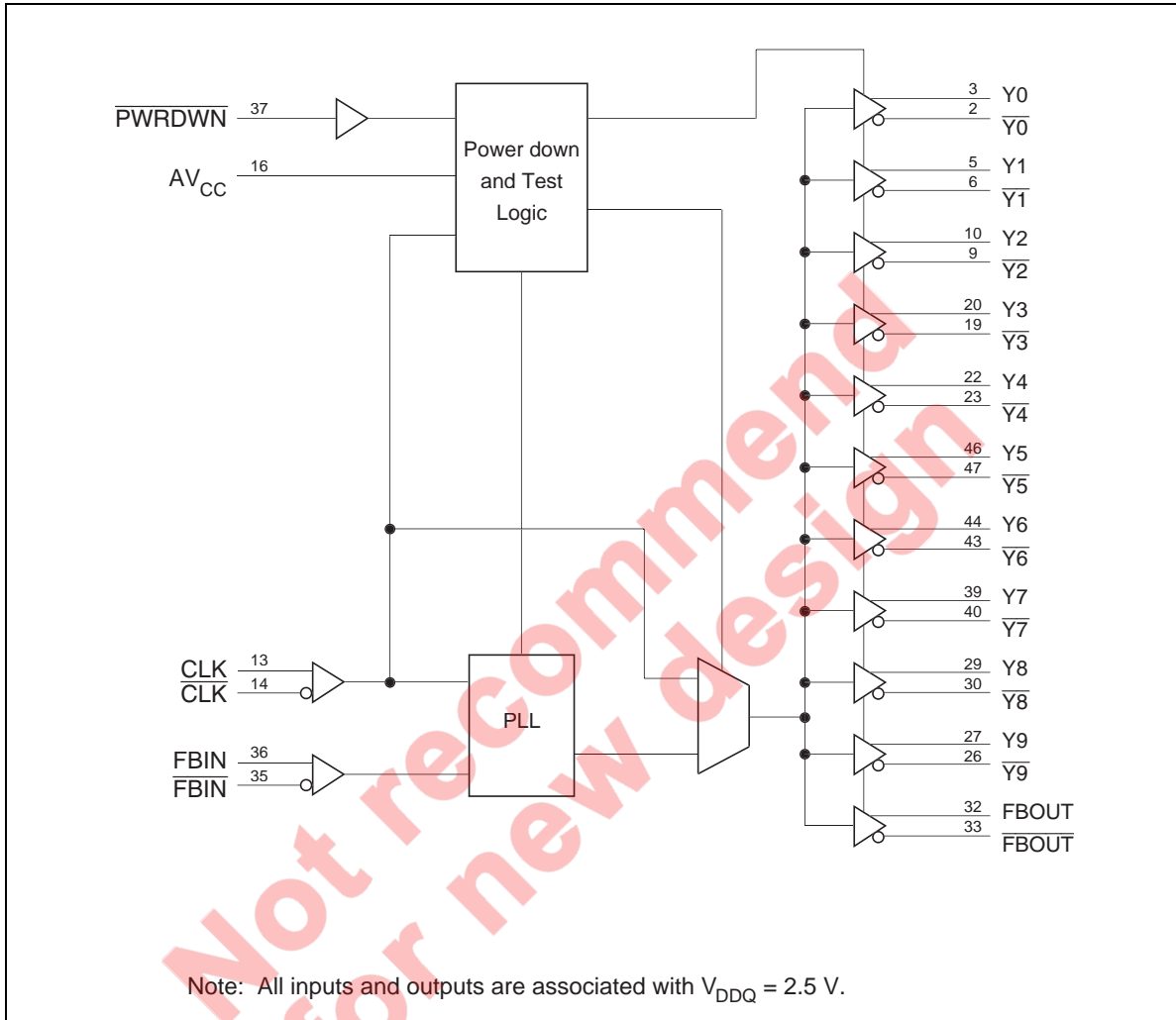


HD74CDCV857A

Pin Function

Pin name	No.	Type	Description
AGND	17	Ground	Analog ground. AGND provides the ground reference for the analog circuitry.
AV _{CC}	16	Power	Analog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. This bypass mode is used for RENESAS test.
CLK, $\overline{\text{CLK}}$	13, 14	I Differential input	Clock input. CLK provides the clock signal to be distributed by the HD74CDCV857A clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal.
FBIN, $\overline{\text{FBIN}}$	35, 36	I Differential input	Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN.
FBOUT, $\overline{\text{FBOUT}}$	32, 33	O Differential output	Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL.
PWRDWN	37	I	Output bank enable. PWRDWN is the output enable for all outputs. When PWRDWN is low, VCO will stop and all outputs are disabled to a high impedance state. When $\overline{\text{PWRDWN}}$ will be returned high, PLL will re-synchroniz to CLK frequency and all outputs are enabled.
GND	1, 7, 8, 18, 24, 25, 31, 41, 42, 48	Ground	Ground
V _{DDQ}	4, 11, 12, 15, 21, 28, 34, 38, 45	Power	Power supply
Y	3, 5, 10, 20, 22, 27, 29, 39, 44, 46	O Differential output	Clock outputs. These outputs provide low-skew copies of CLK.
$\overline{\text{Y}}$	2, 6, 9, 19, 23, 26, 30, 40, 43, 47	O Differential output	Clock outputs. These outputs provide low-skew copies of $\overline{\text{CLK}}$.

Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{DDQ}	-0.5 to 3.6	V	
Input voltage	V_I	-0.5 to $V_{DDQ}+0.5$	V	
Output voltage ^{*1}	V_O	-0.5 to $V_{DDQ} +0.5$	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Output clamp current	I_{OK}	-50	mA	$V_O < 0$
Continuous output current	I_O	±50	mA	$V_O = 0$ to V_{DDQ}
Supply current through each V_{DDQ} or GND	I_{VDDQ} or I_{GND}	±100	mA	
Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air)		0.7	W	
Storage temperature	T_{stg}	-65 to +150	°C	

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

Not recommended for new designs

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit	Conditions	Notes
Output supply voltage	V_{DDQ}	2.3	2.5	2.7	V		
Supply voltage	AV_{CC}	$V_{DDQ}-0.12$	V_{DDQ}	2.7	V		
DC input signal voltage	V_{IN}	-0.3	—	$V_{DDQ}+0.3$	V	All pins	1
High level input voltage	V_{IHG}	1.7	—	$V_{DDQ}+0.3$	V	\overline{PWRDWN} input pin	
Low level input voltage	V_{ILG}	-0.3	—	0.7	V	\overline{PWRDWN} input pin	
Input differential voltage	V_{ID}	0.36	—	$V_{DDQ}+0.6$	V		3
Output differential voltage	V_{OD}	0.70	—	$V_{DDQ}+0.6$	V		
Input differential-pair cross voltage	V_{IX}	$V_{DDQ}/2 - 0.2$	—	$V_{DDQ}/2 + 0.2$	V		2, 3
Output differential-pair cross voltage	V_{OX}	$V_{DDQ}/2 - 0.15$	—	$V_{DDQ}/2 + 0.15$	V		2, 3
Output current	I_{OH}	—	—	-12	mA		
	I_{OL}	—	—	12	mA		
Input clock slew rate	$t_{SL(I)}$	1	—	4	V/ns	20% – 80%	3
Operating temperature	T_a	0	—	70	°C		3

- Notes: Inputs pins must be prevent from floating.
 Feedback inputs (FBIN, FBIN) may float when the device is in low power mode.
- DC input signal voltage specifies the allowable dc execution of differential input.
 - Differential cross point voltage is expected to track variations of V_{DDQ} and is the voltage at which the differential signals must be crossing. (See figure1)
 - Guaranteed by design, not 100% tested in production.

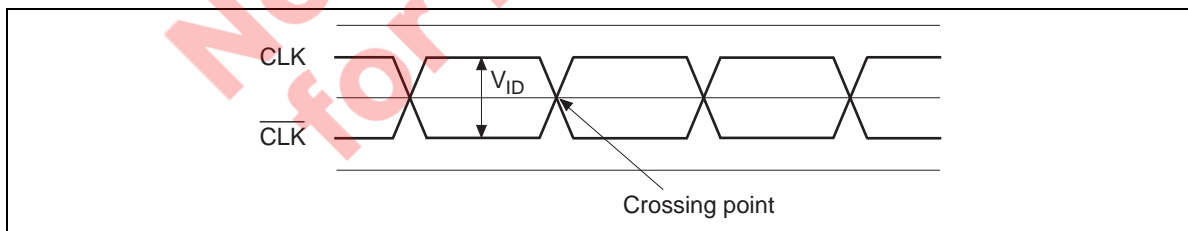


Figure 1 Differential input levels

Electrical Characteristics

Item	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions	Notes	
Input clamp voltage	CLK, $\overline{\text{CLK}}$ FBIN, $\overline{\text{FBIN}}$, G	V_{IK}	—	—	-1.2	V	$I_I = -18 \text{ mA}$, $V_{DDQ} = 2.3 \text{ V}$	
Output voltage	V_{OH}	$V_{DDQ}-0.1$	—	—	—	V	$I_{OH} = -100 \mu\text{A}$, $V_{DDQ} = 2.3 \text{ to } 2.7 \text{ V}$	
		1.7	—	—	—		$I_{OH} = -12 \text{ mA}$, $V_{DDQ} = 2.3 \text{ V}$	
		V_{OL}	—	—	0.1		$I_{OL} = 100 \mu\text{A}$, $V_{DDQ} = 2.3 \text{ to } 2.7 \text{ V}$	
		—	—	0.6		$I_{OL} = 12 \text{ mA}$, $V_{DDQ} = 2.3 \text{ V}$		
Input current	I_I	-10	—	10	μA	$V_I = 0 \text{ V to } 2.7 \text{ V}$, $V_{DDQ} = 2.7 \text{ V}$		
Input capacitance	C_I	—	2.5	—	pF	CLK and $\overline{\text{CLK}}$, FBIN and $\overline{\text{FBIN}}$	2	
Supply current	$D I_{CC}$	—	200	350	mA	$f = 170 \text{ MHz}$, $V_{DDQ} = AV_{CC} = 2.7 \text{ V}$	3	
	$A I_{CC}$	—	9	12				
Supply current in power down mode	I_{CCpd}	—	100	200	μA			

- Note:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.
 2. Guaranteed by design, not 100% tested in production.
 3. All outputs are loaded as shown in Figure2.

Switching Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions	Notes
Period jitter	t_{PER}	-75	—	75	ps	See figure 6, 9	7, 8
Half period jitter	t_{HPER}	-100	—	100	ps	See figure 7, 9	8, 10
Cycle to cycle jitter	t_{CC}	-75	—	75	ps	See figure 5, 9	10
Static phase offset	t_{SPE}	-50	—	50	ps	See figure 3, 9	4, 5, 9, 10
Output clock skew	t_{sk}	—	—	100	ps	See figure 4, 9	
Operating clock frequency	$f_{CLK(O)}$	60	—	200	MHz	See figure 9	1, 2
Application clock frequency	$f_{CLK(A)}$	80	167	170	MHz	See figure 9	1, 3
Input clock duty cycle	t_{DC}	40	—	60	%		10
Output clock Slew rate	$t_{SL(O)}$	1.0	—	2.0	V/ns	See figure 9 20% – 80%	
PLL stabilization time	t_{STAB}	—	—	0.1	ms	See figure 9	6, 10
SSC modulation frequency		30	—	50	KHz		10
SSC clock input frequency deviation		0.00	—	-0.50	%		10
PLL loop bandwidth		—	3	—	MHz		10

- Notes:
1. The PLL must be able to handle spread spectrum induced skew (the specification for this frequency modulation can be found in the latest Intel PC100 Registered DIMM specification)
 2. Operating clock frequency indicates a range over which the PLL must be able to lock, but in which it is not required to meet the other timing parameters.
 3. Application clock frequency indicates a range over which the PLL must meet all timing parameters.
 4. Assumes equal wire length and loading on the clock output and feedback path.
 5. Static phase offset does not include jitter.
 6. Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal after power up.
 7. Period jitter defines the largest variation in clock period, around a nominal clock period.
 8. Period jitter and half-period jitter are independent from each other.
 9. Conditions at $V_{DDQ} = 2.5\text{ V}$, $T_a = 25^\circ\text{C}$.
 10. Guaranteed by design, not 100% tested in production.

HD74CDCV857A

Differential clock outputs are directly terminated by a $120\ \Omega$ resistor. Figure 2 is typical usage conditions of outputs load.

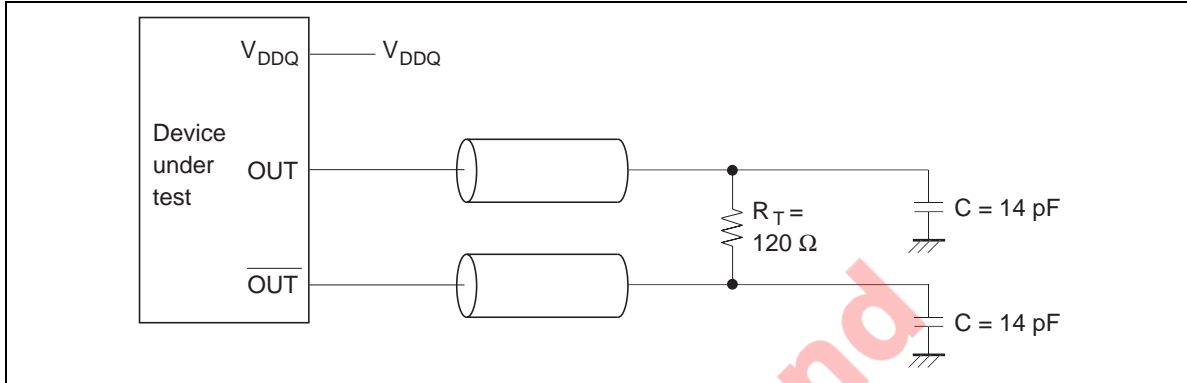


Figure 2 Differential signal using direct termination resistor

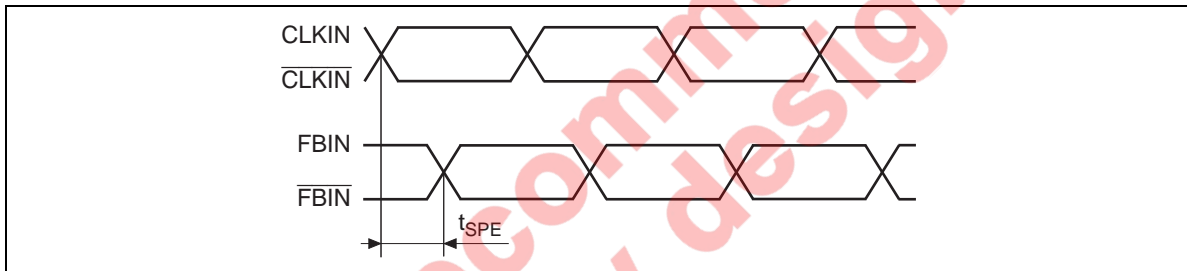


Figure 3 Static phase offset

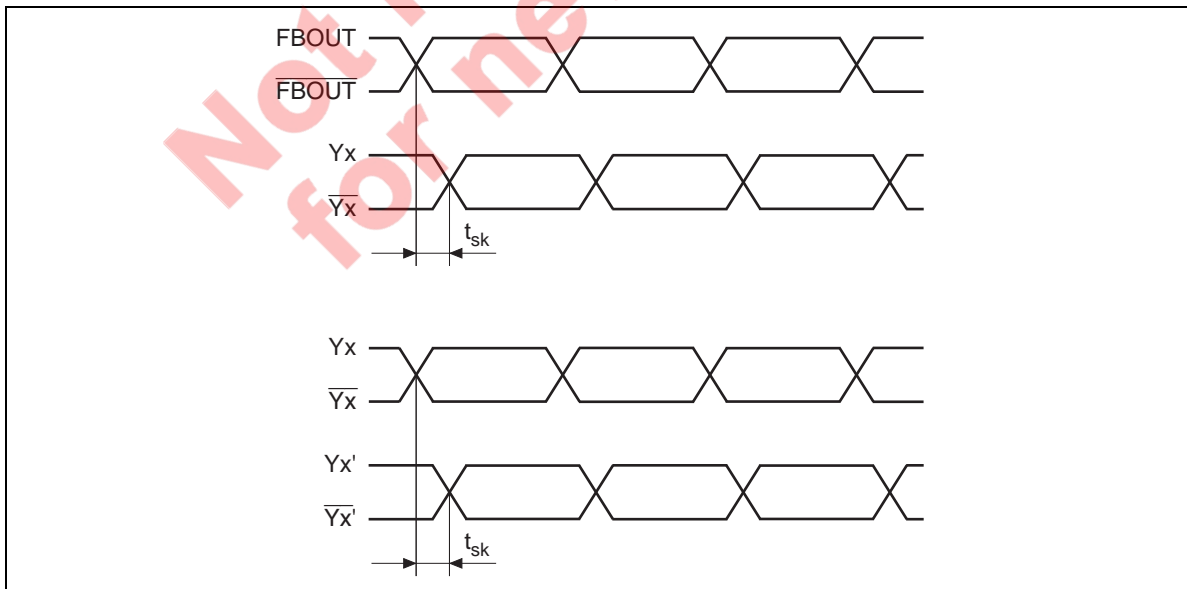


Figure 4 Output skew

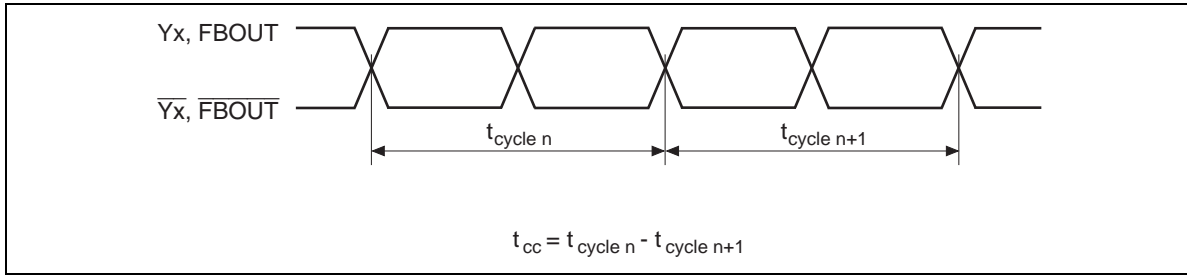


Figure 5 Cycle to cycle jitter

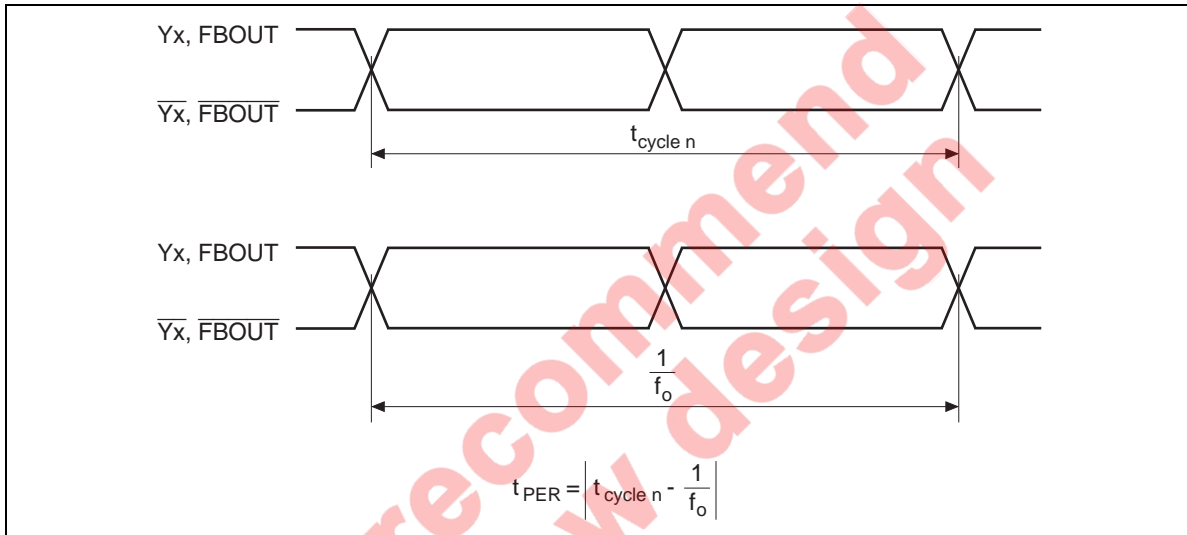


Figure 6 Period jitter

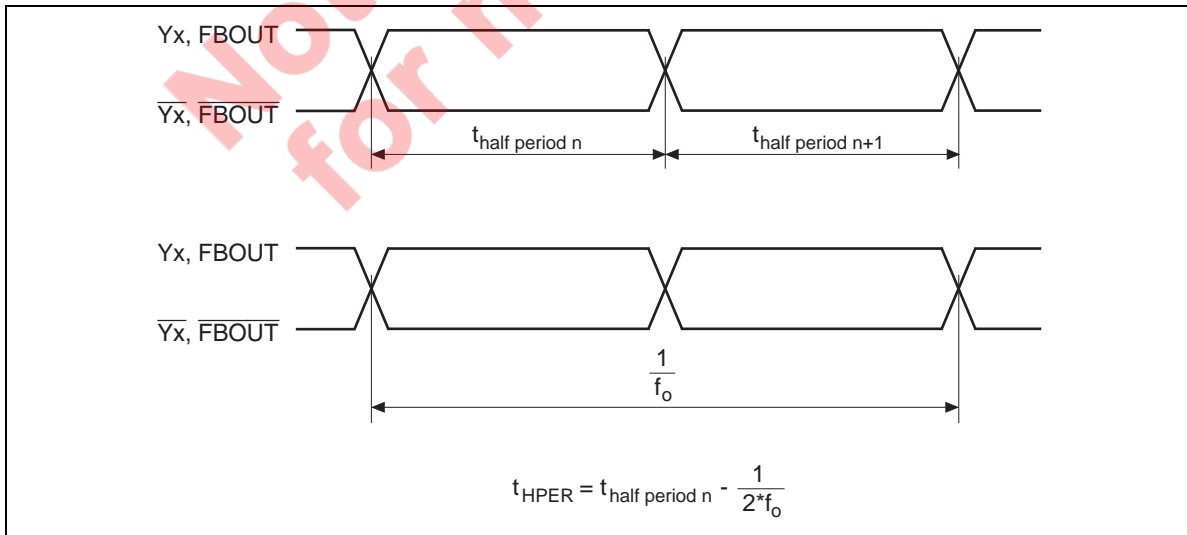


Figure 7 Half period jitter

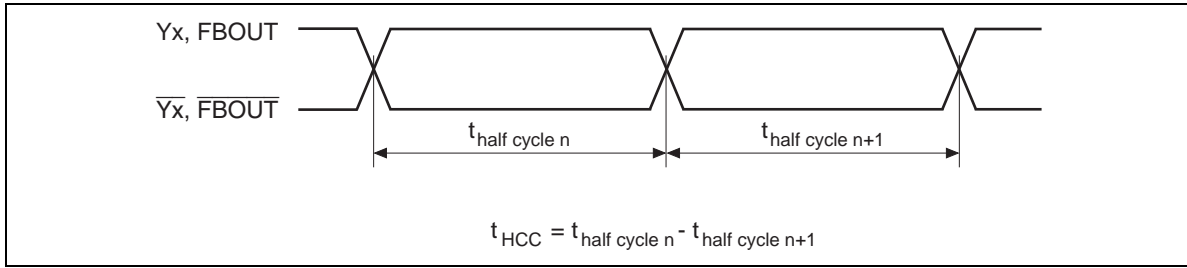


Figure 8 Half cycle to cycle jitter

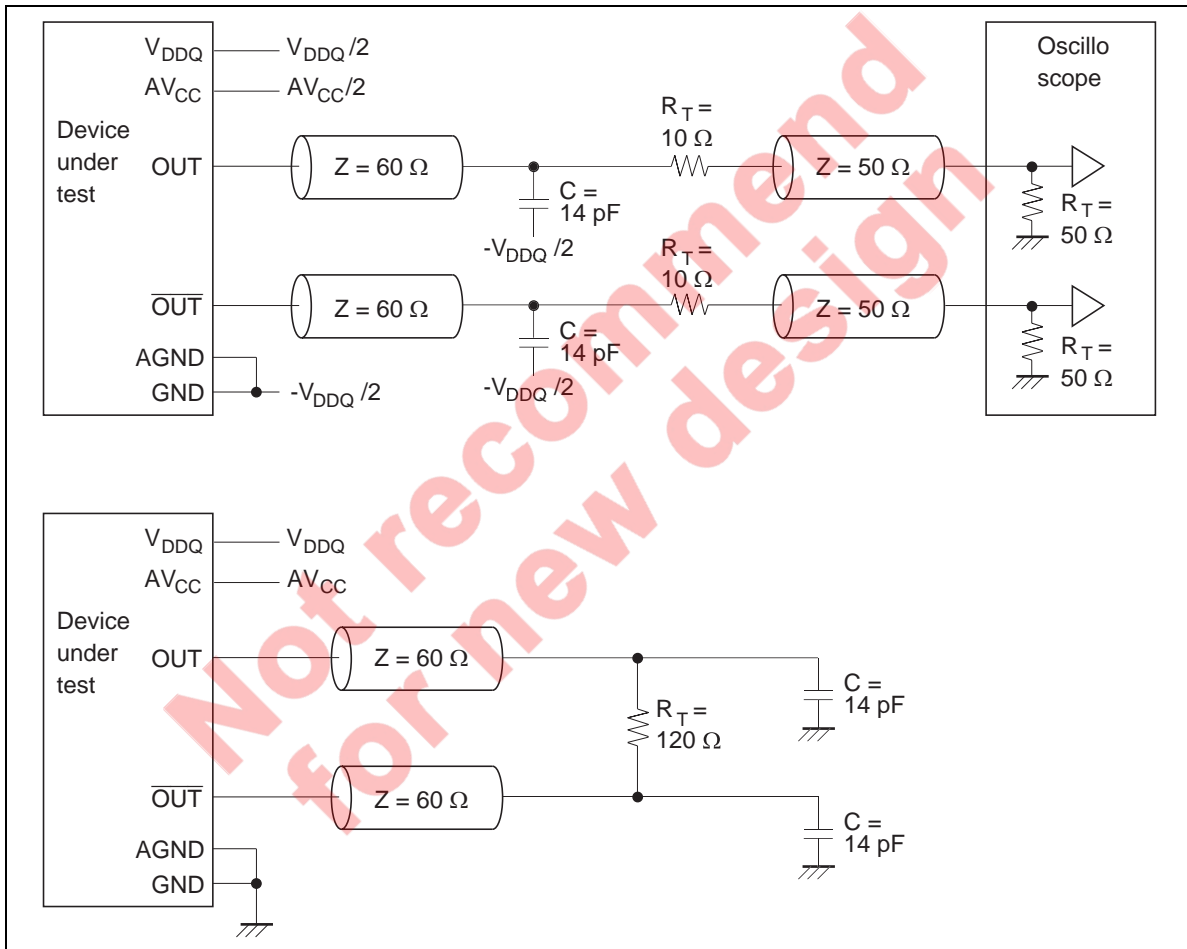
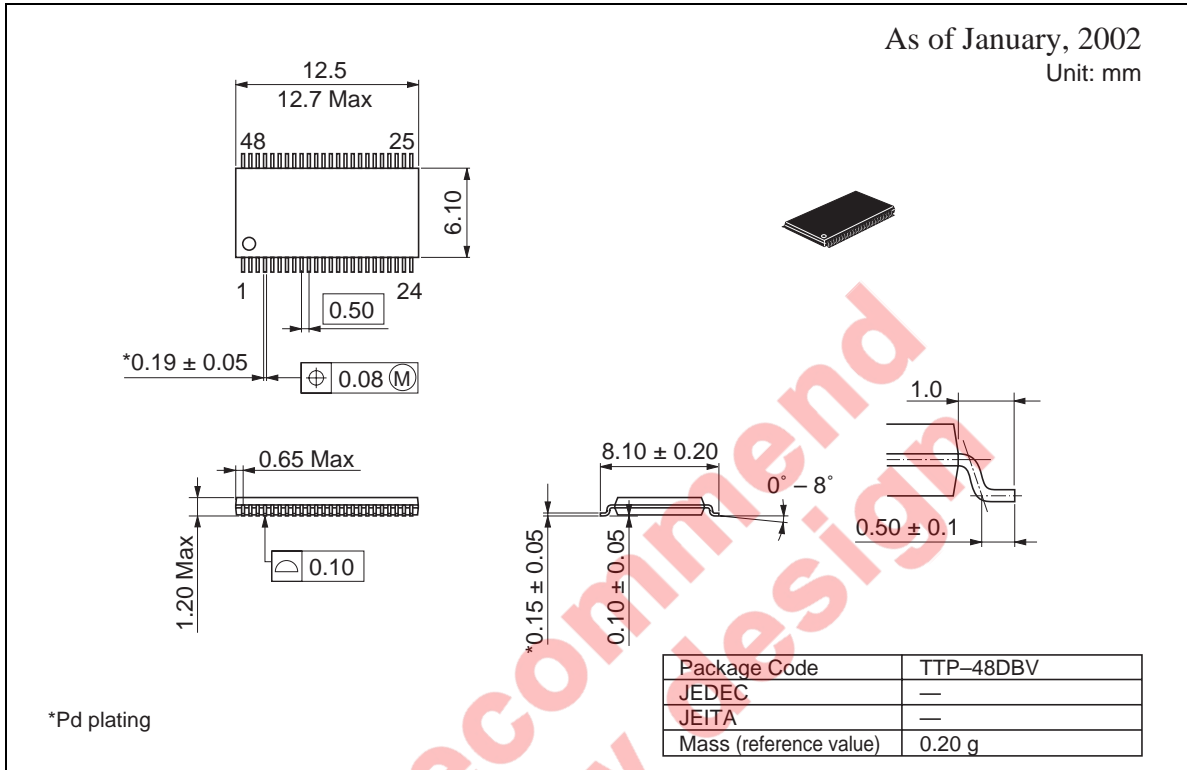


Figure 9 Output load test circuit

Package Dimensions



Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH
Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.
7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.
FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001