
HD74HC114

Dual J-K Flip-Flops (with Preset, Common Clear and
Common Clock)

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Description






This flip-flop is edge sensitive to the clock input and change state on the negative transition of the clock pulse. Each flip-flop has independent J, K and preset inputs and Q and \bar{Q} outputs. Two flip-flops are controlled by a common clear and a common clock. Preset and clear are independent of the clock and accomplished by a low logic level on the corresponding input.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 2 μ A max ($T_a = 25^\circ\text{C}$)

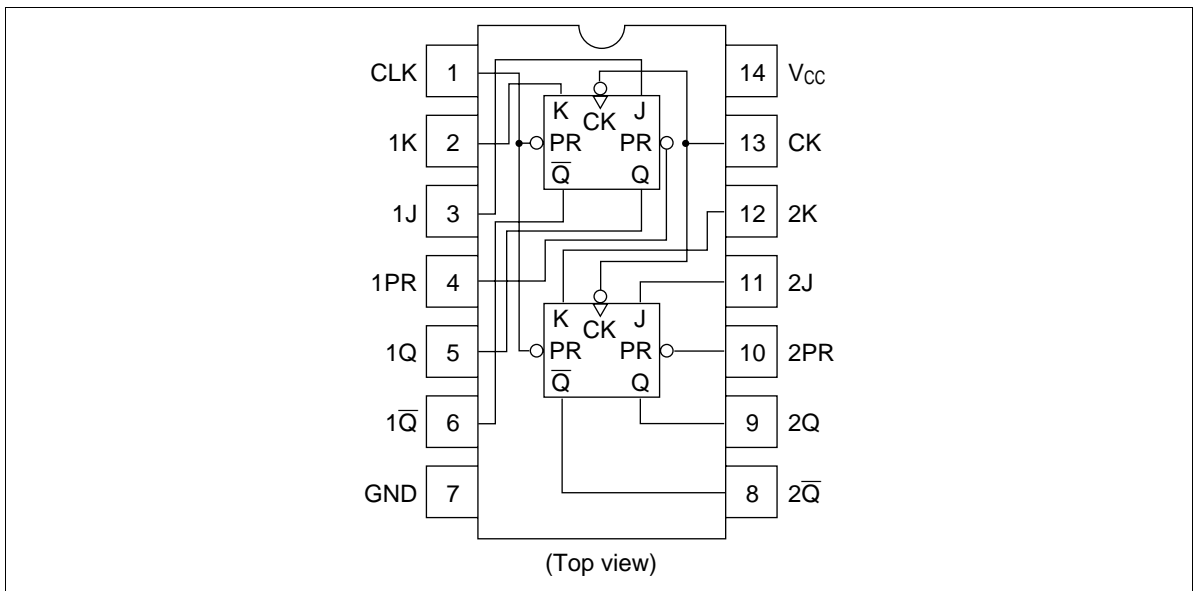
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Function Table

Inputs					Output	
Preset	Clear	Clock	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H* ¹	H* ¹
H	H		L	L	No change	
H	H		L	H	L	H
H	H		H	L	H	L
H	H		H	H	Toggle	
H	H	L	X	X	No change	
H	H	H	X	X	No change	
H	H		X	X	No change	

Note: 1. Q and \bar{Q} will remain HIGH as long as Preset and Clear are Low, but Q and \bar{Q} are unpredictable, if Preset and Clear go HIGH simultaneously.

Pin Arrangement



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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5			V
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL} I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

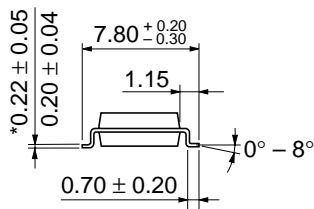
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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Maximum clock frequency	f_{max}	2.0	—	—	6	—	5	MHz			
		4.5	—	—	30	—	24				
		6.0	—	—	35	—	28				
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	Clock to Q or \bar{Q}		
		4.5	—	18	30	—	38				
		6.0	—	—	26	—	33				
		t_{PHL}	2.0	—	—	140	—	175		Clear to Q or \bar{Q}	
			4.5	—	16	28	—	35			
			6.0	—	—	24	—	30			
			2.0	—	—	140	—	175			Preset to Q or \bar{Q}
			4.5	—	16	28	—	35			
			6.0	—	—	24	—	30			
	Pulse width	t_w	2.0	80	—	—	100	—	ns		
			4.5	16	6	—	20	—			
			6.0	14	—	—	17	—			
Setup time	t_{su}	2.0	100	—	—	125	—	ns			
		4.5	20	2	—	25	—				
		6.0	17	—	—	21	—				
Hold time	t_h	2.0	5	—	—	5	—	ns			
		4.5	5	-2	—	5	—				
		6.0	5	—	—	5	—				
Removal time	t_{rem}	2.0	100	—	—	125	—	ns			
		4.5	20	0	—	25	—				
		6.0	17	—	—	21	—				
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns			
		4.5	—	5	15	—	19				
	t_{THL}	6.0	—	—	13	—	16				
Input capacitance	C_{in}	—	—	5	10	—	10	pF			



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

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Hitachi, Ltd.

Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

URL North America : <http://semiconductor.hitachi.com/>
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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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