

HD74HC175

Quad. D-typ Flip-Flops (with Clear)

HITACHI

Description

Information at the D inputs of the HD74HC175 is transferred to the Q and $\overline{Q}$ outputs on the positive going edge of the clock pulse. Both true and compliment outputs from each flip-flop are externally available. All four flip flops are controlled by a common clock and a common clear. Clearing is accomplished by a negative pulse at the clear input. All four Q outputs are cleared to a logic low level and all four $\overline{Q}$ outputs to a logic high level.

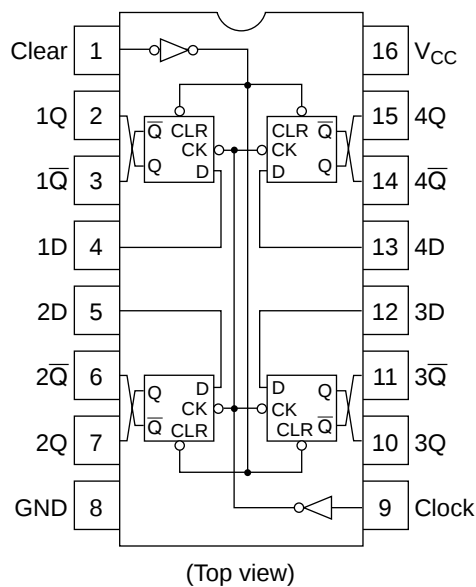
Features

- High Speed Operation: t_{pd} (Clock to Q) = 14 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)

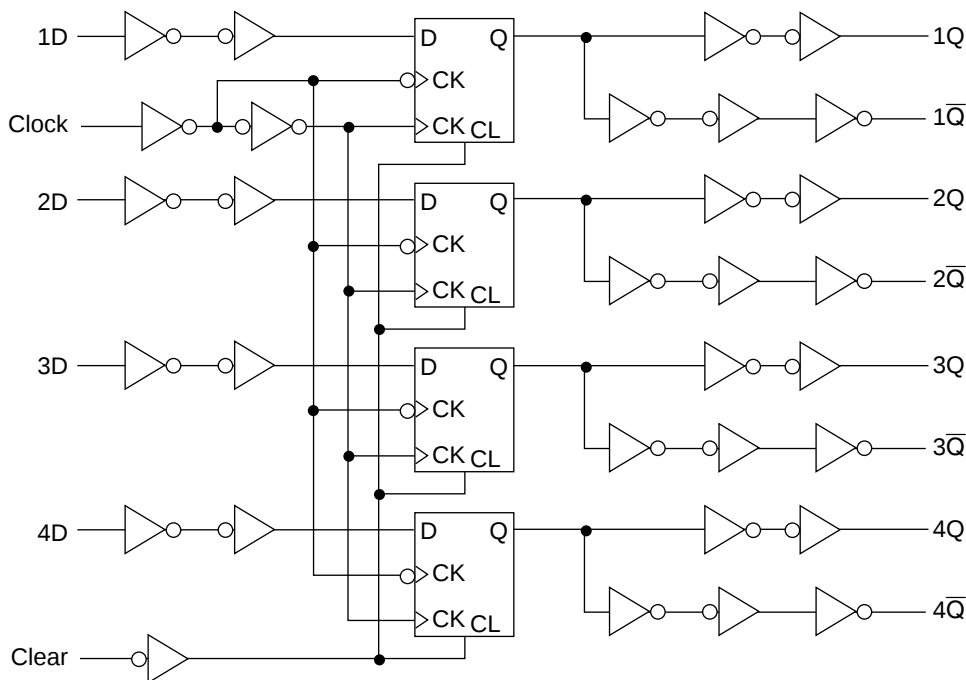
Function Table

Inputs			Outputs	
Clear	Clock	D	Q	$\overline{Q}$
L	X	X	L	H
H		H	H	L
H		L	L	H
H	L	H	no change	

Pin Arrangement



Logic Diagram



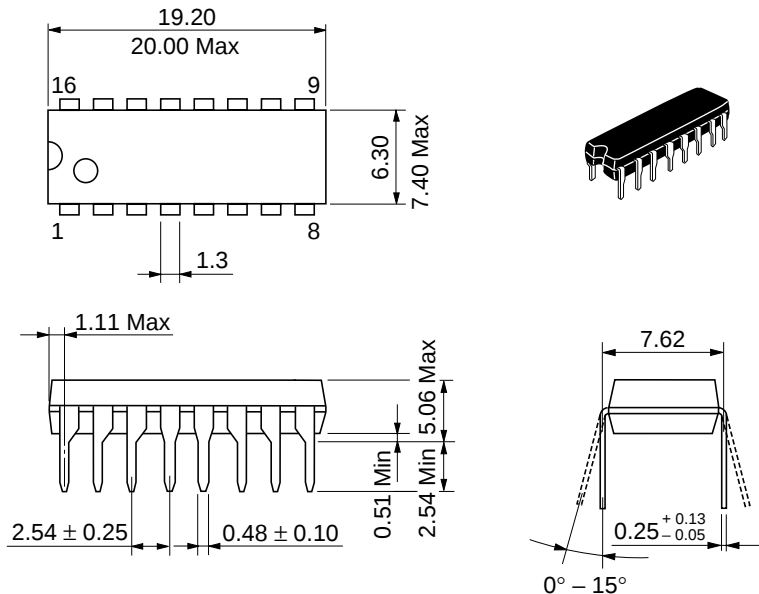
DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = −40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V	Vin = V _{IH} or V _{IL} I _{OH} = −20 μA
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V _{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	I _{OH} = −4 mA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		
		6.0	5.68	—	—	5.63	—		
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	I _{OL} = 20 μA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		
		6.0	—	—	0.26	—	0.33		
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA

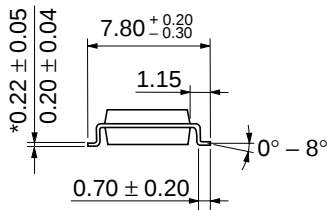
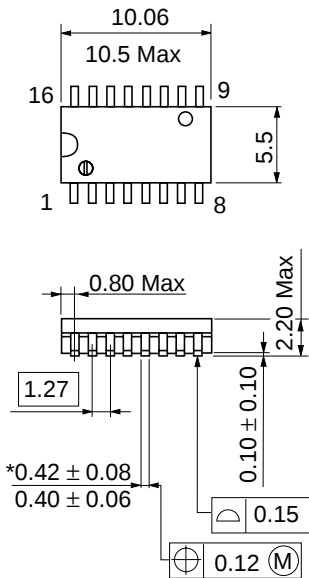
HD74HC175

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{cc} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t _{PLH}	2.0	—	—	150	—	190	ns	Clock to Q or $\overline{Q}$
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
	t _{PHL}	2.0	—	—	185	—	230		Clear to Q or $\overline{Q}$
		4.5	—	14	37	—	46		
		6.0	—	—	31	—	39		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	Data to Clock
		4.5	20	3	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t _h	2.0	5	—	—	5	—	ns	Clock to Data
		4.5	5	-1	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t _{rem}	2.0	100	—	—	125	—	ns	Clear to Clock
		4.5	20	-1	—	25	—		
		6.0	17	—	—	21	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	Clock, Clear
		4.5	16	9	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH} t _{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

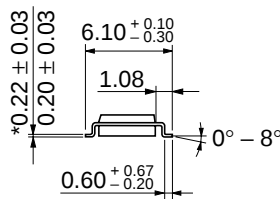
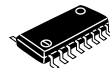
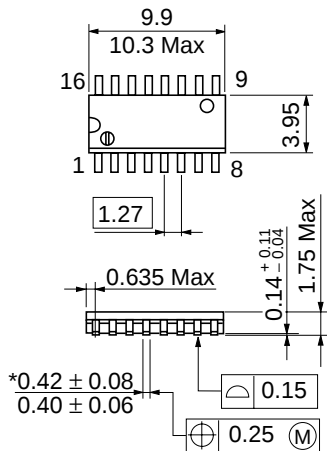


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



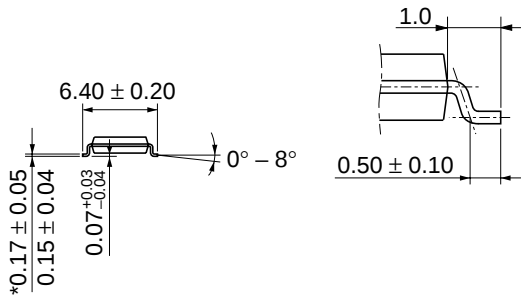
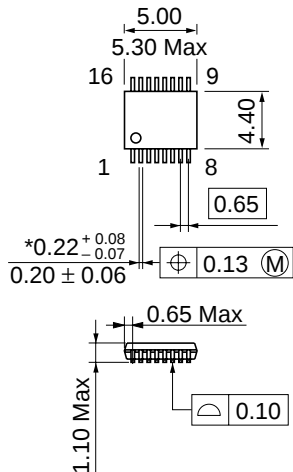
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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