HD74HC190, HD74HC191

Synchronous Up/Down Decade Counter (Single Clock Line)

Synchronous Up/Down 4-bit Binary Counter (Single Clock Line)

REJ03D0587-0300
Rev.3.00
Jan 31, 2006

Description

The HD74HC190 is a 4-bit decade counter and the HD74HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the Enable G input is low. A high at Enable G inhibits counting. The direction of the count is determined by the level of the Down/ Up ($D/\overline{U}$) input. When $D/\overline{U}$ is low, the counter counts up and when $D/\overline{U}$ is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs ($D/\overline{U}$) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Two outputs have been made available to perform the cascading function. Ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

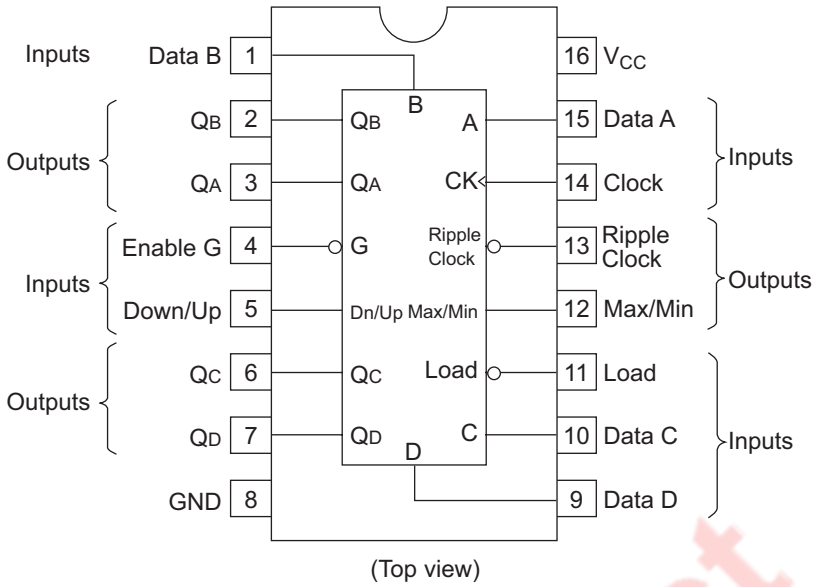
Features

- High Speed Operation: t_{pd} (Clock to Q) = 22 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC190P HD74HC191P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC190FPEL HD74HC191FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC190RPEL HD74HC191RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement

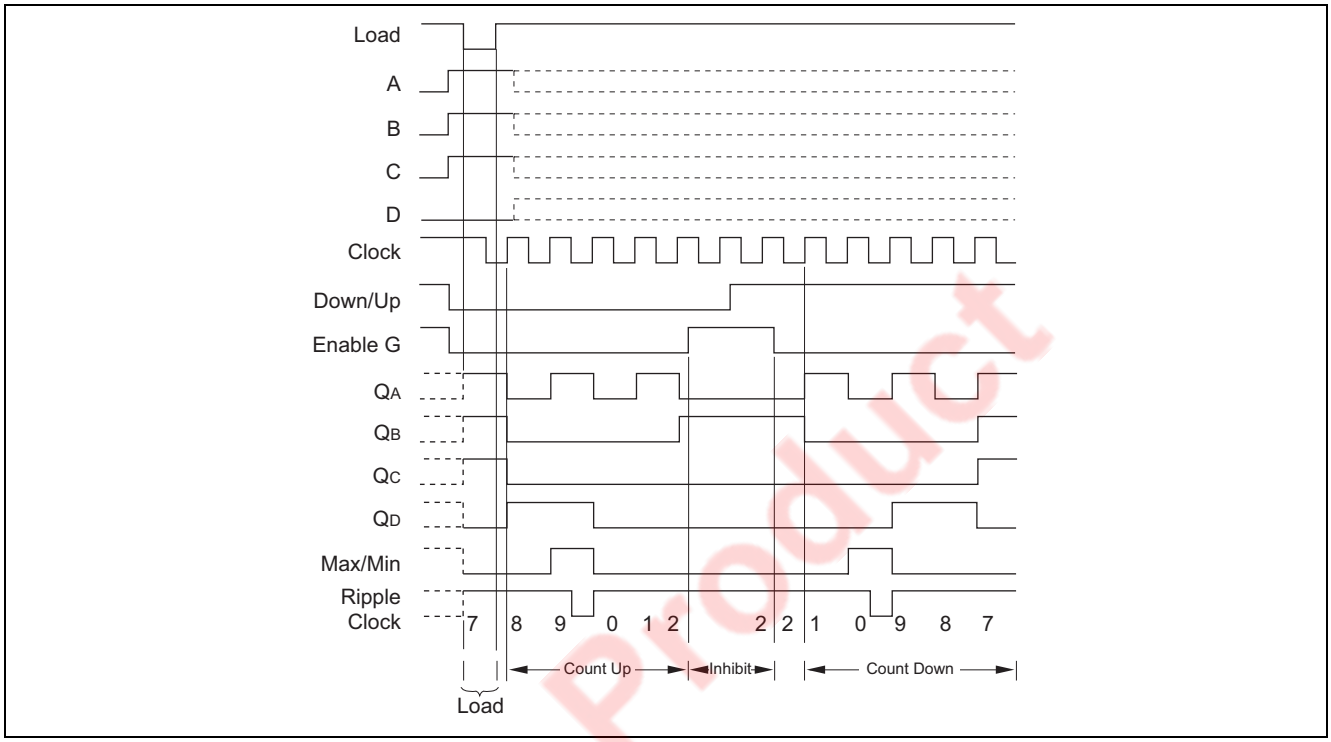


Timing Chart

HD74HC190

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), nine, eight and seven.

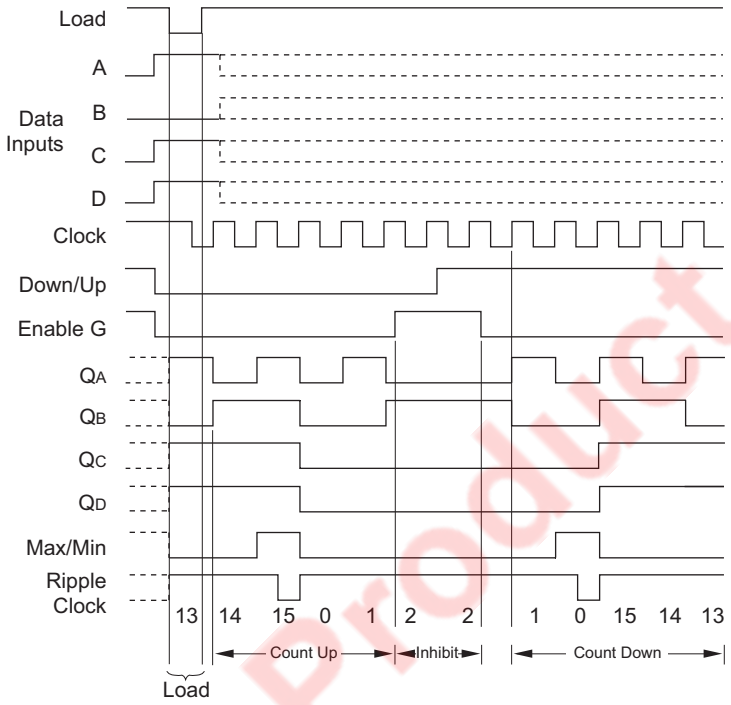


Timing Chart

HD74HC191

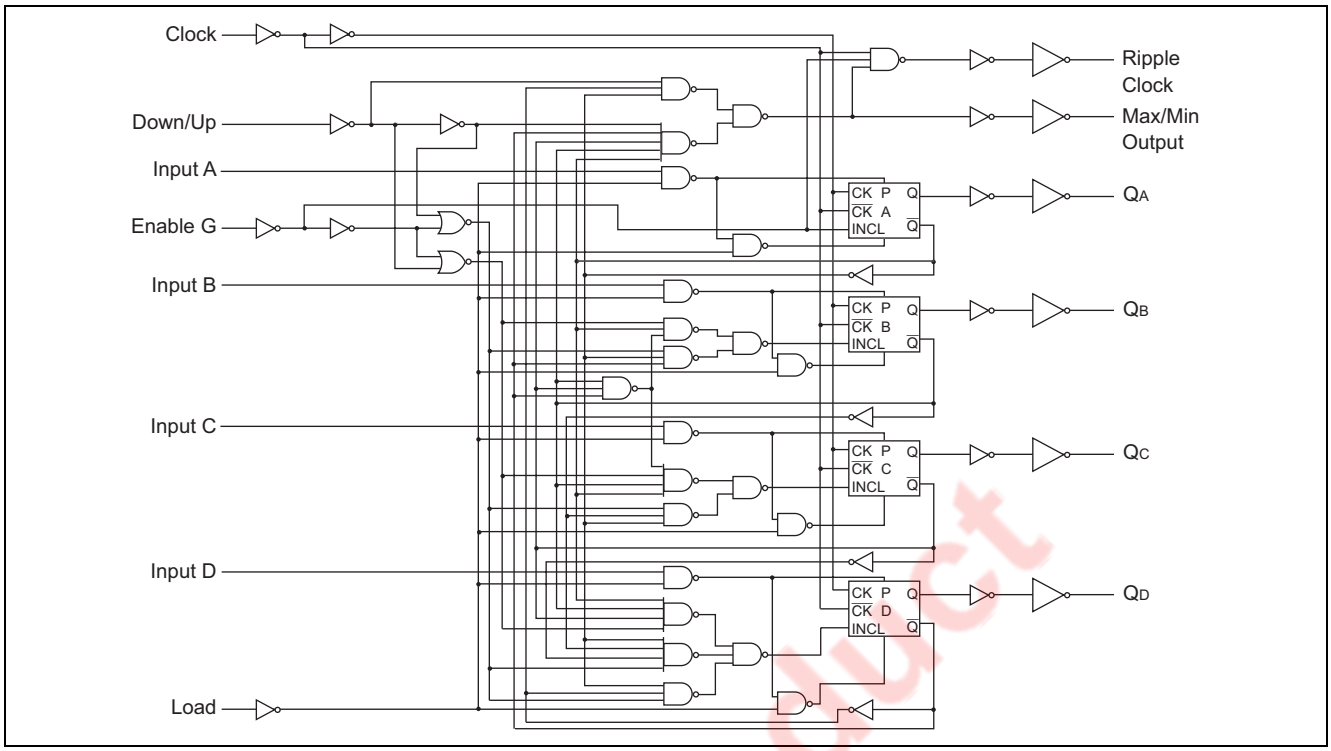
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen and thirteen.

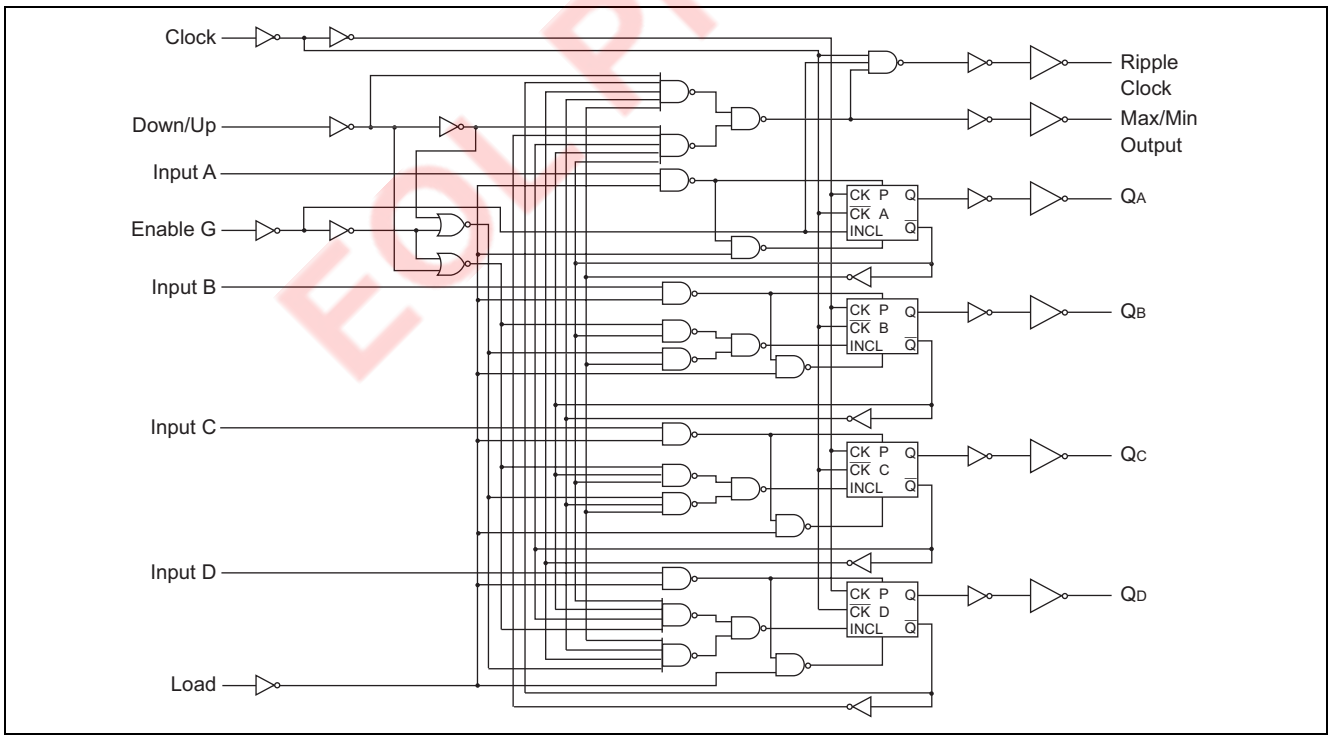


Logic Diagram

HD74HC190



HD74HC191



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	–0.5 to 7.0	V
Input / Output voltage	Vin, Vout	–0.5 to V_{CC} +0.5	V
Input / Output diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC}, GND current	I_{CC} or I_{GND}	±50	mA
Power dissipation	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to 85	°C	
Input rise / fall time*1	t_r, t_f	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

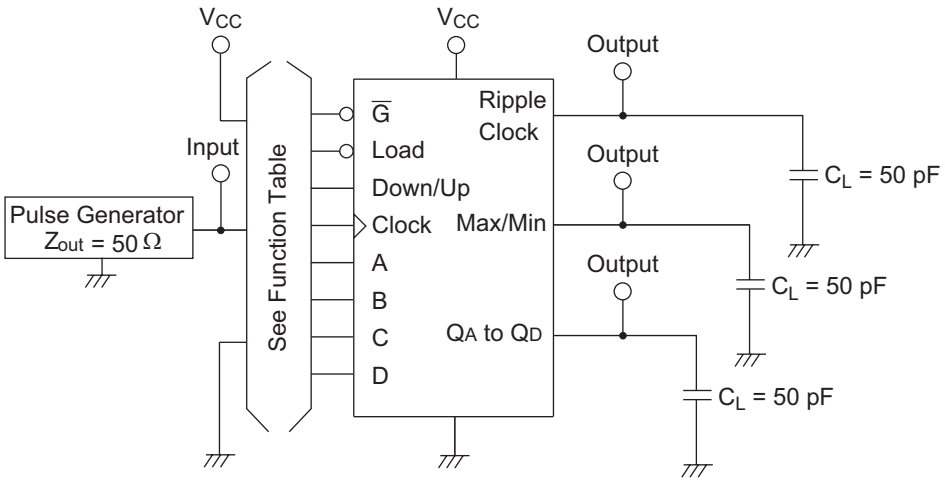
Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to+85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V_{CC} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH}, t_{PHL}	2.0	—	—	265	—	335	ns	Load to Q
		4.5	—	21	53	—	66		
		6.0	—	—	45	—	56		
		2.0	—	—	230	—	290	ns	Data to Q
		4.5	—	18	46	—	58		
		6.0	—	—	39	—	49		
		2.0	—	—	120	—	150	ns	Clock to RC
		4.5	—	14	24	—	30		
		6.0	—	—	20	—	26		
		2.0	—	—	190	—	240	ns	Clock to Q
		4.5	—	22	38	—	48		
		6.0	—	—	32	—	41		
		2.0	—	—	250	—	315	ns	Clock to max/min
		4.5	—	26	50	—	63		
		6.0	—	—	43	—	54		
		2.0	—	—	230	—	290	ns	Down/up to RC
		4.5	—	20	46	—	58		
		6.0	—	—	39	—	49		
		2.0	—	—	130	—	165	ns	G to RC
		4.5	—	14	26	—	33		
		6.0	—	—	22	—	28		
		2.0	—	—	190	—	240	ns	Down/up to max/min
		4.5	—	17	38	—	48		
		6.0	—	—	32	—	41		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	–	—	17	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	
		4.5	0	–6	—	0	—		
		6.0	0	—	—	0	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH}, t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

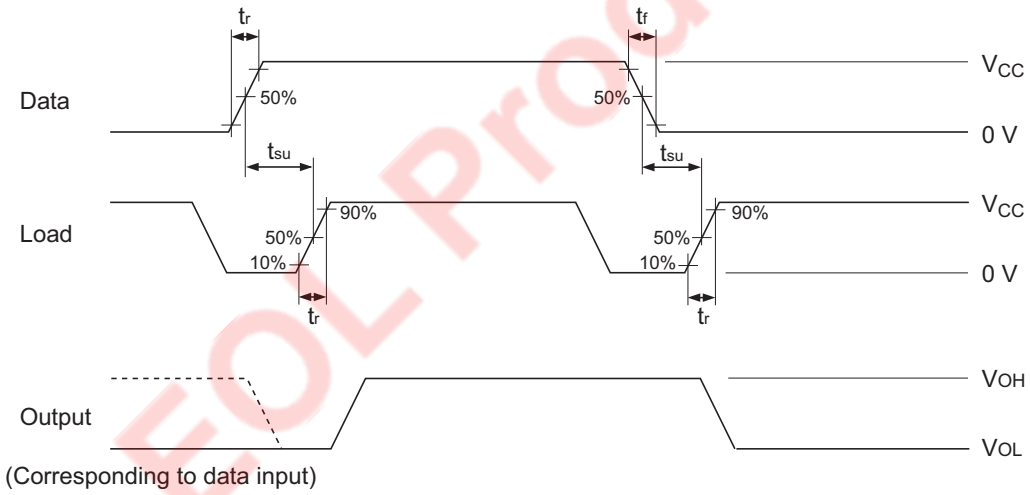
Test Circuit



Note : 1. C_L includes probe and jig capacitance.

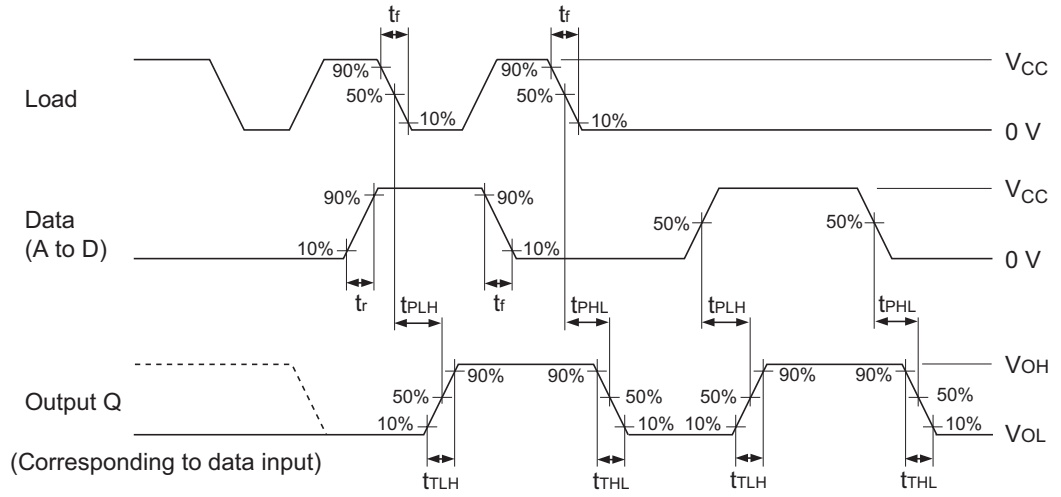
Waveforms

• Wavwform – 1



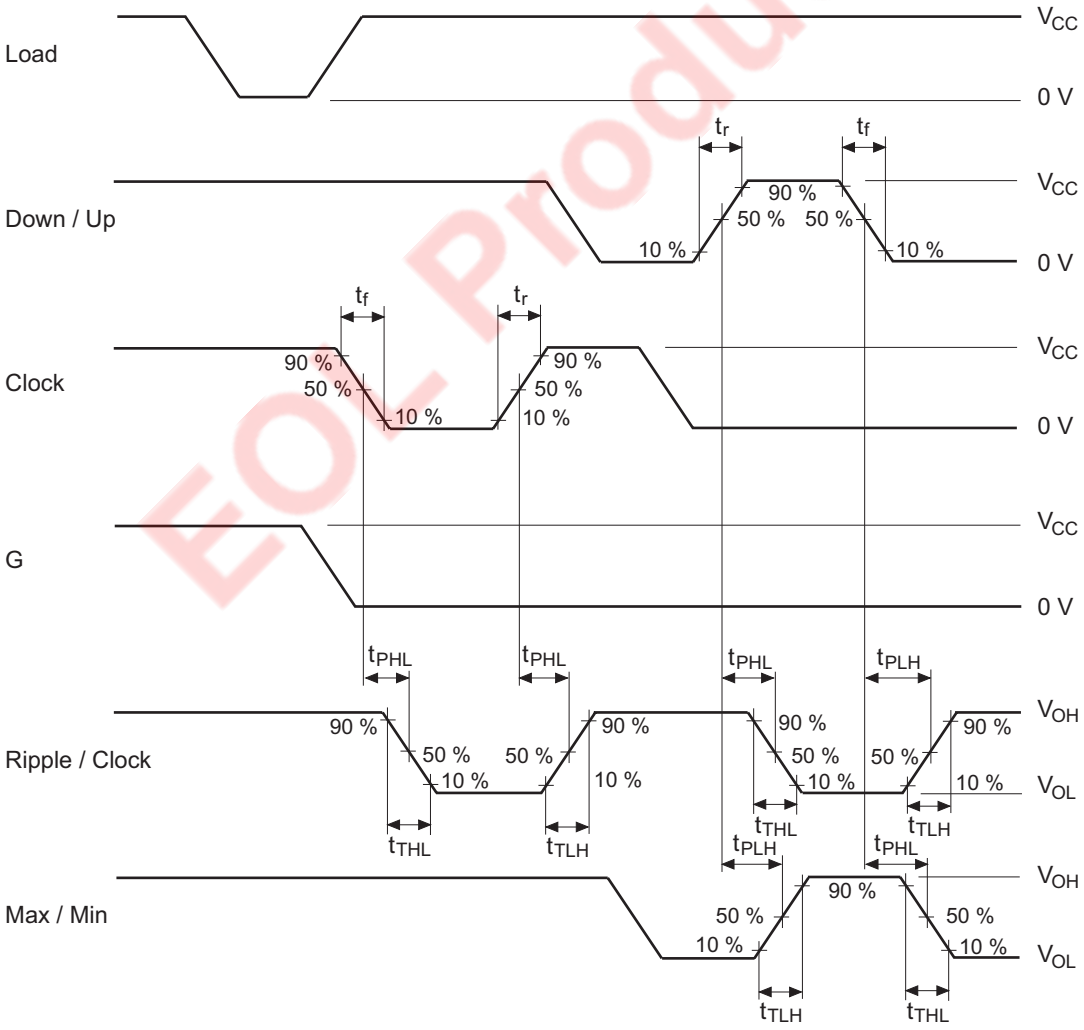
Note : 1. Input : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns

• Waveform – 2



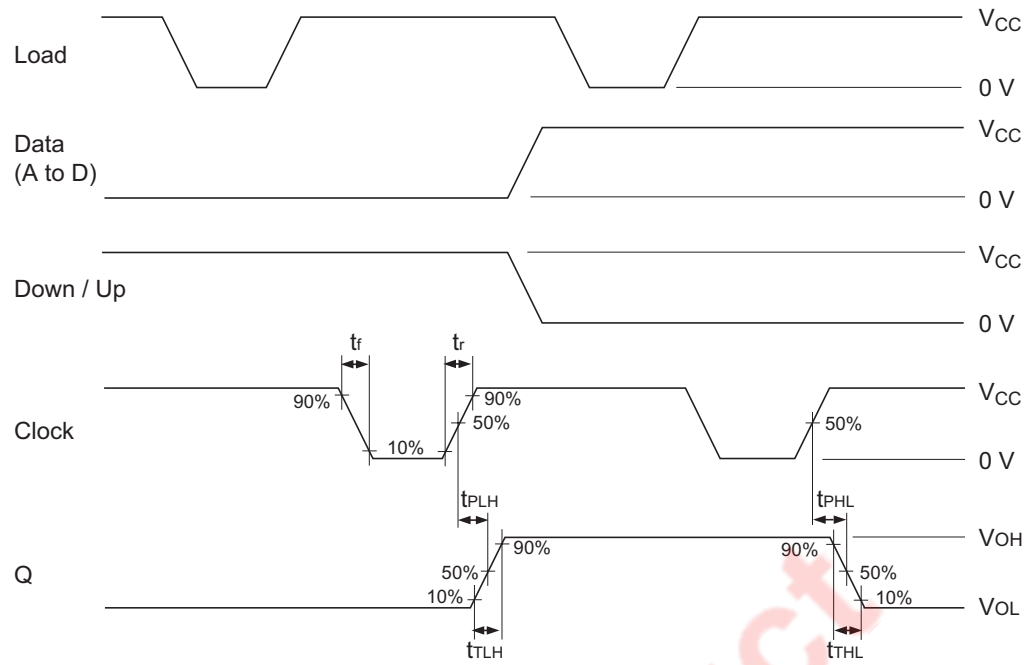
Notes : 1. Input pulse : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. Conditions on other inputs are Vcc.

• Waveform – 3



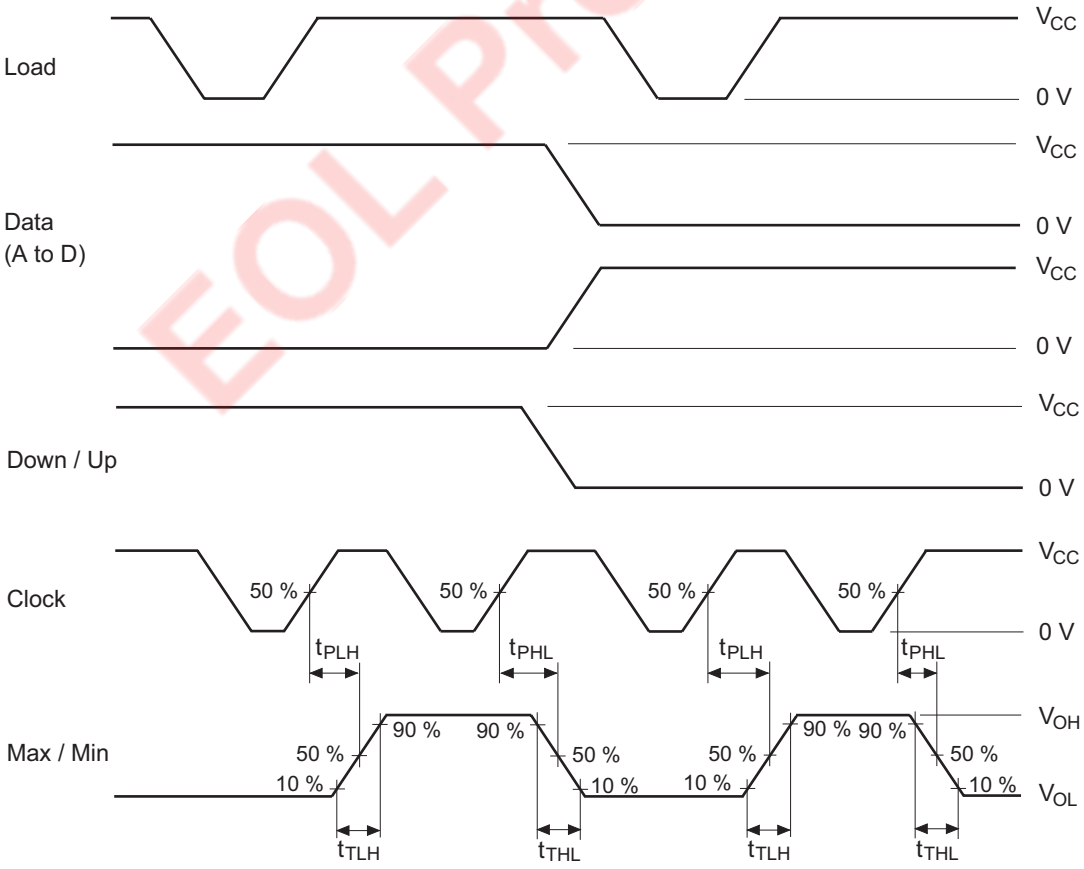
Notes : 1. Input pulse : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. All data inputs are GND.

• Waveform – 4



Notes : 1. Input pulse : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. Enable = GND

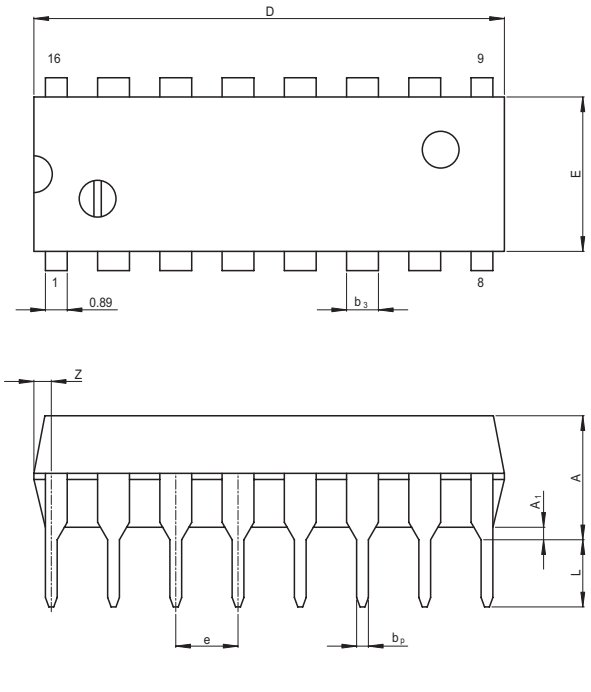
• Waveform – 5



Notes : 1. Input pulse : PRR ≤ 1 MHz, Zo = 50 Ω, t_r ≤ 6 ns, t_f ≤ 6 ns
2. Enable = GND

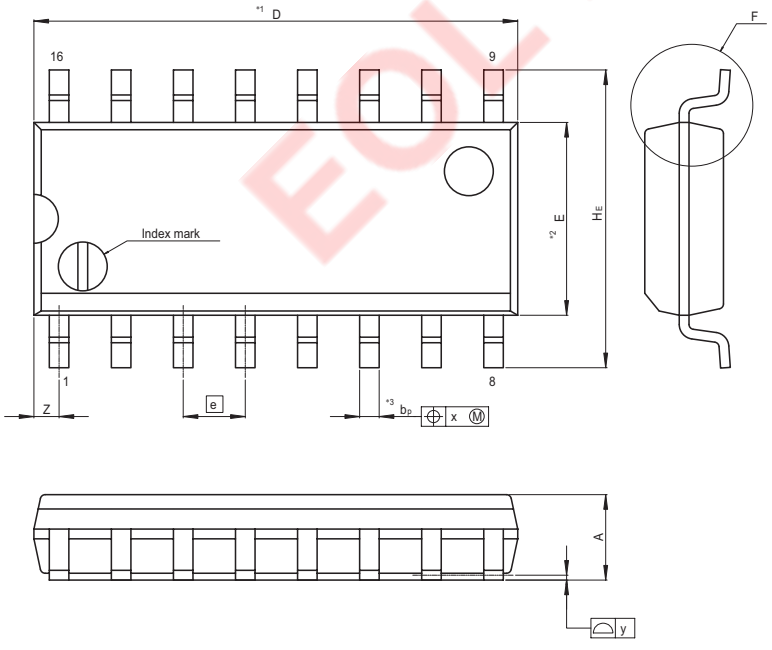
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g

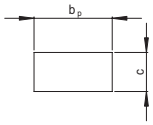


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A 1	0.51	—	—
b p	0.40	0.48	0.56
b 3	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

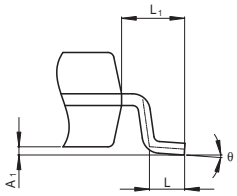
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-3.95x9.9-1.27	PRSP0016DG-A	FP-16DNV	0.15g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



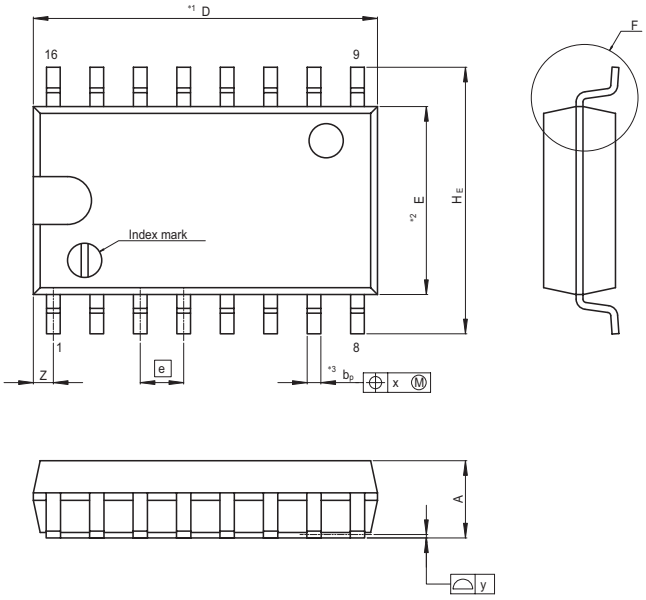
Terminal cross section
(Ni/Pd/Au plating)



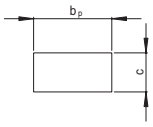
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A 2	—	—	—
A 1	0.10	0.14	0.25
A	—	—	1.75
b p	0.34	0.40	0.46
b 1	—	—	—
c	0.15	0.20	0.25
c 1	—	—	—
θ	0°	—	8°
H E	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L 1	—	1.08	—

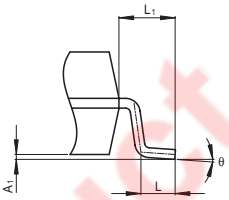
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A_2	——	——	——
A_1	0.00	0.10	0.20
A	——	——	2.20
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.15	0.20	0.25
c_1	——	——	——
θ	0°	——	8°
H_E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L_1	——	1.15	——

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http://www.renesas.com

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