
HD74HC190/HD74HC191

Synchronous Up/Down Decade Counter (Single Clock Line)
Synchronous Up/Down 4-bit Binary Counter (Single Clock Line)

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Description

The HD74HC190 and HD74HC191 are synchronous, reversible up/down counters. The HD74HC190 is a 4-bit decade counter and the HD74HC191 is a 4-bit binary counter. Synchronous counting operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four flip-flops are triggered on a low-to-high-level transition of the clock input if the Enable G input is low. A high at Enable G inhibits counting. The direction of the count is determined by the level of the Down/ Up (D/\bar{U}) input. When D/\bar{U} is low, the counter counts up and when D/\bar{U} is high, it counts down.

These counters feature a fully independent clock circuit. Changes at the control inputs (D/\bar{U}) that will modify the operating mode have no effect on the contents of the counter until clocking occurs. The function of the counter will be dictated solely by the condition meeting the stable setup and hold times.

These counters are fully programmable; that is, the outputs may each be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

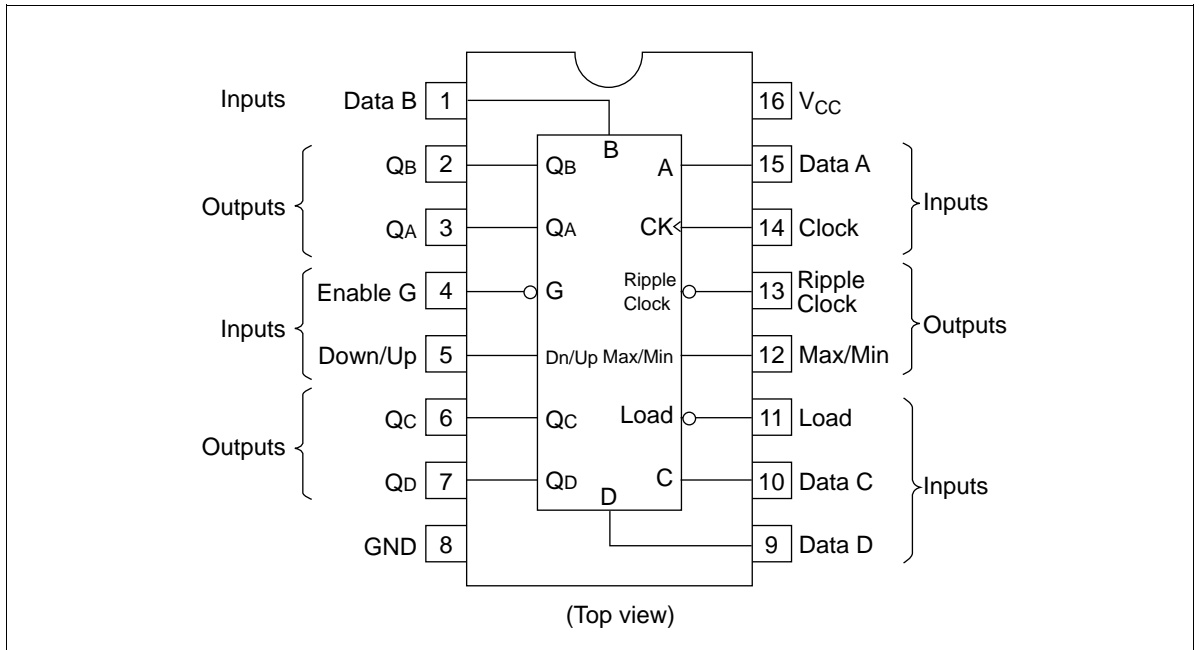
Two outputs have been made available to perform the cascading function. Ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock while the count is zero (all outputs low) counting down or maximum (9 or 15) counting up. The ripple clock output produces a low-level output pulse under those same conditions but only while the clock input is low. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

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Features

- High Speed Operation: t_{pd} (Clock to Q) = 22 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

Pin Arrangement

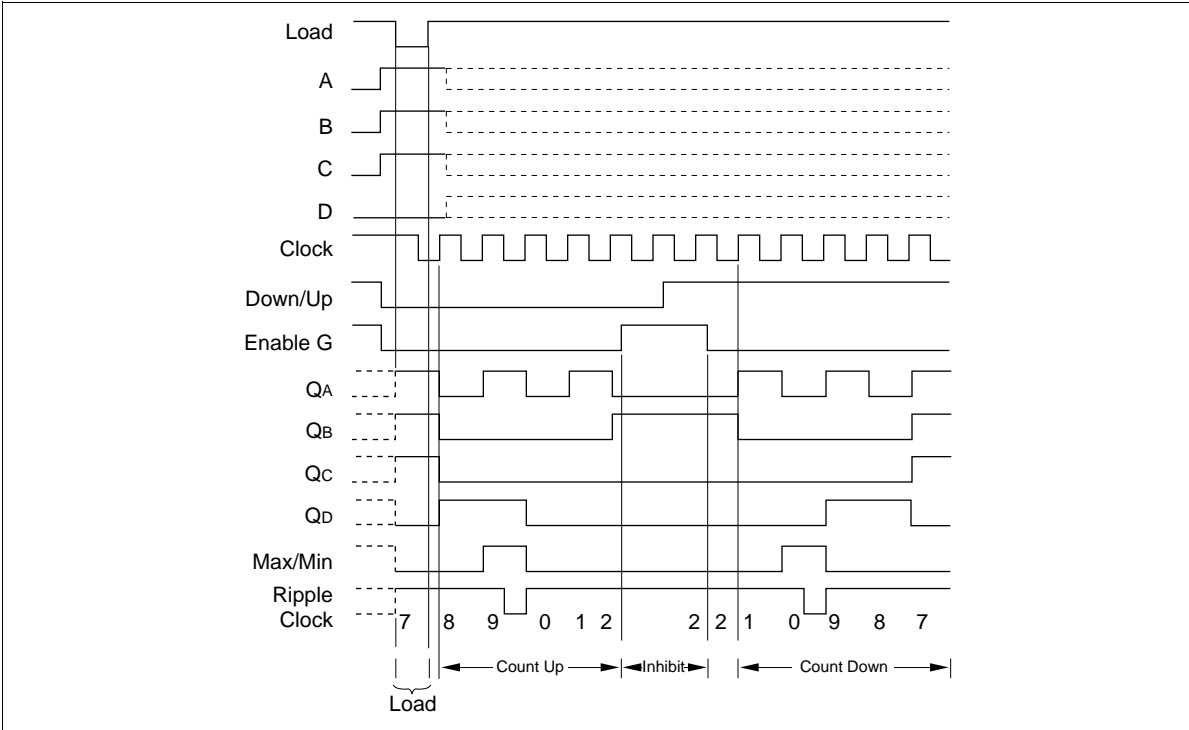


Timing Chart

HD74HC190

Illustrated below is the following sequence:

- 1. Load (preset) to BCD seven.
- 2. Count up to eight, nine (maximum), zero, one and two.
- 3. Inhibit
- 4. Count down to one, zero (minimum), nine, eight and seven.

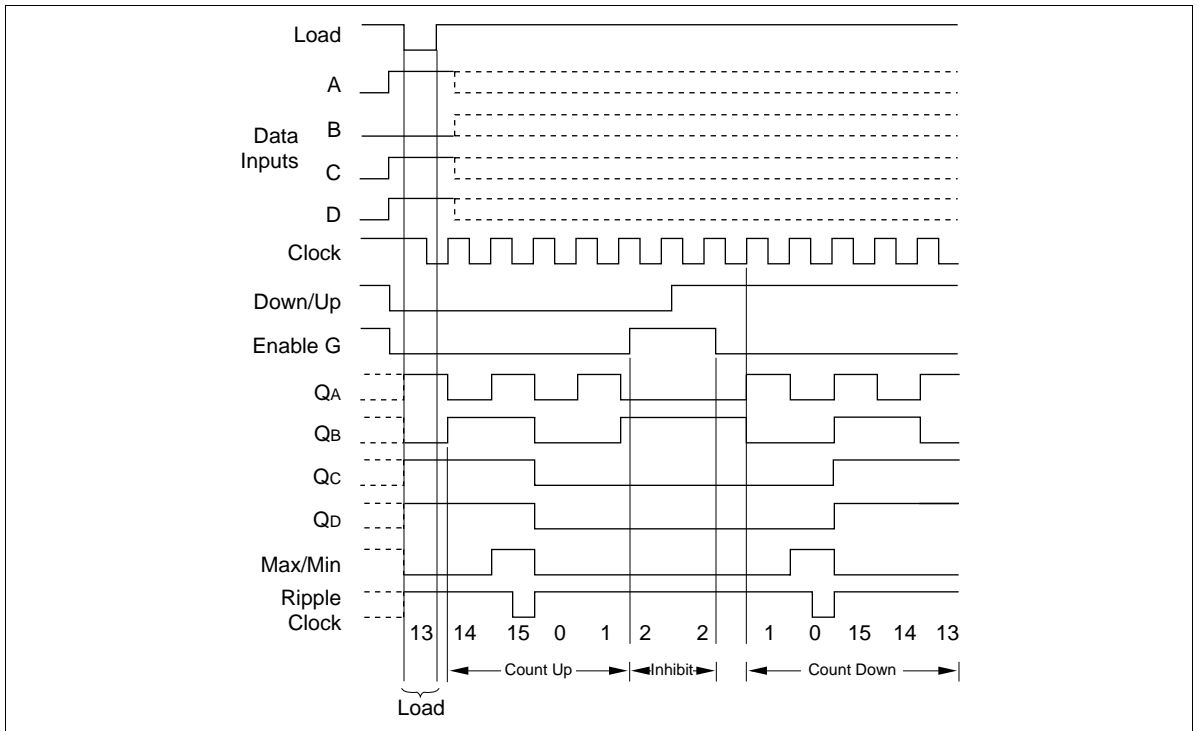


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HD74HC191

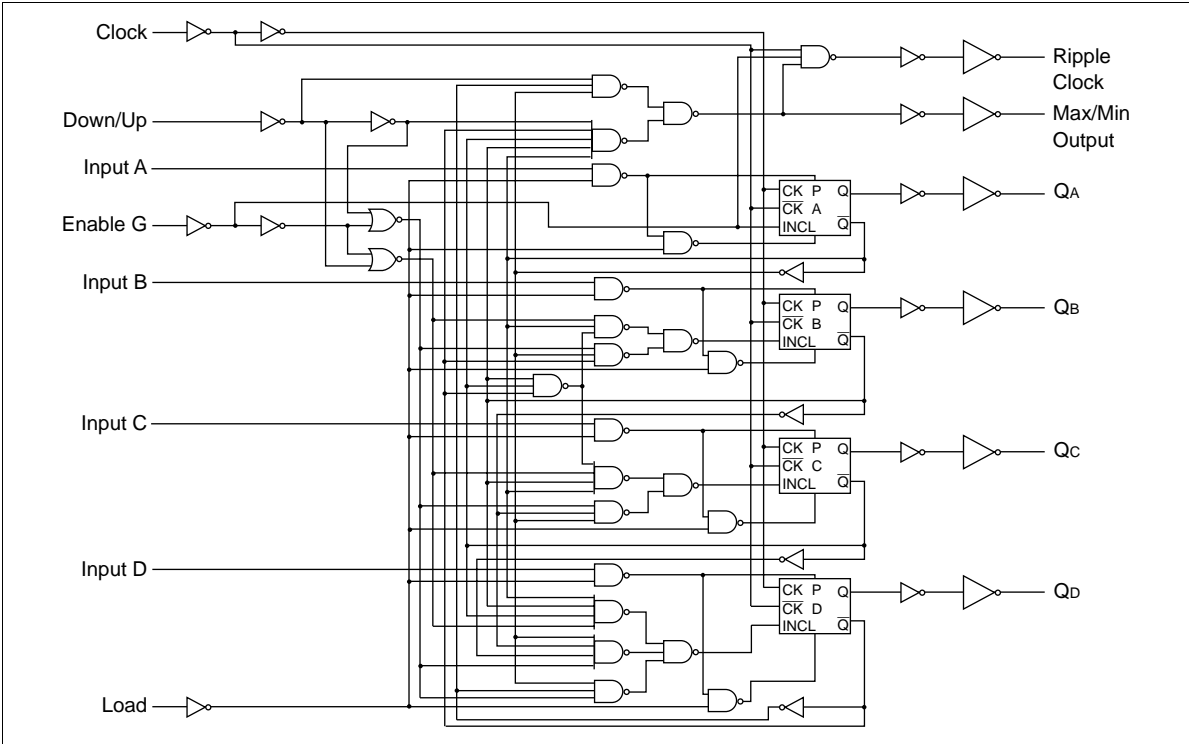
Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one and two.
3. Inhibit
4. Count down to one, zero (minimum), fifteen, fourteen and thirteen.



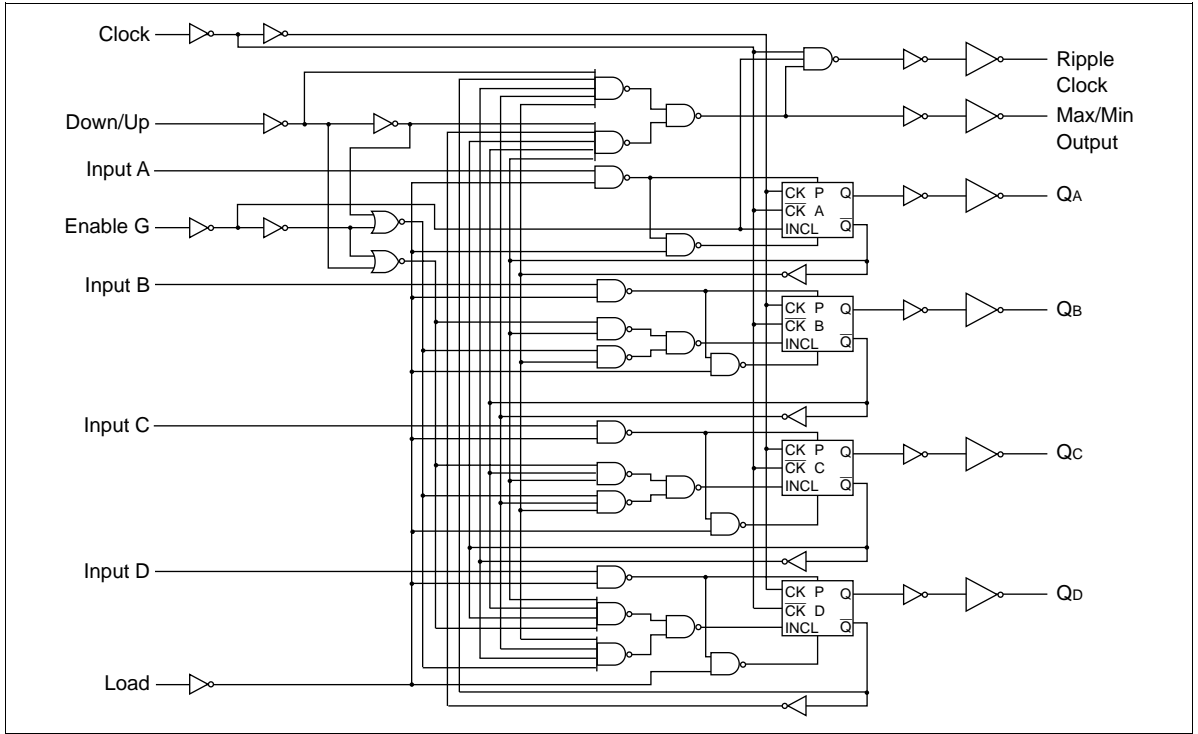
Logic Diagram

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DC Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL} I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
		6.0	—	0.0	0.1	—	0.1			V
	4.5	—	0.0	0.1	—	0.1				
	6.0	—	0.0	0.1	—	0.1				
	4.5	—	—	0.26	—	0.33	I _{OL} = 4 mA			
	6.0	—	—	0.26	—	0.33	I _{OL} = 5.2 mA			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

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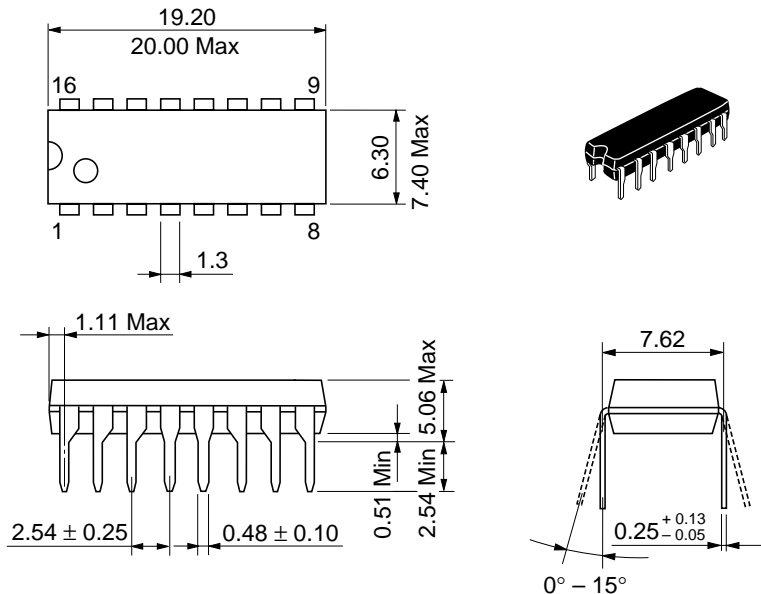
AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40$ to $+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	265	—	335	ns	Load to Q
	t_{PHL}	4.5	—	21	53	—	66		
		6.0	—	—	45	—	56		
		2.0	—	—	230	—	290		Data to Q
		4.5	—	18	46	—	58		
		6.0	—	—	39	—	49		
		2.0	—	—	120	—	150		Clock to RC
		4.5	—	14	24	—	30		
		6.0	—	—	20	—	26		
		2.0	—	—	190	—	240		Clock to Q
		4.5	—	22	38	—	48		
		6.0	—	—	32	—	41		
		2.0	—	—	250	—	315		Clock to max/min
		4.5	—	26	50	—	63		
		6.0	—	—	43	—	54		
		2.0	—	—	230	—	290		Down/up to RC
		4.5	—	20	46	—	58		
		6.0	—	—	39	—	49		
		2.0	—	—	130	—	165		G to RC
		4.5	—	14	26	—	33		
	6.0	—	—	22	—	28			
	2.0	—	—	190	—	240		Down/up to max/min	
	4.5	—	17	38	—	48			
	6.0	—	—	32	—	41			
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Hold time	t_h	2.0	0	—	—	0	—	ns	
		4.5	0	-6	—	0	—		
		6.0	0	—	—	0	—		

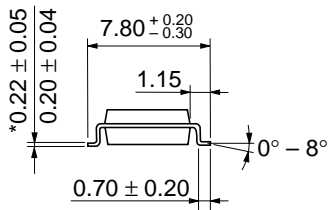
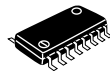
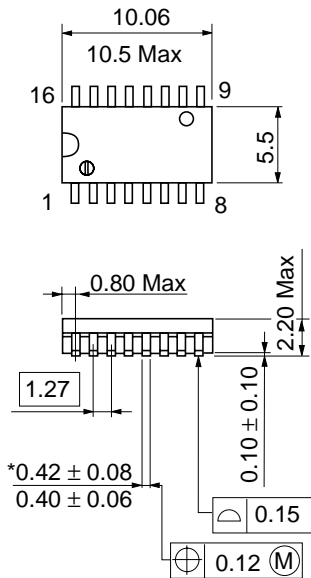
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AC Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$) (cont)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

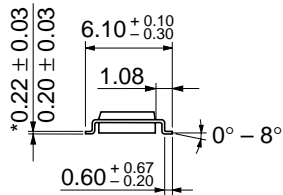
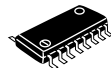
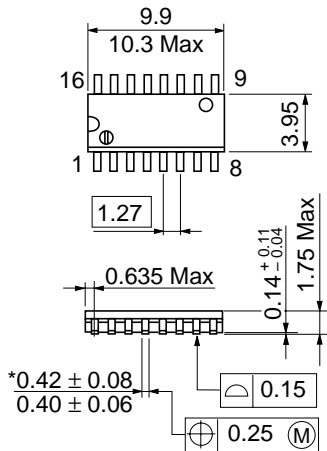


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JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

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JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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