

HD74HC279

Octal D-type Flip-Flops (with Clear)

REJ03D0605-0200
(Previous ADE-205-483)
Rev.2.00
Jan 31, 2006

Description

The latch is ideally suited for use as temporary stage for binary information processing and input/output units. When either $\bar{S}$ or $\bar{R}$ is low, output is dependent on $\bar{R}$ input. When both inputs are high, Output is stored before the indicated steady-state input conditions were established. And when both inputs are low, output is high, but this high level are uncontinuance, if either of input goes high.

Features

- High Speed Operation: $t_{pd}(\bar{S} \text{ to } Q) = 10 \text{ ns typ } (C_L = 50 \text{ pF})$
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2 \text{ to } 6 \text{ V}$
- Low Input Current: $1 \mu\text{A max}$
- Low Quiescent Supply Current: $I_{CC}(\text{static}) = 2 \mu\text{A max } (T_a = 25^\circ\text{C})$
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC279FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC279RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

Function Table

Inputs		Output
$\bar{S}^{*2}$	$\bar{R}$	Q
H	H	Q_0
L	H	H
H	L	L
L	L	H^{*1}

H : High level

L : Low level

Q_0 : The level of Q respectively, before the indicated steady-state input conditions were established.

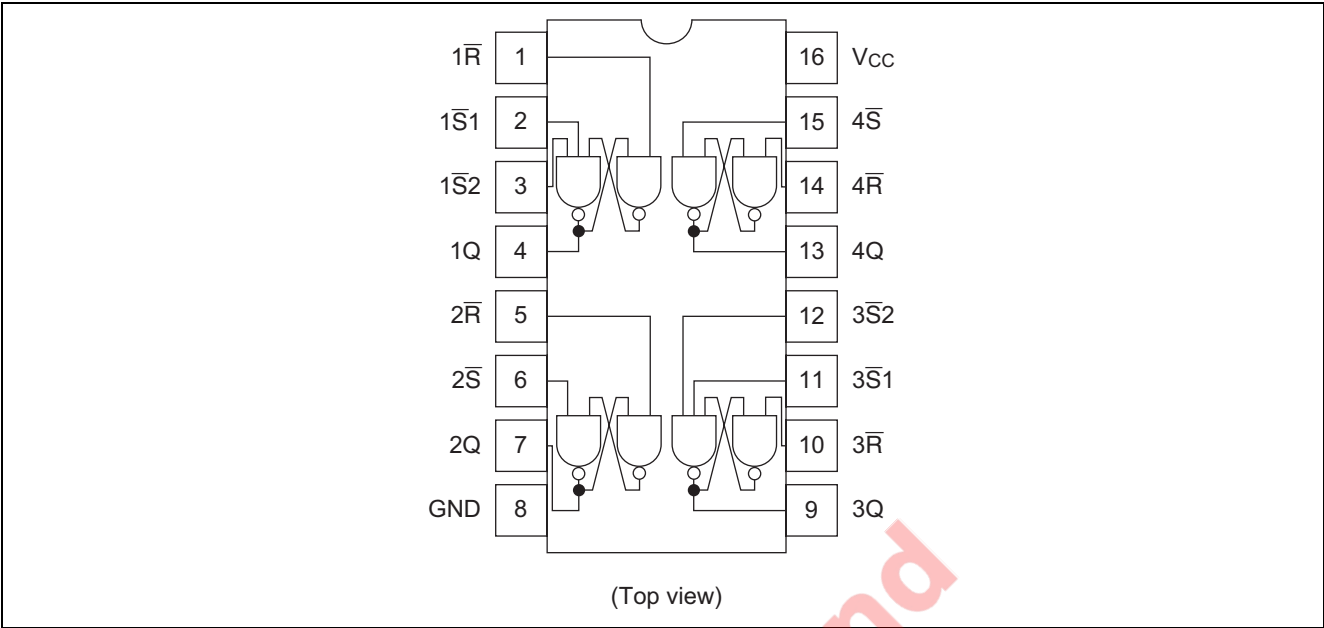
Notes: 1. It is unpredictable, if $\bar{S}$ or $\bar{R}$ goes High.

2. As to latches which has two $\bar{S}$ inputs.

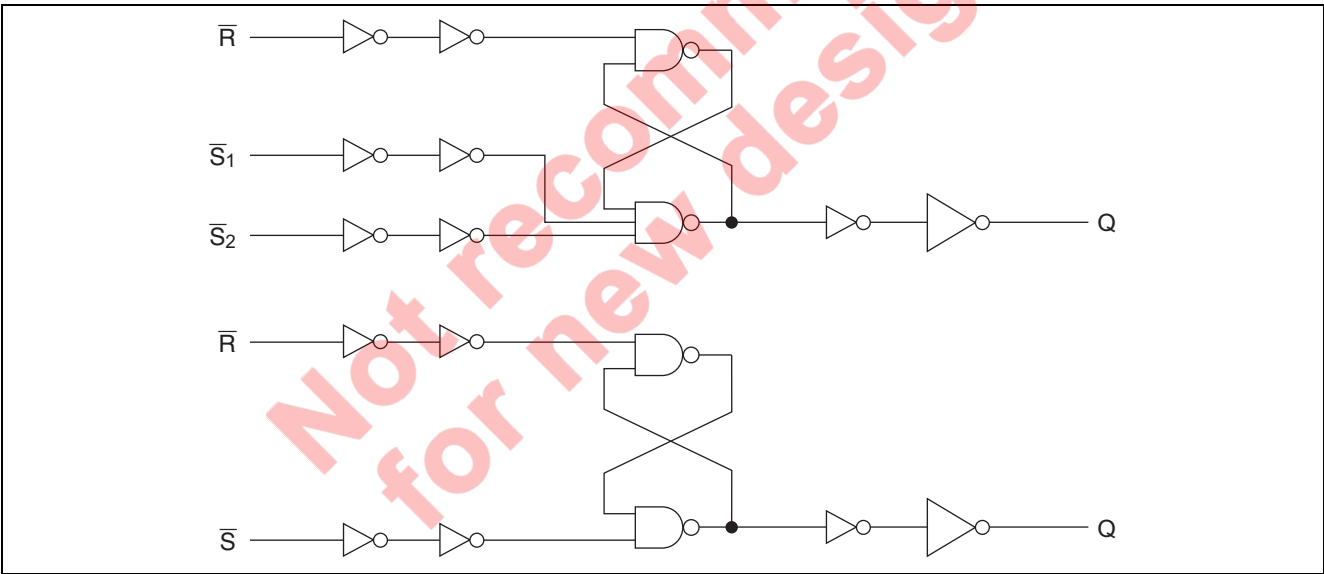
H: Both of $\bar{S}$ inputs are high.

L: Either or both of $\bar{S}$ inputs are low.

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

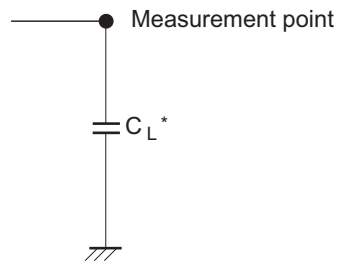
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions		
			Min	Typ	Max	Min	Max				
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V			
		4.5	3.15	—	—	3.15	—				
		6.0	4.2	—	—	4.2	—				
	V _{IL}	2.0	—	—	0.5	—	0.5	V			
		4.5	—	—	1.35	—	1.35				
		6.0	—	—	1.8	—	1.8				
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA	
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -4 mA	
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -5.2 mA	
		4.5	4.18	—	—	4.13	—				
		6.0	5.68	—	—	5.63	—				
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		4.5	—	0.0	0.1	—	0.1				
		6.0	—	0.0	0.1	—	0.1				
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA	
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA	
	Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND	
	Quiescent supply current	I _{CC}	6.0	—	—	2.0	—	20	μA	Vin = V _{CC} or GND, I _{out} = 0 μA	

Switching Characteristics

($C_L = 50\text{ pF}$, Input $t_r = t_f = 6\text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t_{PLH}	2.0	—	—	130	—	165	ns	$\bar{S}$ to Q
		4.5	—	10	26	—	33		
		6.0	—	—	22	—	28		
	t_{PHL}	2.0	—	—	120	—	150	ns	$\bar{R}$ to Q
		4.5	—	12	24	—	30		
		6.0	—	—	20	—	26		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

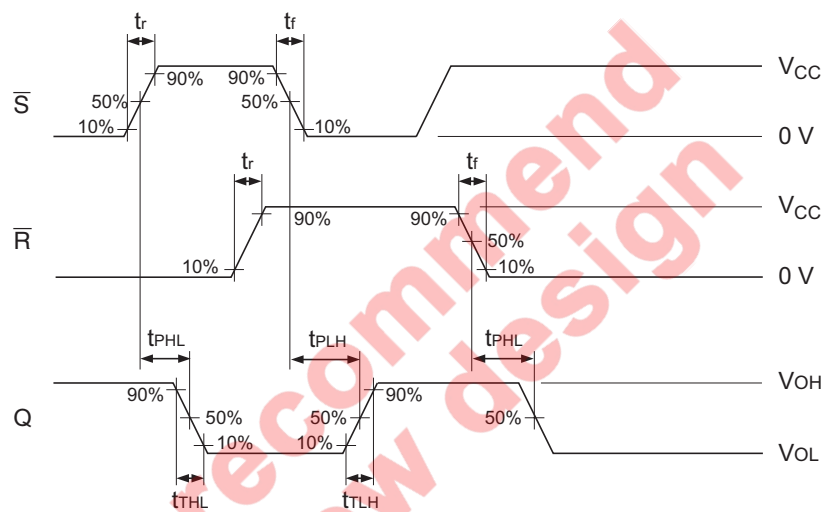
Test Circuit



Note: C_L includes the probe and fig capacitance.

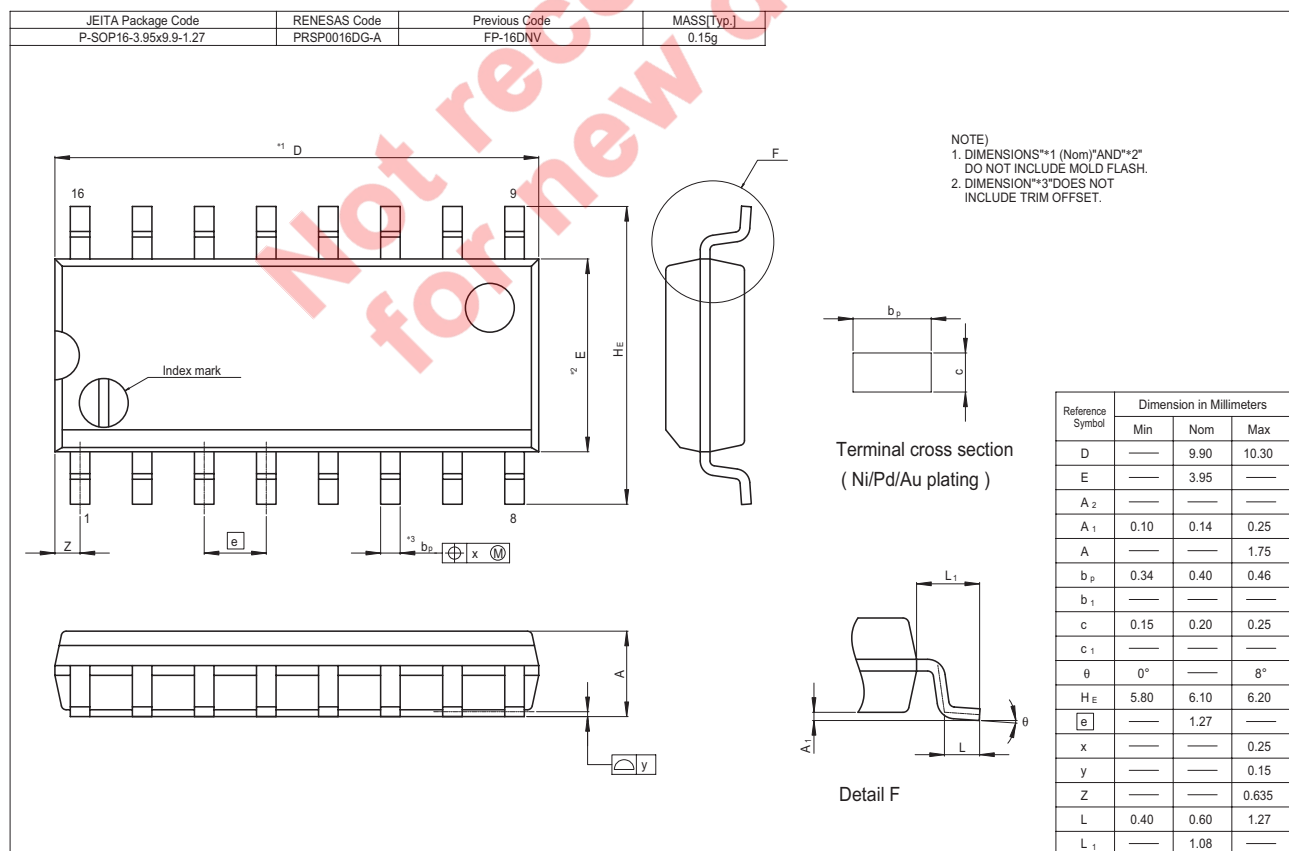
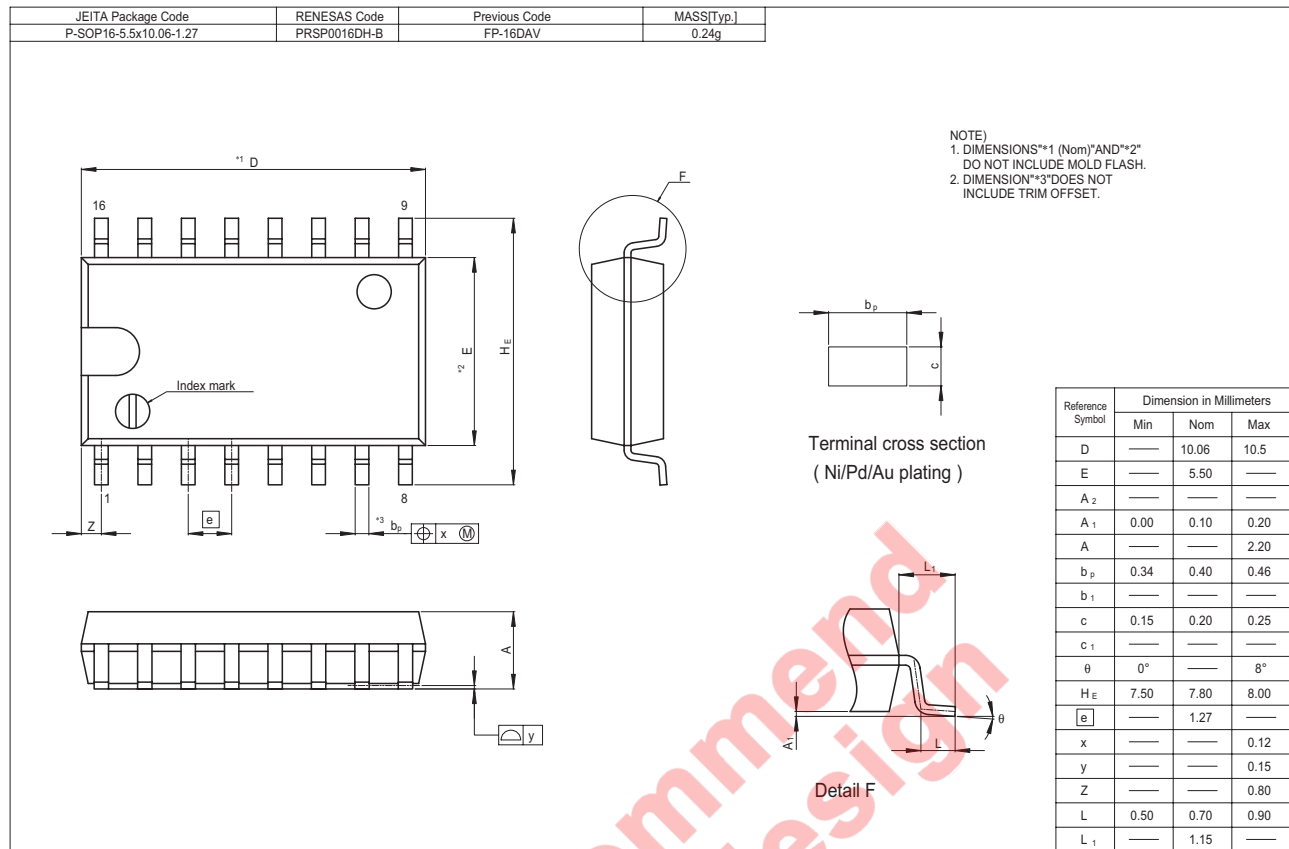
Waveforms

• Waveform



Note : 1. Input pulse : $PRR \leq 1\text{ MHz}$, $Z_o = 50\ \Omega$, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$

Package Dimensions



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