

HD74HC356

8-to-1-line Data Selector/Multiplexer/Register (with 3-state outputs)

REJ03D0614-0200
 (Previous ADE-205-493)
 Rev.2.00
 Jan 31, 2006

Description

This data selectors/multiplexers contain full on-chip binary decoding to select one of eight data sources. The data select address is stored in transparent latches that are enabled by a low level address on pin 11, Select Control. Data on the 8 input lines is stored in a parallel input/output register which in the HD74HC356 is composed of 8 edge-triggered flip-flops, clocked by a low to high transition on pin 9, clock. Both true (Y) and complementary (W) 3-state outputs are available.

Features

- High Speed Operation: t_{pd} (Clock to W, Y) = 27 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC356FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HC356RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

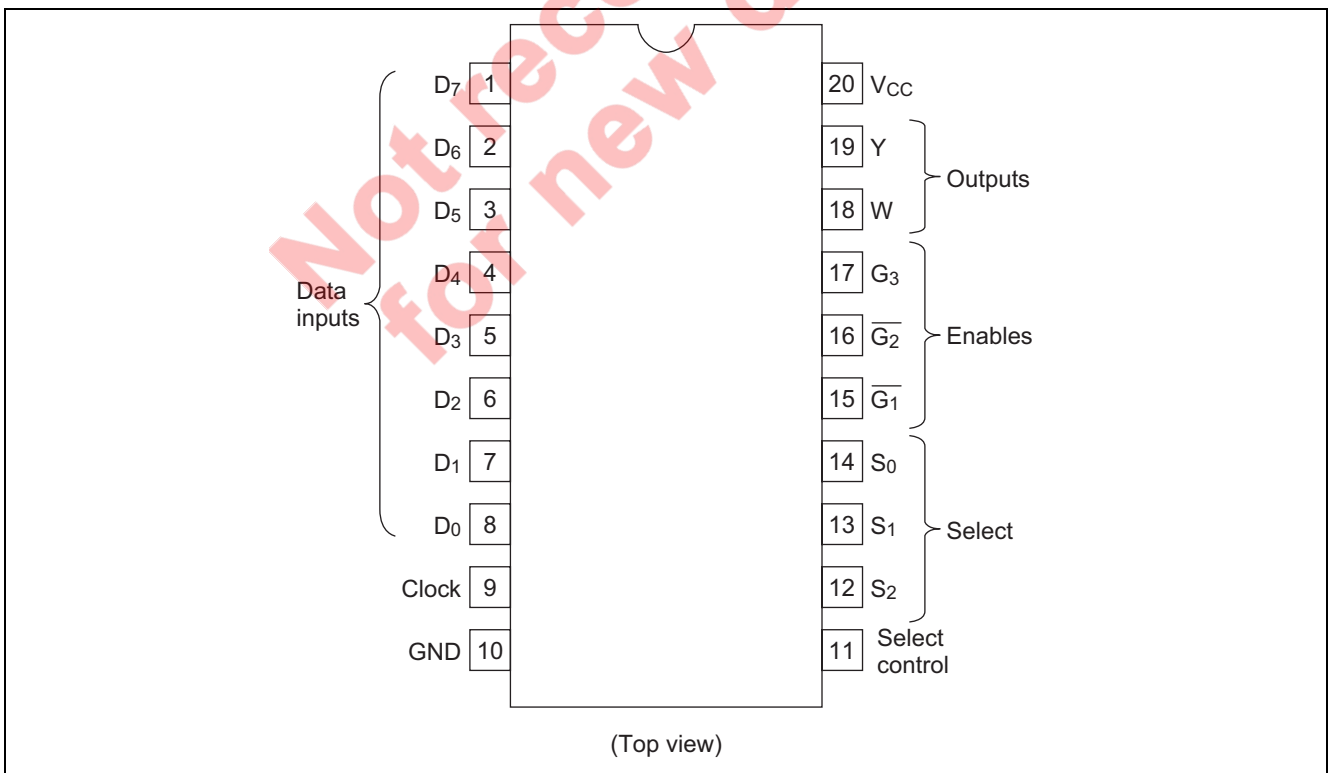
Note: Please consult the sales office for the above package availability.

Function Table

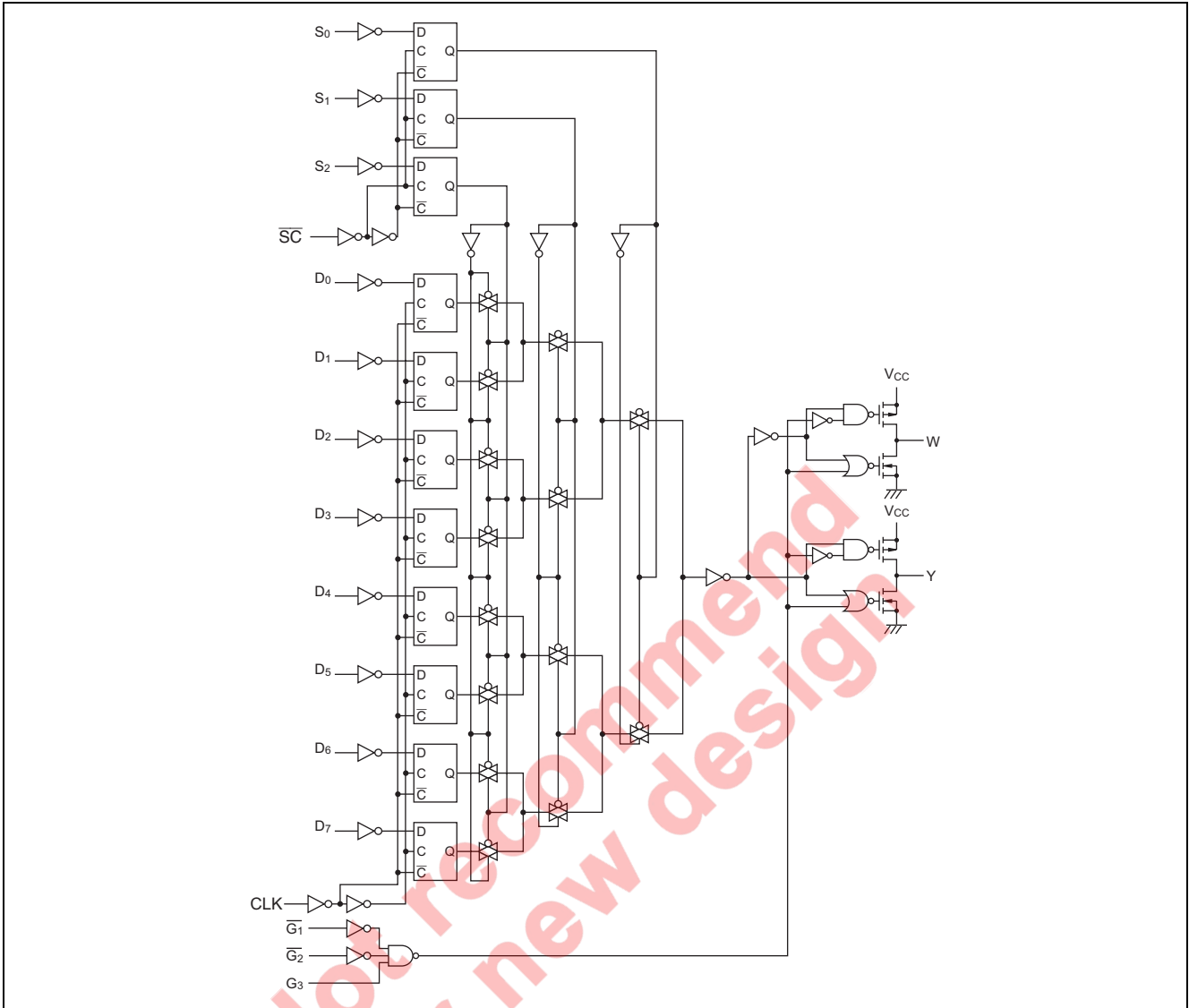
Select			Inputs				Outputs	
S ₁	S ₂	S ₀	Clock	\overline{G}_1	\overline{G}_2	G ₃	W	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	\int	L	L	H	\overline{D}_0	D ₀
L	L	L	H or L	L	L	H	\overline{D}_{0n}	D _{0n}
L	L	H	\int	L	L	H	\overline{D}_1	D ₁
L	L	H	H or L	L	L	H	\overline{D}_{1n}	D _{1n}
L	H	L	\int	L	L	H	\overline{D}_2	D ₂
L	H	L	H or L	L	L	H	\overline{D}_{2n}	D _{2n}
L	H	H	\int	L	L	H	\overline{D}_3	D ₃
L	H	H	H or L	L	L	H	\overline{D}_{3n}	D _{3n}
H	L	L	\int	L	L	H	\overline{D}_4	D ₄
H	L	L	H or L	L	L	H	\overline{D}_{4n}	D _{4n}
H	L	H	\int	L	L	H	\overline{D}_5	D ₅
H	L	H	H or L	L	L	H	\overline{D}_{5n}	D _{5n}
H	H	L	\int	L	L	H	\overline{D}_6	D ₆
H	H	L	H or L	L	L	H	\overline{D}_{6n}	D _{6n}
H	H	H	\int	L	L	H	\overline{D}_7	D ₇
H	H	H	H or L	L	L	H	\overline{D}_{7n}	D _{7n}

Notes: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

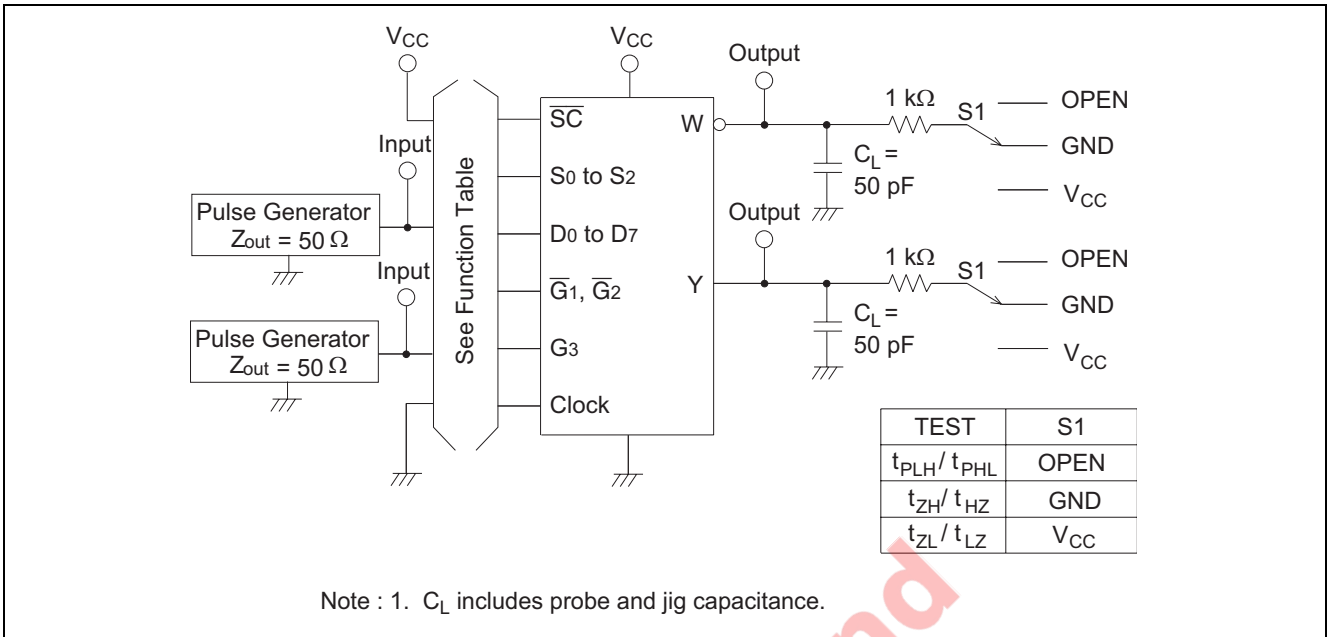
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\ \mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -6\ \text{mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -7.8\ \text{mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\ \mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OH} = 6\ \text{mA}$
		6.0	—	—	0.26	—	0.33			$I_{OH} = 7.8\ \text{mA}$
Off-state output current	I_{OZ}	6.0	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH}\text{ or }V_{IL}$, $V_{out} = V_{CC}\text{ or GND}$	
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}\text{ or GND}$	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}\text{ or GND}$, $I_{out} = 0\ \mu\text{A}$	

Switching Characteristics

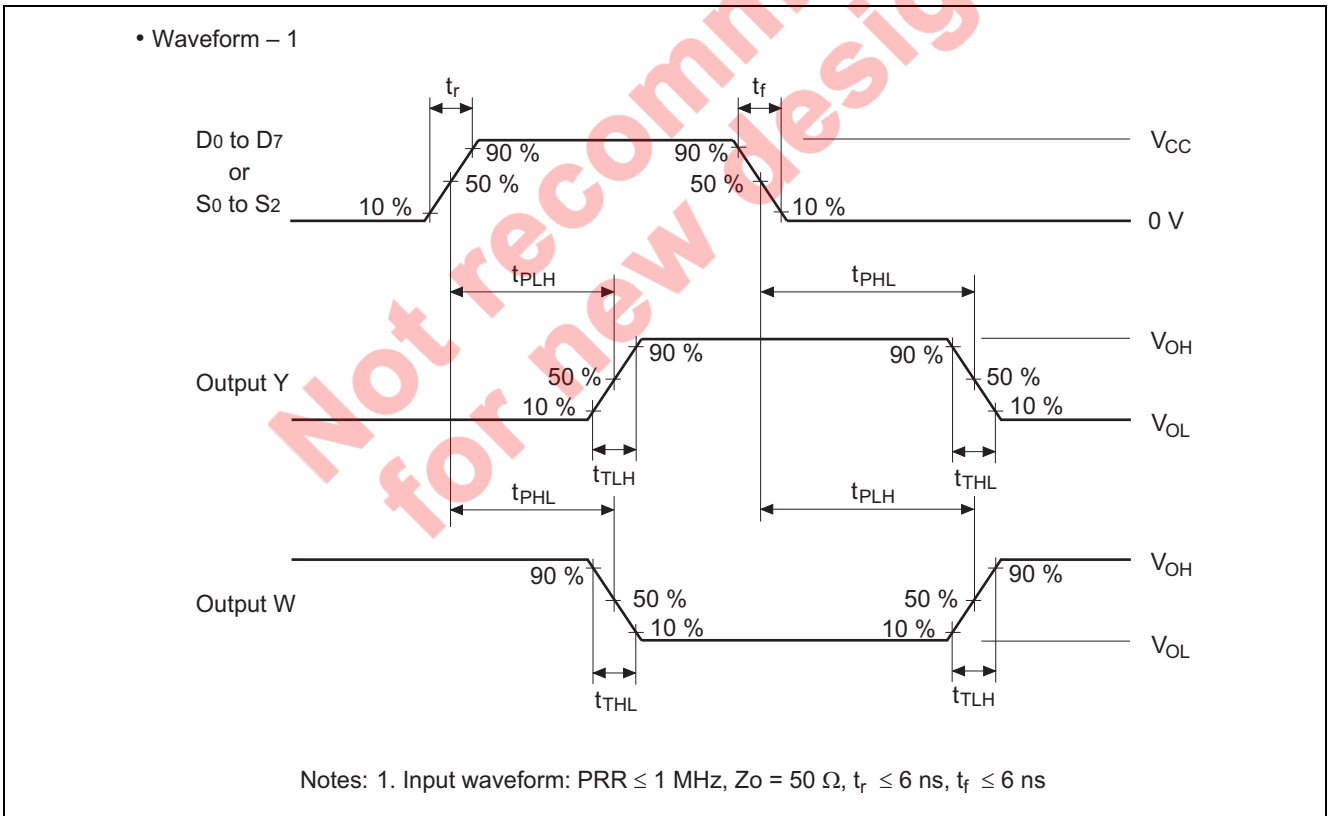
(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Propagation delay time	t _{PLH} t _{PHL}	2.0	—	—	255	—	320	ns	Clock to output
		4.5	—	27	51	—	64		
		6.0	—	—	43	—	54		
	t _{PLH} t _{PHL}	2.0	—	—	285	—	355	ns	S ₀ – S ₂ to output
		4.5	—	25	57	—	71		
		6.0	—	—	48	—	60		
	t _{PLH} t _{PHL}	2.0	—	—	300	—	375	ns	Select control to output
		4.5	—	25	60	—	75		
		6.0	—	—	51	—	64		
Output enable time	t _{ZH} t _{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t _{LZ} t _{HZ}	2.0	—	—	165	—	205	ns	
		4.5	—	17	33	—	41		
		6.0	—	—	28	—	35		
Setup time	t _{su}	2.0	50	—	—	65	—	ns	D ₀ to D ₇ to Clock S ₀ to S ₇ to Select control
		4.5	10	2	—	13	—		
		6.0	10	—	—	13	—		
Hold time	t _h	2.0	5	—	—	5	—	ns	D ₀ to D ₇ to Clock S ₀ to S ₇ to Select control
		4.5	5	1	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t _w	2.0	80	—	—	100	—	ns	
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t _{TLH} t _{THL}	2.0	—	—	60	—	75	ns	
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

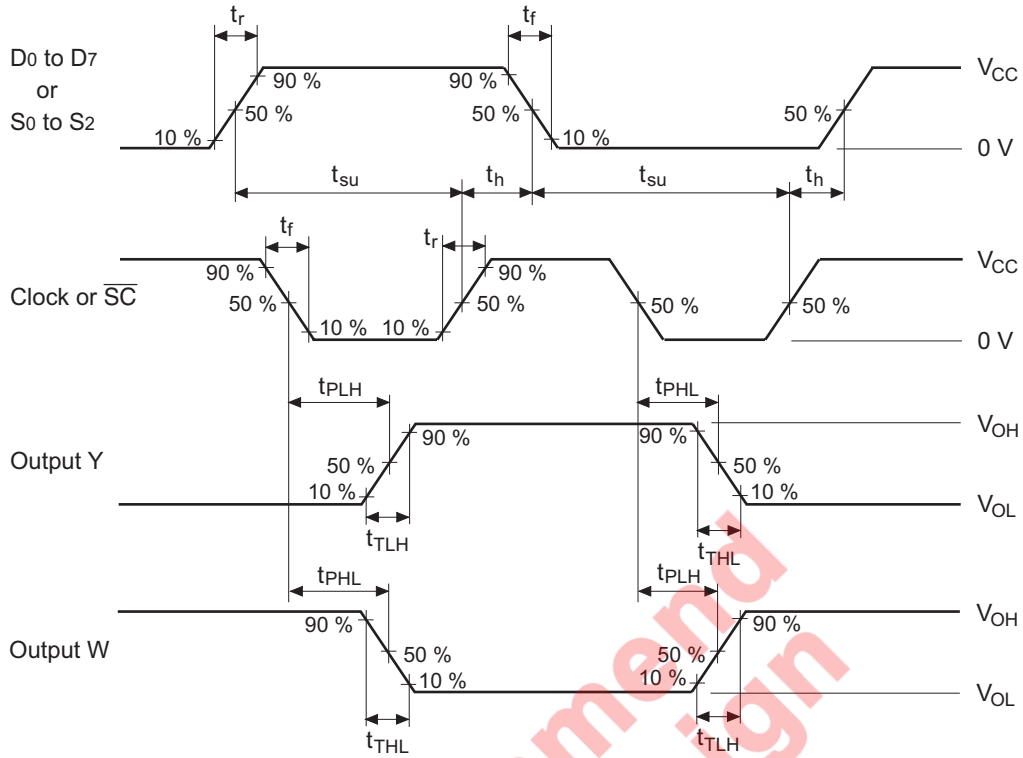
Test Circuit



Waveforms

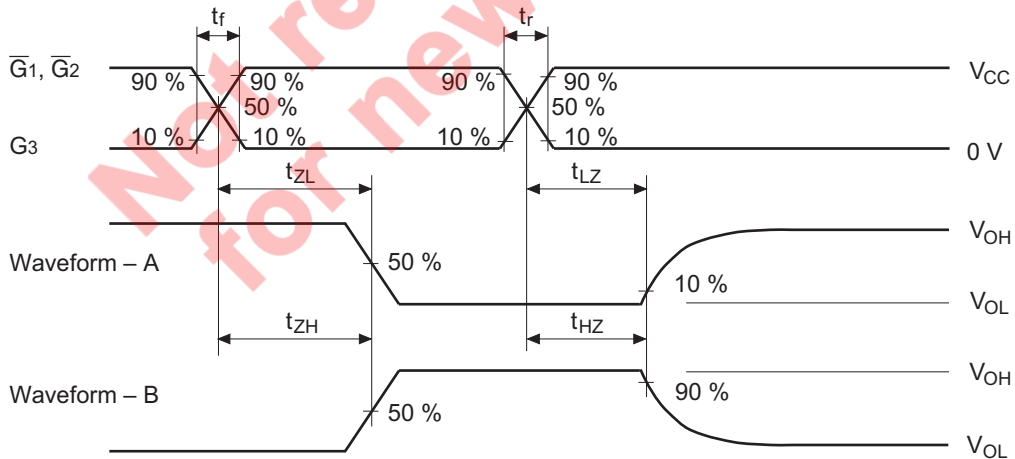


• Waveform – 2



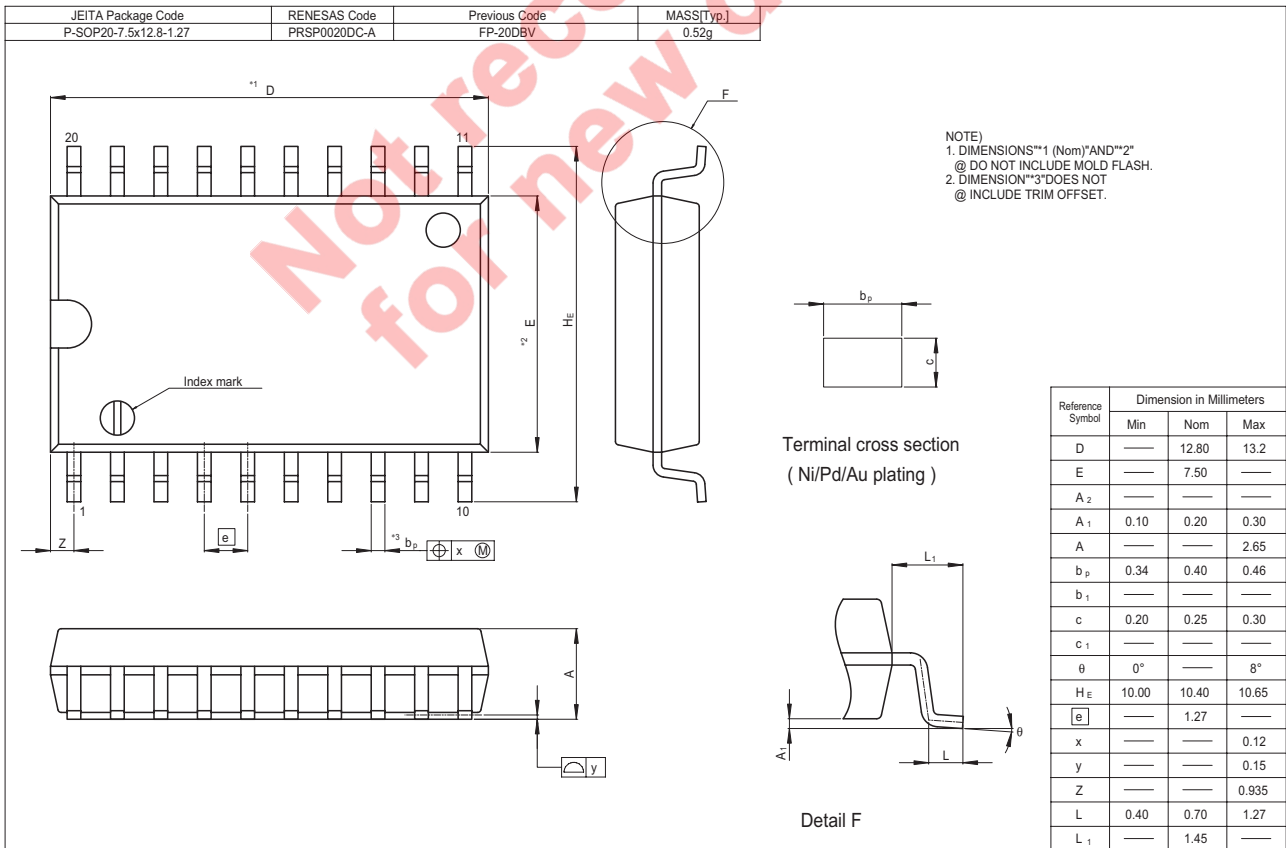
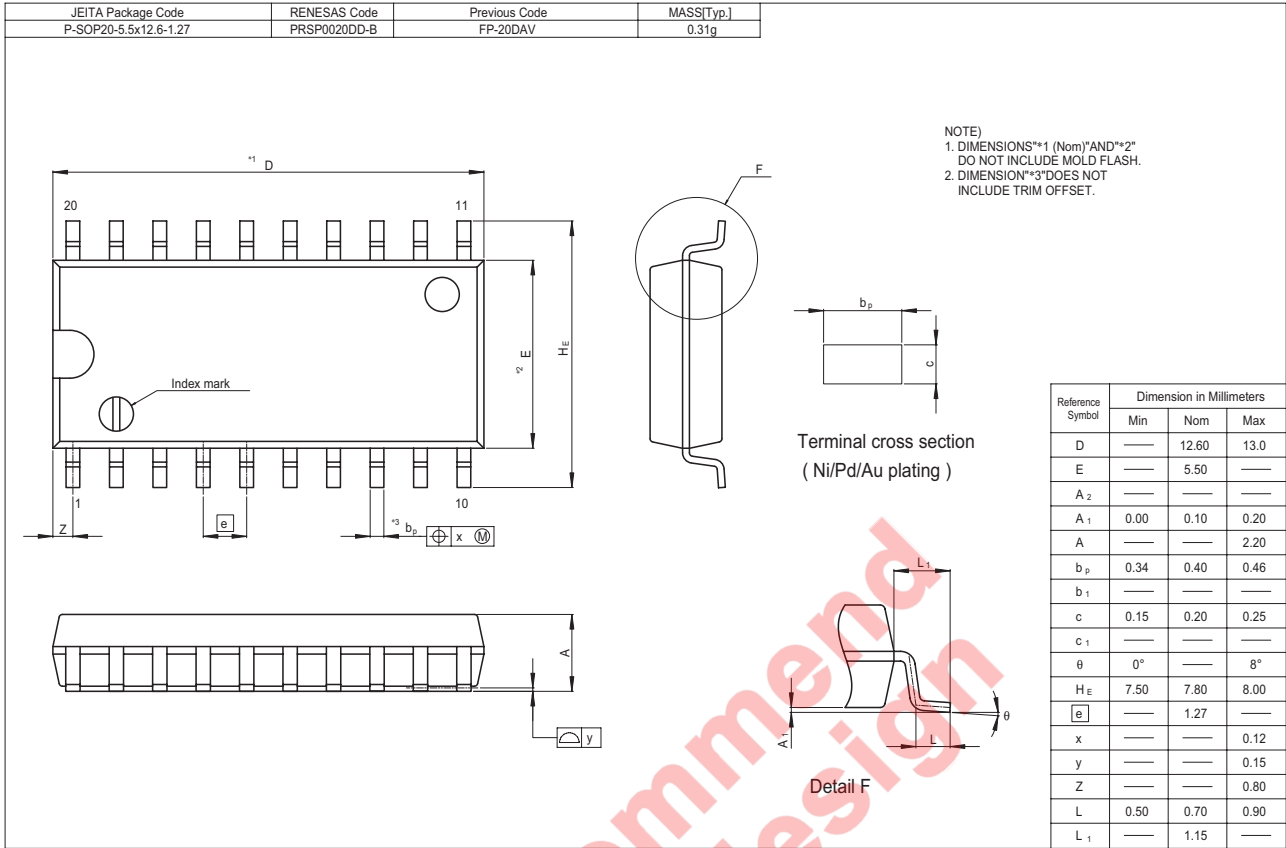
Notes: 1. Input waveform: PRR \leq 1 MHz, $Z_o = 50 \Omega$, $t_r \leq 6$ ns, $t_f \leq 6$ ns

• Waveform – 3



- Notes :
1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. Waveform– A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform– B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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