

HD74HC373, HD74HC533

Octal D-type Transparent Latches (with 3-state outputs)

Octal D-type Transparent Latches (with inverted 3-state outputs)

REJ03D0619-0200
(Previous ADE-205-498)
Rev.2.00
Mar 30, 2006

Description

When the latch enable input is high, the Q outputs of HD74HC373 will follow the D inputs and the Q outputs of HD74HC533 will follow the inversion of the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- High Speed Operation: t_{pd} (D to Q) = 16 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max (T_a = 25°C)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC373P HD74HC533P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74HC373FPEL HD74HC533FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74HC533RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)
HD74HC373TELL	TSSOP-20 pin	PTSP0020JB-A (TTP-20DAV)	T	ELL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

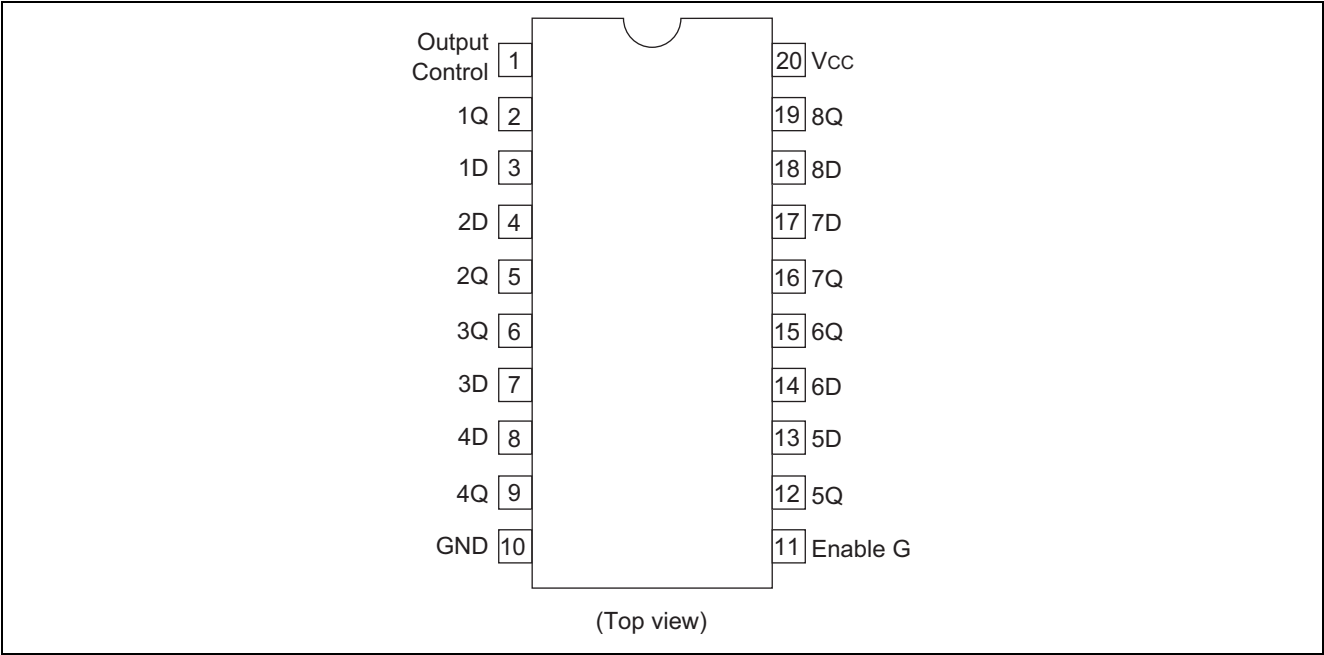
Function Table

Output Control	Enable G	D	HD74HC373 Q	HD74HC533 $\bar{Q}$
L	H	H	H	L
L	H	L	L	H
L	L	X	No change	No change
H	X	X	Z	Z

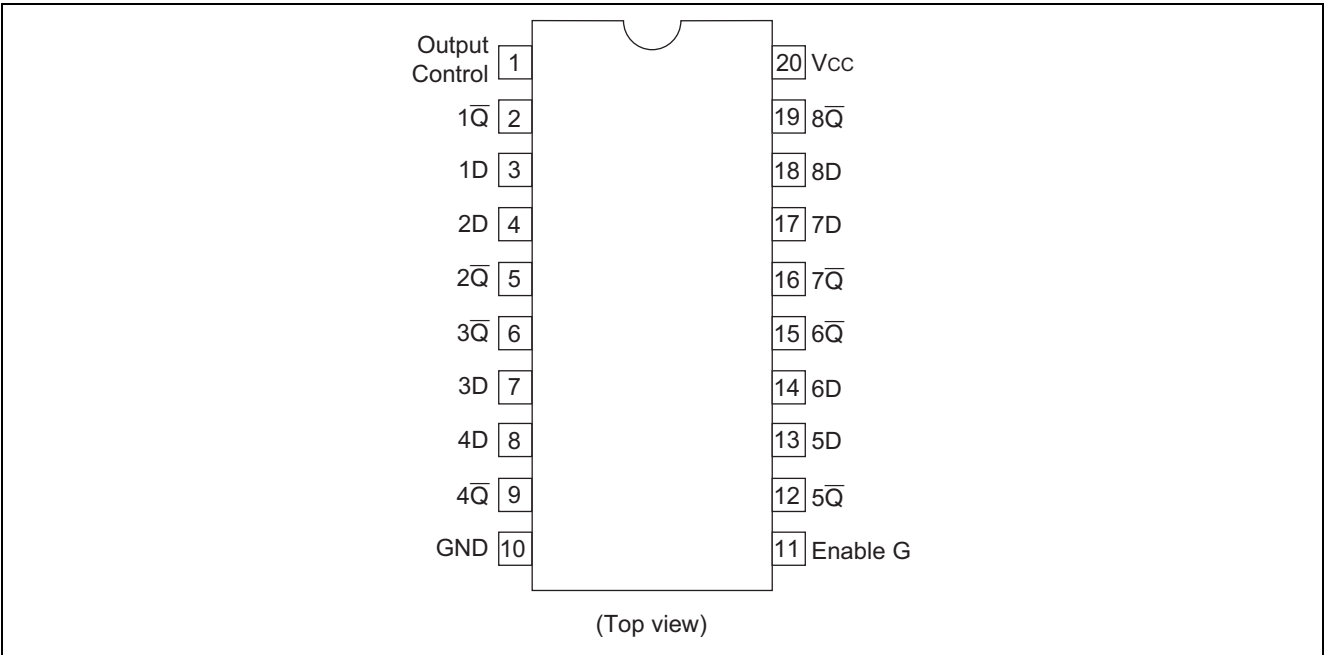
Note: 1. H; High level, L; Low level, X; Irrelevant, Z; High impedance

Pin Arrangement

HD74HC373

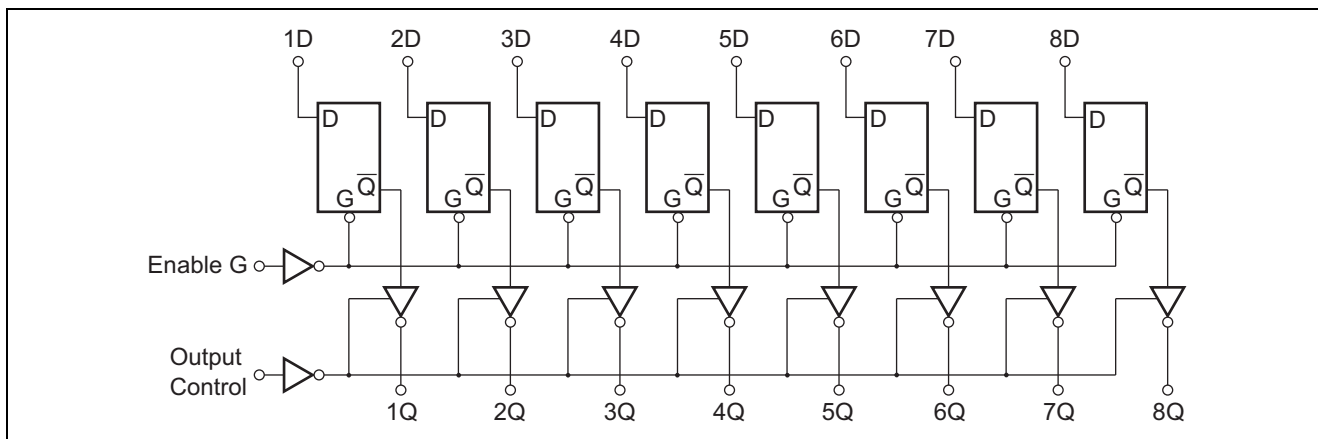


HD74HC533

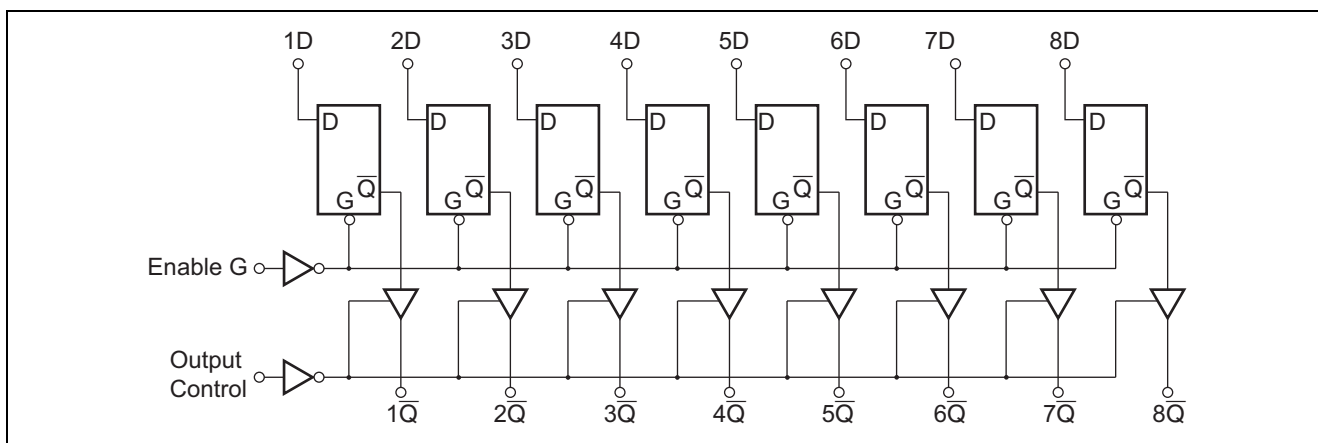


Logic Diagram

HD74HC373



HD74HC533



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

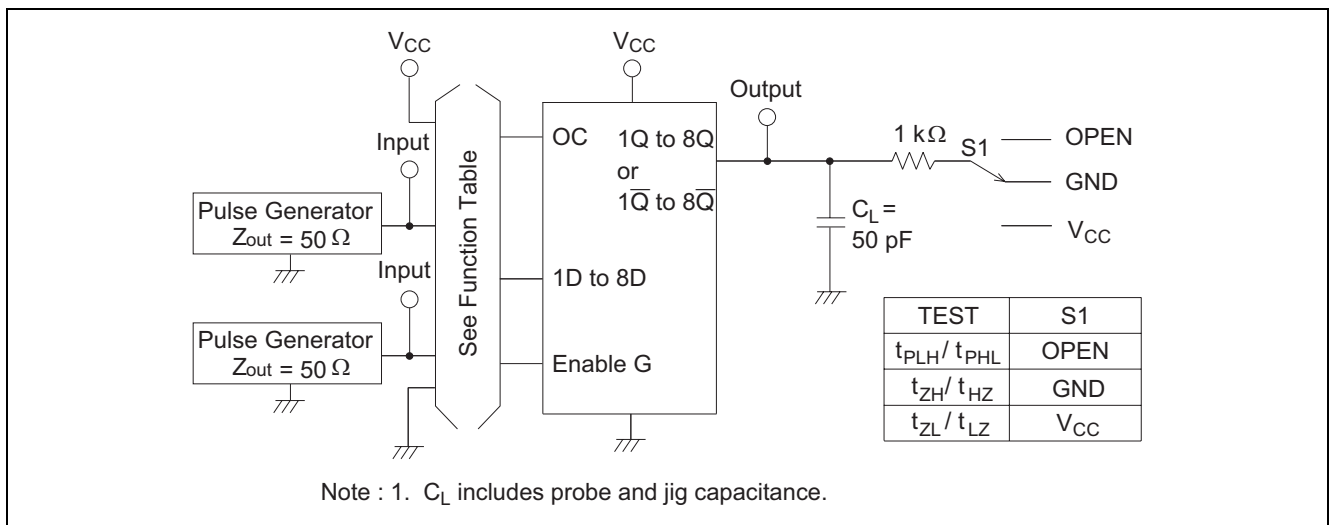
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -6\text{ mA}$
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -7.8\text{ mA}$
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OH} = 6\text{ mA}$
		6.0	—	—	0.26	—	0.33			$I_{OH} = 7.8\text{ mA}$
Off-state output current	I_{OZ}	6.0	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH}\text{ or }V_{IL}$, $V_{out} = V_{CC}\text{ or GND}$	
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}\text{ or GND}$	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}\text{ or GND}$, $I_{out} = 0\text{ }\mu\text{A}$	

Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

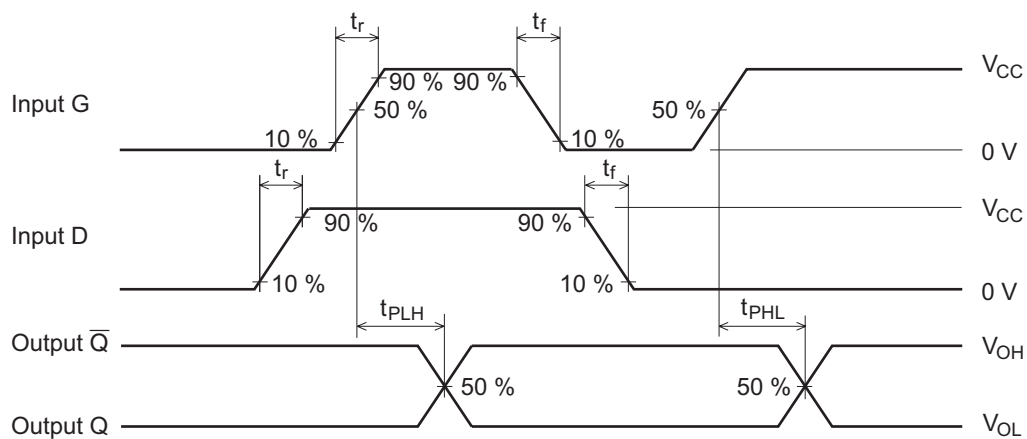
Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ			Max		
Propagation delay time	t_{PLH}	2.0	—	—	150	—	190	ns	G to Q
		4.5	—	18	30	—	38		
		6.0	—	—	26	—	33		
	t_{PHL}	2.0	—	—	125	—	155	ns	D to Q
		4.5	—	16	25	—	31		
		6.0	—	—	21	—	26		
Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	12	30	—	38		
		6.0	—	—	26	—	33		
	t_{ZH}	2.0	—	—	150	—	190	ns	
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	
		4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
	t_{HZ}	2.0	—	—	150	—	190	ns	
		4.5	—	16	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{SU}	2.0	100	—	—	125	—	ns	
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_H	2.0	50	—	—	65	—	ns	
		4.5	10	1	—	13	—		
		6.0	9	—	—	11	—		
Pulse width	t_W	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

Test Circuit

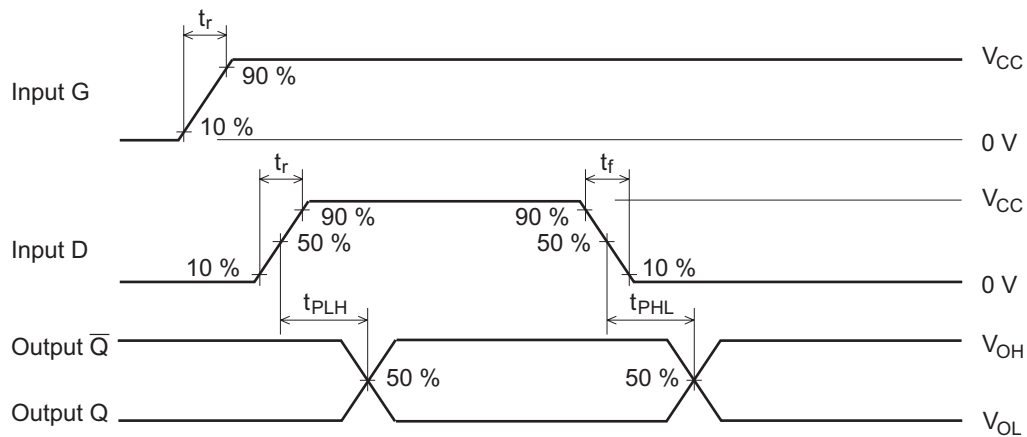


Waveforms

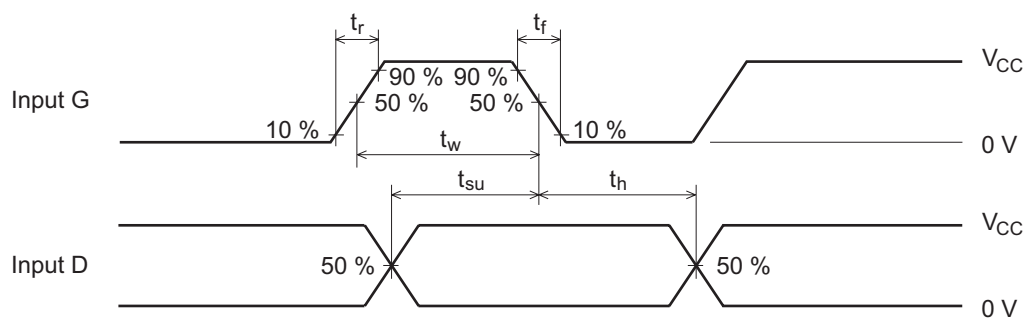
• Waveform – 1



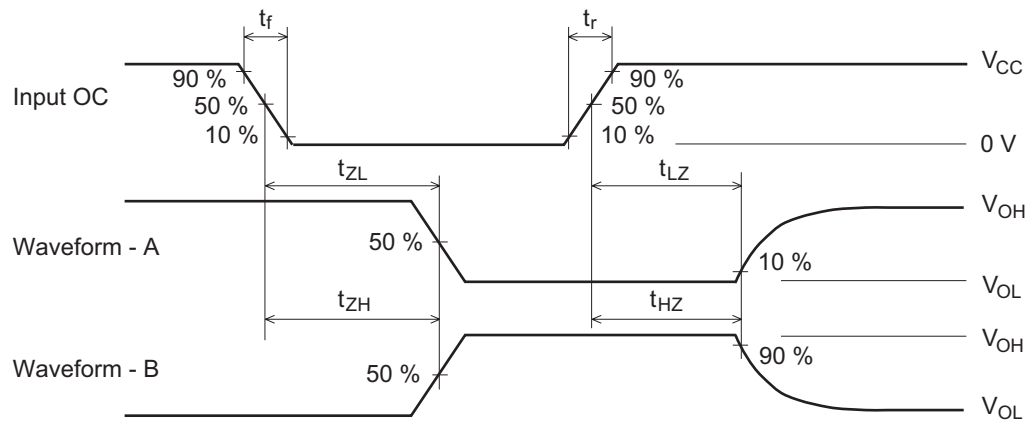
• Waveform – 2



• Waveform – 3

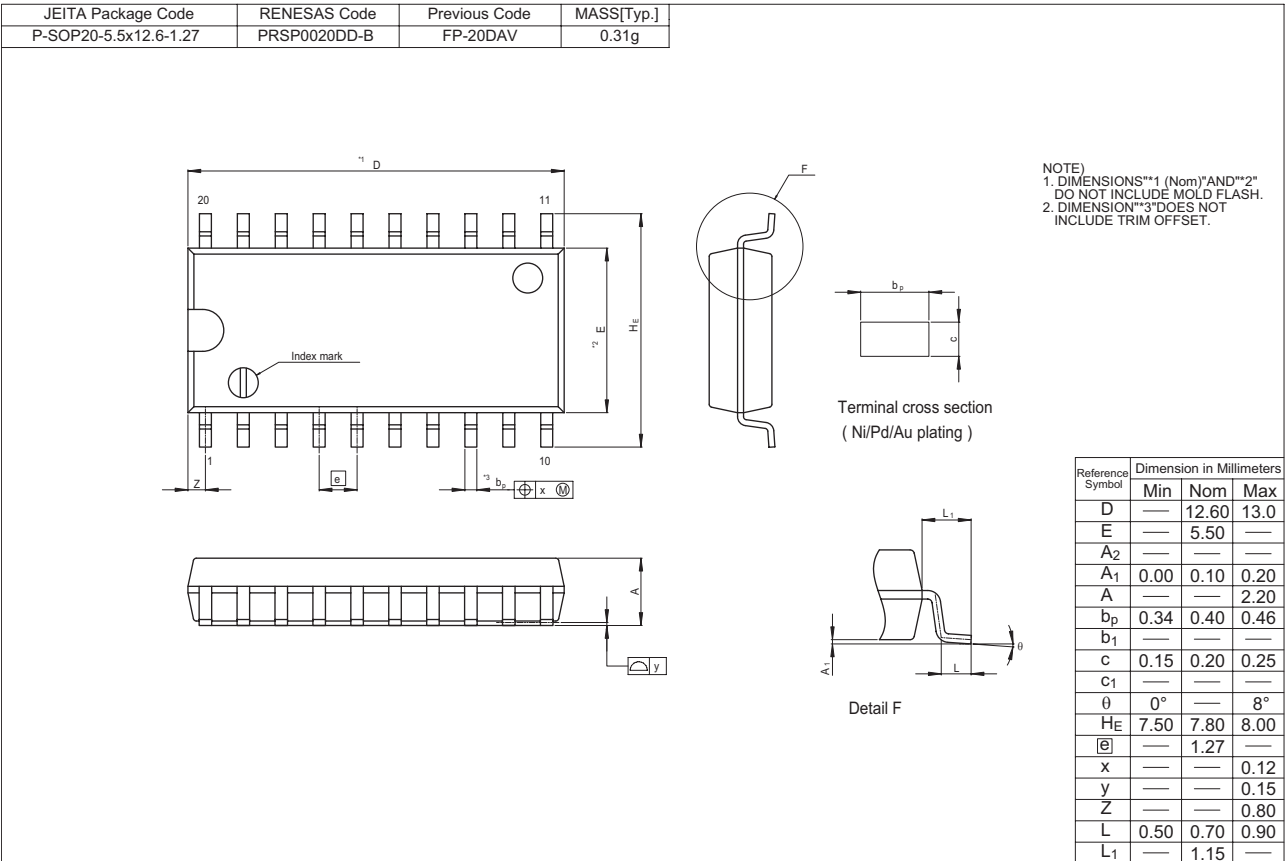
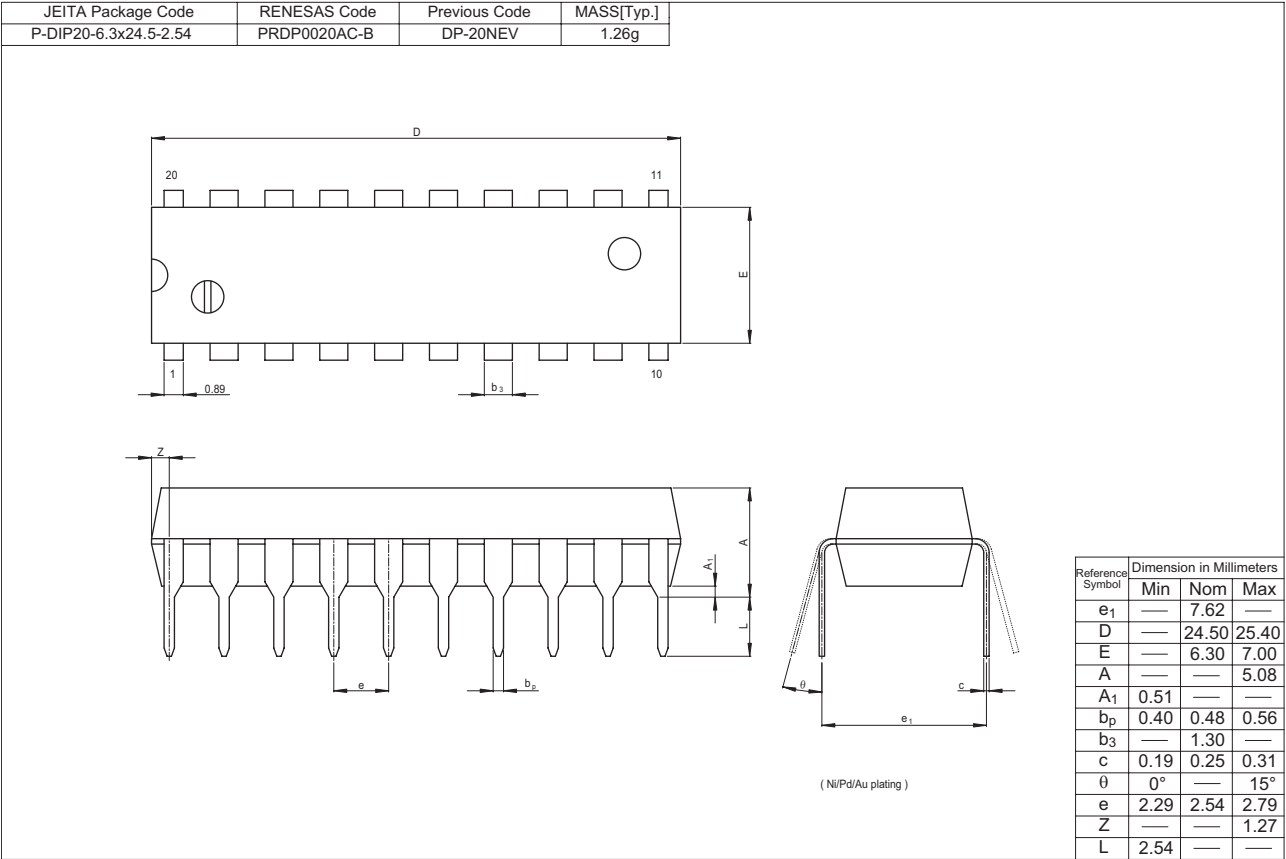


• Waveform – 4



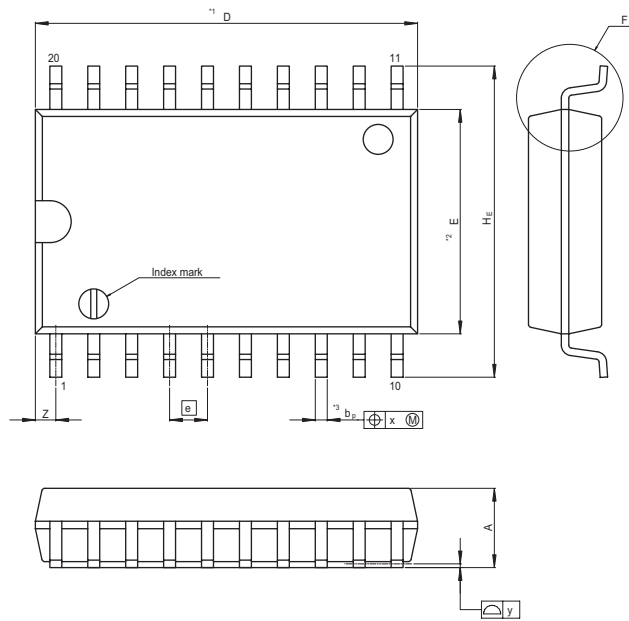
- Notes :
1. Input waveform : $PRR \leq 1\text{ MHz}$, duty cycle 50%, $t_r \leq 6\text{ ns}$, $t_f \leq 6\text{ ns}$
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

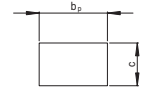


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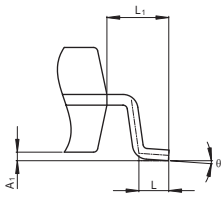
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-7.5x12.8-1.27	PRSP0020DC-A	FP-20DBV	0.52g



NOTE)
1. DIMENSIONS**1 (Nom)**AND**2*
@ DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3*DOES NOT
@ INCLUDE TRIM OFFSET.



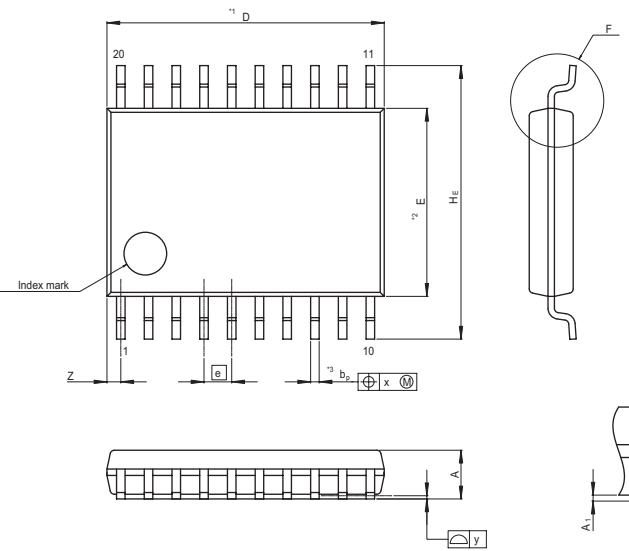
Terminal cross section
(Ni/Pd/Au plating)



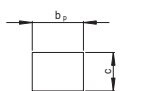
Detail F

Reference Symbol	Min	Nom	Max
D	—	12.80	13.2
E	—	7.50	—
A ₂	—	—	—
A ₁	0.10	0.20	0.30
A	—	—	2.65
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.20	0.25	0.30
c ₁	—	—	—
θ	0°	—	8°
H _E	10.00	10.40	10.65
@	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.935
L	0.40	0.70	1.27
L ₁	—	1.45	—

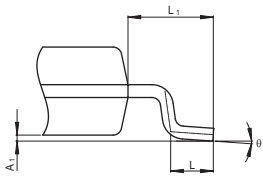
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP20-4.4x6.5-0.65	PTSP0020JB-A	TTP-20DAV	0.07g



NOTE)
1. DIMENSIONS**1 (Nom)**AND**2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3*DOES NOT
INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Min	Nom	Max
D	—	6.50	6.80
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
H _E	6.20	6.40	6.60
@	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.65
L	0.4	0.5	0.6
L ₁	—	1.0	—

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