

# HD74HC589

## 8-bit Serial or Parallel-input/Serial-output Shift Register (with 3-state outputs)

REJ03D0631-0200  
(Previous ADE-205-511)  
Rev.2.00  
Mar 30, 2006

### Description

The HD74HC589 is similar in function to the HD74HC597, which is not a 3-state device.

This device consists of an 8-bit storage latch which feeds parallel data to an 8-bit shift register. Data can also be loaded serially (see Function Table). The shift register output,  $Q_H$ , is a three-state output, allowing this device to be used in bus-oriented systems.






### Features

- High Speed Operation:  $t_{pd}$  (Shift Clock to  $Q_H$ ) = 15 ns typ ( $C_L = 50$  pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage:  $V_{CC} = 2$  to 6 V
- Low Input Current: 1  $\mu$ A max
- Low Quiescent Supply Current:  $I_{CC}$  (static) = 4  $\mu$ A max ( $T_a = 25^\circ\text{C}$ )
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC589FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74HC589RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

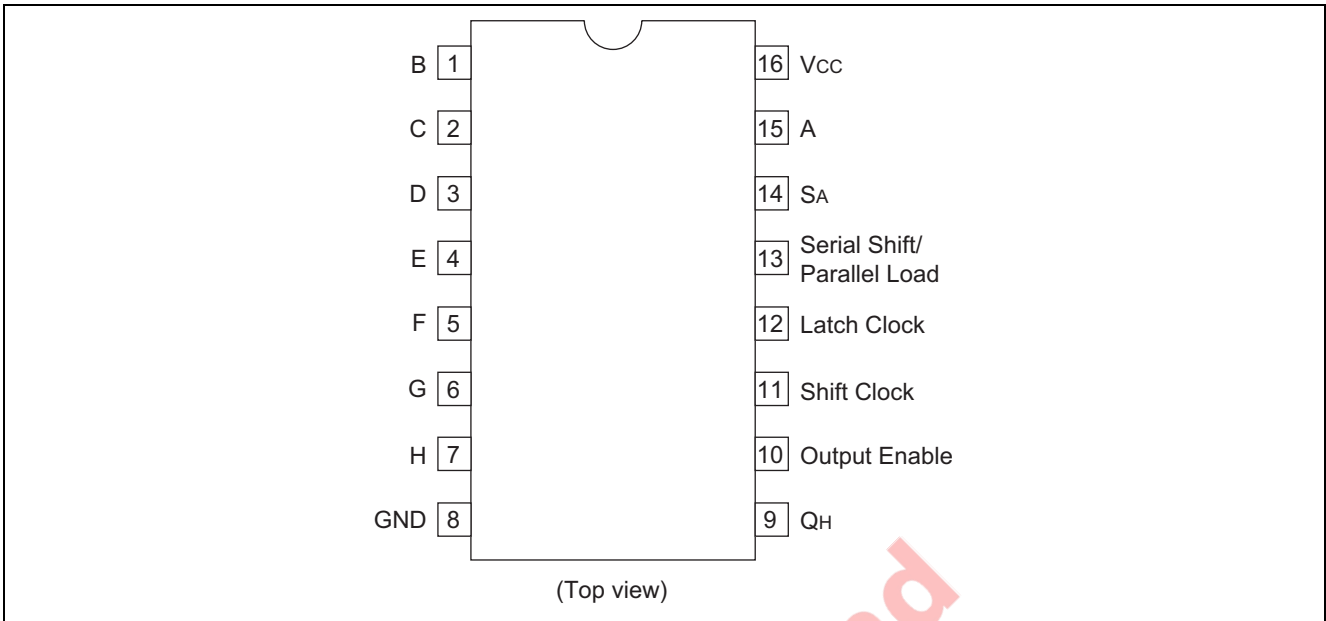
Note: Please consult the sales office for the above package availability.

### Function Table

Latch Clock LCK	Shift Clock SCK	Serial Shift/ Parallel Load	Output Enable OE	Function
	X	X	X	Data are loaded into input latches
	X	L	L	Data are loaded from input into shift registers
X	X	L	L	Data are transferred from input latches to shift registers
L, H, 	L, H, 	X	H	Outputs are disabled
X		H	L	Serial shift $Q_n = Q_{n-1}$ , $Q_0 = SER$

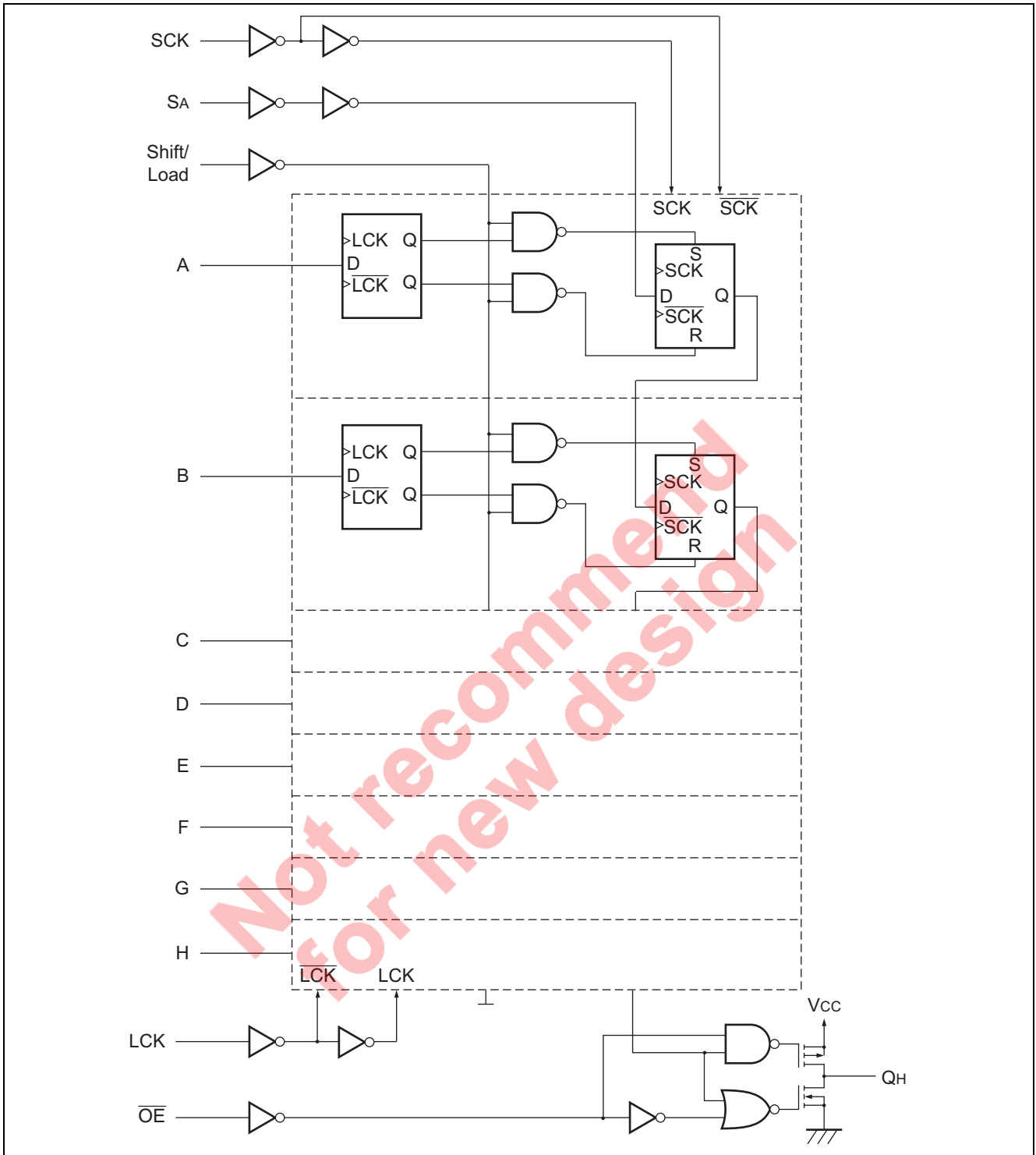
Note: 1. H; High level, L; Low level, X; Irrelevant

### Pin Arrangement



Not recommend  
for new design

Logic Diagram



### Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
Input / Output voltage	$V_{IN}, V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	$I_{IK}, I_{OK}$	$\pm 20$	mA
Output current	$I_{OUT}$	$\pm 35$	mA
$V_{CC}$ , GND current	$I_{CC}$ or $I_{GND}$	$\pm 75$	mA
Power dissipation	$P_T$	500	mW
Storage temperature	$T_{stg}$	-65 to +150	$^{\circ}C$

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

### Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	$V_{CC}$	2 to 6	V	
Input / Output voltage	$V_{IN}, V_{OUT}$	0 to $V_{CC}$	V	
Operating temperature	$T_a$	-40 to 85	$^{\circ}C$	
Input rise / fall time <sup>*1</sup>	$t_r, t_f$	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

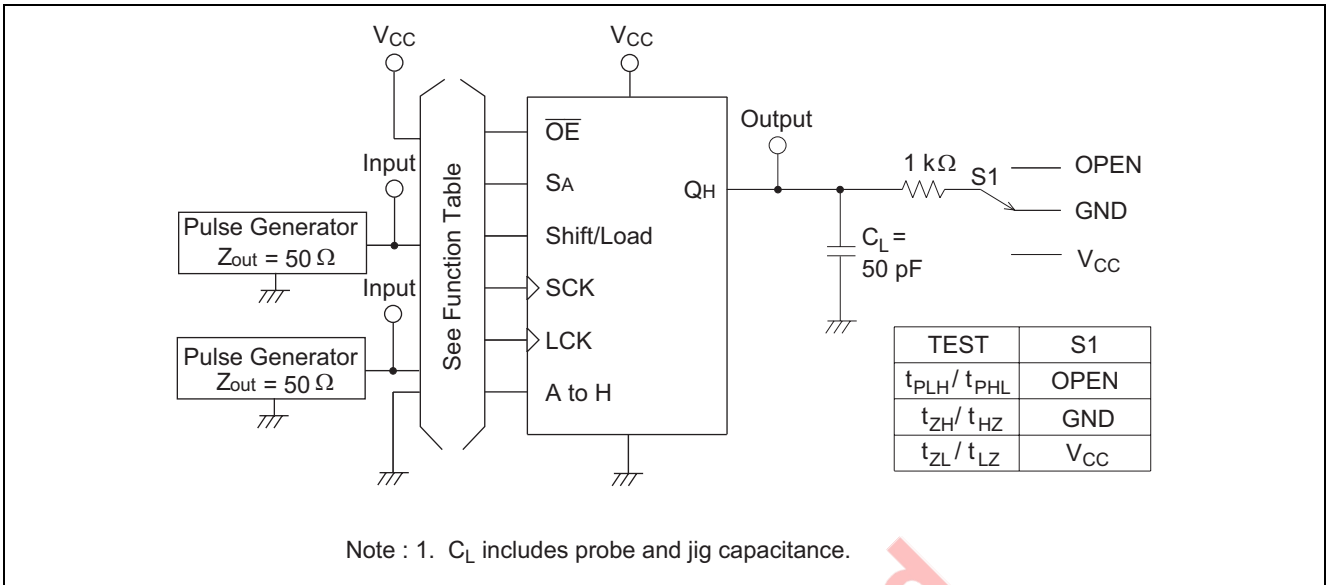
### Electrical Characteristics

Item	Symbol	$V_{CC}$ (V)	$T_a = 25^{\circ}C$			$T_a = -40$ to $+85^{\circ}C$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	$V_{IH}$	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	$V_{IL}$	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	$V_{OH}$	2.0	1.9	2.0	—	1.9	—	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -20$ $\mu A$
		4.5	4.4	4.5	—	4.4	—			$I_{OH} = -6$ mA
		6.0	5.9	6.0	—	5.9	—			$I_{OH} = -7.8$ mA
		4.5	4.18	—	—	4.13	—			
		6.0	5.68	—	—	5.63	—			
	$V_{OL}$	2.0	—	0.0	0.1	—	0.1	V	$V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 20$ $\mu A$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OH} = 6$ mA
		6.0	—	—	0.26	—	0.33			$I_{OH} = 7.8$ mA
Off-state output current	$I_{oz}$	6.0	—	—	$\pm 0.5$	—	$\pm 5.0$	$\mu A$	$V_{in} = V_{IH}$ or $V_{IL}$ $V_{out} = V_{CC}$ or GND	
Input current	$I_{in}$	6.0	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu A$	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	$I_{CC}$	6.0	—	—	4.0	—	40	$\mu A$	$V_{in} = V_{CC}$ or GND, $I_{out} = 0$ $\mu A$	

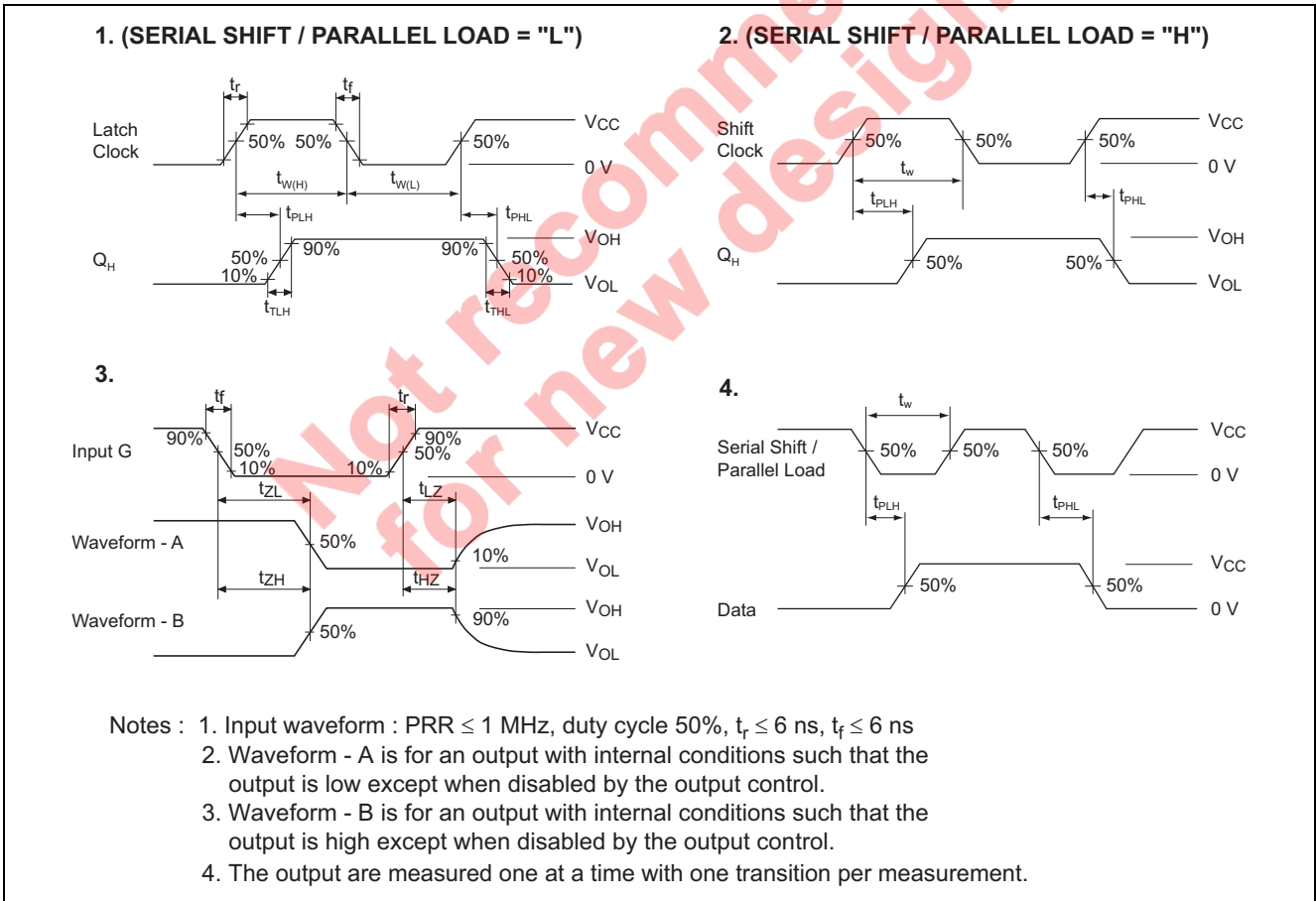
Switching Characteristics ( $C_L = 50 \text{ pF}$ , Input  $t_r = t_f = 6 \text{ ns}$ )

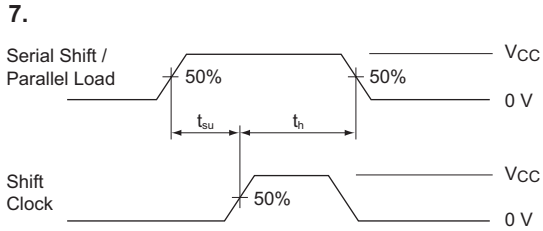
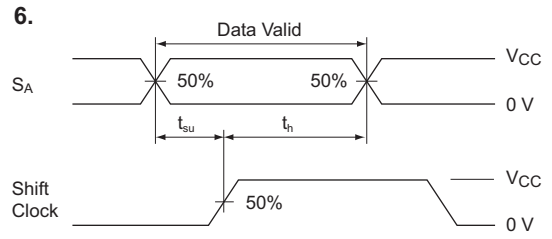
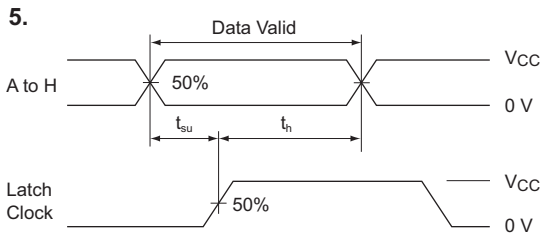
Item	Symbol	$V_{CC}$ (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	$t_{PLH}$	2.0	—	—	200	—	250	ns	Latch clock to $Q_H$
		4.5	—	20	40	—	50		
		6.0	—	—	34	—	43		
	$t_{PHL}$	2.0	—	—	175	—	220	ns	Shift clock to $Q_H$
		4.5	—	15	35	—	44		
		6.0	—	—	30	—	37		
	$t_{PLH}$	2.0	—	—	175	—	220	ns	Serial shift/parallel load to $Q_H$
		4.5	—	16	35	—	44		
		6.0	—	—	30	—	37		
Output enable time	$t_{ZL}$	2.0	—	—	150	—	190	ns	
		4.5	—	9	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	$t_{LZ}$	2.0	—	—	150	—	190	ns	
		4.5	—	14	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	$t_w$	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Setup time	$t_{su}$	2.0	100	—	—	125	—	ns	Data to latch clock
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	$t_{su}$	2.0	100	—	—	125	—	ns	$S_A$ to shift clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
	$t_{su}$	2.0	100	—	—	125	—	ns	Serial shift/parallel load to shift clock
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	$t_h$	2.0	5	—	—	5	—	ns	Latch clock to data
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
	$t_h$	2.0	5	—	—	5	—	ns	Shift clock to $S_A$
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
	$t_h$	2.0	5	—	—	5	—	ns	Shift clock to serial shift/parallel load
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	$t_{TLH}$	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	$C_{in}$	—	—	5	10	—	10	pF	

Test Circuit



Waveforms

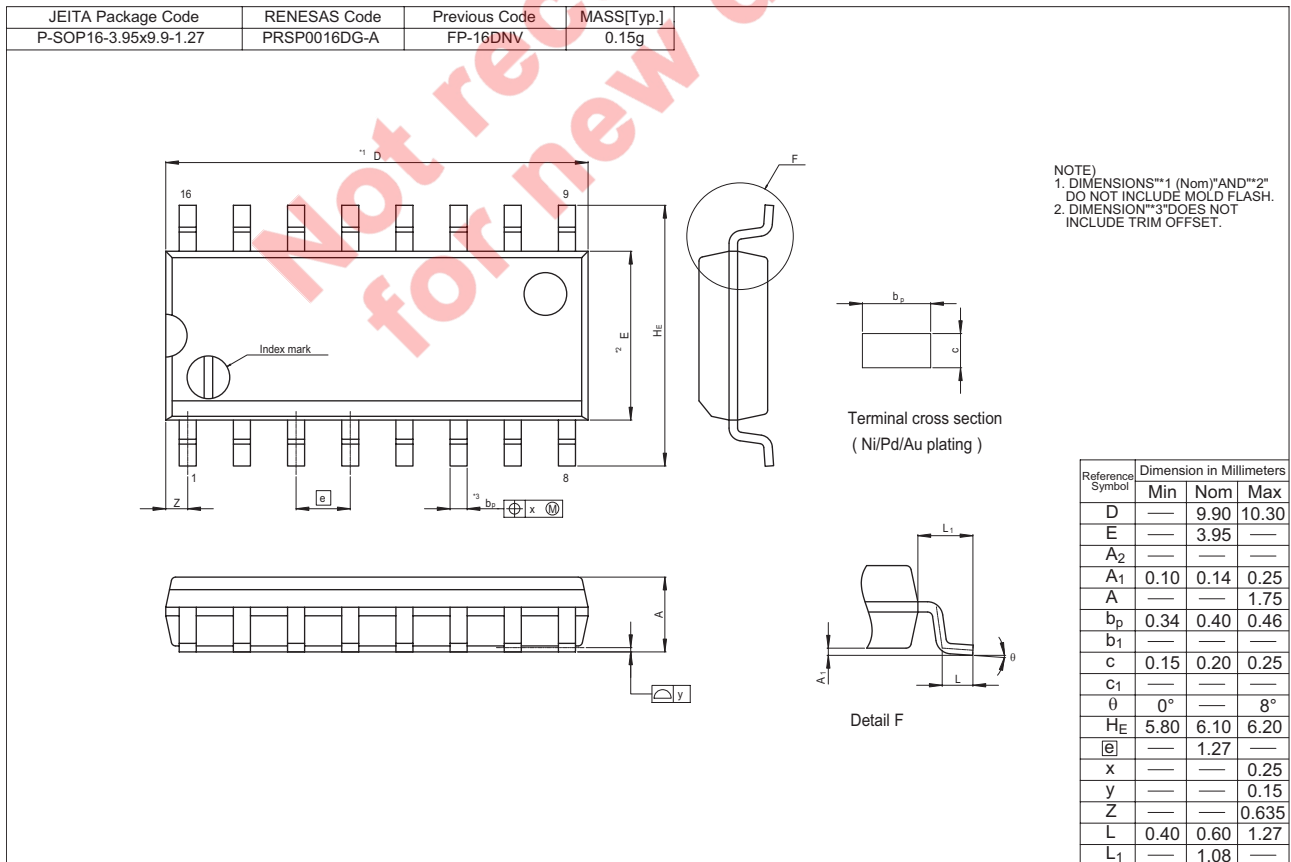
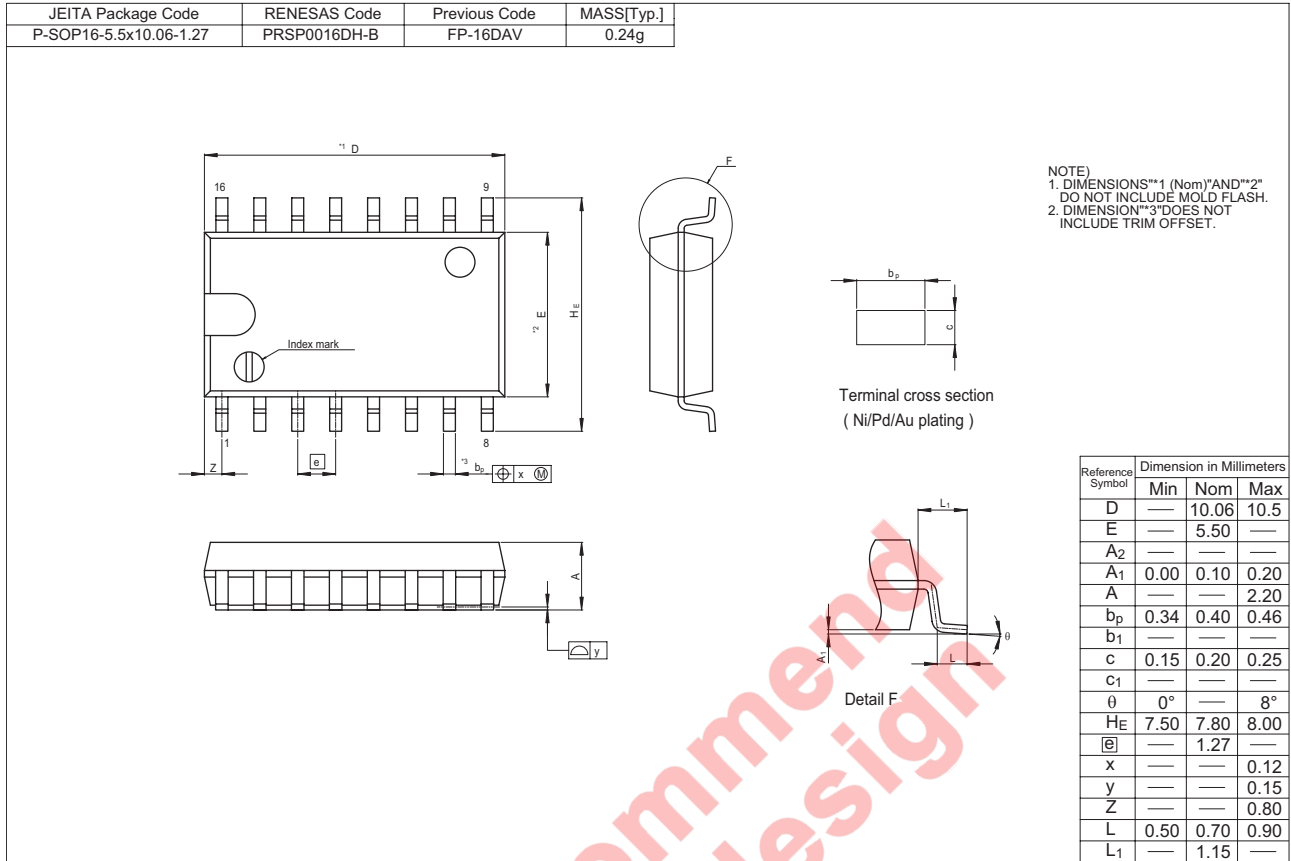




- Notes :
1. Input waveform : PRR ≤ 1 MHz, duty cycle 50%, t<sub>r</sub> ≤ 6 ns, t<sub>f</sub> ≤ 6 ns
  2. The output are measured one at a time with one transition per measurement.

Not recommended for new design

Package Dimensions





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Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

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Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

**Renesas Technology Malaysia Sdn. Bhd**

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: <603> 7955-9390, Fax: <603> 7955-9510