

HD74HC595

8-bit Shift Register/Latch (with 3-state outputs)

REJ03D0634-0200
 (Previous ADE-205-514)
 Rev.2.00
 Mar 30, 2006

Description

This device each contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.



Features

- High Speed Operation: t_{pd} (RCK to Q) = 17 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads (Q_A to Q_H outputs)
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

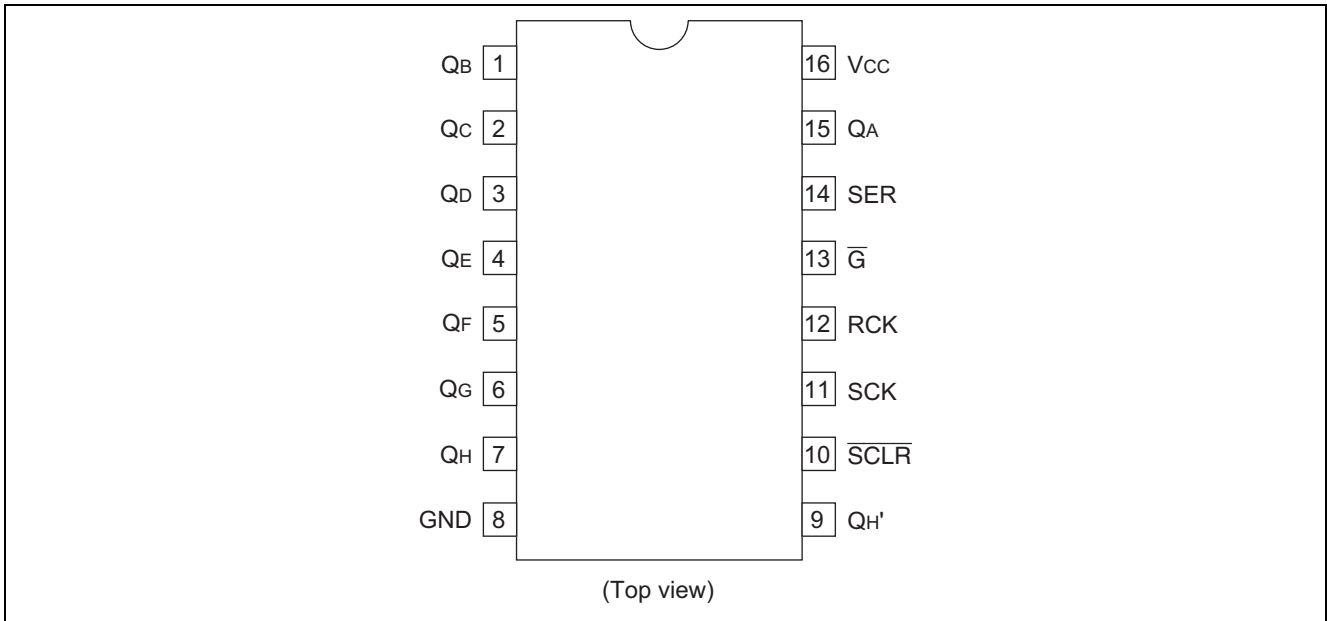
Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC595P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC595FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

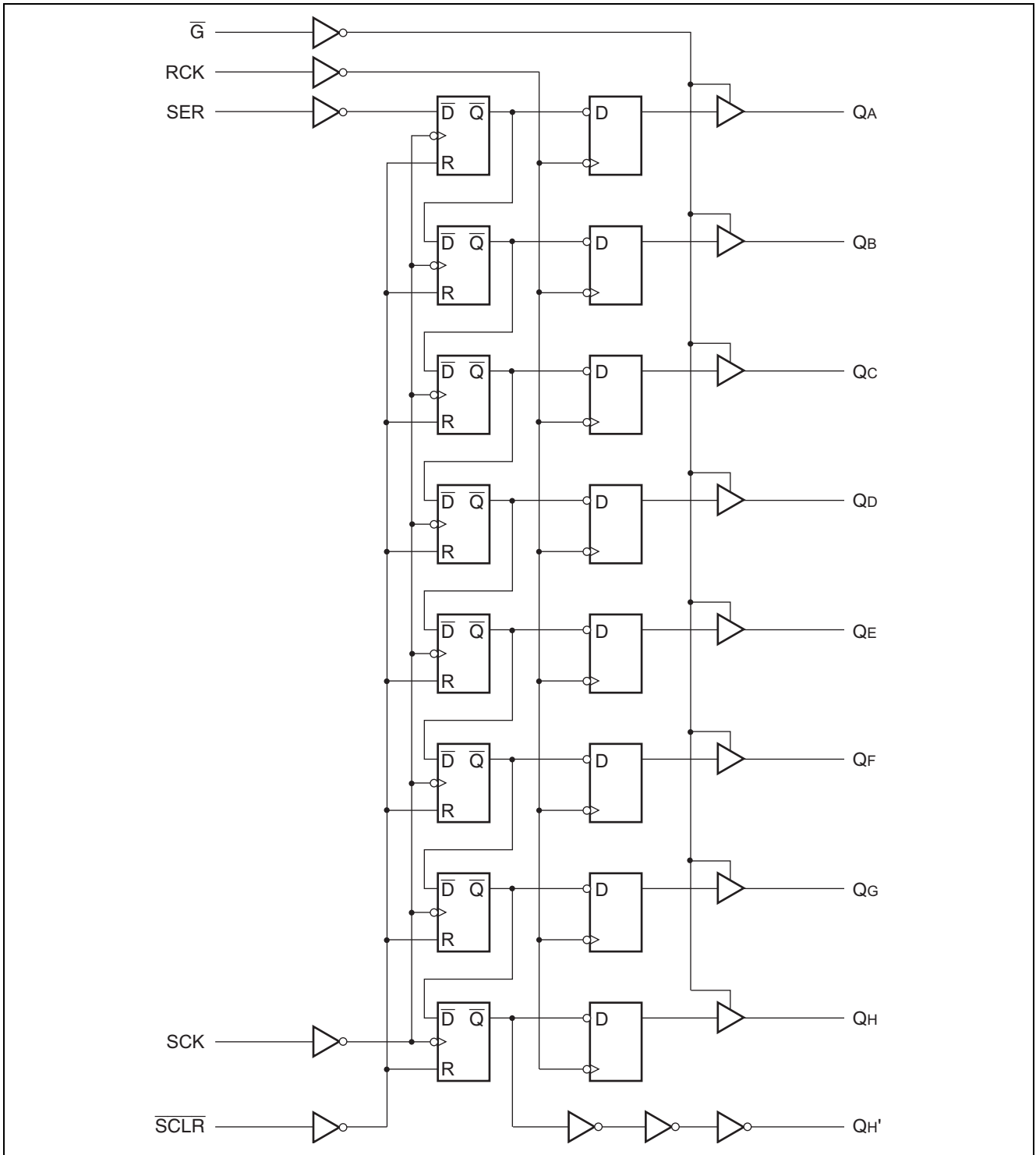
Function Table

Inputs				Function
RCK	SCK	SCLR	\bar{G}	
X	X	X	H	Q_A to Q_H high impedance
X	X	L	X	Shift register cleared $Q_H' = L$
X		H	X	Shift register clocked $Q_n = Q_{n-1}$, $Q_A = SER$
	X	H	X	Contents of shift register transferred to output latches

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time *1	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0$ V
		0 to 500		$V_{CC} = 4.5$ V
		0 to 400		$V_{CC} = 6.0$ V

Note: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

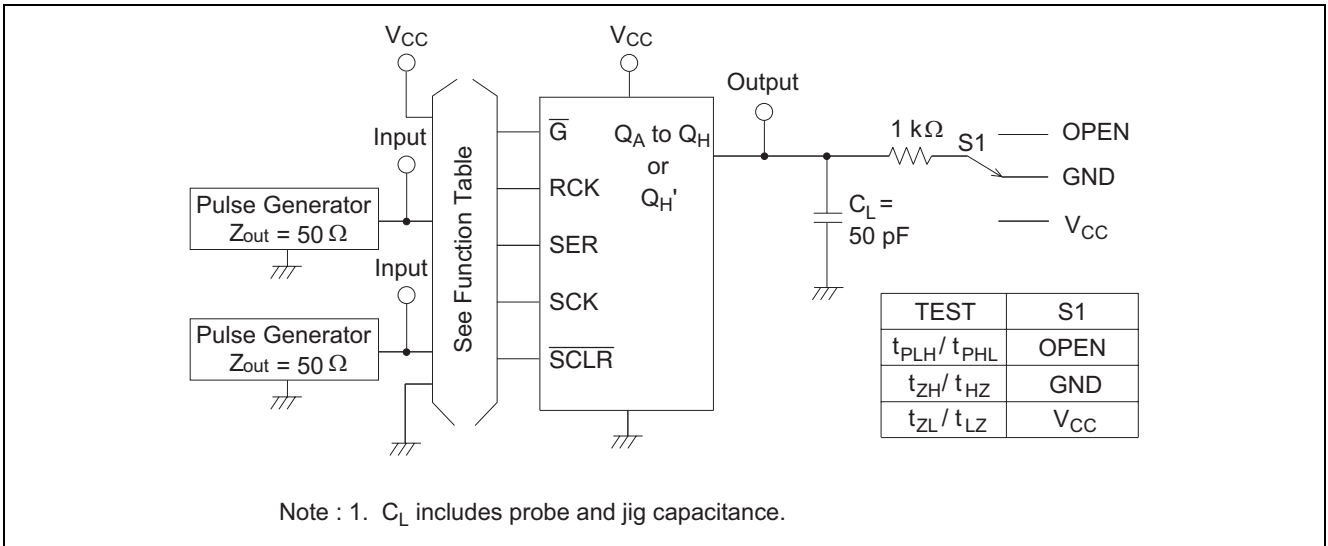
Electrical Characteristics

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to+85°C		Unit	Test Conditions			
			Min	Typ	Max	Min	Max					
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V				
		4.5	3.15	—	—	3.15	—					
		6.0	4.2	—	—	4.2	—					
	V _{IL}	2.0	—	—	0.5	—	0.5	V				
		4.5	—	—	1.35	—	1.35					
		6.0	—	—	1.8	—	1.8					
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Q _A to Q _H Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA		
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -6 mA		
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -7.8 mA		
		4.5	4.18	—	—	4.13	—		V	Q _A to Q _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		6.0	5.68	—	—	5.63	—				I _{OL} = 6 mA	
		4.5	—	—	0.26	—	0.33				I _{OL} = 7.8 mA	
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Q' _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA		
		4.5	—	0.0	0.1	—	0.1			I _{OL} = 6 mA		
		6.0	—	0.0	0.1	—	0.1			I _{OL} = 7.8 mA		
		4.5	—	—	0.26	—	0.33		V	Q' _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA	
		6.0	—	—	0.26	—	0.33				I _{OL} = 4 mA	
		4.5	—	—	0.26	—	0.33				I _{OL} = 5.2 mA	
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Q' _H Vin = V _{IH} or V _{IL}	I _{OH} = -20 μA		
		4.5	4.4	4.5	—	4.4	—			I _{OH} = -4 mA		
		6.0	5.9	6.0	—	5.9	—			I _{OH} = -5.2 mA		
		4.5	4.18	—	—	4.13	—			V	Q' _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		6.0	5.68	—	—	5.63	—					I _{OL} = 4 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Q' _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA		
		4.5	—	0.0	0.1	—	0.1			I _{OL} = 4 mA		
		6.0	—	0.0	0.1	—	0.1			I _{OL} = 5.2 mA		
		4.5	—	—	0.26	—	0.33			V	Q' _H Vin = V _{IH} or V _{IL}	I _{OL} = 20 μA
		6.0	—	—	0.26	—	0.33					I _{OL} = 4 mA
Off-state output current	I _{OZ}	6.0	—	—	±0.5	—	±5.0	μA	Vin = V _{IH} or V _{IL} , Vout = V _{CC} or GND			
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	μA	Vin = V _{CC} or GND			
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	μA	Vin = V _{CC} or GND, Iout = 0 μA			

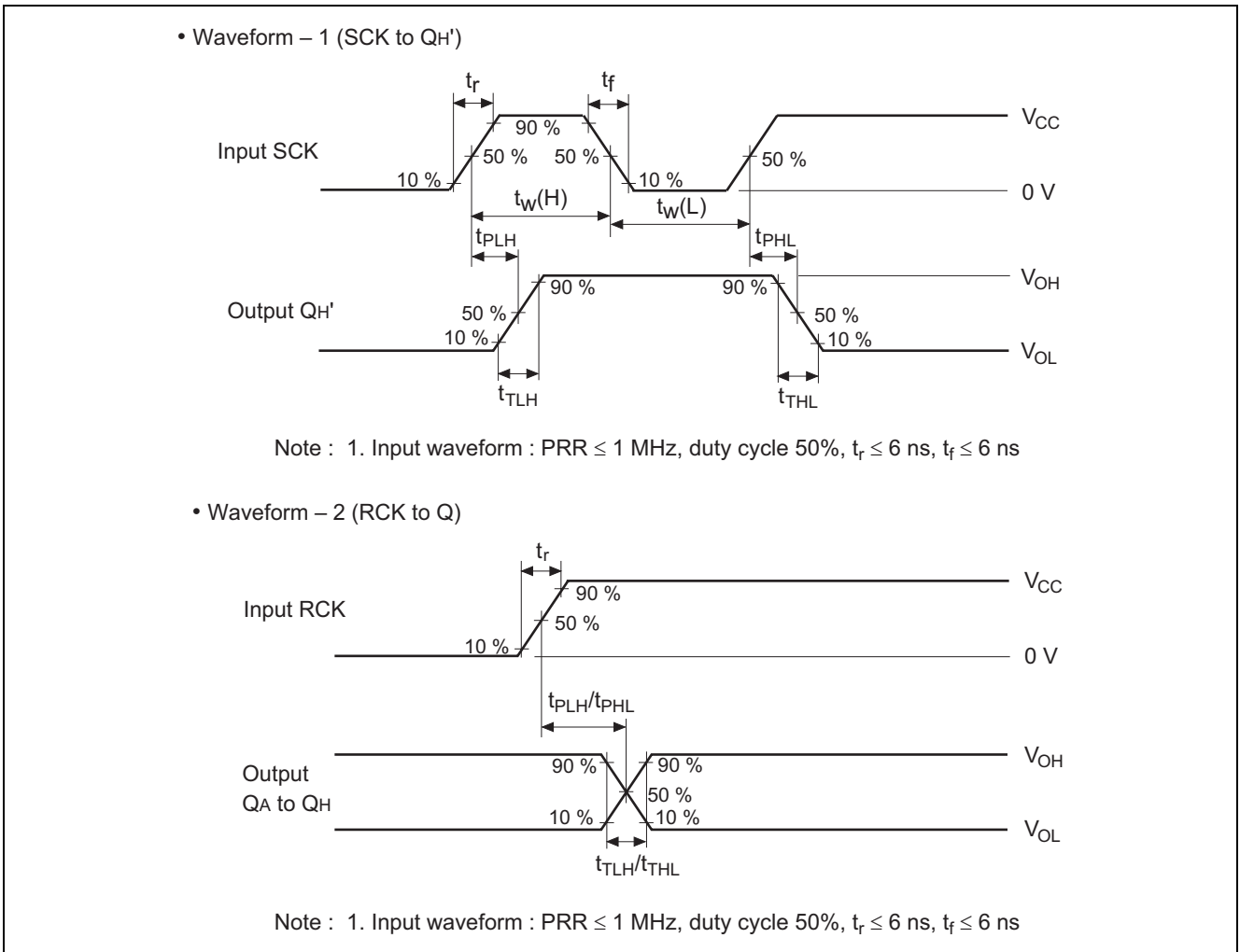
Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{\max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	31	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	115	—	145	ns	SCK to Q_H'
		4.5	—	12	23	—	29		
		6.0	—	—	20	—	25		
	t_{PHL}	2.0	—	—	150	—	190	ns	RCK to Q
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
	t_{PLH}	2.0	—	—	175	—	220	ns	$\overline{\text{SCLR}}$ to Q_H'
		4.5	—	20	35	—	44		
		6.0	—	—	30	—	37		
Output enable time	t_{ZL}	2.0	—	—	150	—	190	ns	
		4.5	—	13	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ}	2.0	—	—	150	—	190	ns	
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	SER to SCK
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	200	—	—	250	—	ns	SCK to RCK
		4.5	40	8	—	50	—		
		6.0	34	—	—	43	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	100	—	—	125	—	ns	
		4.5	20	—	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	
		4.5	5	1	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH}	2.0	—	—	75	—	95	ns	Q_H'
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
	t_{THL}	2.0	—	—	60	—	75	ns	Q
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
Input capacitance	C_{in}	—	—	5	10	—	5	pF	

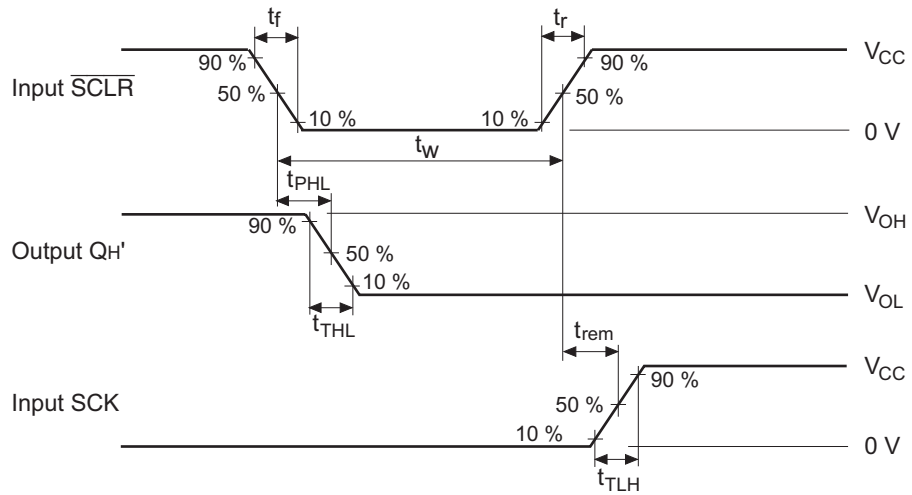
Test Circuit



Waveforms

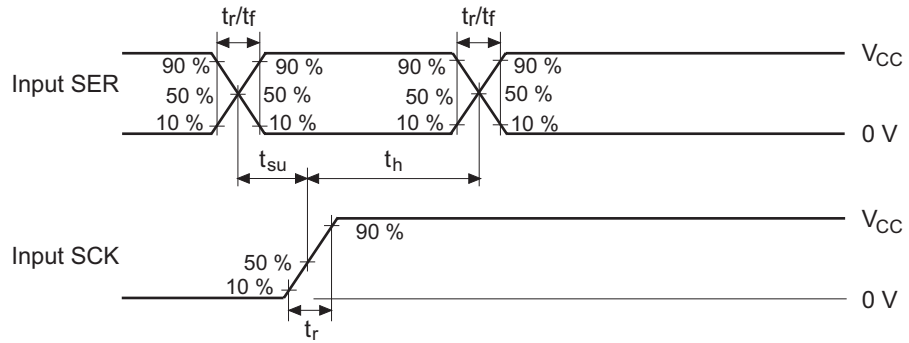


• Waveform – 3 ($\overline{\text{SCLR}}$ to QH')



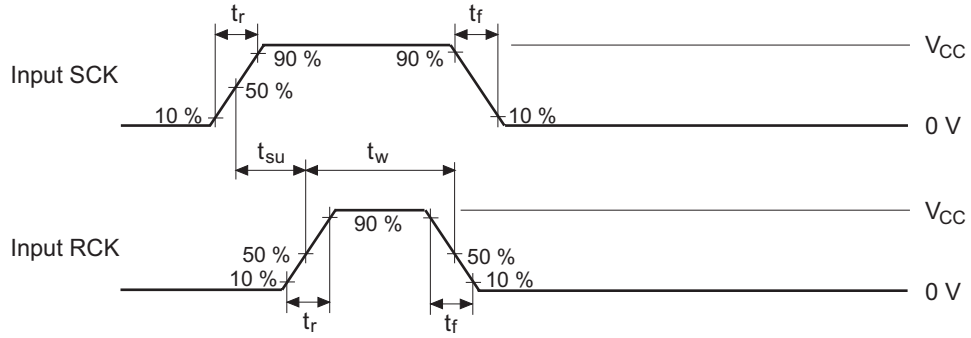
Note : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns

• Waveform – 4 (SER to SCK)



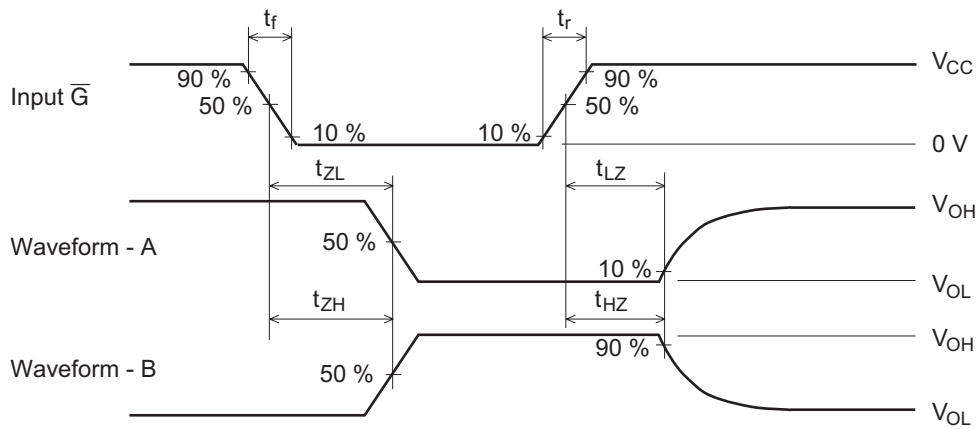
Note : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq$ 6 ns, $t_f \leq$ 6 ns

• Waveform – 5 (SCK to RCK)



Note : 1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns

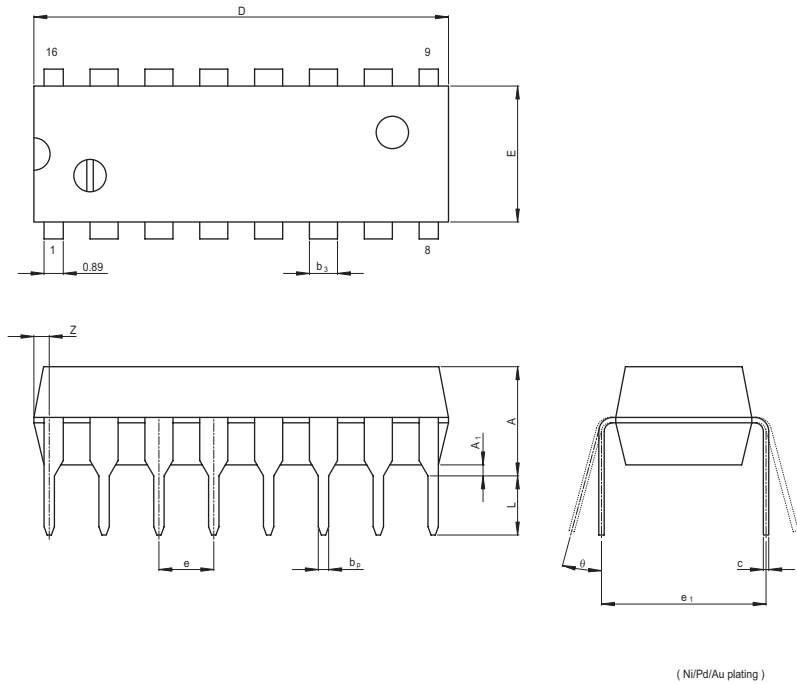
• Waveform – 6 (t_{zL} , t_{zH} , t_{LZ} , t_{HZ})



- Notes :
1. Input waveform : PRR \leq 1 MHz, duty cycle 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions

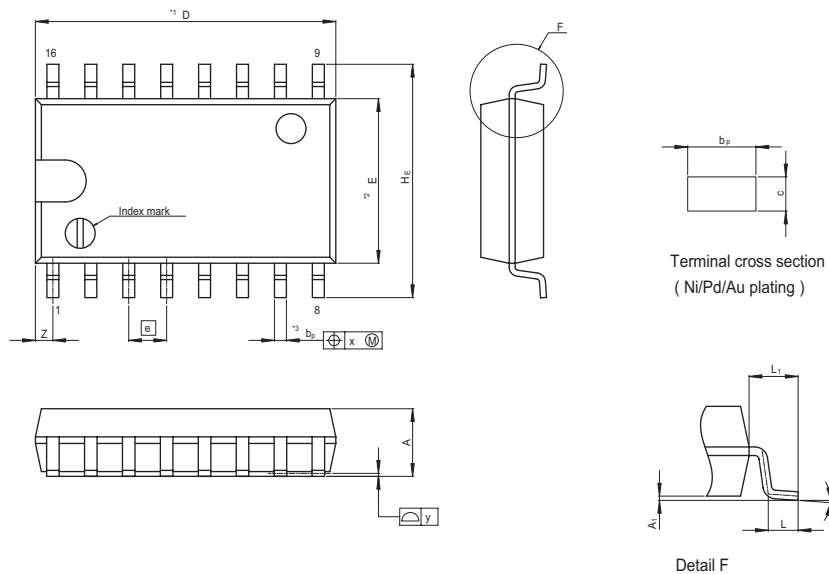
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e ₁	—	7.62	—
D	—	19.2	20.32
E	—	6.3	7.4
A	—	—	5.06
A ₁	0.51	—	—
b _p	0.40	0.48	0.56
b ₃	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.12
L	2.54	—	—

(Ni/Pd/Au plating)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g



NOTE
 1. DIMENSIONS**1 (Nom)**AND**2* DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION**3*DOES NOT INCLUDE TRIM OFFSET.

Terminal cross section
 (Ni/Pd/Au plating)

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	10.06	10.5
E	—	5.50	—
A ₂	—	—	—
A ₁	0.00	0.10	0.20
A	—	—	2.20
b _p	0.34	0.40	0.46
b ₁	—	—	—
c	0.15	0.20	0.25
c ₁	—	—	—
θ	0°	—	8°
HE	7.50	7.80	8.00
Ⓧ	—	1.27	—
x	—	—	0.12
y	—	—	0.15
Z	—	—	0.80
L	0.50	0.70	0.90
L ₁	—	1.15	—

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Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

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Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

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Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510