HD74HC673

16-bit Shift Register

HITACHI

Description

The HD74HC673 is a 16-bit shift register and a 16-bit storage register in a single 24-pin package. A three-state input/output (data I/O) port to the shift register allows serial entry and/or reading of data. The storage register is connected in a parallel data loop with the shift register and may be asynchronously cleared by taking the store-clear input low. The storage register may be parallel loaded with shift-register data to provide shift-register status via the parallel outputs. The shift register can be parallel loaded with the storage-register data upon command.

A high logic level at the chip-select ($\overline{CS}$) input disables both the shift-register clock and the storage register clock and places the data I/O in the high-impedance state. The store-clear function is not disabled by the chip select.

Caution must be exercised to prevent false clocking of either the shift register or the storage register via the chip-select input. The shift clock should be low during the low-to-high transition of chip select and the store clock should be low during the high-to-low transition of chip select.

Features

- High Speed Operation: t_{pd} (MODE/STRCLK to Y) = 23 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 15 LSTTL Loads (Q_{15} output)
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max (Ta = 25°C)

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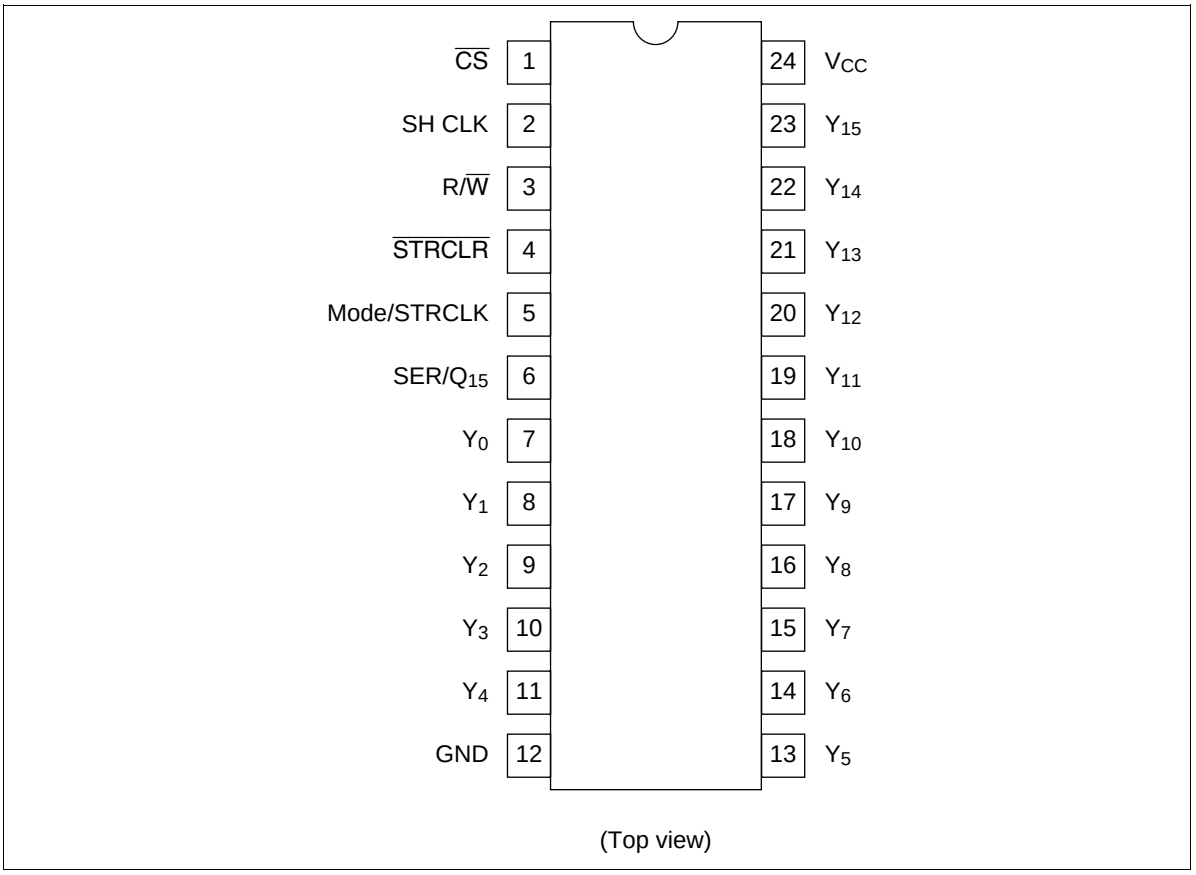
Function Table

Inputs						Shift Register Functions				Storage Register Functions	
$\overline{CS}$	R/$\overline{W}$	SHCLK	$\overline{STRCLR}$	Mode/ STRCLK	SER/ Q_{15}	Shift	Read from Serial Output	Write into Serial Input	Parallel Load	Clear	Load
H	X	X	X	X	Z	No	No	No	No		No
X	X	X	L	X						Yes	
L	L	↓	X	X	Z	Yes	No	Yes	No		
L	H	X	X	X	Q_{15}		Yes	No			No
L	H	↓	X	L	Q_{14n}	Yes	Yes	No	No		No
L	H	↓	L	H	L	No	Yes		Yes	Yes	No
L	H	↓	H	H	Y_{15n}	No	Yes		Yes	No	No
L	L	X	H	↑	Z		No		No	No	Yes

Pin Arrangement

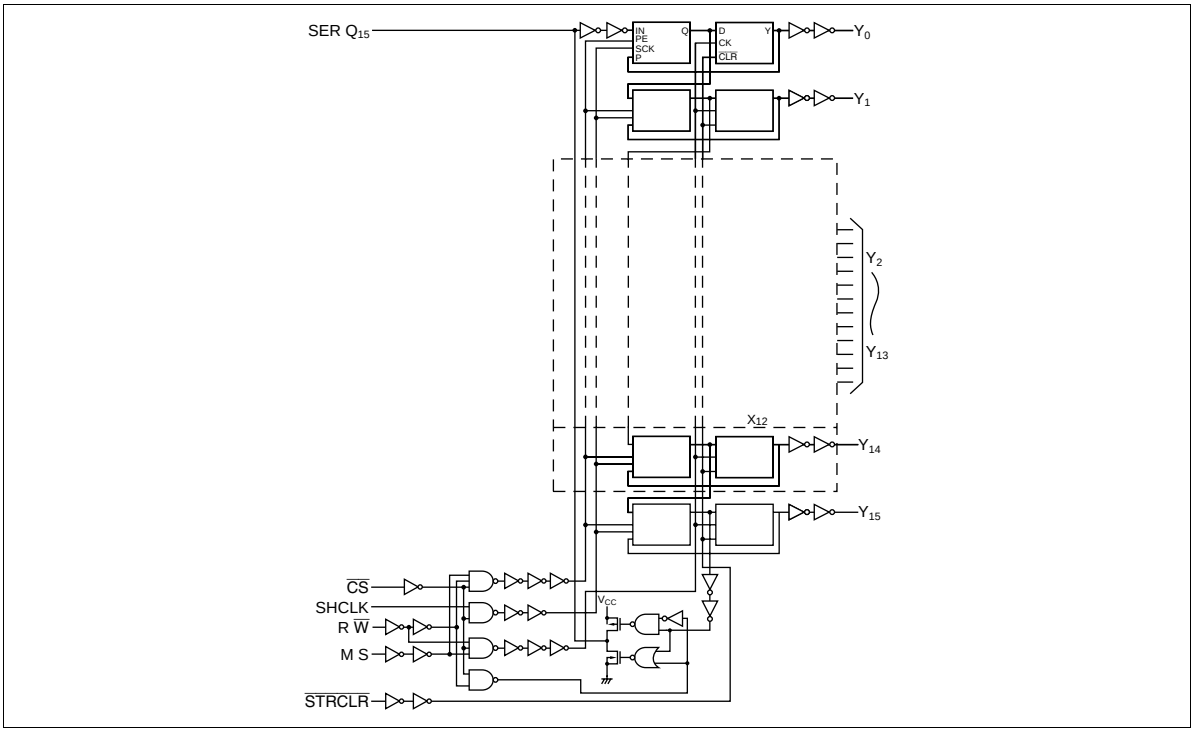


(Top view)

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage range	V_{CC}	–0.5 to +7.0	V
Input voltage	V_{IN}	–0.5 to V_{CC} + 0.5	V
Output voltage	V_{OUT}	–0.5 to V_{CC} + 0.5	V
Output current	I_{OUT}	±35	mA
DC current drain per V_{CC}, GND	I_{CC}, I_{GND}	±75	mA
DC input diode current	I_{IK}	±20	mA
DC output diode current	I_{OK}	±20	mA
Power dissipation per package	P_T	500	mW
Storage temperature	Tstg	–65 to +150	°C

Logic Diagram



DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions	
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Q_{15}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		Vin = V_{IH} or V_{IL}	
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –6 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –7.8 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Q_{15}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		Vin = V_{IH} or V_{IL}	
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 6 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 7.8 mA
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Y_0 to Y_{15}	I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		Vin = V_{IH} or V_{IL}	
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—			I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Y_0 to Y_{15}	I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		Vin = V_{IH} or V_{IL}	
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I_{OL} = 5.2 mA
Off-state output current	I_{OZ}	6.0	—	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}, Vout = V_{CC} or GND	
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA	

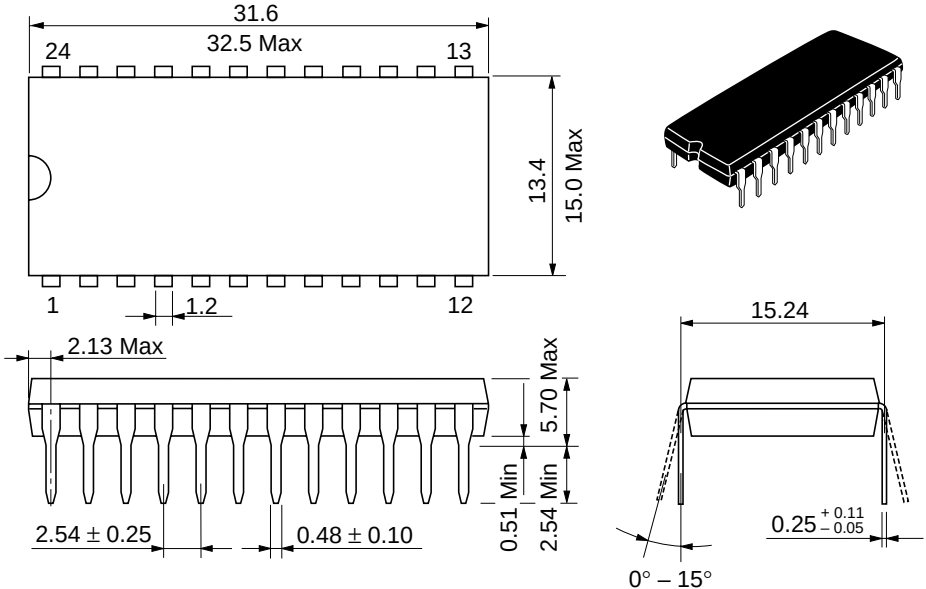
AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{cc} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	27	—	21		
		6.0	—	—	32	—	25		
Propagation delay time	t_{PLH}	2.0	—	—	200	—	250	ns	$\overline{\text{STRCLR}}$ to Y
	t_{PHL}	4.5	—	23	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	200	—	250	ns	Mode/STRCLK to Y
	t_{PHL}	4.5	—	23	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	200	—	250	ns	SHCLK to SER/Q_{15}
	t_{PHL}	4.5	—	19	40	—	50		
		6.0	—	—	34	—	43		
Output enable time	t_{ZH}	2.0	—	—	150	—	190	ns	
	t_{ZL}	4.5	—	—	30	—	38		
		6.0	—	—	26	—	33		
Output disable time	t_{HZ}	2.0	—	—	150	—	190	ns	
	t_{LZ}	4.5	—	—	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	SER/Q_{15} to SH CLK
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
	t_{su}	2.0	100	—	—	125	—	ns	$\overline{\text{CS}}$ to R/$\overline{\text{W}}$
		4.5	20	7	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	SH CLK to SER/Q_{15}
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		

AC Characteristics (C_L = 50 pF, Input t_r = t_f = 6 ns) (cont)

			Ta = 25°C			Ta = –40 to +85°C			
Item	**Symbol**	**V_{CC} (V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Output rise/fall time	t_{TLH}	2.0	—	—	60	—	75	ns	6 Pin
	t_{THL}	4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
	t_{TLH}	2.0	—	—	75	—	95	ns	Other Pins
	t_{THL}	4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm



Hitachi Code	DP-24
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	3.1 g

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