
HD74HCT00A

Quad. 2-input Positive NAND Gates

HITACHI

ADE-205-286 (Z)
1st. Edition
June 1999

Description

The HD74HCT00A has four 2-input NAND gates in a 14 pin package. $Y = \overline{A \cdot B}$ or $Y = \overline{A} + \overline{B}$

Features

- $V_{CC} = 4.5$ to 5.5 V operation
- Input terminal has protection diode

Function Table

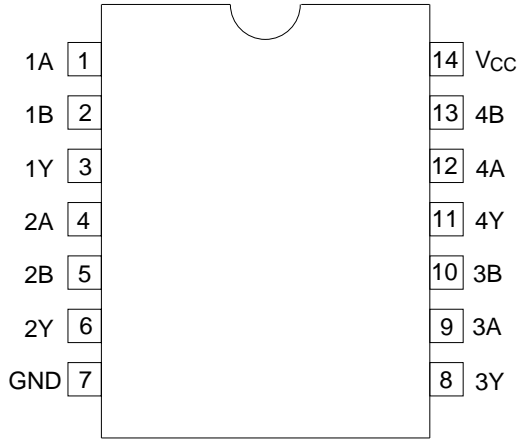
Inputs		Output Y
A	B	
H	H	L
L	X	H
X	L	H

H : High level

L : Low level

X : Immaterial

Pin Arrangement



(Top view)

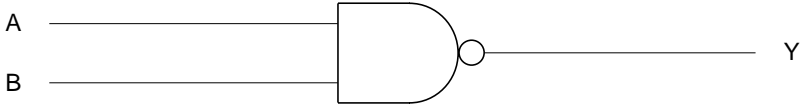
Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input diode peak current	I_{IK}	± 20	mA
Output diode peak current	I_{OK}	± 20	mA
Output current	I_o	± 25	mA
V_{CC} , GND current / pin	I_{CC} or I_{GND}	± 50	mA
Storage temperature	T _{stg}	-65 to 150	°C

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.0	—	—	V
	V_{IL}	0	—	0.8	
	V_I	0	—	V_{CC}	
Output voltage	V_O	0	—	V_{CC}	V
Output current	I_{OH}	—	-4	—	mA
	I_{OL}	—	4	—	
Input rise / fall time	t_r, t_f	—	—	500	ns
Operating temperature	T_a	-40	—	85	°C

Logic Diagram (1/4 Circuit)



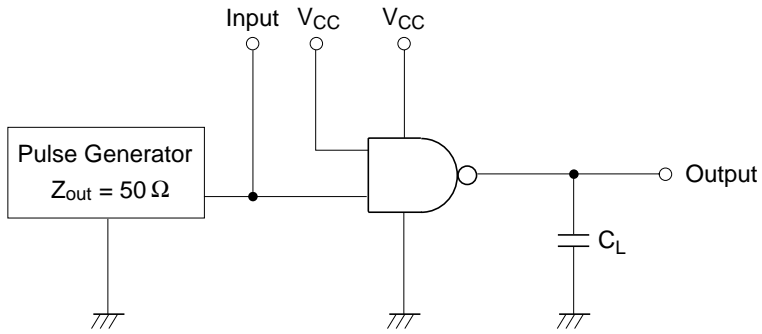
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Output voltage	V_{OH}	4.5	4.40	—	—	4.40	—	V	$I_o = -20 \mu\text{A}$
		4.5	3.98	—	—	3.84	—		$I_o = -4 \text{ mA}$
	V_{OL}	4.5	—	—	0.10	—	0.10		$I_o = 20 \mu\text{A}$
		4.5	—	—	0.26	—	0.33		$I_o = 4 \text{ mA}$
Input current	I_I	5.5	—	± 0.1	± 100	—	± 1000	nA	$V_I = V_{CC}$ or GND
Quiescent supply voltage	I_{CC}	5.5	—	—	2.0	—	20	μA	$V_I = V_{CC}$ or GND, $I_o = 0$

Switching Characteristics ($C_L = 50 \text{ pF}$)

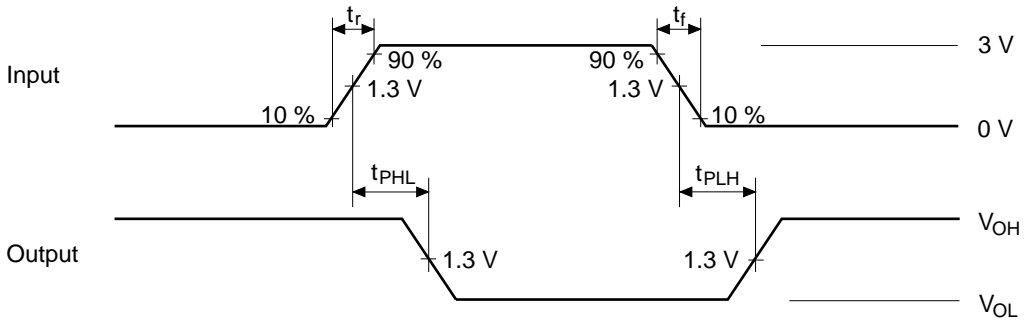
Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Input FROM	Output TO
			Min	Typ	Max	Min	Max			
Propagation delay time	t_{PLH}	4.5	—	11	17	—	21	ns	A or B	Y
	t_{PHL}	5.5	—	10	15	—	19			
Output rise / fall time	t_r	4.5	—	7	15	—	19	ns		Y
	t_f	5.5	—	6	13	—	16			
Input capacitance	C_I	—	—	3	10	—	10	pF		
Power dissipation capacitance	C_{PD}	—	—	20	—	—	—	pF		

Test Circuit



Note: 1. C_L includes probe and jig capacitance.

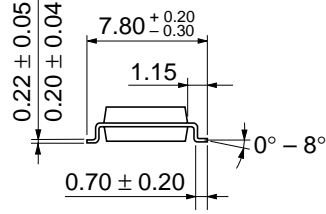
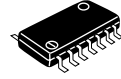
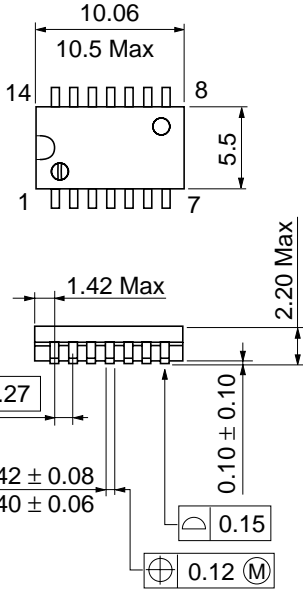
• Waveform



Note: 1. Input waveform : PRR = 1 MHz, duty cycle 50%, $t_r = 6$ ns, $t_f = 6$ ns

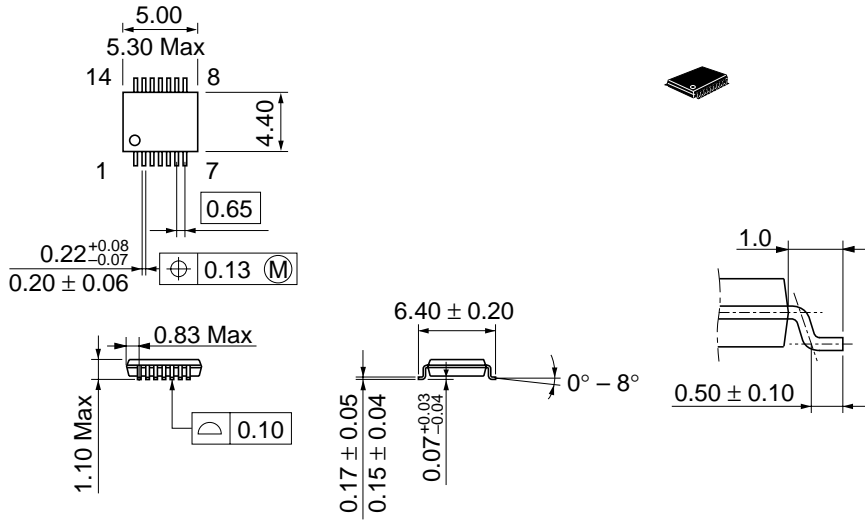
Package Dimensions

Unit : mm



Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-14D
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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