
HD74HCT137

3-to-8-line Decoder/Demultiplexer with Address Latch

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Description

The HD74HCT137 implements a three-to-eight line decoder with latches on the three address inputs. When \overline{GL} goes from low to high, the address present at the select inputs (A, B and C) is stored in the latches. As long as \overline{GL} remains high no address changes will be recognized. Output enable controls, G_1 and $\overline{G_2}$, control the state of the outputs independently of the select or latch-enable inputs.

All of the outputs are high unless G_1 is high and $\overline{G_2}$ is low. The HD74HCT137 is ideally suited for the implementation of glitchfree decoders in stored-address applications in bus oriented systems.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A, B, C to Y) = 18 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

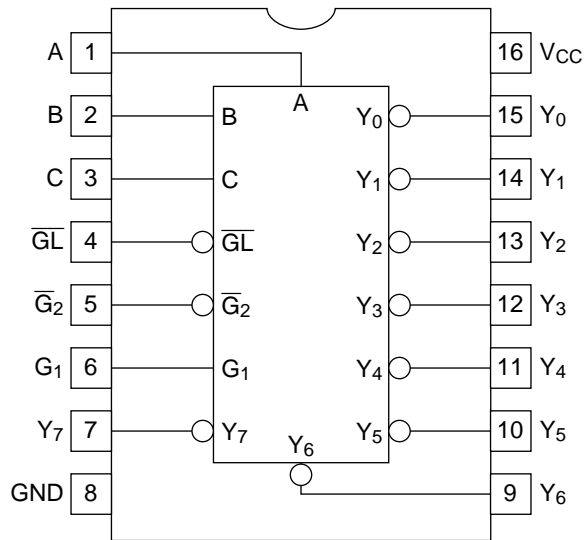
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Function Table

Inputs

Enable			Select			Outputs							
$\overline{G_L}$	G_1	$\overline{G_2}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L
H	H	L	X	X	X	Output Corresponding to stored address L; all others H							

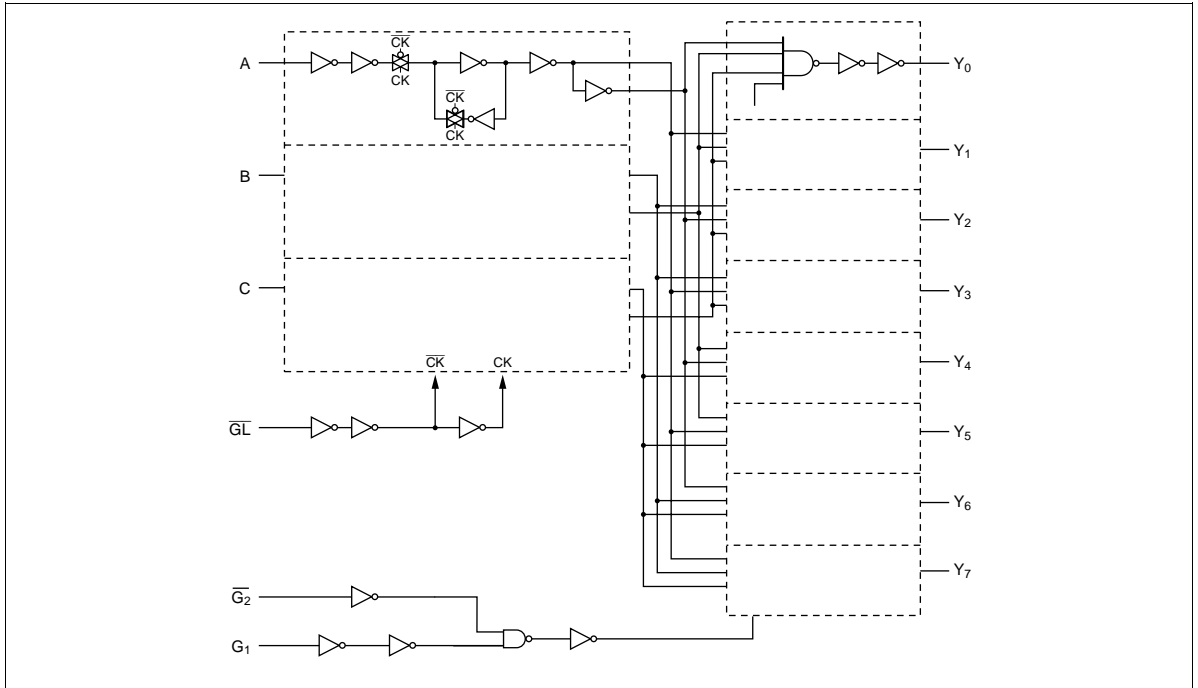
Pin Arrangement



(Top view)

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Logic Diagram



DC Characteristics

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min		Max	V _{CC} (V)
Input voltage	V _{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5
	V _{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5
Output voltage	V _{OH}	4.4	—	—	4.4	—	V	4.5 Vin = V _{IH} or V _{IL} I _{OH} = -20 μA
		4.18	—	—	4.13	—		4.5 I _{OH} = -4 mA
	V _{OL}	—	—	0.1	—	0.1	V	4.5 Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		—	—	0.26	—	0.33		4.5 I _{OL} = 4 mA
Input current	I _{in}	—	—	±0.1	—	±1.0	μA	5.5 Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	—	—	4.0	—	40	μA	5.5 Vin = V _{CC} or GND, I _{out} = 0 μA

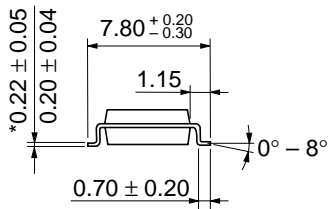
HD74HCT137

AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
		Min	Typ	Max	Min		Max	V _{cc} (V)	
Propagation delay time	t _{PLH}	—	14	34	—	43	ns	4.5	A, B or C to Y
	t _{PHL}	—	22	48	—	60		4.5	
	t _{PLH}	—	11	26	—	33	ns	4.5	\overline{G}_2 to Y
	t _{PHL}	—	23	39	—	49		4.5	
	t _{PLH}	—	13	30	—	38	ns	4.5	G ₁ to Y
	t _{PHL}	—	17	39	—	49		4.5	
	t _{PLH}	—	16	35	—	44	ns	4.5	\overline{GL} to Y
	t _{PHL}	—	23	50	—	63		4.5	
Pulse width	t _w	16	6	—	20	—	ns	4.5	
Setup time	t _{su}	20	3	—	25	—	ns	4.5	
Hold time	t _h	10	0	—	13	—	ns	4.5	
Output rise/fall time	t _{TLH}	—	5	15	—	19	ns	4.5	
	t _{THL}								
Input capacitance	C _{in}	—	5	10	—	10	pF	—	



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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