HD74HCT1G00

2–input NAND Gate

REJ03D0191–0500Z
(Previous ADE-205-301C (Z))
Rev.5.00
Jan.28.2004

Description

The HD74HCT1G00 is high-speed CMOS two input NAND gate using silicon gate CMOS process. With CMOS low power dissipation, it provides high-speed equivalent to LS–TTL series. The internal circuit of three stages construction with buffer provides wide noise margin and stable output.

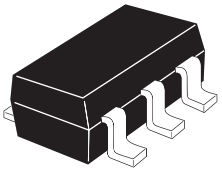
Features

- The basic gate function is lined up as Renesas uni logic series.
- Supplied on emboss taping for high-speed automatic mounting.
- TTL compatible input level.
  Supply voltage range : 4.5 to 5.5 V
  Operating temperature range : –40 to +85°C
- $|I_{OH}| = I_{OL} = 2$ mA (min)
- Ordering Information

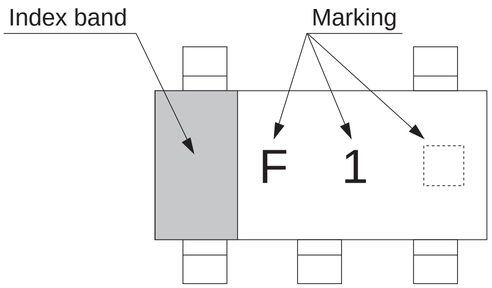
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HCT1G00CME	CMPAK-5 pin	CMPAK-5V	CM	E (3,000 pcs/reel)

Outline and Article Indication

- HD74HCT1G00



CMPAK–5



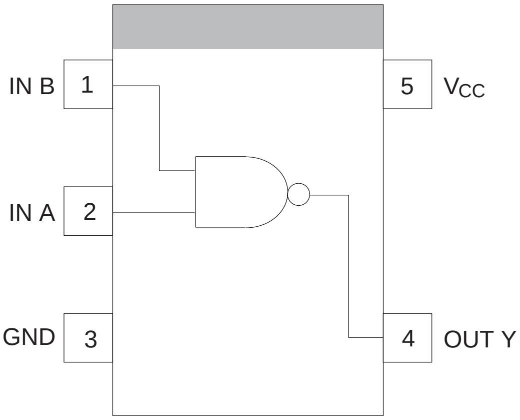
⬚ = Control code

Function Table

Inputs		
A	**B**	**Output Y**
L	L	H
L	H	H
H	L	H
H	H	L

H : High level
L : Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Test Conditions
Supply voltage range	V_{CC}	–0.5 to 7.0	V	
Input voltage range [*1]	V_I	–0.5 to V_{CC} + 0.5	V	
Output voltage range [*1, 2]	V_O	–0.5 to V_{CC} + 0.5	V	Output : H or L
Input clamp current	I_{IK}	±20	mA	$V_I < 0$ or $V_I > V_{CC}$
Output clamp current	I_{OK}	±20	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	±25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	±25	mA	
Maximum power dissipation at Ta = 25°C (in still air) [*3]	P_T	200	mW	
Storage temperature	Tstg	–65 to 150	°C	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Test Conditions
Supply voltage range	V_{CC}	4.5	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	
Output current	I_{OL}	—	2	mA	V_{CC} = 4.5 to 5.5 V
	I_{OH}	—	–2		V_{CC} = 4.5 to 5.5 V
Input rise / fall time (0.3 V to 2.7 V)	t_r, t_f	0	500	ns	V_{CC} = 4.5 to 5.5 V
Operating temperature	Ta	–40	85	°C	

Note: Unused or floating inputs must be held high or low.

Electrical Characteristics

		V_{CC}	T_a = 25°C			T_a = –40 to 85°C				
Item	**Symbol**	**(V)**	**Min**	**Typ**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**	
Input voltage	V_{IH}	4.5 to 5.5	2.0	—	—	2.0	—	V		
	V_{IL}	4.5 to 5.5	—	—	0.8	—	0.8			
Output voltage	V_{OH}	4.5	4.4	4.5	—	4.4	—	V	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –20 µA
		4.5	4.18	4.31	—	4.13	—			I_{OH} = –2 mA
	V_{OL}	4.5	—	0.0	0.1	—	0.1			I_{OL} = 20 µA
		4.5	—	0.17	0.26	—	0.33			I_{OL} = 2 mA
Input current	I_{IN}	5.5	—	—	±0.1	—	±1.0	µA	V_{IN} = V_{CC} or GND	
Operating current	I_{CC}	5.5	—	—	1.0	—	10.0	µA	V_{IN} = V_{CC} or GND	
Quiescent supply current	I_{CCT}	5.5	—	—	2.0	—	2.9	mA	One input V_{IN} = 2.4 V, other input V_{CC} or GND	

Switching Characteristics

Item	Symbol	Ta = 25°C Min	Ta = 25°C Typ	Ta = 25°C Max	Unit	Test Conditions
Output rise / fall time	t_{TLH} t_{THL}	—	5	10	ns	Test circuit
Propagation delay time	t_{PLH}	—	6.9	12	ns	Test circuit
	t_{PHL}	—	9.8	17		

(C_L = 15 pF, t_r = t_f = 6 ns, V_{CC} = 5 V)

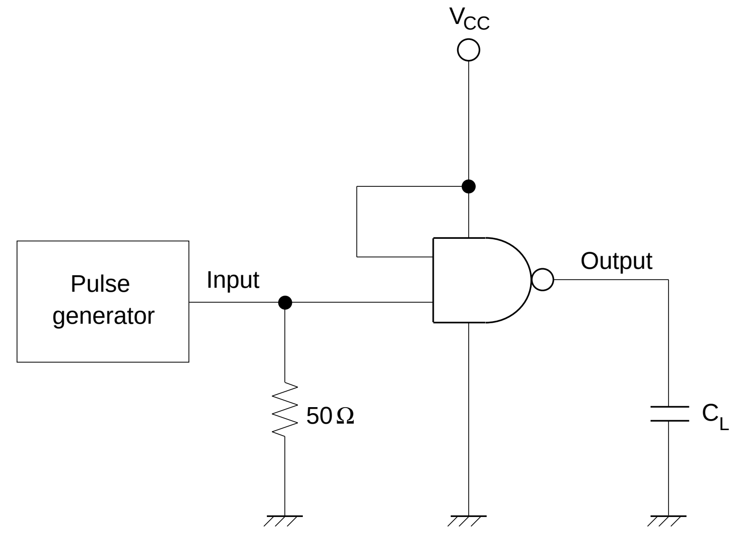
Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Ta = 25°C Typ	Ta = 25°C Max	Ta = –40 to 85°C Min	Ta = –40 to 85°C Max	Unit	Test Conditions
Output rise / fall time	t_{TLH} t_{THL}	4.5	—	14	25	—	31	ns	Test circuit
Propagation delay time	t_{PLH}	4.5	—	10.5	16	—	20	ns	Test circuit
	t_{PHL}	4.5	—	16.0	27	—	31		
Input capacitance	C_{IN}	—	—	2.5	5	—	5	pF	
Equivalent capacitance	C_{PD}	—	—	10	—	—	—	pF	

(C_L = 50 pF, t_r = t_f = 6 ns)

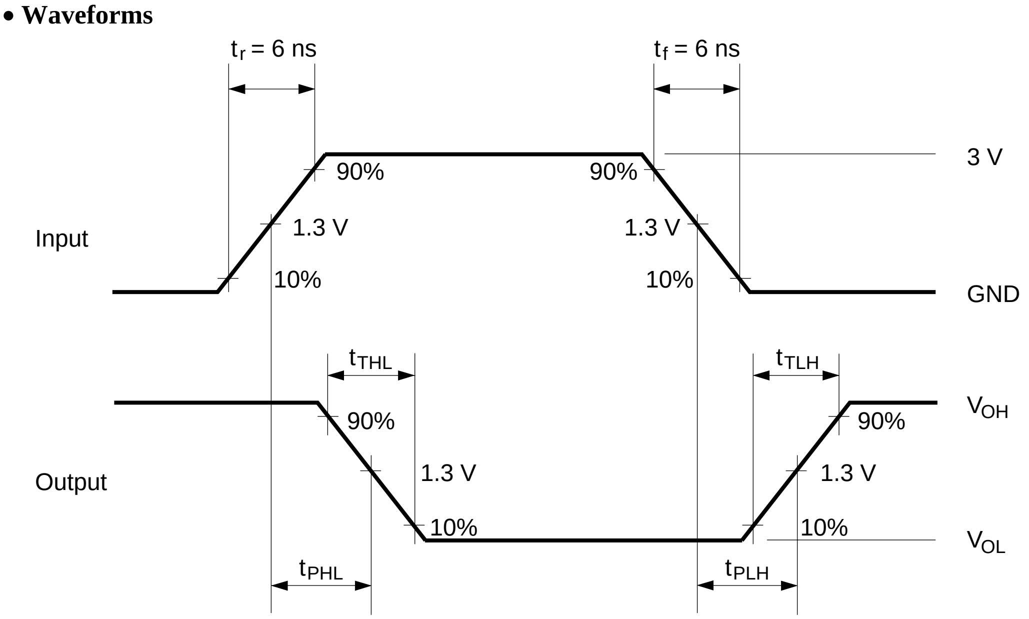
Note: C_{PD} is equivalent capacitance inside of the IC calculated from the operating current without load (see test circuit). The average operating current without load is calculated according to the expression below.

I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

Test Circuit

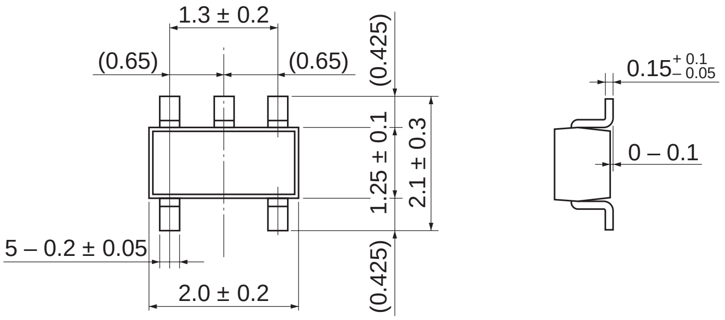


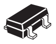
Note: 1. C_L includes probe and jig capacitance.

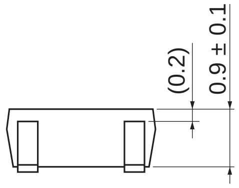


Package Dimensions

Unit: mm







Package Code	CMPAK–5V
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.006 g

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