
HD74HCT238

3-to-8-line Decoder/Demultiplexer

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Description

The HD74HCT238 has 3 binary select inputs (A, B, and C). If the device is enabled these inputs determined which one of the eight normally high outputs will go low. Two active low and one active high enables ($\overline{G_1}$, $\overline{G_{2A}}$ and $\overline{G_{2B}}$) are provided to ease the cascading of decoders.

Features

- LSTTL Output Logic Level Compatibility as well as CMOS Output Compatibility
- High Speed Operation: t_{pd} (A, B, C to Y) = 18.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 4.5$ to 5.5 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)

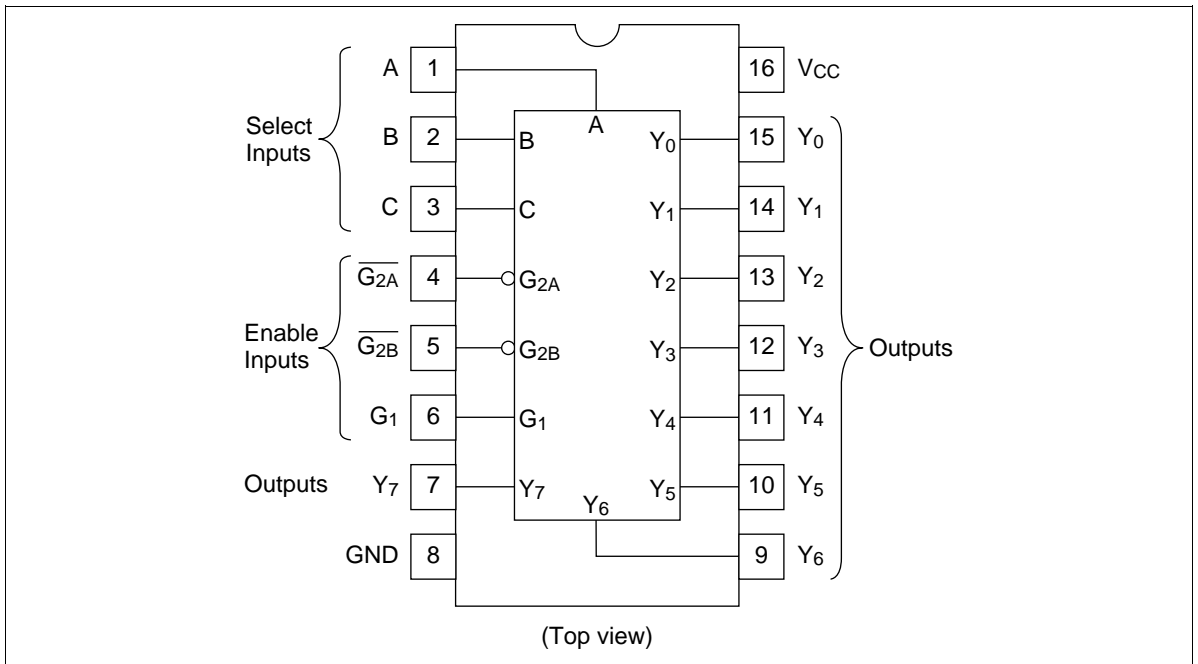
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Function Table

Inputs

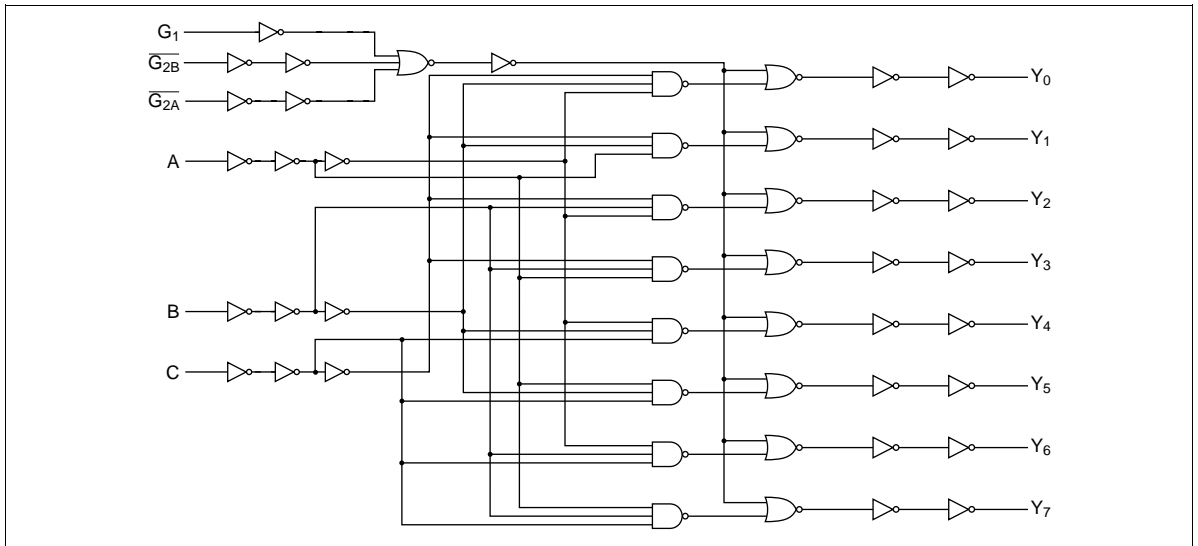
Enable			Select			Outputs							
G_1	$\overline{G_{2A}}$	$\overline{G_{2B}}$	C	B	A	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	L	H	L	L	L	L	L	H	L	L
H	L	L	H	H	L	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Pin Arrangement



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Logic Diagram



DC Characteristics

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions	
		Min	Typ	Max	Min		Max	V _{cc} (V)
Input voltage	V _{IH}	2.0	—	—	2.0	—	V	4.5 to 5.5
	V _{IL}	—	—	0.8	—	0.8	V	4.5 to 5.5
Output voltage	V _{OH}	4.4	—	—	4.4	—	V	4.5 Vin = V _{IH} or V _{IL} I _{OH} = -20 μA
		4.18	—	—	4.13	—		4.5 I _{OH} = -4 mA
	V _{OL}	—	—	0.1	—	0.1	V	4.5 Vin = V _{IH} or V _{IL} I _{OL} = 20 μA
		—	—	0.26	—	0.33		4.5 I _{OL} = 4 mA
Input current	I _{in}	—	—	±0.1	—	±1.0	μA	5.5 Vin = V _{CC} or GND
Quiescent supply current	I _{CC}	—	—	4.0	—	40	μA	5.5 Vin = V _{CC} or GND, I _{out} = 0 μA

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AC Characteristics ($C_L = 50$ pF, Input $t_r = t_f = 6$ ns)

Item	Symbol	Ta = 25°C		Ta = -40 to +85°C		Unit	Test Conditions		
		Min	Typ	Max	Min		Max	V _{cc} (V)	
Propagation delay time	t _{PLH}	—	18	30	—	38	ns	4.5	A, B or C to Y
	t _{PHL}	—	19	30	—	38		4.5	
	t _{PLH}	—	17	30	—	38	ns	4.5	\overline{G}_{2A} to Y
	t _{PHL}	—	17	30	—	39		4.5	
	t _{PLH}	—	17	30	—	38	ns	4.5	\overline{G}_{2B} to Y
	t _{PHL}	—	17	30	—	38		4.5	
	t _{PLH}	—	17	30	—	38	ns	4.5	G ₁ to Y
	t _{PHL}	—	17	30	—	38		4.5	
Output rise/fall time	t _{TLH}	—	5	15	—	19	ns	4.5	
	t _{THL}								
Input capacitance	C _{in}	—	5	10	—	10	pF	—	



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
 Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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