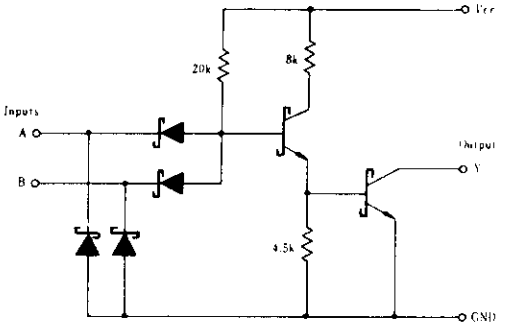
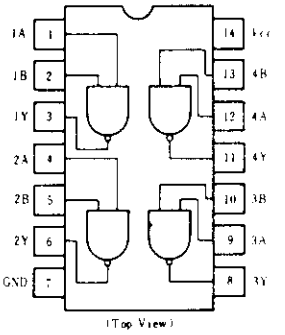
HD74LS03 ●Quadruple 2-input Positive NAND Gates (with Open Collector Outputs)

■CIRCUIT SCHEMATIC(¼)



■PIN ARRANGEMENT



■RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
High level output voltage	V_{OH}	–	–	5.5	V
Low level output current	I_{OL}	–	–	8	mA

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item	Symbol	Test Conditions		min	typ*	max	Unit
Input voltage	V_{IH}			2.0	–	–	V
	V_{IL}			–	–	0.8	V
Output voltage	V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$	$I_{OL}=8mA$	–	–	0.5	V
			$I_{OL}=4mA$	–	–	0.4	
Input current	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	I_{IL}	$V_{CC}=5.25V$ $V_I=0.4V$		–	–	−0.4	mA
	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
Output current	I_{OH}	$V_{CC}=4.75V$, $V_{IL}=0.8V$, $V_{OH}=5.5V$		–	–	100	μA
Supply current	I_{CCH}	$V_{CC}=5.25V$		–	0.8	1.6	mA
	I_{CCL}	$V_{CC}=5.25V$		–	2.4	4.4	mA
Input clamp voltage	V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

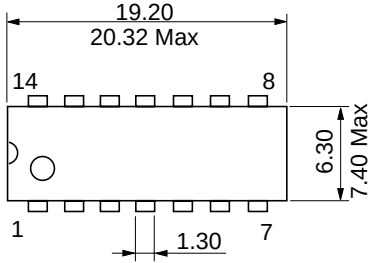
* $V_{CC}=5V$, $Ta=25°C$

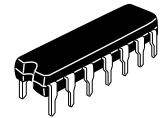
■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

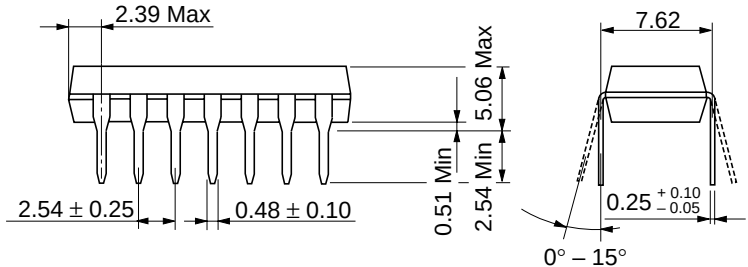
Item	Symbol	Test Conditions	min	typ	max	Unit
Propagation delay time	t_{PLH}	$C_L=15pF$, $R_L=2k\Omega$	–	17	32	ns
	t_{PHL}		–	15	28	ns

Note) Refer to Test Circuit and Waveform of the Common Item

Unit: mm

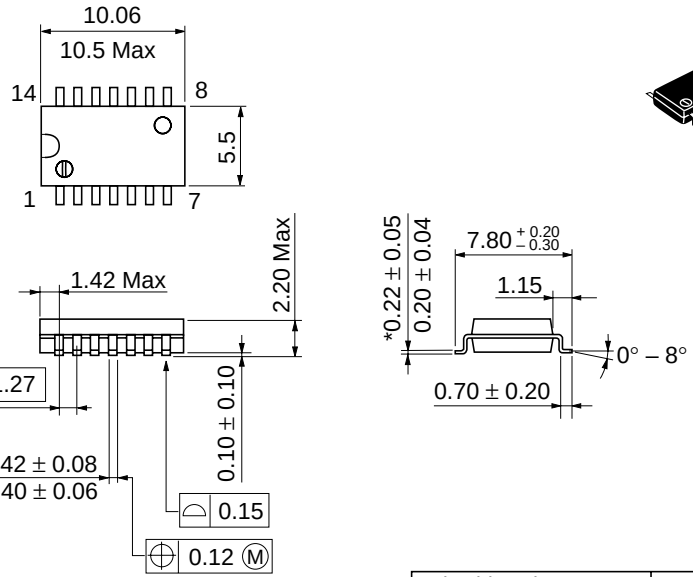


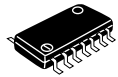




Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

Unit: mm

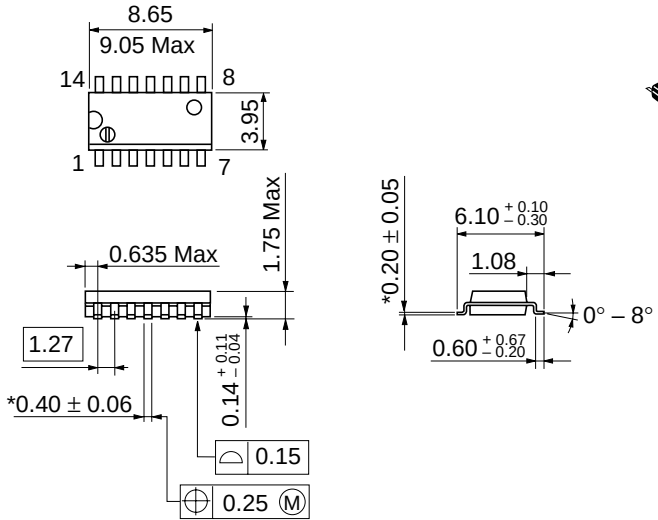




Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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