

# HD74LS112

## Dual J-K Negative-edge-triggered Flip-Flops (with Preset and Clear)

REJ03D0426-0300

Rev.3.00

Jul.13.2005

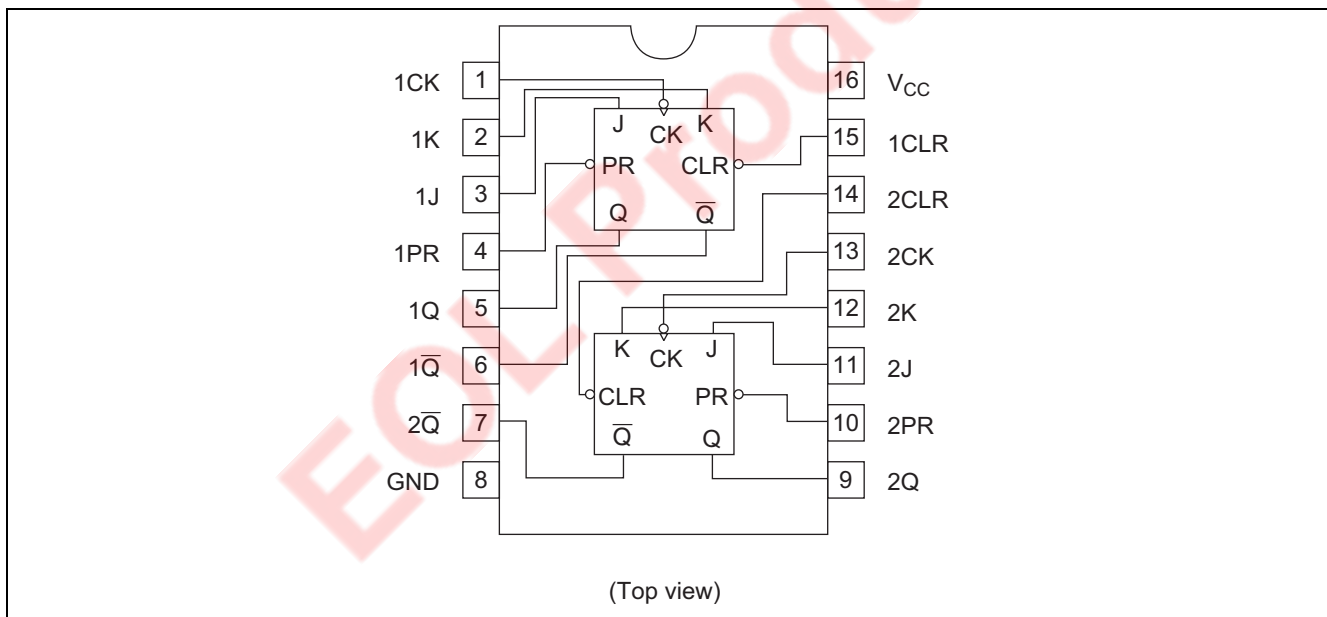
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS112P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS112FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)
HD74LS112RPEL	SOP-16 pin (JEDEC)	PRSP0016DG-A (FP-16DNV)	RP	EL (2,500 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



**Function Table**

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q <sub>0</sub>	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q <sub>0</sub>	$\bar{Q}_0$

Notes: H; high level, L; low level, X; irrelevant  
 ↓; transition from high to low level

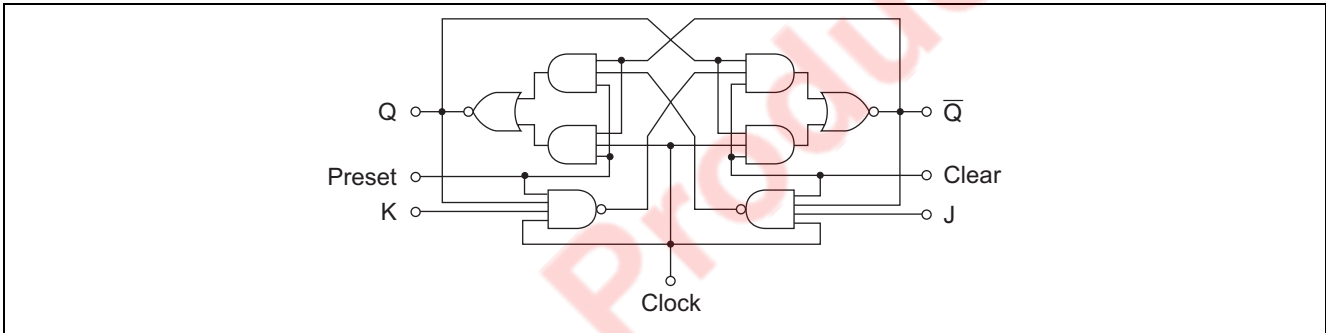
Q; level of Q before the indicated steady-state input conditions were established.

$\bar{Q}$ ; complement of Q<sub>0</sub> or level of  $\bar{Q}$  before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by ↓.

\*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

**Block Diagram (1/2)**



**Absolute Maximum Ratings**

Item	Symbol	Ratings	Unit
Supply voltage	V <sub>CC</sub>	7	V
Input voltage	V <sub>IN</sub>	7	V
Power dissipation	P <sub>T</sub>	400	mW
Storage temperature	T <sub>stg</sub>	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

### Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	$\mu A$
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	$^{\circ}C$
Clock frequency	$f_{clock}$	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Clear Preset Low	25	—	—	ns
Setup time	"H" Data	20 $\downarrow$	—	—	ns
	"L" Data	20 $\downarrow$	—	—	ns
Hold time	$t_h$	0 $\downarrow$	—	—	ns

### Electrical Characteristics

( $T_a = -20$  to  $+75$   $^{\circ}C$ )

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	$V_{IH}$	2.0	—	—	V		
	$V_{IL}$	—	—	0.8	V		
Output voltage	$V_{OH}$	2.7	—	—	V	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V, $I_{OH} = -400$ $\mu A$	
	$V_{OL}$	—	—	0.5	V		$I_{OL} = 8$ mA
—		—	0.4	$V_{CC} = 4.75$ V, $V_{IH} = 2$ V, $V_{IL} = 0.8$ V		$I_{OL} = 4$ mA	
Input current	J, K Clear Preset Clock	$I_{IH}$	—	—	20	$\mu A$	$V_{CC} = 5.25$ V, $V_I = 2.7$ V
			—	—	60		
			—	—	60		
			—	—	80		
	J, K Clear Preset Clock	$I_{IL}^{**}$	—	—	-0.4	mA	$V_{CC} = 5.25$ V, $V_I = 0.4$ V
			—	—	-0.8		
			—	—	-0.8		
			—	—	-0.8		
	J, K Clear Preset Clock	$I_I$	—	—	0.1	mA	$V_{CC} = 5.25$ V, $V_I = 7$ V
			—	—	0.3		
			—	—	0.3		
			—	—	0.4		
Short-circuit output current	$I_{OS}$	-20	—	-100	mA	$V_{CC} = 5.25$ V	
Supply current***	$I_{CC}$	—	4	8	mA	$V_{CC} = 5.25$ V	
Input clamp voltage	$V_{IK}$	—	—	-1.5	V	$V_{CC} = 4.75$ V, $I_{IN} = -18$ mA	

Notes: \*  $V_{CC} = 5$  V,  $T_a = 25^{\circ}C$

\*\*  $I_{IL}$  should not be measured when preset and clear inputs are low at same time.

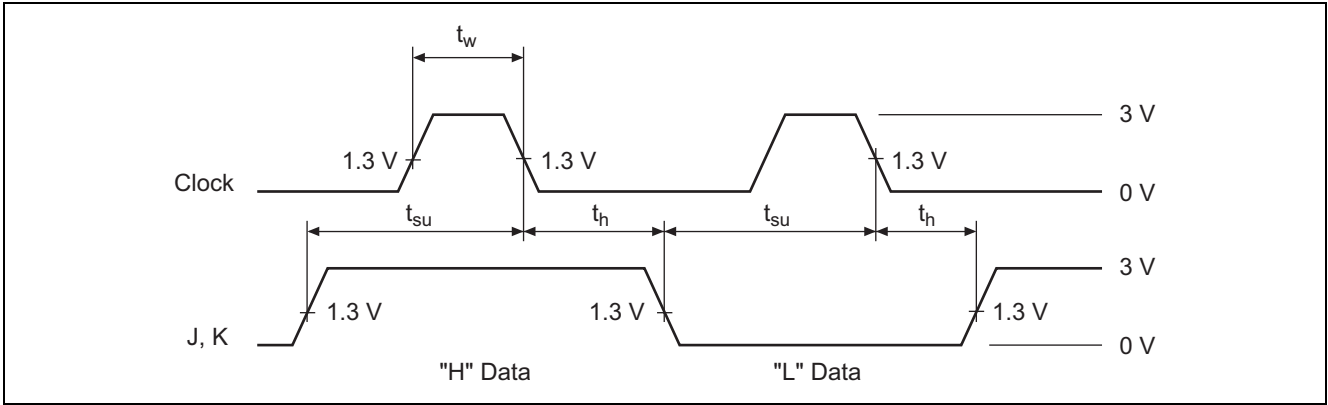
\*\*\* With all outputs open,  $I_{CC}$  is measured with the Q and  $\bar{Q}$  outputs high in turn. At the tires of measurement, the clock input is grounded.

### Switching Characteristics

( $V_{CC} = 5$  V,  $T_a = 25^{\circ}C$ )

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum clock frequency	$f_{max}$			30	45	—	MHz	$C_L = 15$ pF, $R_L = 2$ k $\Omega$
Propagation delay time	$t_{PLH}$	Clear	Q, $\bar{Q}$	—	11	20	ns	
	$t_{PHL}$	Preset Clock		—	15	30	ns	

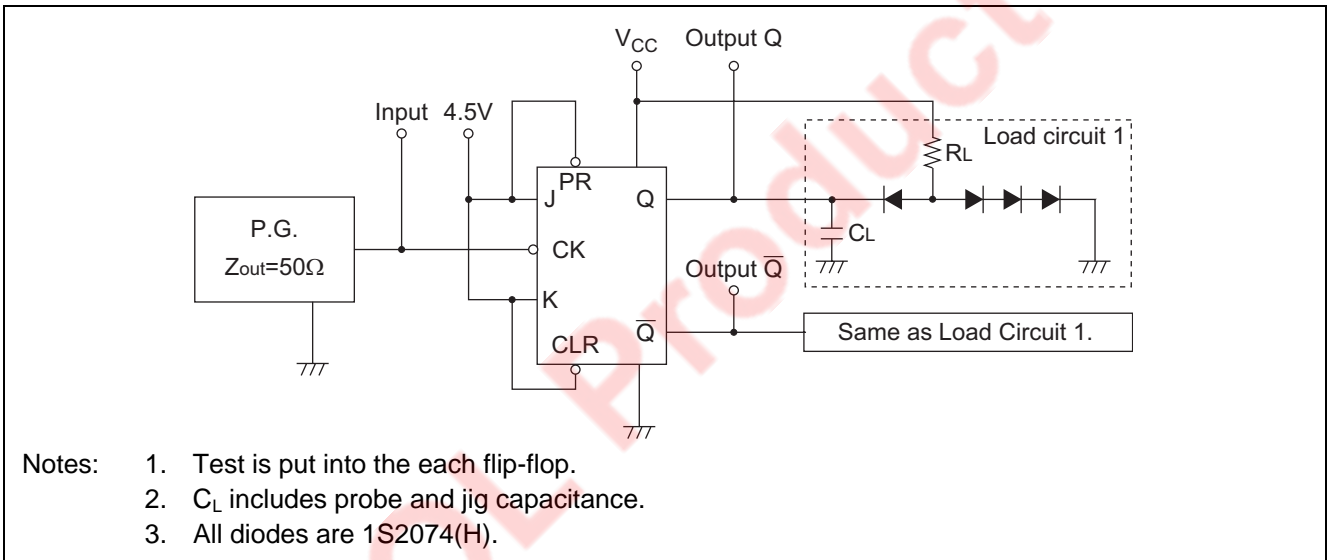
**Timing Definition**



**Testing Method**

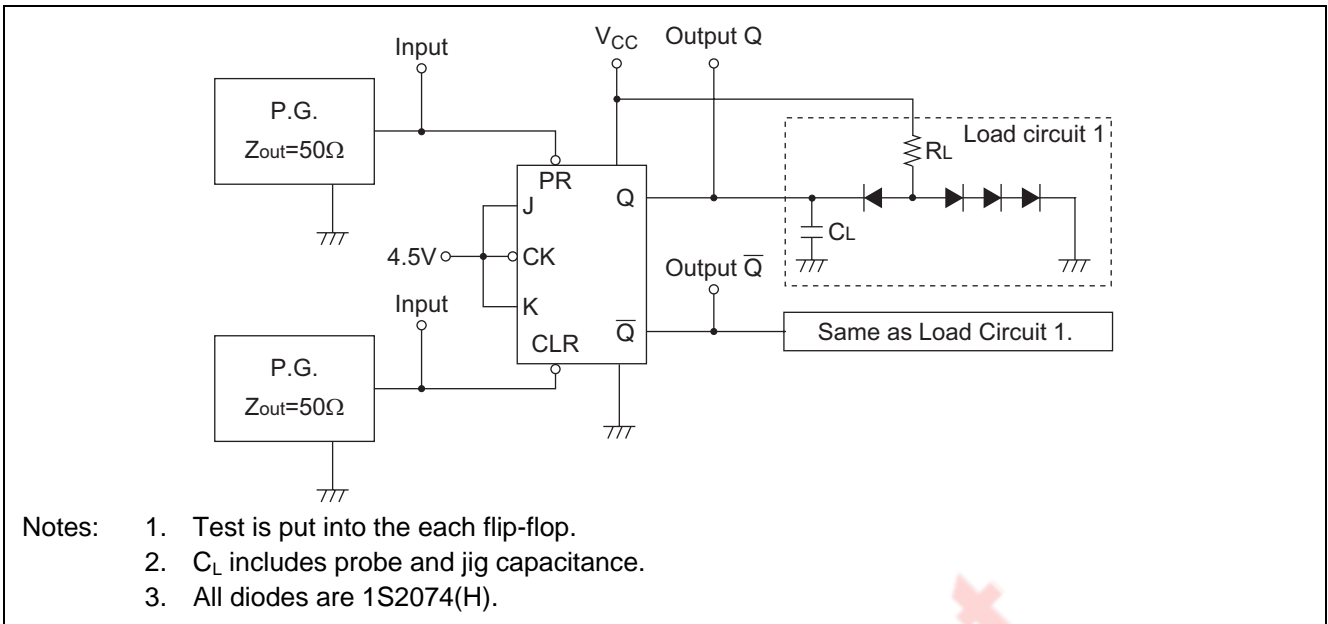
**Test Circuit**

1.  $f_{max}$ ,  $t_{PLH}$ ,  $t_{PHL}$ , (Clock  $\rightarrow$  Q,  $\bar{Q}$ )

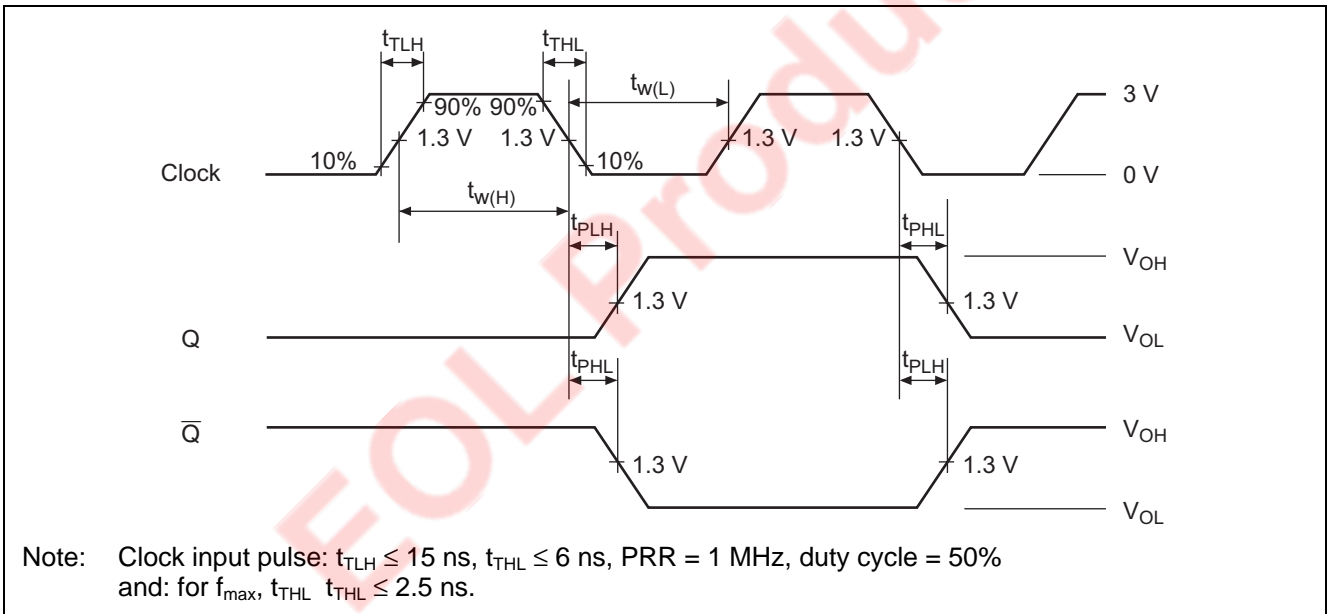


- Notes:
1. Test is put into the each flip-flop.
  2.  $C_L$  includes probe and jig capacitance.
  3. All diodes are 1S2074(H).

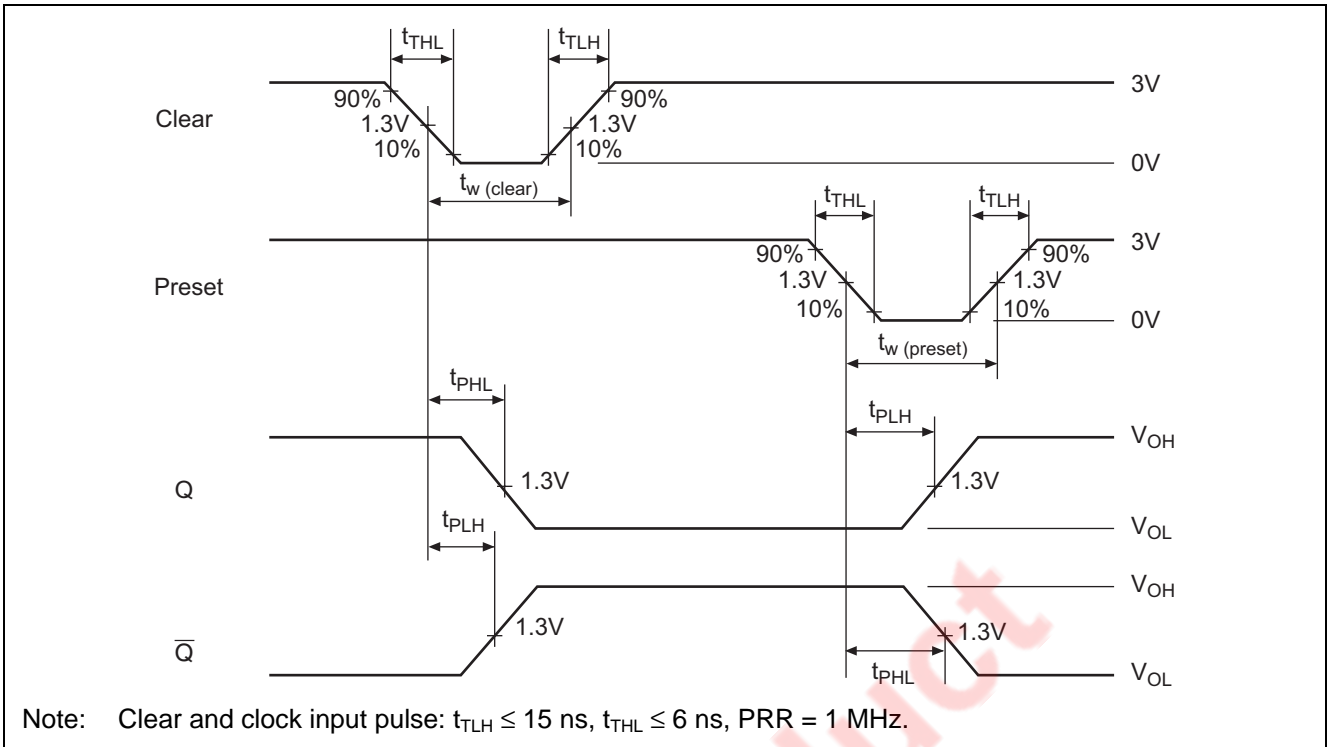
2.  $t_{PHL}$ ,  $t_{PLH}$ , (Clear, Preset  $\rightarrow$  Q,  $\bar{Q}$ )



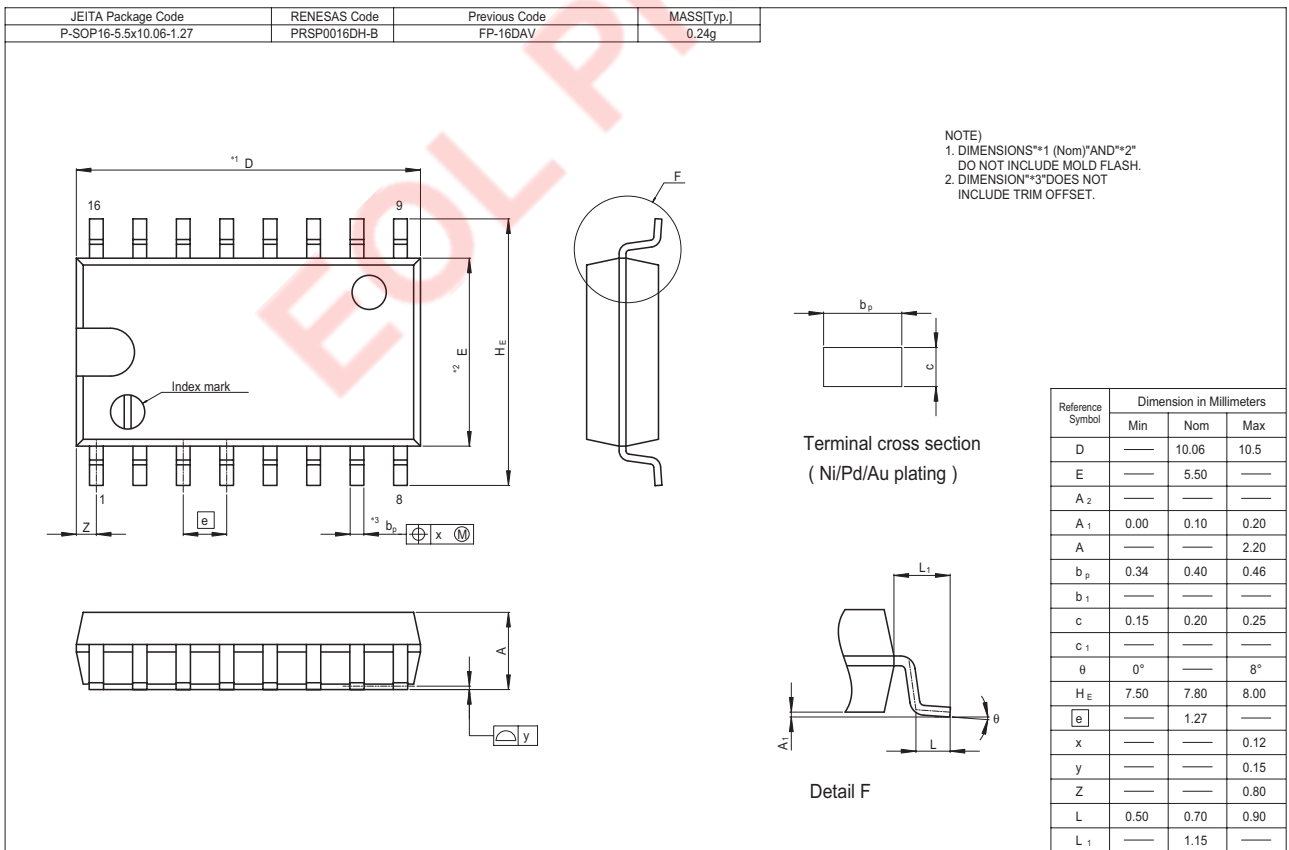
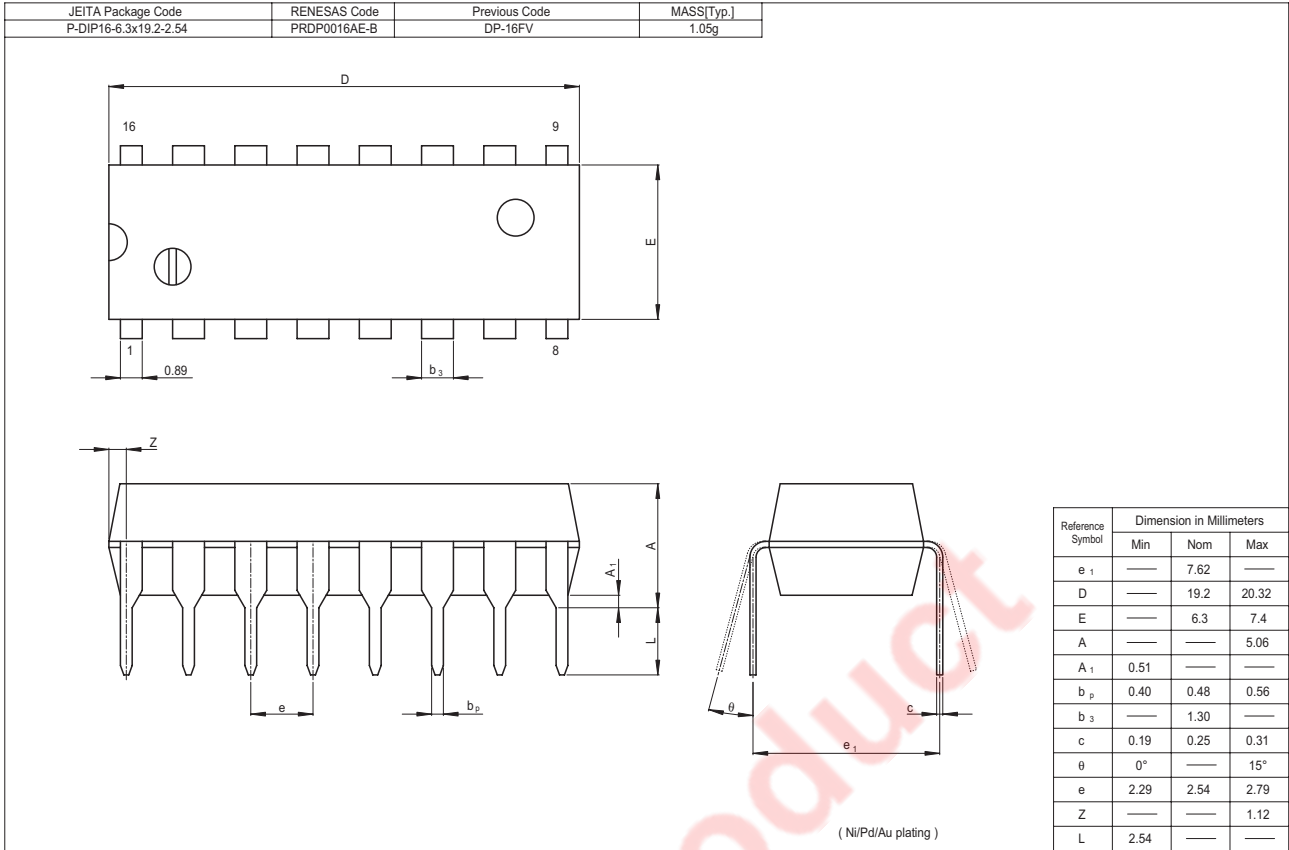
Waveforms 1



Waveforms 2

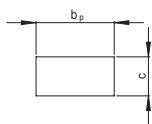
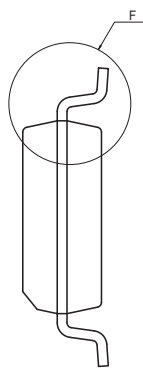
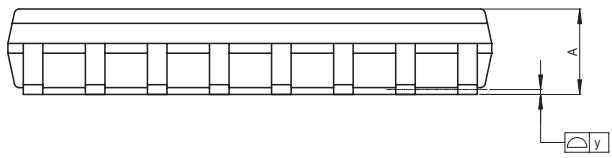
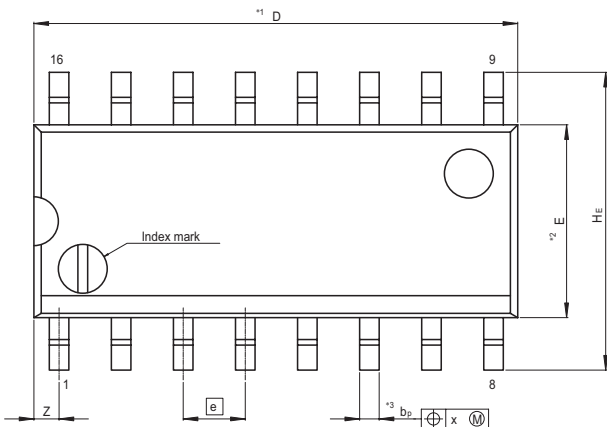


Package Dimensions

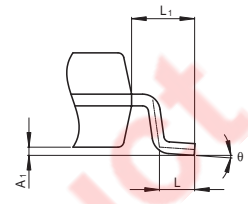


# HD74LS112

JEITA Package Code P-SOP16-3.95x9.9-1.27	RENESAS Code PRSP0016DG-A	Previous Code FP-16DNV	MASS[Typ.] 0.15g
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Terminal cross section  
( Ni/Pd/Au plating )



Detail F

NOTE)  
1. DIMENSIONS  $^{*1}$  (Nom)  $^{*2}$  AND  $^{*3}$   
DO NOT INCLUDE MOLD FLASH.  
2. DIMENSION  $^{*3}$  DOES NOT  
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.90	10.30
E	—	3.95	—
A <sub>2</sub>	—	—	—
A <sub>1</sub>	0.10	0.14	0.25
A	—	—	1.75
b <sub>p</sub>	0.34	0.40	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
$\theta$	0°	—	8°
H <sub>E</sub>	5.80	6.10	6.20
e	—	1.27	—
x	—	—	0.25
y	—	—	0.15
Z	—	—	0.635
L	0.40	0.60	1.27
L <sub>1</sub>	—	1.08	—

EOL Product



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