

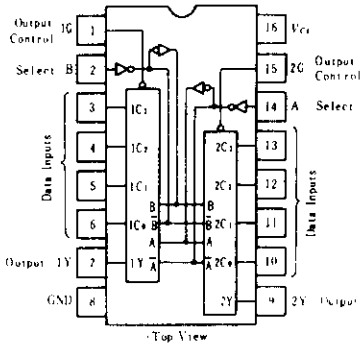
HD74LS253

●Dual 4-line-to-1-line Data Selectors/Multiplexers (with three-state outputs)

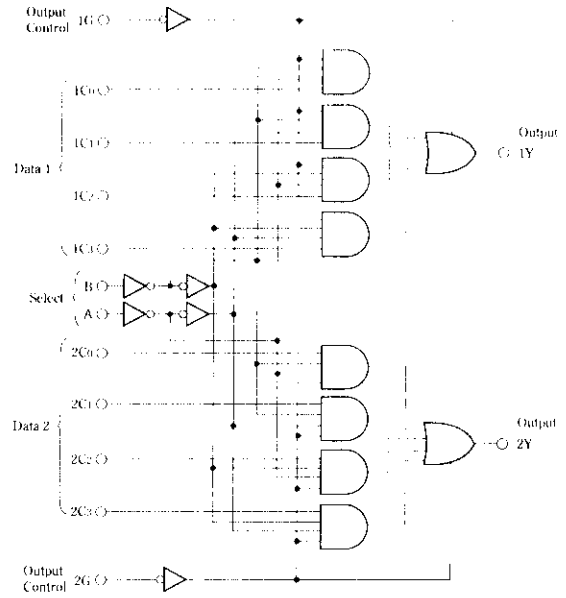
This data selector/multiplexer contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to AND-OR gates.

Separate output control inputs are provided for each of the two four-line sections. The three-state outputs can interface with and drive data lines of bus-organized systems. With all but one of the common outputs disabled (at high-impedance state) the low-impedance of the single enabled output will drive the bus line to a high or low logic level.

■PIN ARRANGEMENT



■BLOCK DIAGRAM



■FUNCTION TABLE

Select inputs		Data inputs				Output control	Output
B	A	C ₀	C ₁	C ₂	C ₃	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

- Notes) 1. H; high level, L; low level, X; irrelevant
 2. Address inputs A and B are common to both sections.

■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7.0	V
Input voltage	V_{IN}	7.0	V
Output voltage (off-state)	$V_{O(off)}$	5.5	V
Operating temperature range	T_{OP}	-20 ~ +75	°C
Storage temperature range	T_{STG}	-65 ~ +150	°C

■ ELECTRICAL CHARACTERISTICS ($T_a = -20 \sim +75^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V_{IH}		2.0	—	—	V	
	V_{IL}		—	—	0.8	V	
Output voltage	V_{OH}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}, I_{OH}=-2.6\text{mA}$	2.4	—	—	V	
	V_{OL}	$V_{CC}=4.75\text{V}, V_{IH}=2\text{V}, V_{IL}=0.8\text{V}$					
					0.4	V	
					0.5		
Input current	I_{IH}	$V_{CC}=5.25\text{V}, V_I=2.7\text{V}$	—	—	20	μA	
	I_{IL}	$V_{CC}=5.25\text{V}, V_I=0.4\text{V}$	—	—	-0.4	mA	
	I_I	$V_{CC}=5.25\text{V}, V_I=7\text{V}$	—	—	0.1	mA	
Output current	I_{OZ}	$V_{CC}=5.25\text{V}, V_{IH}=2\text{V}$	$V_O=2.7\text{V}$	—	—	20	μA
			$V_O=0.4\text{V}$	—	—	-20	
Short-circuit output current	I_{OS}	$V_{CC}=5.25\text{V}$	-30	—	-130	mA	
Supply current**	I_{CC}	$V_{CC}=5.25\text{V}$	Condition A	—	7	12	mA
			Condition B	—	8.5	14	
Input clamp voltage	V_{IK}	$V_{CC}=4.75\text{V}, I_{IN}=-18\text{mA}$	—	—	-1.5	V	

* $V_{CC}=5\text{V}, T_a=25^\circ\text{C}$

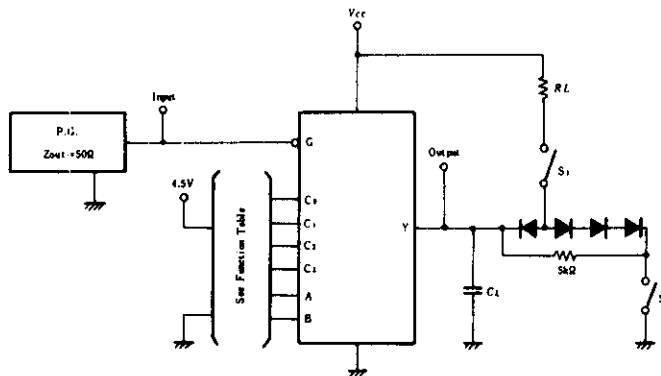
** I_{CC} is measured with the outputs open under the following conditions: A. All inputs grounded, B. Output control at 4.5V, all inputs grounded.

■ SWITCHING CHARACTERISTICS ($V_{CC}=5\text{V}, T_a=25^\circ\text{C}$)

Item	Inputs	Output	Symbol	Test Conditions	min	typ	max	Unit	
Propagation delay time	Data	Y	t_{PLH}	$C_L=15\text{pF}$ $R_L=2\text{k}\Omega$	—	17	25	ns	
			t_{PHL}		—	13	20		
	Select	Y	t_{PLH}		—	30	45		
			t_{PHL}		—	21	32		
Output enable time	Output Control	Y	t_{ZH}	$C_L=5\text{pF}$ $R_L=2\text{k}\Omega$	—	15	28	ns	
			t_{ZL}		—	15	23		
Output disable time	Output Control	Y	t_{HZ}		$C_L=5\text{pF}$ $R_L=2\text{k}\Omega$	—	27	41	ns
			t_{LZ}			—	18	27	

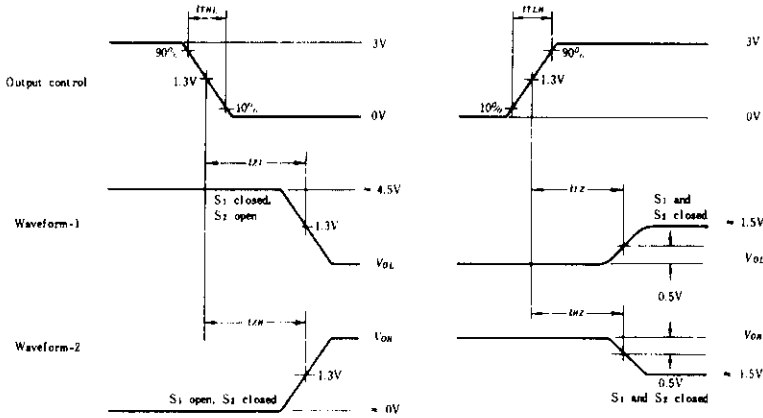
■ TESTING METHOD

1) Test Circuit

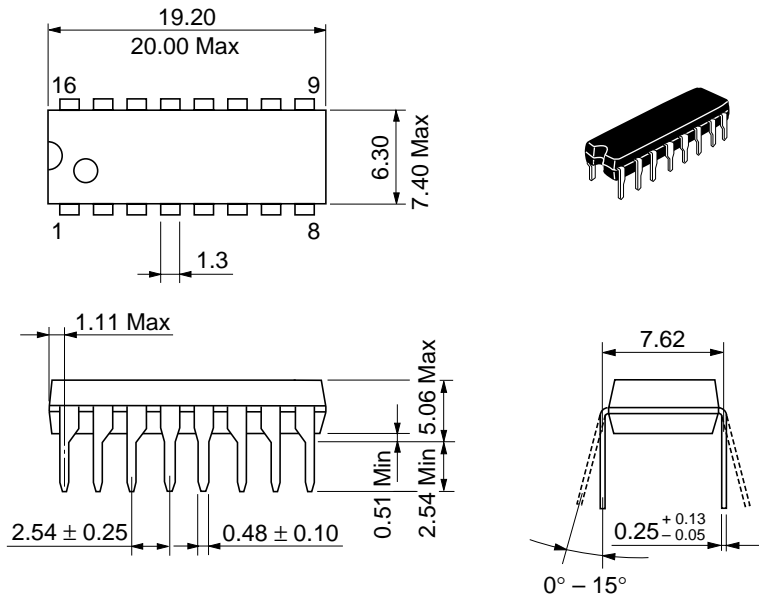


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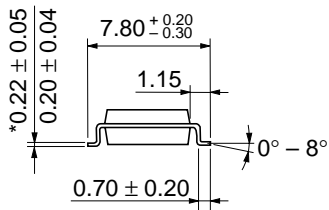
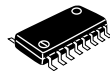
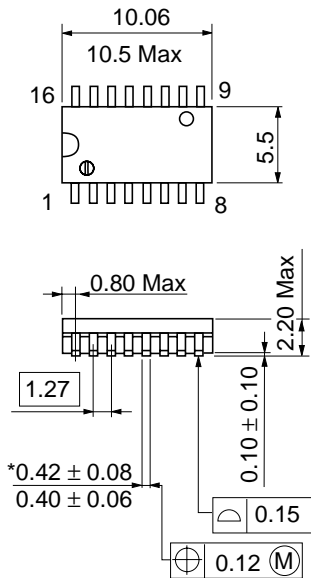
Waveform



- Notes)
1. Input pulse: $t_{TLH} \leq 15\text{ns}$, $t_{THL} \leq 6\text{ns}$, $PRR=1\text{MHz}$, duty cycle = 50%.
 2. C_L includes probe and jig capacitance.
 3. All diodes are 1S2074 (G).
 4. Waveform-1 is for an output with internal conditions such that the output is low except when disabled by the output control.
 5. Waveform-2 is for an output with internal conditions such that the output is high except when disabled by the output control.

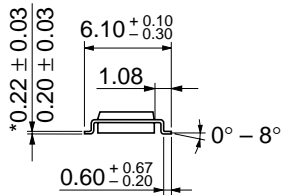
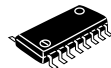
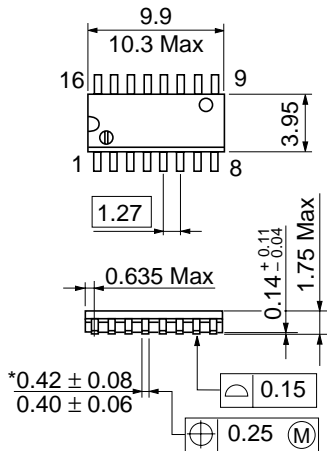


Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

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