HD74LS283

4-bit Binary Full Adder

REJ03D0476–0300
Rev.3.00
Jul.15.2005

The HD74LS283 adder is electrically and functionally identical to the HD74LS83A, respectively; only the arrangement of the terminals has been changed.

This improved full adder performs the addition of two 4-bit binary words.

The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bits generating the carry term in then nanoseconds.

The adder logic, including the carry, is implemented in its true form.

End around carry can be accomplished without the need for logic or level inversion.

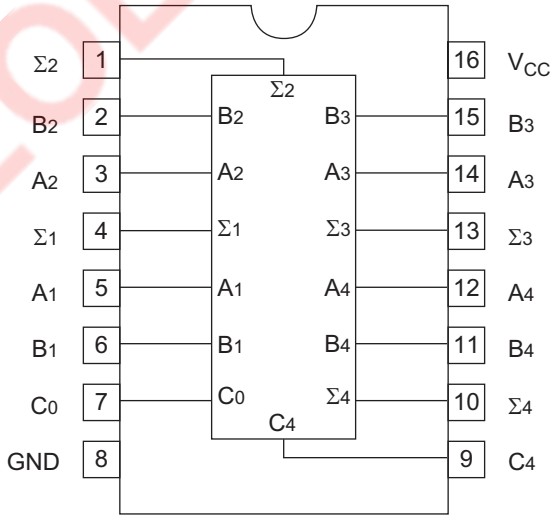
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS283P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS283FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



(Top view)

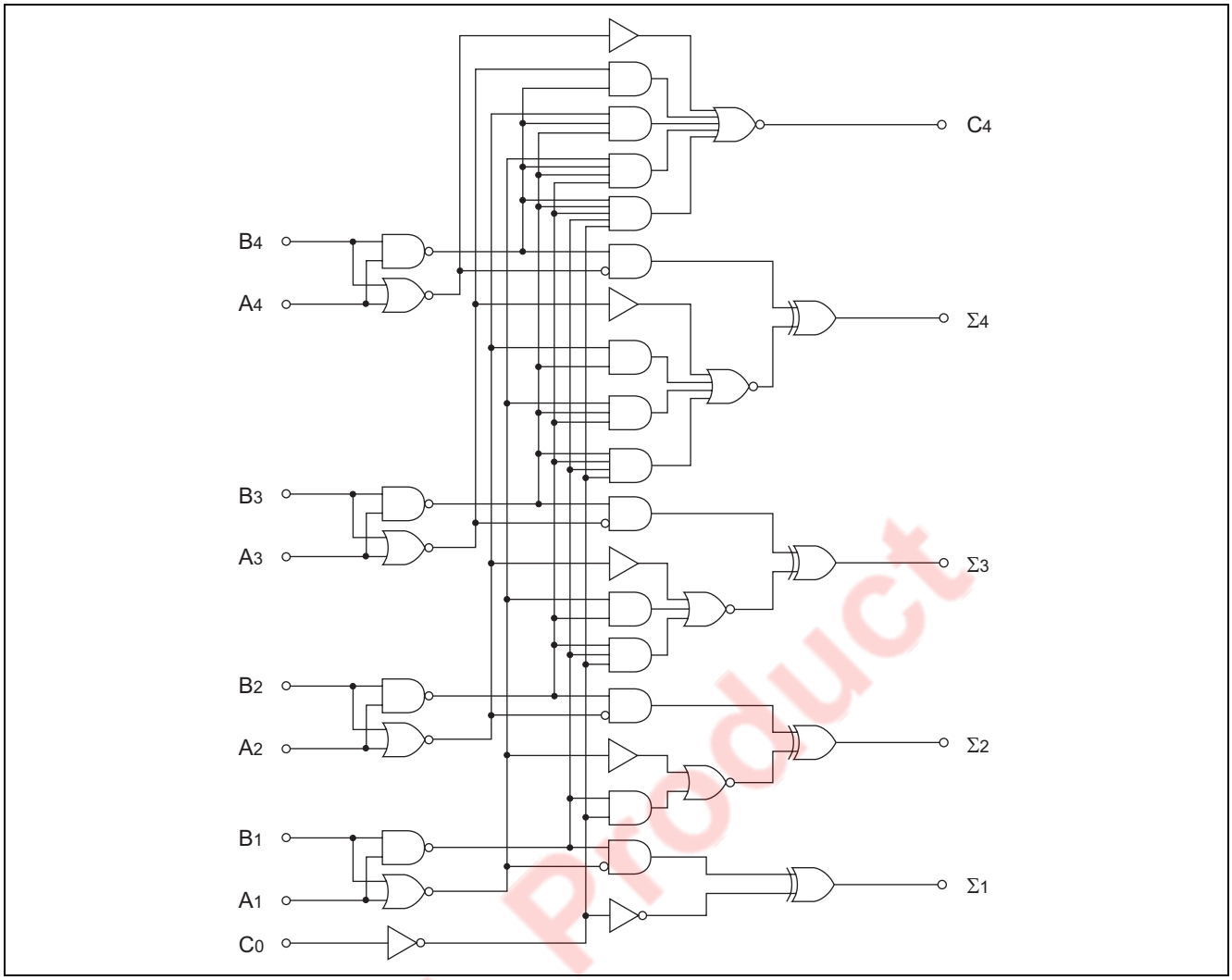
Function Table

Inputs				Outputs					
				When C_0 = L			When C_0 = H		
				When C_2 = L			When C_2 = H		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H; high level, L; low level

Note: Input conditions at A_1, B_1, A_2, B_2, and $C_0$are use to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4 are then used to determine outputs Σ_3, Σ_4, and C_4.

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.75	5.00	5.25	V
Output current	I_{OH}	—	—	–400	µA
	I_{OL}	—	—	8	mA
Operating temperature	Topr	–20	25	75	°C

Electrical Characteristics

(Ta = –20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V_{IH}	2.0	—	—	V		
		V_{IL}	—	—	0.8	V		
Output voltage		V_{OH}	2.7	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –400 µA	
		V_{OL}	—	—	0.4	V	I_{OL} = 4 mA	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
			—	—	0.5		I_{OL} = 8 mA	
Input current	except C_0	I_{IH}	—	—	40	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	C_0		—	—	20			
	except C_0	I_{IL}	—	—	–0.8	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	C_0		—	—	–0.4			
	except C_0	I_I	—	—	0.2	mA	V_{CC} = 5.25 V, V_I = 7 V	
	C_0		—	—	0.1			
Short-circuit output current		I_{OS}	–20	—	–100	mA	V_{CC} = 5.25 V	
Supply current		I_{CC}	—	22	39	mA	All inputs grounded	V_{CC} = 5.25 V
			—	19	34		All B low other inputs at 4.5V	
			—	19	34		All inputs at 4.5V	
Input clamp voltage		V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Note: * V_{CC} = 5 V, Ta = 25°C

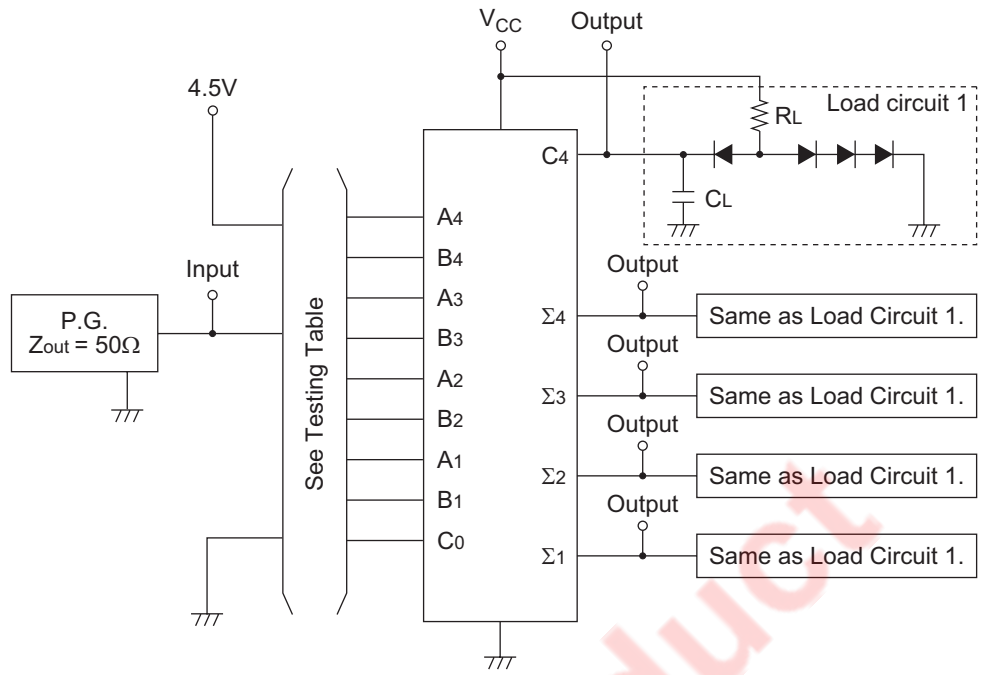
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Propagation delay time	t_{PLH}	C_0	Σi	—	16	24	ns	C_L = 15 pF, R_L = 2 kΩ
	t_{PHL}			—	15	24	ns	
	t_{PLH}	Ai, Bi	Σi	—	15	24	ns	
	t_{PHL}			—	15	24	ns	
	t_{PLH}	C_0	C_4	—	11	17	ns	
	t_{PHL}			—	11	22	ns	
	t_{PLH}	Ai, Bi	C_4	—	11	17	ns	
	t_{PHL}			—	12	17	ns	

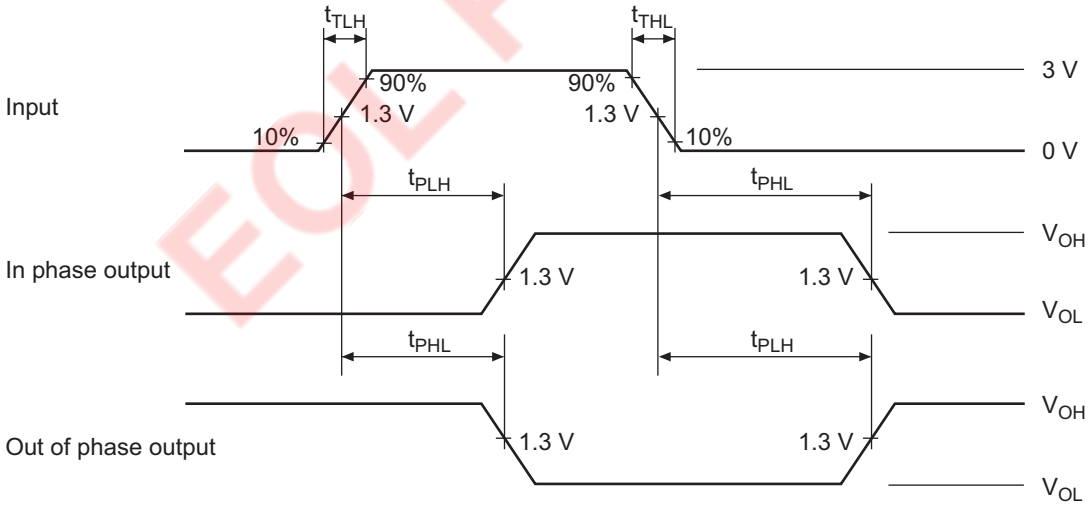
Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

Waveform



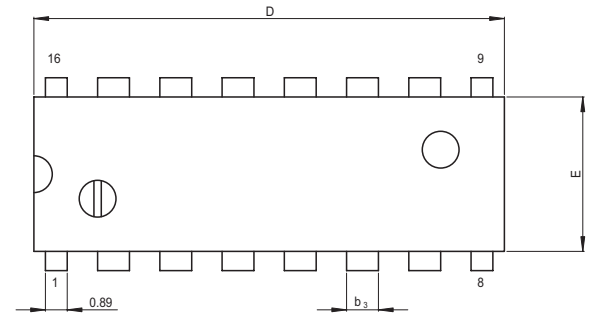
Notes: Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%.

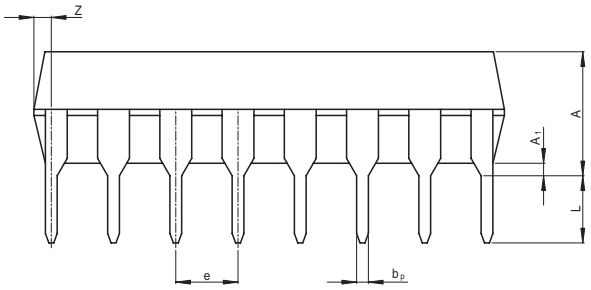
Testing Table

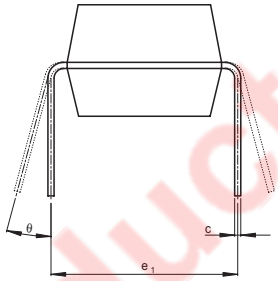
Item	From input to output	Inputs									Outputs				
		B_4	A_4	B_3	A_3	B_2	A_2	B_1	A_1	C_0	C_4	Σ_4	Σ_3	Σ_2	Σ_1
t_{PLH} t_{PHL}	$C_0 \rightarrow \Sigma i$ or C_4	GND	GND	GND	GND	GND	GND	GND	GND	IN	—	—	—	—	OUT
		GND	4.5V	GND	4.5V	GND	4.5V	GND	4.5V	IN	OUT	OUT	OUT	OUT	OUT
	Ai or Bi $\rightarrow \Sigma i$ or C_4	GND	GND	GND	GND	GND	GND	GND	IN	GND	—	—	—	—	OUT
								IN	GND						
		GND	GND	GND	GND	GND	IN	GND	GND	GND	—	—	—	OUT	—
						IN	GND								
		GND	GND	GND	IN	GND	GND	GND	GND	GND	—	—	OUT	—	—
				IN	GND										
		GND	IN	GND	GND	GND	GND	GND	GND	GND	—	OUT	—	—	—
		IN	GND												
		GND	GND	GND	GND	GND	GND	4.5V	IN	GND	—	—	—	OUT	OUT
								IN	4.5V						
		GND	GND	GND	GND	4.5V	IN	GND	GND	GND	—	—	OUT	OUT	—
						IN	4.5V								
		GND	GND	4.5V	IN	GND	GND	GND	GND	GND	—	OUT	OUT	—	—
				IN	4.5V										
		4.5V	IN	GND	GND	GND	GND	GND	GND	GND	OUT	OUT	—	—	—
		IN	4.5V												

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP16-6.3x19.2-2.54	PRDP0016AE-B	DP-16FV	1.05g



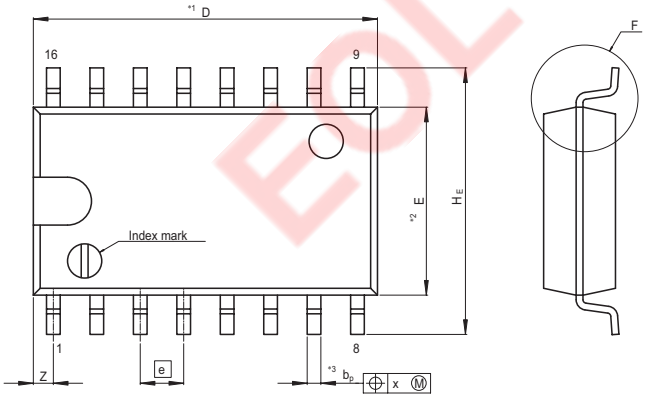


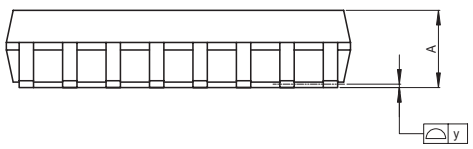


(Ni/Pd/Au plating)

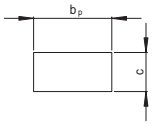
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	19.2	20.32
E	——	6.3	7.4
A	——	——	5.06
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.12
L	2.54	——	——

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP16-5.5x10.06-1.27	PRSP0016DH-B	FP-16DAV	0.24g

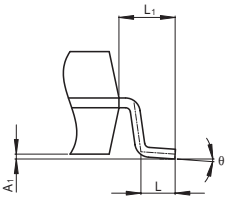




NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	10.06	10.5
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

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