HD74LS374

Octal D-type Edge-triggered Flip-Flops (with three-state outputs)

REJ03D0483–0200
Rev.2.00
Feb.18.2005

The HD74LS374, 8-bit register features totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide this register with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers. The eight flip-flops are edge-triggered D-type flip-flops. On the positive transition the clock, the Q outputs will be set to the logic states that ware setup at the D inputs.

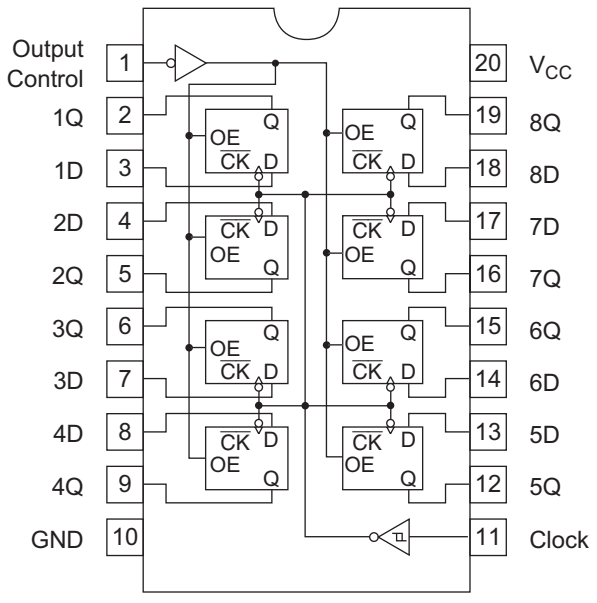
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS374P	DILP-20 pin	PRDP0020AC-B (DP-20NEV)	P	—
HD74LS374FPEL	SOP-20 pin (JEITA)	PRSP0020DD-B (FP-20DAV)	FP	EL (2,000 pcs/reel)
HD74LS374RPEL	SOP-20 pin (JEDEC)	PRSP0020DC-A (FP-20DBV)	RP	EL (1,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



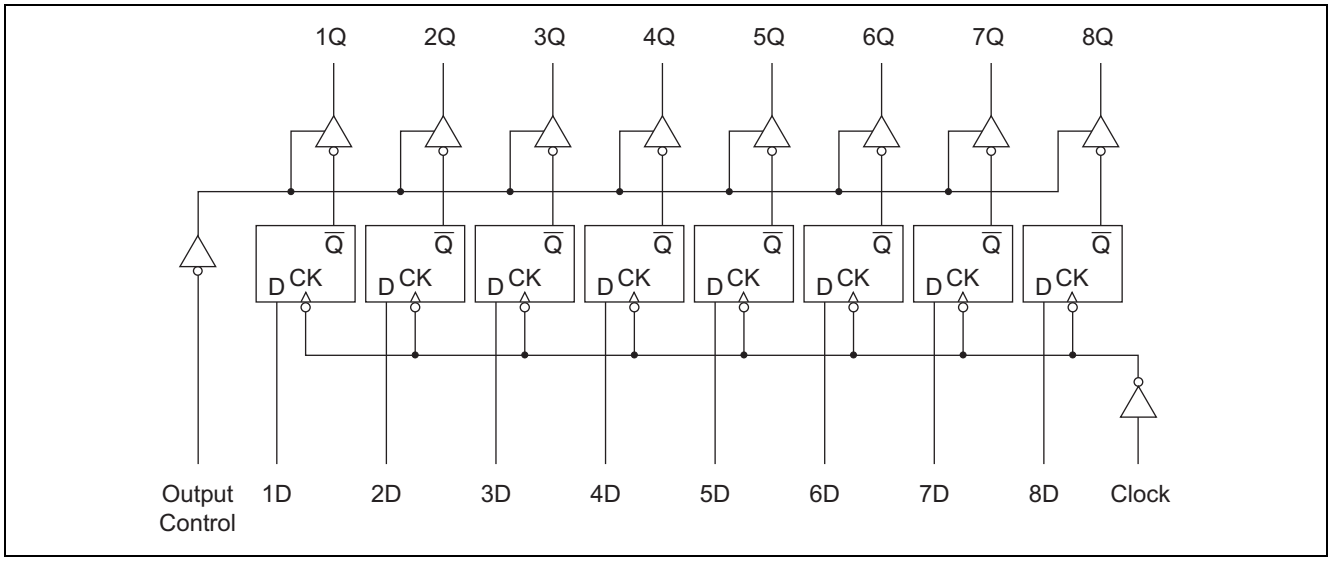
(Top view)

Function Table

Inputs			Outputs
Output control	**Clock**	**D**	**Q**
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Notes: H; high level, L; low level, X; irrelevant
↑; transition from low to high level
Q_0; level of Q before the indicated steady state input conditions were established
Z; off (high-impedance) state of a three state output

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V_{CC}	7	V
Input voltage	V_{IN}	7	V
Power dissipation	P_T	400	mW
Storage temperature	Tstg	–65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output voltage		V_{OH}	—	—	5.5	V
Output current		I_{OH}	—	—	–2.6	mA
		I_{OL}	—	—	24	mA
Operating temperature		Topr	–20	25	75	°C
Clock pulse width	“H” Level	t_w	15	—	—	ns
	“L” Level		15	—	—	ns
Data setup time		t_{su}	20↑	—	—	ns
Data hold time		t_h	0↑	—	—	ns

Electrical Characteristics

(Ta = –20 to +75 °C)

Item	Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage	V_{IH}	2.0	—	—	V		
	V_{IL}	—	—	0.8	V		
Output voltage	V_{OH}	2.4	—	—	V	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = –2.6 mA	
	V_{OL}	—	—	0.4	V	I_{OL} = 12 mA	V_{CC} = 4.75 V, V_{IH} = 2 V, V_{IL} = 0.8 V
		—	—	0.5		I_{OL} = 24 mA	
Output current	I_{OZH}	—	—	20	µA	V_O = 2.7 V	V_{CC} = 5.25 V, V_{IH} = 2 V, V_{IL} = 0.8 V
	I_{OZL}	—	—	–20		V_O = 0.4 V	
Input current	I_{IH}	—	—	20	µA	V_{CC} = 5.25 V, V_I = 2.7 V	
	I_{IL}	—	—	–0.4	mA	V_{CC} = 5.25 V, V_I = 0.4 V	
	I_I	—	—	0.1	mA	V_{CC} = 5.25 V, V_I = 7 V	
Short-circuit output current	I_{OS}	–30	—	–130	mA	V_{CC} = 5.25 V	
Supply current	I_{CC}	—	27	40	mA	V_{CC} = 5.25 V, V_I = 4.5 V (Output control)	
Input clamp voltage	V_{IK}	—	—	–1.5	V	V_{CC} = 4.75 V, I_{IN} = –18 mA	

Note: * V_{CC} = 5 V, Ta = 25°C

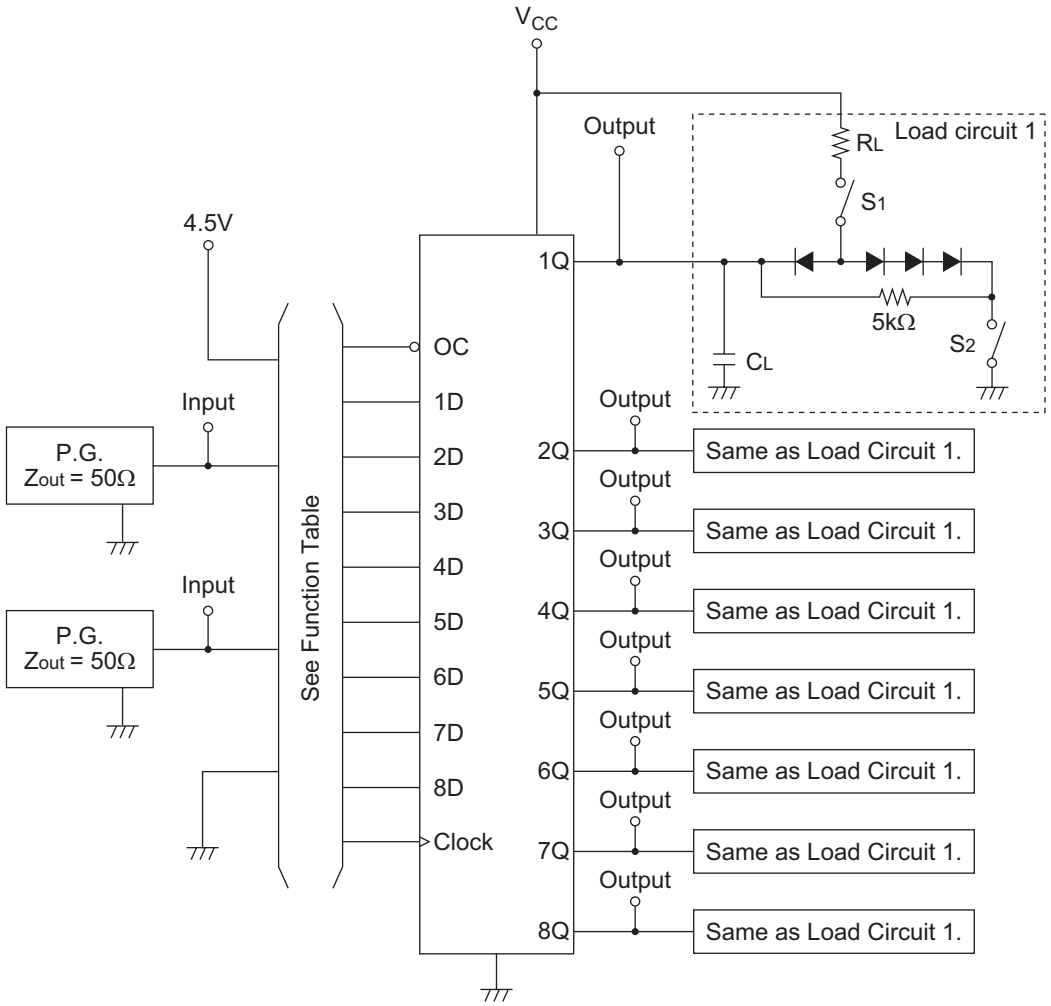
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Output	min.	typ.	max.	Unit	Condition
Maximum clock frequency	f_{max}	Clock	Q	35	50	—	MHz	C_L = 45 pF, R_L = 667 Ω
Propagation delay time	t_{PLH}	Clock	Q	—	15	28	ns	
	t_{PHL}			—	19	28		
Output enable time	t_{ZH}	OC	Q	—	20	28		
	t_{ZL}			—	21	28		
Output disable time	t_{HZ}	OC	Q	—	12	20		C_L = 5 pF, R_L = 667 Ω
	t_{LZ}			—	14	25		

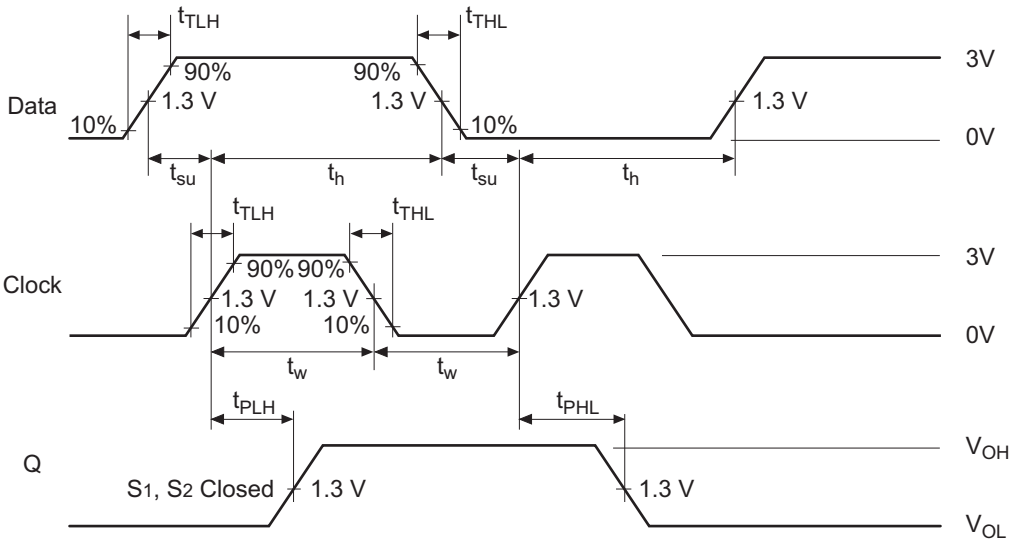
Testing Method

Test Circuit



Notes: 1. C_L includes probe and jig capacitance.
2. All diodes are 1S2074(H).

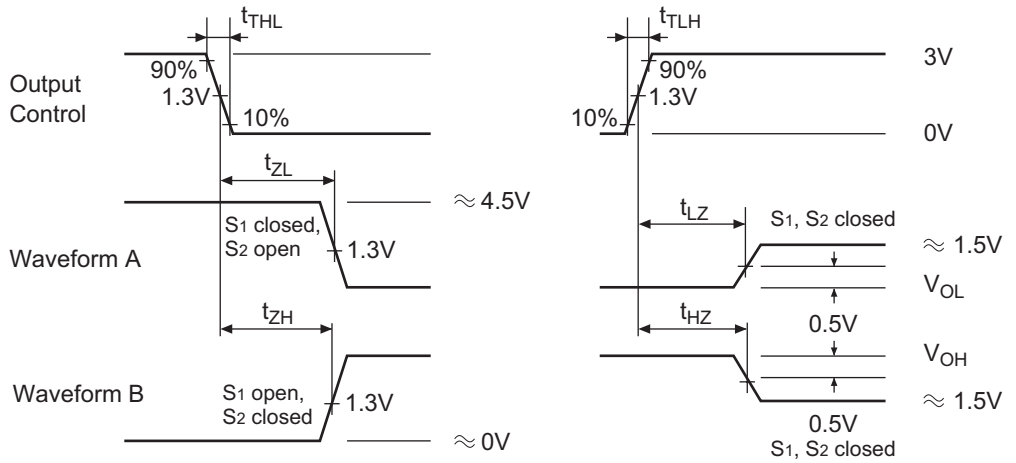
Waveforms 1



Notes: 1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns
Clock input; PRR = 1 MHz, duty cycle 50%
Data input pulse; PRR = 500 kHz, duty cycle 50%

2. f_{max}: $t_{TLH} \leq 2.5$ ns, $t_{THL} \leq 2.5$ ns

Waveforms 2

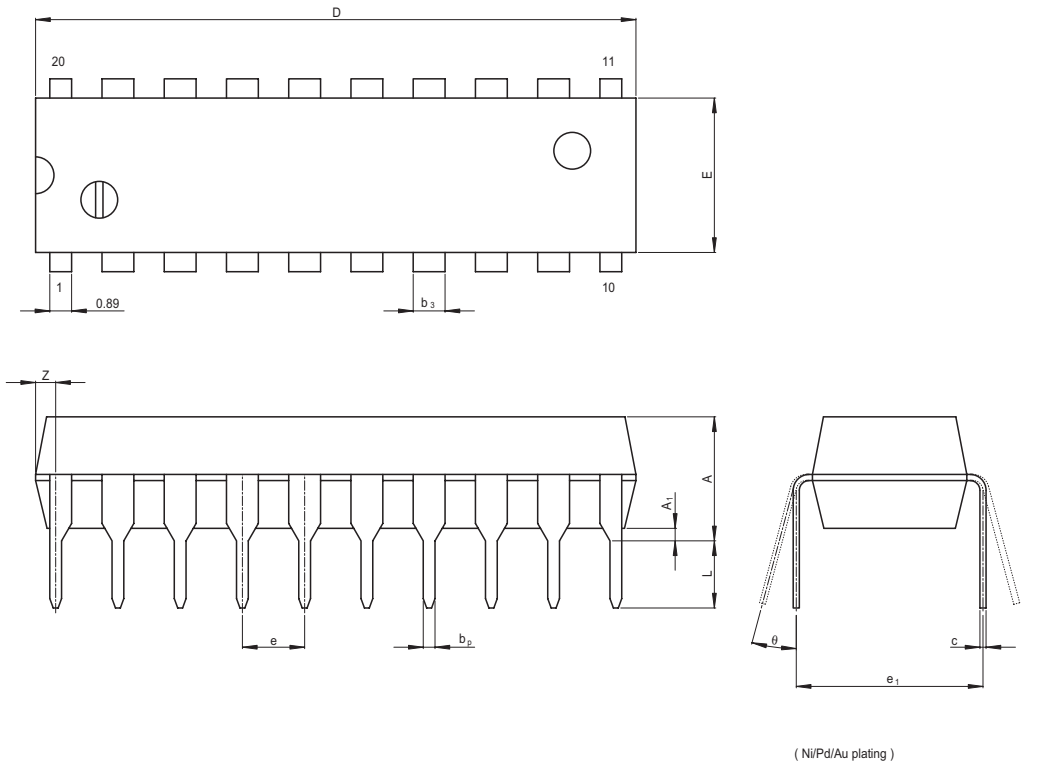


Notes: 1. Input pulse; $t_{TLH} \leq 15$ ns, $t_{THL} \leq 6$ ns, PRR = 1 MHz, duty cycle 50%

2. Waveform A if for an output with internal conditions such that the output is low except when disabled by the output control. Waveform B is for an output with internal conditions such that the output is high except when disabled by the output control.

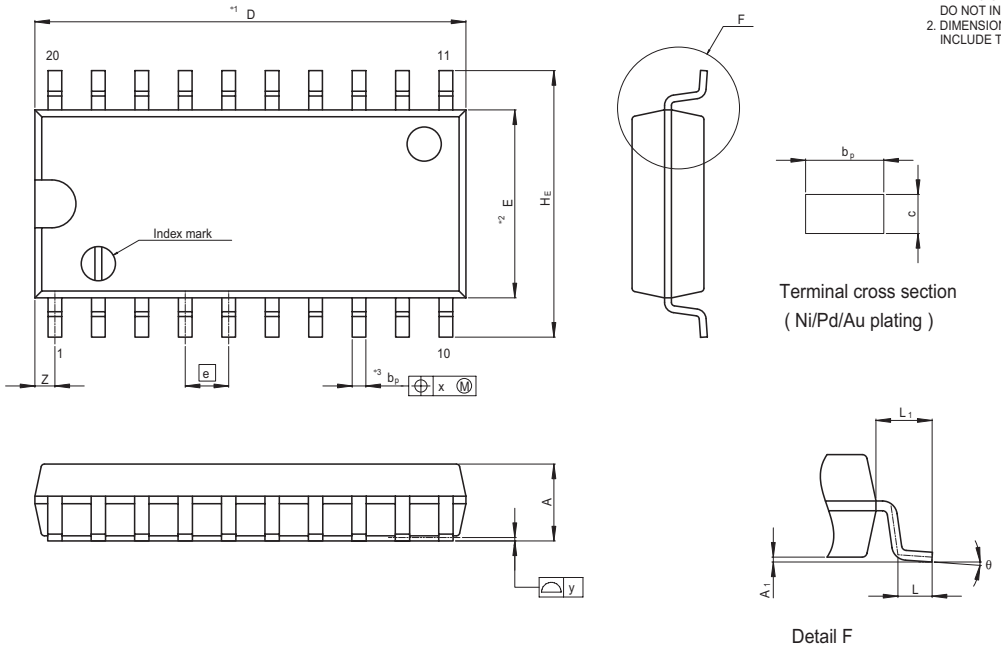
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP20-6.3x24.5-2.54	PRDP0020AC-B	DP-20NEV	1.26g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e 1	——	7.62	——
D	——	24.50	25.40
E	——	6.30	7.00
A	——	——	5.08
A 1	0.51	——	——
b p	0.40	0.48	0.56
b 3	——	1.30	——
c	0.19	0.25	0.31
θ	0°	——	15°
e	2.29	2.54	2.79
Z	——	——	1.27
L	2.54	——	——

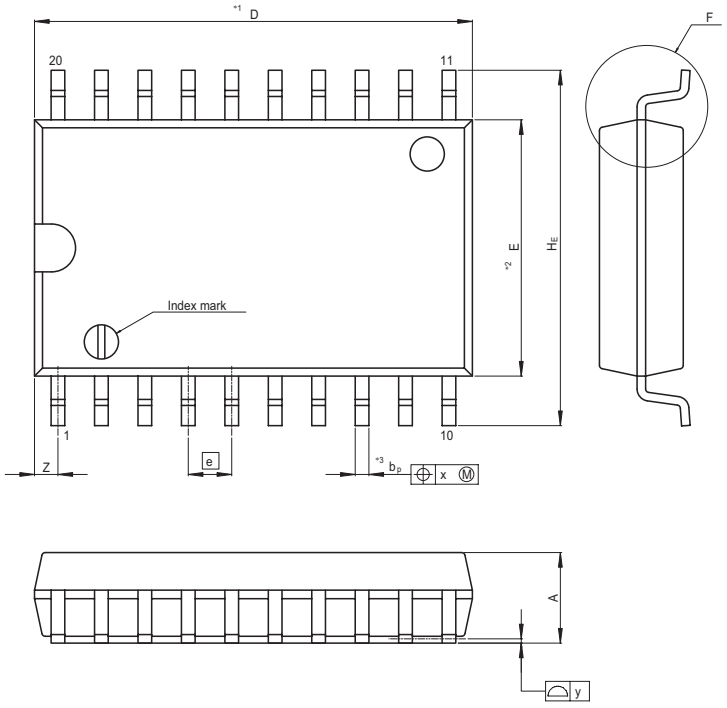
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-5.5x12.6-1.27	PRSP0020DD-B	FP-20DAV	0.31g



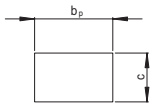
NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12.60	13.0
E	——	5.50	——
A 2	——	——	——
A 1	0.00	0.10	0.20
A	——	——	2.20
b p	0.34	0.40	0.46
b 1	——	——	——
c	0.15	0.20	0.25
c 1	——	——	——
θ	0°	——	8°
H E	7.50	7.80	8.00
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.80
L	0.50	0.70	0.90
L 1	——	1.15	——

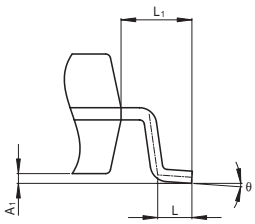
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP20-7.5x12.8-1.27	PRSP0020DC-A	FP-20DBV	0.52g



NOTE)
1. DIMENSIONS"*1 (Nom)"AND"*2"
   @ DO NOT INCLUDE MOLD FLASH.
2. DIMENSION"*3"DOES NOT
   @ INCLUDE TRIM OFFSET.



Terminal cross section
(Ni/Pd/Au plating)



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	12.80	13.2
E	——	7.50	——
A_2	——	——	——
A_1	0.10	0.20	0.30
A	——	——	2.65
b_p	0.34	0.40	0.46
b_1	——	——	——
c	0.20	0.25	0.30
c_1	——	——	——
θ	0°	——	8°
H_E	10.00	10.40	10.65
e	——	1.27	——
x	——	——	0.12
y	——	——	0.15
Z	——	——	0.935
L	0.40	0.70	1.27
L_1	——	1.45	——

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

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Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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