

HD74LS390

Dual Decade Counters

REJ03D0485-0400

Rev.4.00

May 10, 2006

This circuit contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters. The HD74LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and / or cumulative multiples of 2 and / or 5 up to divide-by-100. When connected as a binary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage.

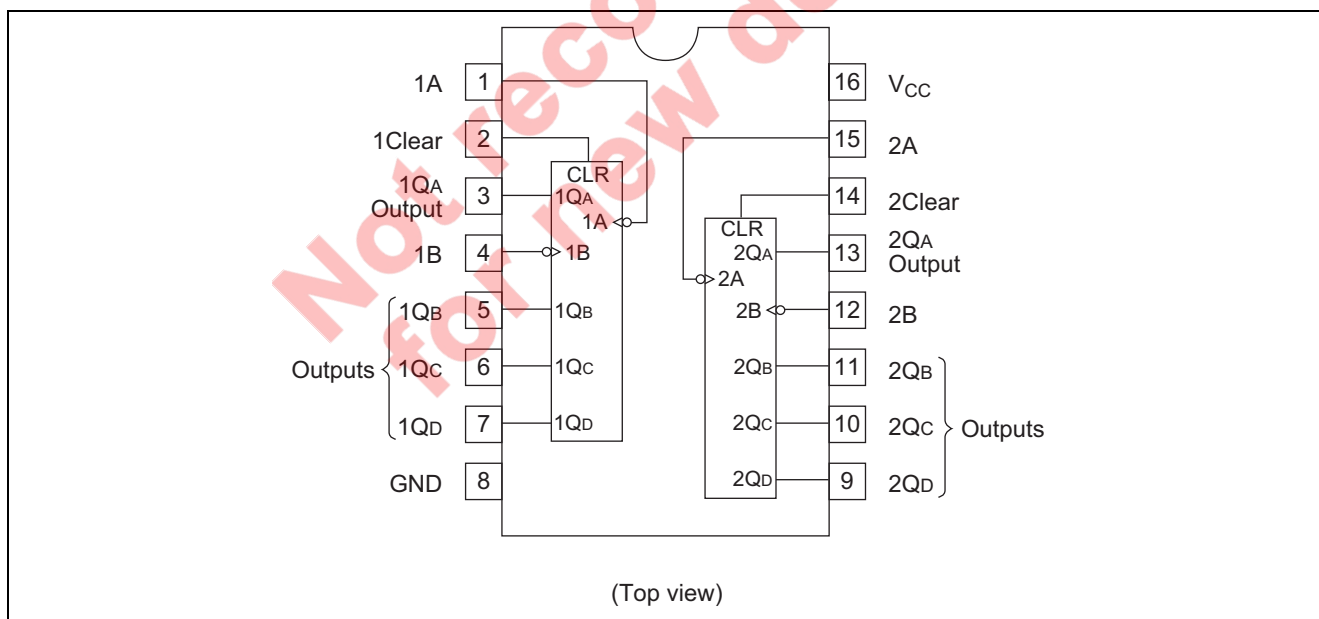
Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS390P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS390FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

Pin Arrangement



Function Table

BCD Count Sequence (Notes 1)

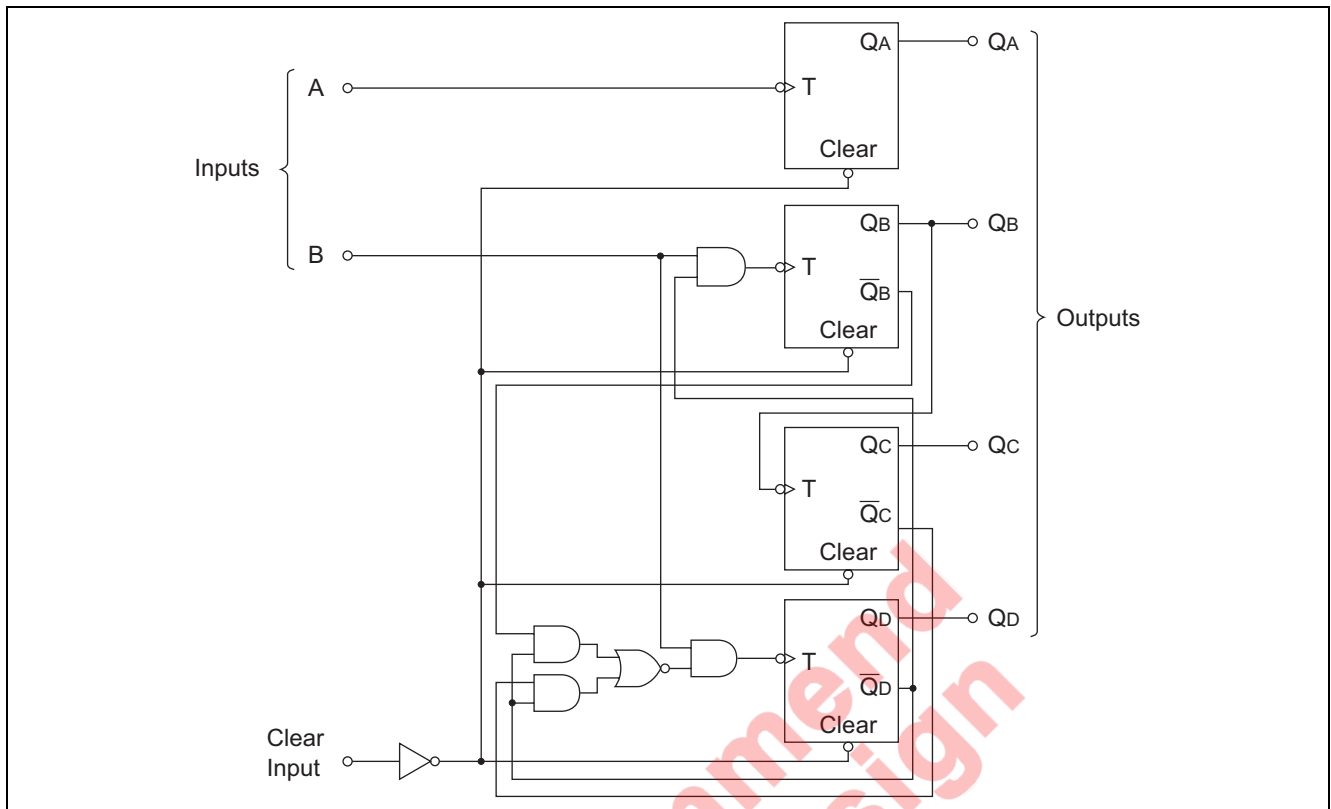
Count	Outputs			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

Bi-quinary (Notes 2)

Count	Outputs			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

- Notes: 1. Output Q_A is connected to input B for BCD count.
 2. Output Q_D is connected to input A for bi-quinary count.
 3. H; high level, L; low level, X; irrelevant

Block Diagram (1/2)



Absolute Maximum Ratings

Item		Symbol	Ratings	Unit
Supply voltage		V_{CC}	7	V
Input voltage	Clear	V_{IN}	7	V
	A, B	V_{IN}	5.5	
Power dissipation		P_T	400	mW
Storage temperature		T_{stg}	-65 to +150	°C
Operating temperature		T_{opr}	-20 to +75	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item		Symbol	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}	—	—	-400	μA
		I_{OL}	—	—	8	mA
Operating temperature		T_{opr}	-20	25	75	°C
Count frequency	A input	f_{count}	0	—	25	MHz
	B input		0	—	20	
Pulse width	A input	t_w	20	—	—	ns
	B input		25	—	—	
	Clear		20	—	—	
Clear setup time		t_{su}	25↓	—	—	ns

Electrical Characteristics

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V _{IH}	2.0	—	—	V		
		V _{IL}	—	—	0.7	V		
Output voltage		V _{OH}	2.7	—	—	V	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.7 V, I _{OH} = −400 μA	
		V _{OL}	—	—	0.4	V	I _{OL} = 4 mA	V _{CC} = 4.75 V, V _{IH} = 2 V, V _{IL} = 0.7 V
—	—		0.5	I _{OL} = 8 mA				
Input current	Clear	I _{IH}	—	—	20	μA	V _{CC} = 5.25 V, V _I = 2.7 V	
	Input A		—	—	100			
	Input B		—	—	200			
	Clear	I _{IL}	—	—	−0.4	mA	V _{CC} = 5.25 V, V _I = 0.4 V	
	Input A		—	—	−1.6			
	Input B		—	—	−2.4			
	Clear	I _I	—	—	0.1	mA	V _I = 7 V	V _{CC} = 5.25 V
	Input A		—	—	0.2		V _I = 5.5 V	
Input B	—		—	0.4				
Short-circuit output current		I _{OS}	−20	—	−100	mA	V _{CC} = 5.25 V	
Supply current		I _{CC}	—	15	26	mA	V _{CC} = 5.25 V	
Input clamp voltage		V _{IK}	—	—	−1.5	V	V _{CC} = 4.75 V, I _{IN} = −18 mA	

Notes: * V_{CC} = 5 V, Ta = 25°C** I_{CC} is measured with all outputs open, both Clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

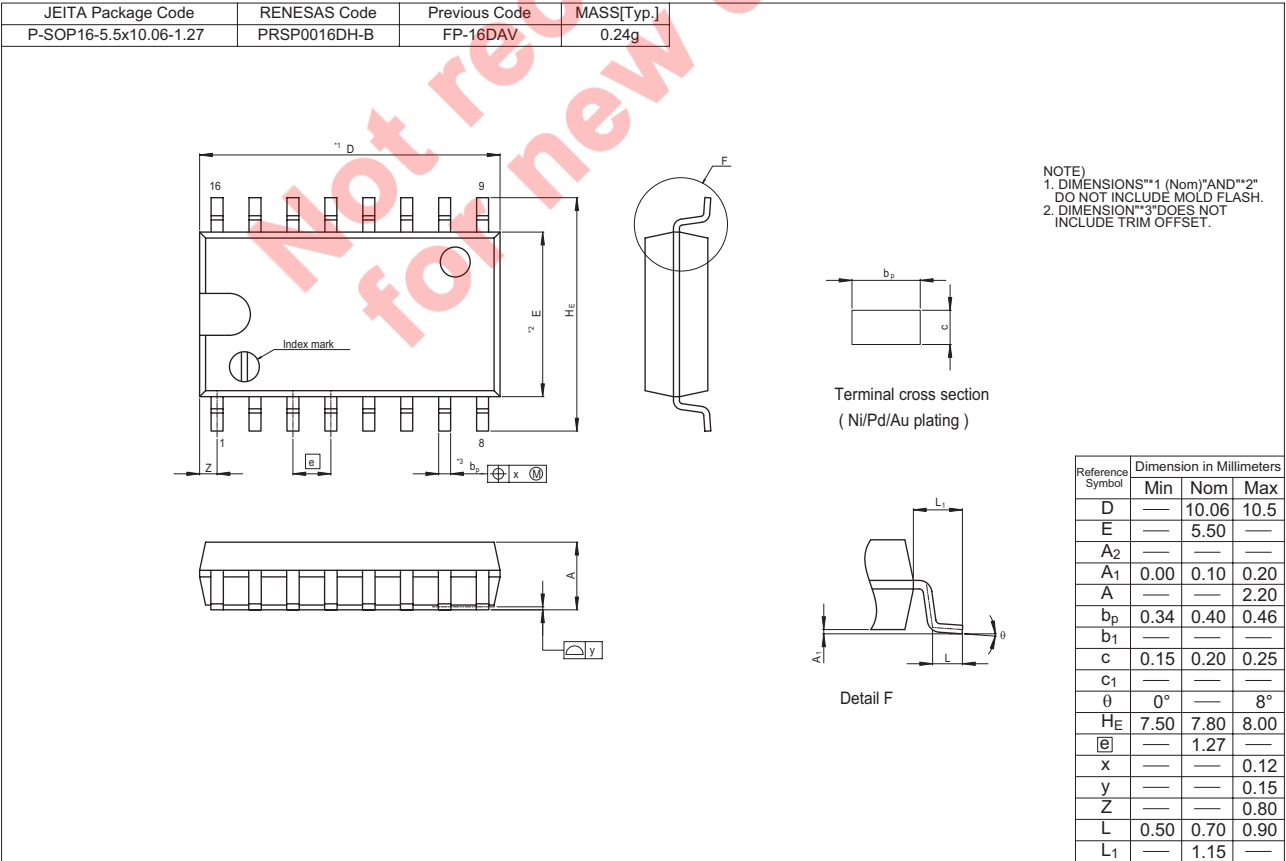
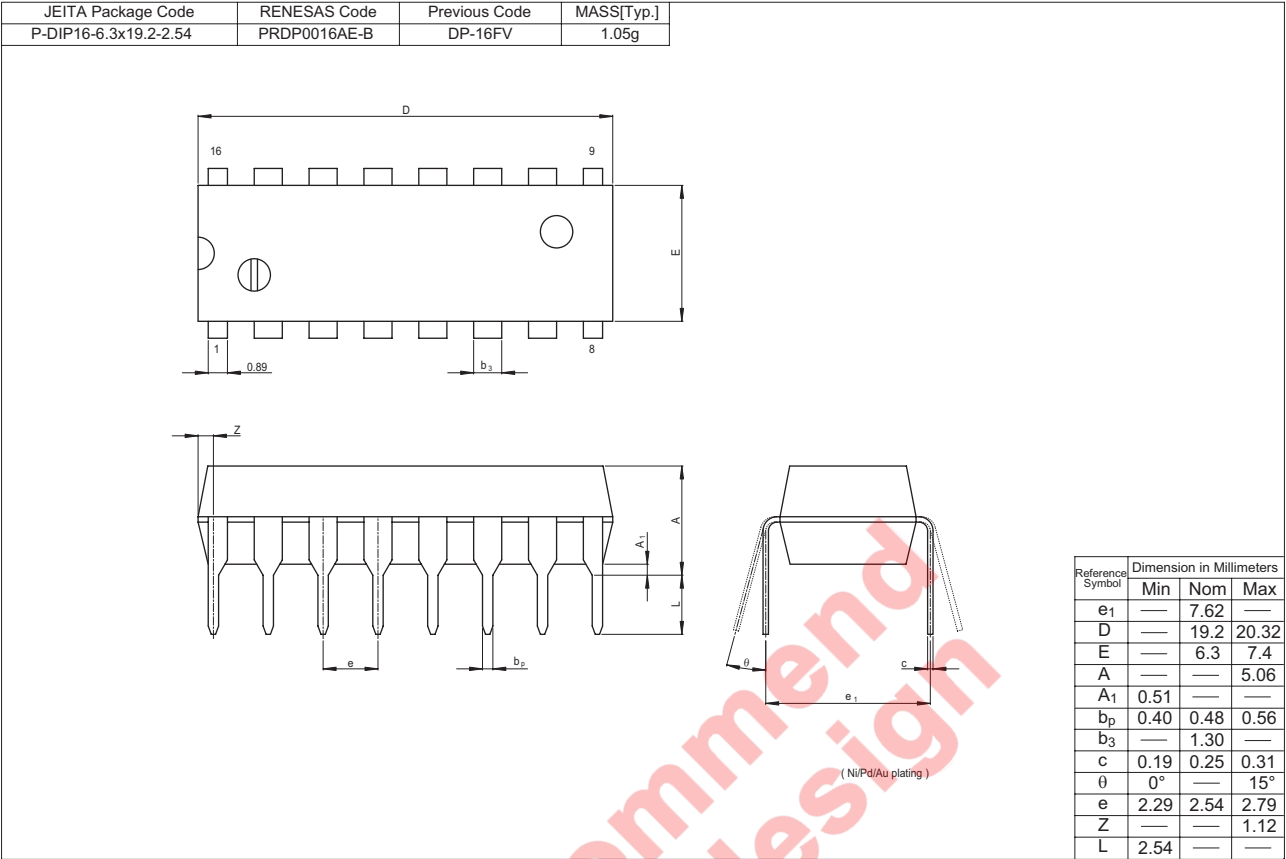
Switching Characteristics

(V_{CC} = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	$f_{\max}$	A	Q_A	25	35	—	MHz	$C_L = 15\text{ pF}$, $R_L = 2\text{ k}\Omega$
		B	Q_B	20	30	—		
Propagation delay time	t_{PLH}	A	Q_A	—	12	20	ns	
	t_{PHL}			—	13	20		
	t_{PLH}	A	Q_C	—	37	60	ns	
	t_{PHL}			—	39	60		
	t_{PLH}	B	Q_B	—	13	21	ns	
	t_{PHL}			—	14	21		
	t_{PLH}	B	Q_C	—	24	39	ns	
	t_{PHL}			—	26	39		
	t_{PLH}	B	Q_D	—	13	21	ns	
	t_{PHL}			—	14	21		
	t_{PHI}	Clear	Any	—	24	39	ns	

Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Package Dimensions



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