

HD74LV06A

Hex Inverter Buffers / Drivers with Open Drain Outputs

REJ03D0230-0600

Rev.6.00

Dec 23, 2005

Description

The HD74LV06A has six inverter buffers / drivers with open drain outputs in a 14-pin package.

Low-voltage and high-speed operation is suitable for the battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs V_{IH} (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 0\text{ V}$)
- All outputs V_O (Max.) = 5.5 V (@ $V_{CC} = 2.0\text{ V}$ to 5.5 V , Output "Z" state)
- Typical V_{OL} ground bounce < 0.8 V (@ $V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 8\text{ mA}$ (@ $V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 16\text{ mA}$ (@ $V_{CC} = 4.5\text{ V}$ to 5.5 V)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LV06AFPEL	SOP-14 pin (JEITA)	PRSP0014DF-B (FP-14DAV)	FP	EL (2,000 pcs/reel)
HD74LV06ARPEL	SOP-14 pin (JEDEC)	PRSP0014DE-A (FP-14DNV)	RP	EL (2,500 pcs/reel)
HD74LV06ATELL	TSSOP-14 pin	PTSP0014JA-B (TTP-14DV)	T	ELL (2,000 pcs/reel)

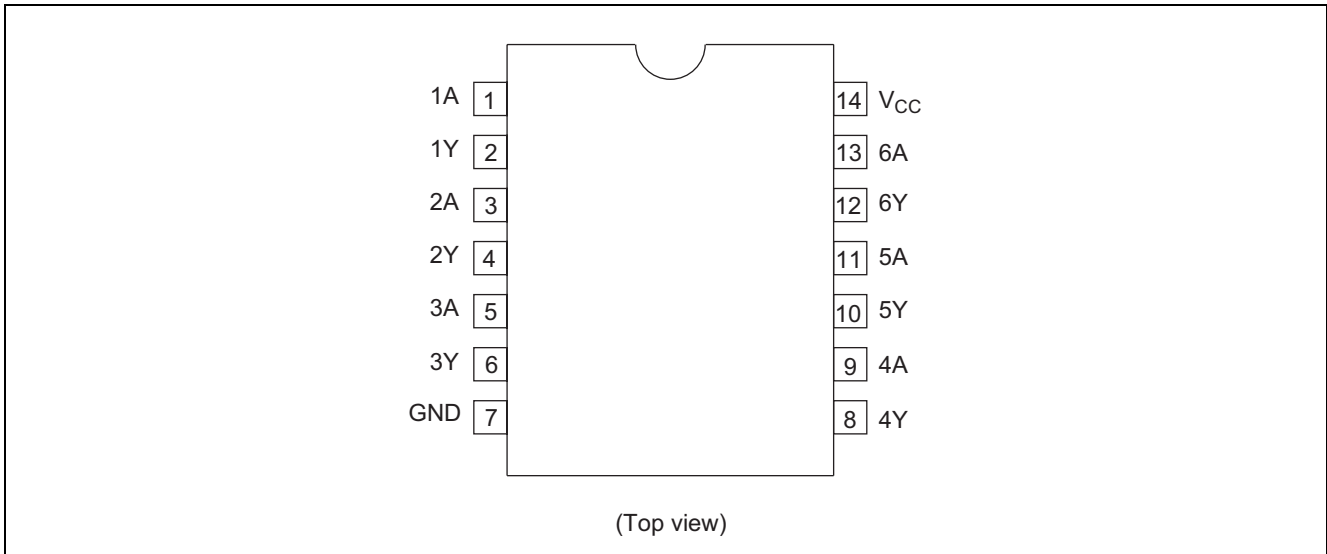
Note: Please consult the sales office for the above package availability.

Function Table

Input A	Output Y
L	Z
H	L

Note: H: High level
L: Low level
Z: High impedance

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1, 2}	V_O	-0.5 to $V_{CC} + 0.5$	V	Output: L
		-0.5 to 7.0		V_{CC} : OFF Output: Z
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$
Continuous output current	I_O	± 35	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

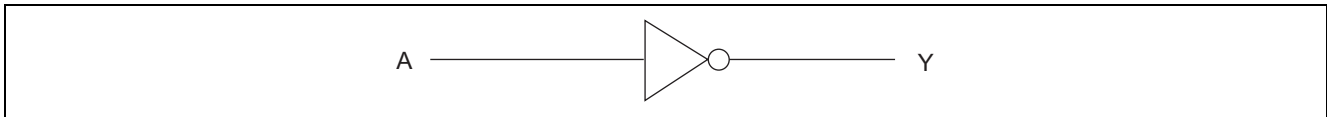
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 7.0 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150 $^\circ\text{C}$.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	5.5	V	
Output current	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	8		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	16		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

$T_a = -40 \text{ to } 85^{\circ}C$

Item	Symbol	$V_{CC} (V)^*$	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OL}	Min to Max	—	—	0.1	V	$I_{OL} = 50 \mu A$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 8 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 16 \text{ mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_{IN} = 5.5 V \text{ or } GND$
Off state output current	I_{OZ}	Min to Max	—	—	± 2.5	μA	$V_O = 5.5 V$
Quiescent supply current	I_{CC}	5.5	—	—	20	μA	$V_{IN} = V_{CC} \text{ or } GND, I_O = 0$
Output leakage current	I_{OFF}	0	—	—	5	μA	$V_I \text{ or } V_O = 0 \text{ to } 5.5 V$
Input capacitance	C_{IN}	3.3	—	2.3	—	pF	$V_I = V_{CC} \text{ or } GND$

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

$V_{CC} = 2.5 \pm 0.2 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.7	10.4	1.0	13.0	ns	C _L = 15 pF	A	Y
		—	9.5	15.2	1.0	18.0		C _L = 50 pF		
	t _{PHL}	—	5.4	10.4	1.0	13.0		C _L = 15 pF		
		—	7.9	15.2	1.0	18.0		C _L = 50 pF		

$V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	4.0	7.1	1.0	8.5	ns	C _L = 15 pF	A	Y
		—	7.3	10.6	1.0	12.0		C _L = 50 pF		
	t _{PHL}	—	4.3	7.1	1.0	8.5		C _L = 15 pF		
		—	5.8	10.6	1.0	12.0		C _L = 50 pF		

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Propagation delay time	t _{PLH}	—	3.3	5.5	1.0	6.5	ns	C _L = 15 pF	A	Y
		—	5.6	7.5	1.0	8.5		C _L = 50 pF		
	t _{PHL}	—	3.4	5.5	1.0	6.5		C _L = 15 pF		
		—	4.1	7.5	1.0	8.5		C _L = 50 pF		

Operating Characteristics

$C_L = 50 \text{ pF}$

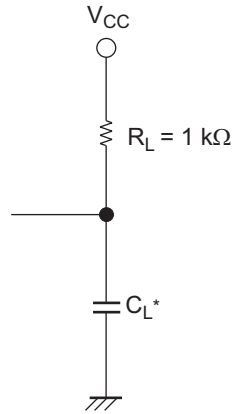
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C _{PD}	3.3	—	9.6	—	pF	f = 10 MHz
		5.0	—	11.4	—		

Noise Characteristics

$C_L = 50 \text{ pF}$

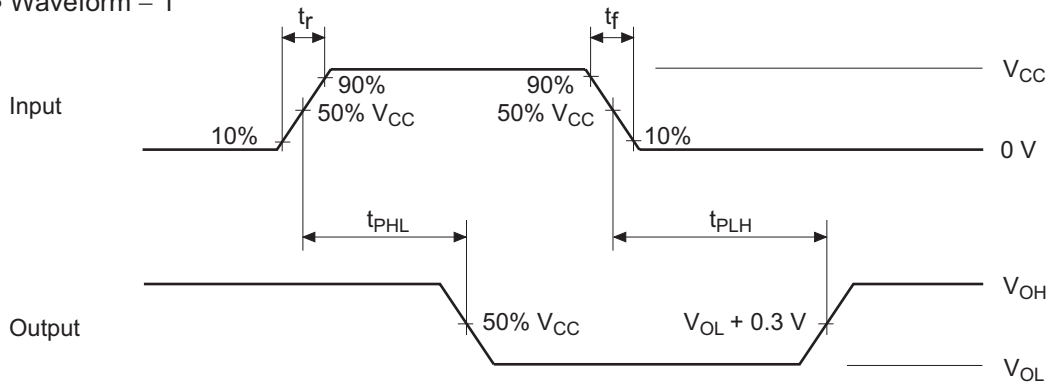
Item	Symbol	V _{CC} (V)	Ta = 25°C			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V _{OL}	V _{OL(P)}	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V _{OL}	V _{OL(V)}	3.3	—	-0.1	-0.8	V	
High-level dynamic input voltage	V _{IH(D)}	3.3	2.31	—	—	V	
Low-level dynamic input voltage	V _{IL(D)}	3.3	—	—	0.99	V	

Test Circuit



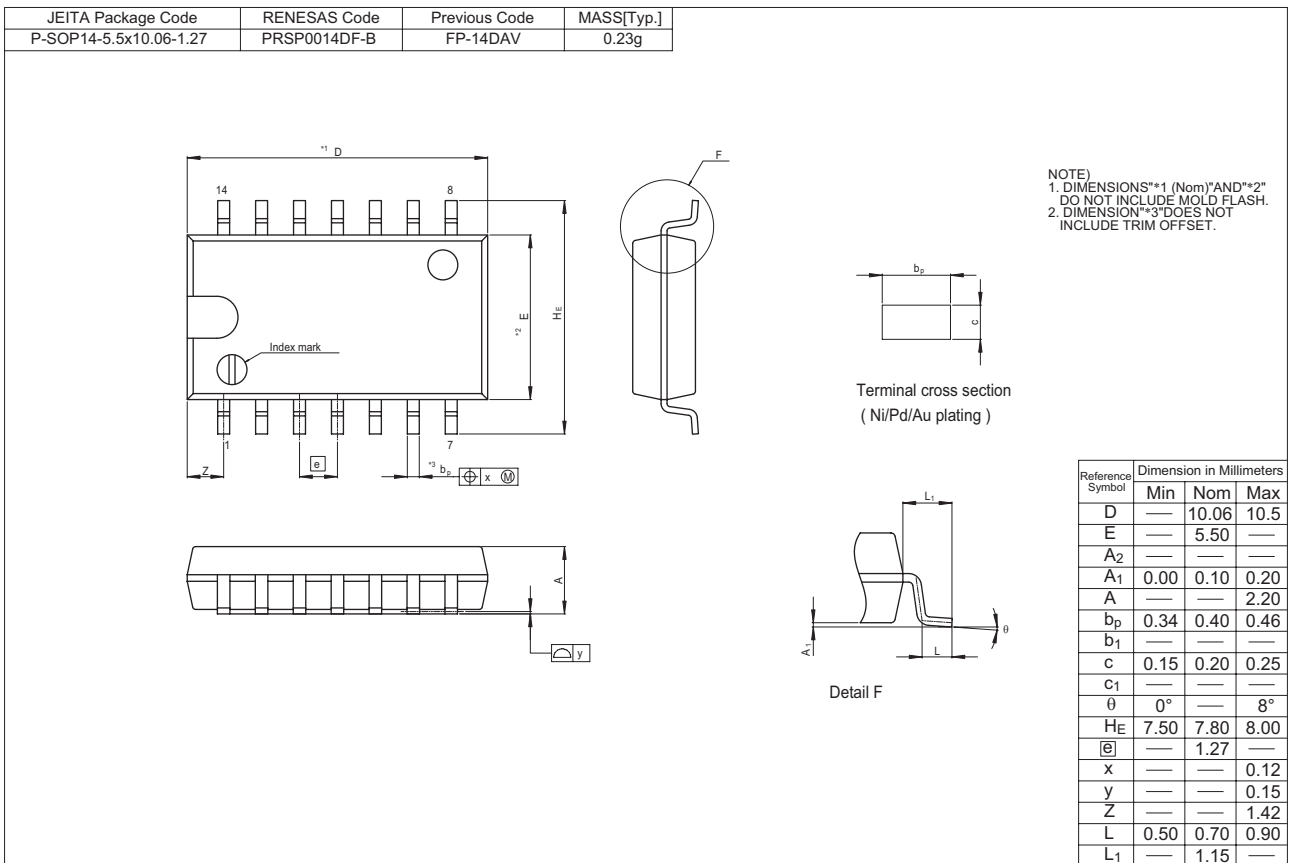
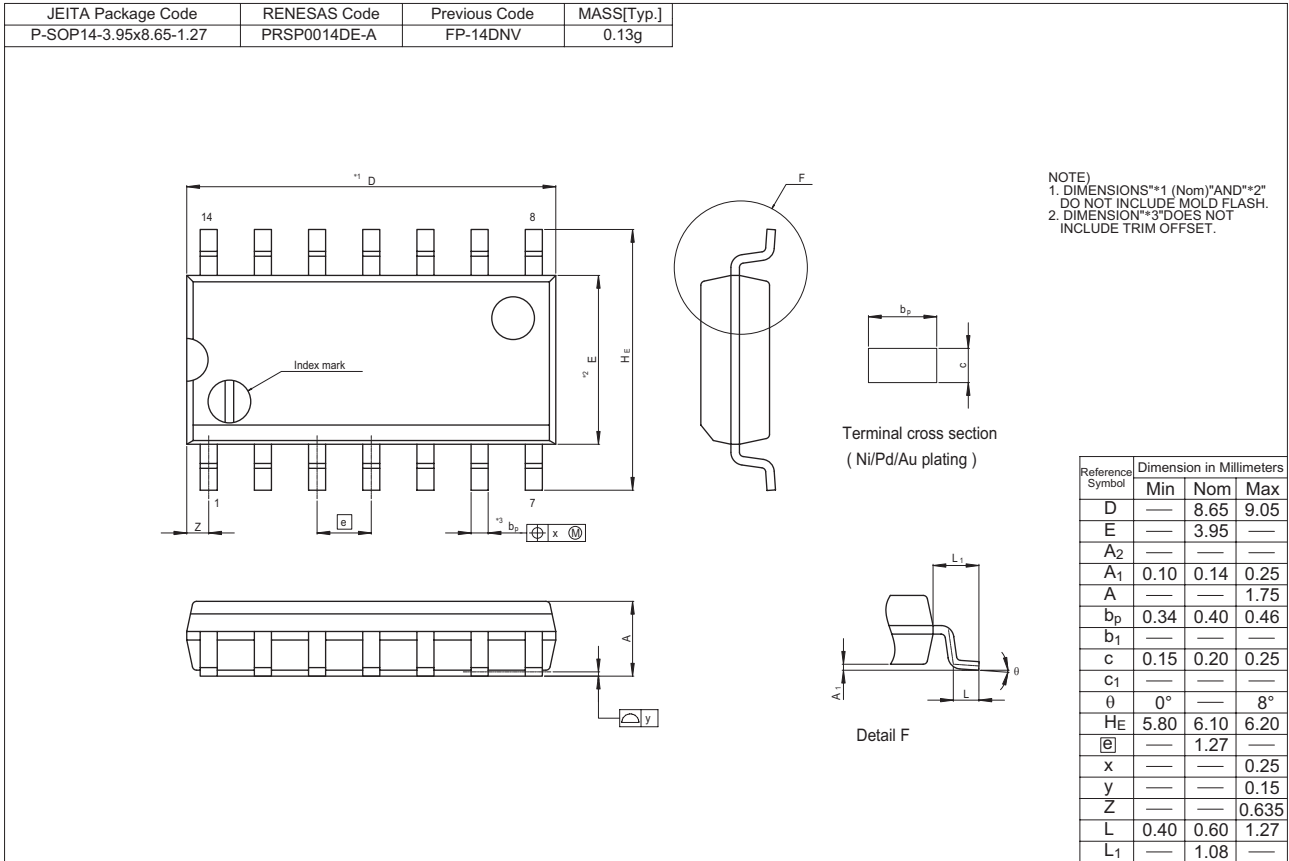
Note: C_L includes the probe and jig capacitance.

• Waveform – 1



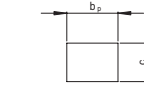
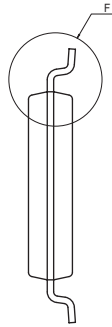
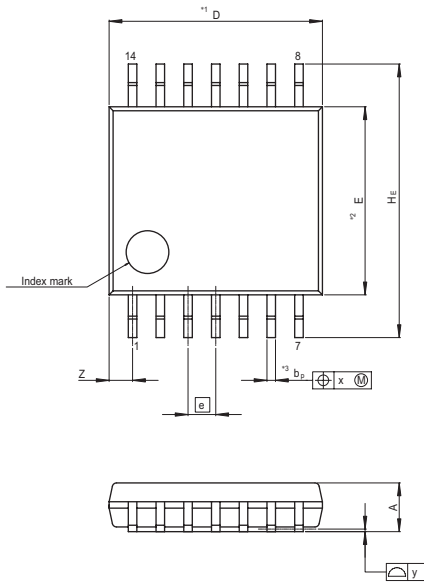
- Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
- 2. The output are measured one at a time with one transition per measurement.

Package Dimensions

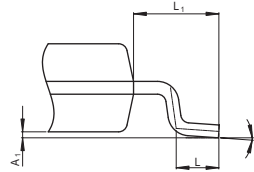


HD74LV06A

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TSSOP14-4.4x5-0.65	PTSP0014JA-B	TTP-14DV	0.05g



Terminal cross section
(Ni/Pd/Au plating)



Detail F

NOTE)
1. DIMENSIONS*1 (Nom)*AND*2*
DO NOT INCLUDE MOLD FLASH.
2. DIMENSION*3*DOES NOT
INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	5.00	5.30
E	—	4.40	—
A ₂	—	—	—
A ₁	0.03	0.07	0.10
A	—	—	1.10
b _p	0.15	0.20	0.25
b ₁	—	—	—
c	0.10	0.15	0.20
c ₁	—	—	—
θ	0°	—	8°
HE	6.20	6.40	6.60
⓪	—	0.65	—
x	—	—	0.13
y	—	—	0.10
Z	—	—	0.83
L	0.4	0.5	0.6
L ₁	—	1.0	—

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.
Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
 2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
 3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
 4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
 5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
 6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
 7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
 8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.
-



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510