

HD74LV175A

Quad. D-type Flip-Flops with Clear

HITACHI

ADE-205-270 (Z)

1st Edition

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Description

Information at the D inputs of the HD74LV175A is transferred to the Q and \bar{Q} outputs on the positive going edge of the clock pulse. Both true and complement outputs from each flip-flop are externally available. All four flip-flops are controlled by a common clock and common clear. Clearing is accomplished by a negative pulse at the clear input. All four Q outputs are cleared to a logic low level and all four \bar{Q} outputs to a logic high level. Low-voltage and high-speed operation is suitable for battery-powered products (e.g., notebook computers), and the low-power consumption extends the battery life.

Features

- $V_{CC} = 2.0\text{ V}$ to 5.5 V operation
- All inputs $V_{IH}(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$ to 5.5 V)
- All outputs $V_O(\text{Max.}) = 5.5\text{ V}$ ($@V_{CC} = 0\text{ V}$)
- Typical V_{OL} ground bounce $< 0.8\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Typical V_{OH} undershoot $> 2.3\text{ V}$ ($@V_{CC} = 3.3\text{ V}$, $T_a = 25^\circ\text{C}$)
- Output current $\pm 6\text{ mA}$ ($@V_{CC} = 3.0\text{ V}$ to 3.6 V), $\pm 12\text{ mA}$ ($@V_{CC} = 4.5\text{ V}$ to 5.5 V)

Function Table

Inputs			Outputs	
$\overline{\text{CLR}}$	CLK	D	Q	\bar{Q}
L	X	X	L	H
H	\uparrow	H	H	L
H	\uparrow	L	L	H
H	\downarrow	X	no change	no change

Note: H: High level

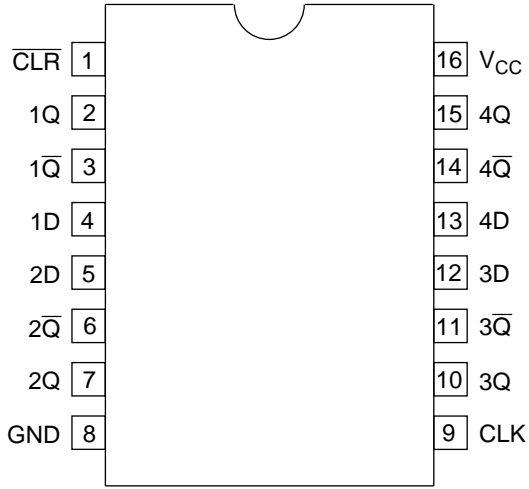
L: Low level

X: Immaterial

\uparrow : Low to high transition

\downarrow : High to low transition

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range* ¹	V_I	-0.5 to 7.0	V	
Output voltage range* ^{1,2}	V_O	-0.5 to $V_{CC} + 0.5$ -0.5 to 7.0	V	Output: H or L V_{CC} : OFF
Input clamp current	I_{IK}	-20	mA	$V_I < 0$
Output clamp current	I_{OK}	± 50	mA	$V_O < 0$ or $V_O > V_{CC}$
Continuous output current	I_O	± 25	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 50	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air)* ³	P_T	785	mW	SOP
		500		TSSOP
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

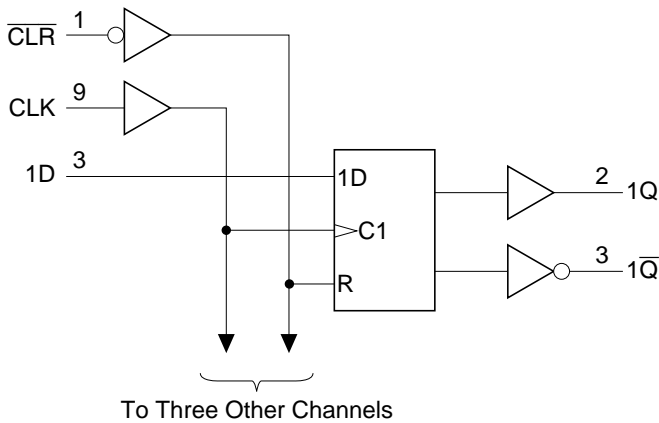
1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The maximum package power dissipation was calculated using a junction temperature of 150°C.

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	2.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_O	0	V_{CC}	V	H or L
Output current	I_{OH}	—	-50	μA	$V_{CC} = 2.0 V$
		—	-2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	-6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	-12		$V_{CC} = 4.5 \text{ to } 5.5 V$
	I_{OL}	—	50	μA	$V_{CC} = 2.0 V$
		—	2	mA	$V_{CC} = 2.3 \text{ to } 2.7 V$
		—	6		$V_{CC} = 3.0 \text{ to } 3.6 V$
		—	12		$V_{CC} = 4.5 \text{ to } 5.5 V$
Input transition rise or fall rate	$\Delta t / \Delta v$	0	200	ns/V	$V_{CC} = 2.3 \text{ to } 2.7 V$
		0	100		$V_{CC} = 3.0 \text{ to } 3.6 V$
		0	20		$V_{CC} = 4.5 \text{ to } 5.5 V$
Operating free-air temperature	T_a	-40	85	$^{\circ}C$	

Note: Unused or floating inputs must be held high or low.

Logic Diagram



DC Electrical Characteristics

- $T_a = -40$ to 85°C

Item	Symbol	V_{CC} (V)*	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	V	
		2.3 to 2.7	$V_{CC} \times 0.7$	—	—		
		3.0 to 3.6	$V_{CC} \times 0.7$	—	—		
		4.5 to 5.5	$V_{CC} \times 0.7$	—	—		
	V_{IL}	2.0	—	—	0.5		
		2.3 to 2.7	—	—	$V_{CC} \times 0.3$		
		3.0 to 3.6	—	—	$V_{CC} \times 0.3$		
		4.5 to 5.5	—	—	$V_{CC} \times 0.3$		
Output voltage	V_{OH}	Min to Max	$V_{CC} - 0.1$	—	—	V	$I_{OH} = -50 \mu\text{A}$
		2.3	2.0	—	—		$I_{OH} = -2 \text{ mA}$
		3.0	2.48	—	—		$I_{OH} = -6 \text{ mA}$
		4.5	3.8	—	—		$I_{OH} = -12 \text{ mA}$
	V_{OL}	Min to Max	—	—	0.1		$I_{OL} = 50 \mu\text{A}$
		2.3	—	—	0.4		$I_{OL} = 2 \text{ mA}$
		3.0	—	—	0.44		$I_{OL} = 6 \text{ mA}$
		4.5	—	—	0.55		$I_{OL} = 12 \text{ mA}$
Input current	I_{IN}	0 to 5.5	—	—	± 1	μA	$V_I = 5.5 \text{ V}$ or GND
Quiescent supply current	I_{CC}	5.5	—	—	20	μA	$V_I = V_{CC}$ or GND, $I_O = 0$
Output leakage current	I_{OFF}	0	—	—	5	μA	V_I or $V_O = 0 \text{ V}$ to 5.5 V
Input capacitance	C_{IN}	3.3	—	1.4	—	pF	$V_I = V_{CC}$ or GND

Note: For conditions shown as Min or Max, use the appropriate values under recommended operating conditions.

Switching Characteristics

- $V_{CC} = 2.5 \pm 0.2 \text{ V}$

$T_a = 25^\circ\text{C}$ $T_a = -40 \text{ to } 85^\circ\text{C}$

Item	Symbol	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } 85^\circ\text{C}$		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	50	105	—	45	—	MHz	$C_L = 15 \text{ pF}$		
		40	80	—	35	—				
Propagation delay time	t_{PLH} / t_{PHL}	—	9.3	18.8	1.0	22.0	ns	$C_L = 15 \text{ pF}$	CLK	Q, \bar{Q}
		—	12.0	23.3	1.0	27.0				
	t_{PHL}	—	7.9	16.6	1.0	20.0	ns	$C_L = 15 \text{ pF}$	$\overline{\text{CLR}}$	
		—	10.4	21.6	1.0	25.5				
Setup time	t_{SU}	7.0	—	—	7.5	—	ns			Data before CLK \uparrow
		7.0	—	—	7.5	—				$\overline{\text{CLR}}$ inactive before CLK \uparrow
Hold time	t_h	0.5	—	—	1.0	—	ns			Data after CLK \uparrow
Pulse width	t_w	6.0	—	—	6.0	—	ns			$\overline{\text{CLR}}$ L
		6.5	—	—	7.0	—				CLK H or L

Switching Characteristics (cont)

$V_{CC} = 3.3 \pm 0.3 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock fre- quency	fmax	90	155	—	75	—	MHz	CL = 15 pF		
		50	120	—	45	—				
Propa- gation delay time	tPLH / tPHL	—	6.5	11.5	1.0	13.5	ns	CL = 15 pF	CLK	Q, Q̄
		—	8.4	15.0	1.0	17.0				
	tPLH / tPHL	—	5.5	10.1	1.0	12.0	ns	CL = 15 pF	CLR̄	
		—	7.4	13.6	1.0	15.5				
Setup time	tSU	5.0	—	—	5.0	—	ns		Data before CLK↑	
		5.0	—	—	5.0	—				
Hold time	th	1.0	—	—	1.0	—	ns		Data after CLK↑	
Pulse width	tW	5.0	—	—	5.0	—	ns		CLR̄ L	
		5.0	—	—	5.0	—				

Switching Characteristics (cont)

$V_{CC} = 5.0 \pm 0.5 \text{ V}$

Item	Symbol	Ta = 25°C			Ta = -40 to 85°C		Unit	Test Conditions	FROM (Input)	TO (Output)
		Min	Typ	Max	Min	Max				
Maximum clock frequency	fmax	150	215	—	125	—	MHz	CL = 15 pF		
		85	165	—	75	—				
Propagation delay time	tPLH / tPHL	—	4.6	7.3	1.0	8.5	ns	CL = 15 pF	CLK	Q, Q̄
		—	6.0	9.3	1.0	10.5				
	tPLH / tPHL	—	3.7	6.4	1.0	7.5	ns	CL = 15 pF	CLR̄	
		—	5.3	8.4	1.0	9.5				
Setup time	tSU	4.0	—	—	4.0	—	ns		Data before CLK↑	
		5.0	—	—	5.0	—				
Hold time	th	1.0	—	—	1.0	—	ns		Data after CLK↑	
Pulse width	tW	5.0	—	—	5.0	—	ns		CLR̄ L	
		5.0	—	—	5.0	—				

Output-skew Characteristics

Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			$T_a = -40 \text{ to } 85^\circ C$		Unit
			Min	Typ	Max	Min	Max	
Output skew	$t_{sk(O)}$	2.3 to 2.7	—	—	2.0	—	2.0	ns
		3.0 to 3.6	—	—	1.5	—	1.5	
		4.5 to 5.5	—	—	1.0	—	1.0	

Note: Skew between any outputs of the same package switching in the same direction. This parameter is warranted but not production tested.

Operating Characteristics

- $C_L = 50 \text{ pF}$

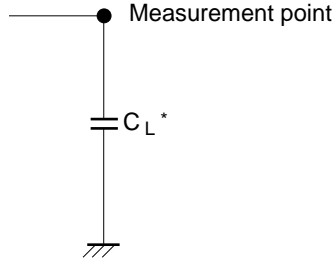
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			Unit	Test Conditions
			Min	Typ	Max		
Power dissipation capacitance	C_{PD}	3.3	—	13.6	—	pF	$f = 10 \text{ MHz}$
		5.0	—	14.5	—		

Noise Characteristics

- $C_L = 50 \text{ pF}$

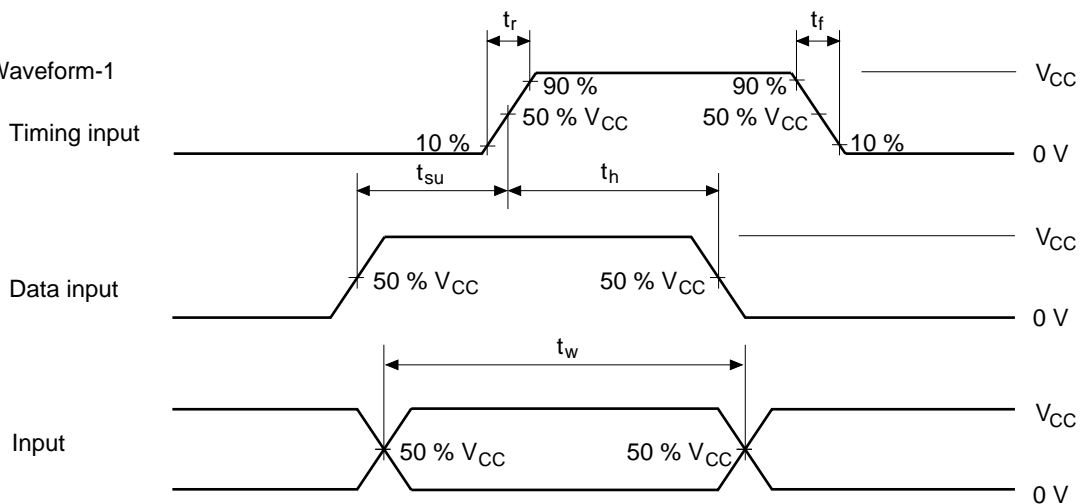
Item	Symbol	$V_{CC} = (V)$	$T_a = 25^\circ C$			Unit	Test Conditions
			Min	Typ	Max		
Quiet output, maximum dynamic V_{OL}	$V_{OL(P)}$	3.3	—	0.3	0.8	V	
Quiet output, minimum dynamic V_{OL}	$V_{OL(V)}$	3.3	—	-0.3	-0.8		
Quiet output, minimum dynamic V_{OH}	$V_{OH(V)}$	3.3	—	3.0	—		
High-level dynamic input voltage	$V_{IH(D)}$	3.3	2.31	—	—	V	
Low-level dynamic input voltage	$V_{IL(D)}$	3.3	—	—	0.99		

Test Circuit

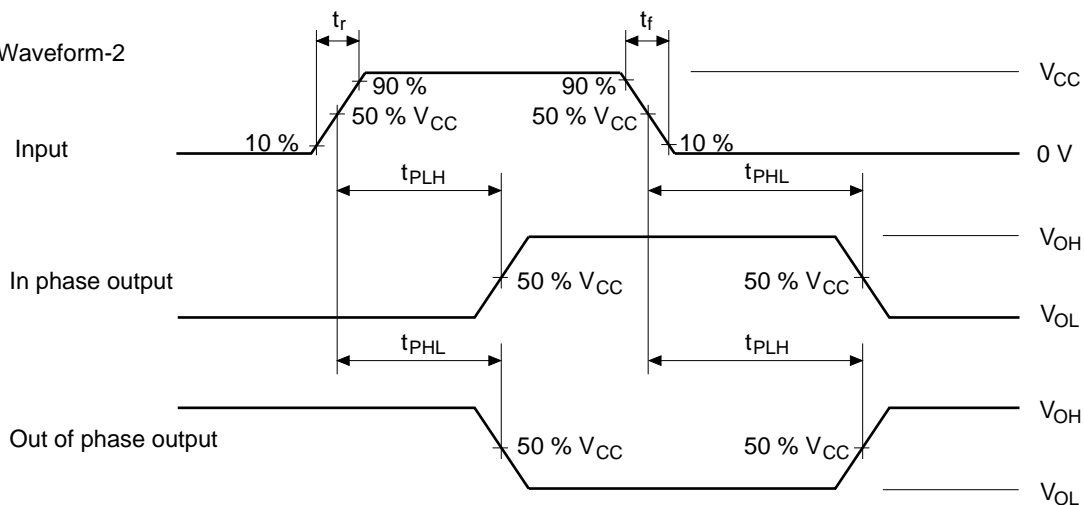


Note: C_L includes the probe and jig capacitance.

• Waveform-1

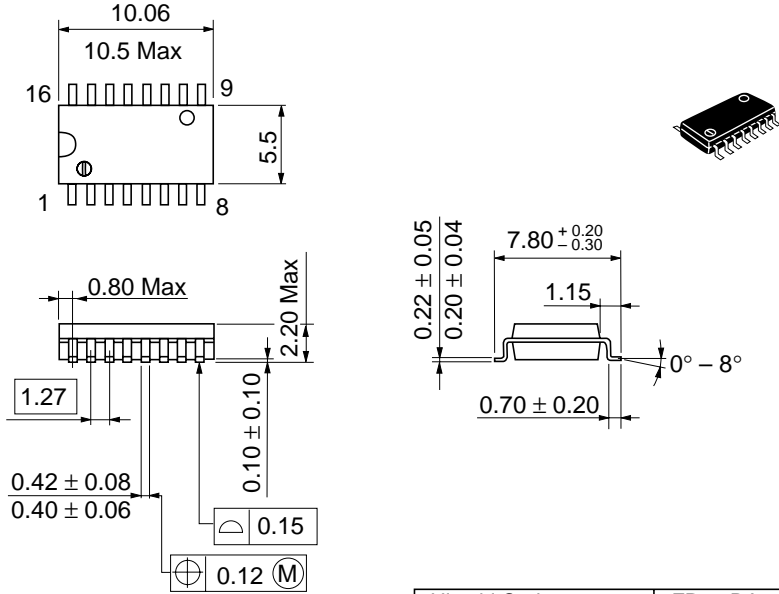


• Waveform-2



- Notes: 1. Input waveform: $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$
 2. The output is measured one at a time with one transition per measurement.

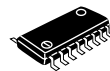
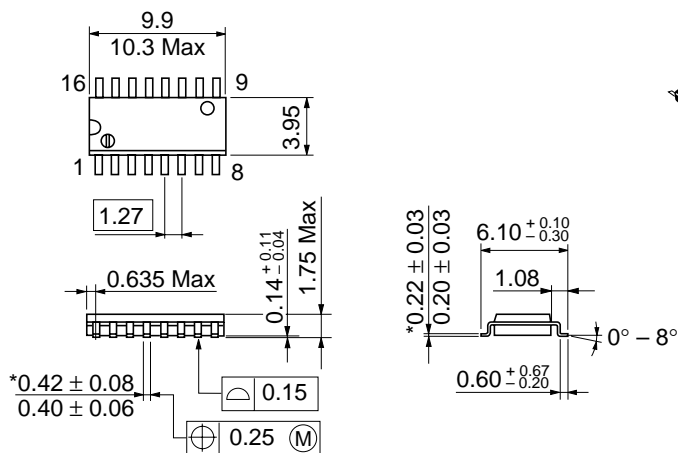
Package Dimensions



Dimension including the plating thickness
Base material dimension

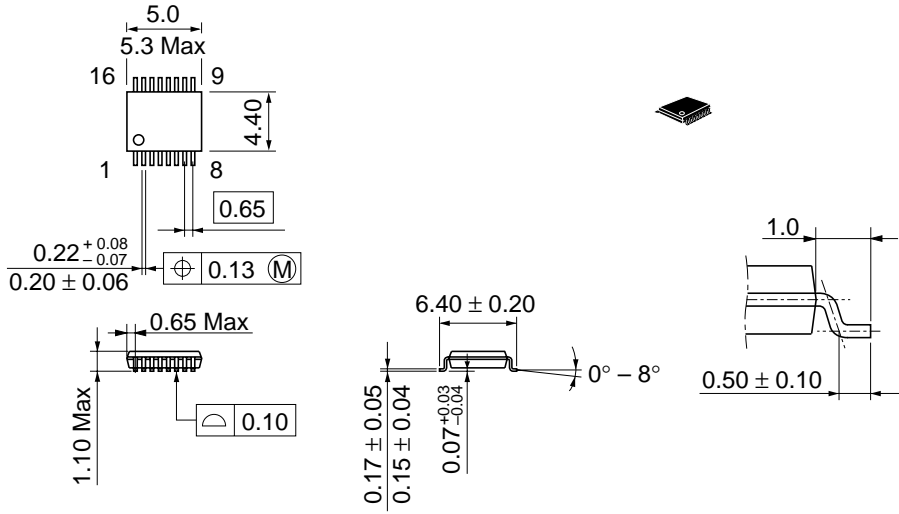
Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g



Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-16DA
JEDEC	—
EIAJ	—
Weight (reference value)	0.05 g

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